

AMRL-TR-67-236

**DESIGN AND OPERATION OF ROOT C,
A SMALL SYNCODER NETWORK SIMULATOR**

ROGER A. GRUENKE, CAPTAIN, USAF

J. RYLAND MUNDIE, MD

Distribution of this document is unlimited. It may be released to the Clearinghouse, Department of Commerce, for sale to the general public.

Foreword

The instrument and models described in this report were designed in support of Project 7233, "Biological Information Handling Systems and Their Functional Analogs," Task 723303, "Biological Components." The research and design were performed in the Neurophysiology Branch, Biodynamics and Bionics Division, Biomedical Laboratory of the Aerospace Medical Research Laboratories during the period October 1964 to January 1967.

This technical report has been reviewed and is approved.

R. H. LANG, LT. COL., USAF, MC
Chief
Biomedical Laboratory
Aerospace Medical Research Laboratories

Abstract

A syncoder is an electronic model of some of the information processing properties of nerve cells. This report describes the equations of operation of a single syncoder and serves as an instruction manual for the programming and operation of a network simulator containing 10 syncoders. The network simulator, called "Root C," also contains a patch panel, voltage sources, a meter, and the necessary input-output lines to permit the simulation of small networks of syncoders. An appendix contains a complete circuit description of a single syncoder.

Table of Contents

<i>Section</i>	<i>Page</i>
I. Introduction.....	1
II. Syncoder Operation.....	2
III. Location and Description of Controls.....	6
IV. Patch Panel Layout.....	9
V. Patch Panel Plug-in Elements.....	10
APPENDIX. Description of the Syncoder Circuit.....	13

List of Illustrations

<i>Figure</i>	<i>Page</i>
1 Syncoder Inputs and Outputs.....	2
2 Encoder Block Diagram.....	4
3 Encoder Performance Characteristic.....	4
4 Synapse Block Diagram.....	5
5 Syncoder Symbols.....	5
6 Root C Front Panel.....	6
7 Patch Panel Inside Top Cover.....	7
8 Rear View.....	8
9 Patch Panel.....	9
10 Plug-in Elements.....	10
11 Encoder Circuit.....	11
12 Buffer Circuit.....	12
13 Schematic of Synapse Button.....	14
14 Diagram of Waveform Produced by Pulse Input.....	14

Tables

<i>Table</i>	<i>Page</i>
I. Permitted Interconnections.....	11

Section I.
INTRODUCTION

Root C is a small simulator composed of ten syncoders, or neuron-like elements, and necessary supporting circuitry to permit the simulation and investigation of small networks of these elements. The networks are programmed by means of patch cords, containing some additional components, which are inserted into the proper holes of the patch panel. Instruments may be connected to jacks on the front panel and inside the top cover to measure the performance of the network. The network may also be used to control external devices through connections to the same jacks. The state of the network may be ascertained by use of the panel meter and the neon indicators. Adjustment of the potentiometers on the front panel changes coefficients and constants in the network equations.

Section II. SYNCODER OPERATION

Since the basic element of the simulator is the syncoder, the following sections will be devoted to a discussion of the operation of a single syncoder. In the course of studies of the firing patterns of neurons in the eighth nerve of the guinea pig, the need arose for a functional model of these neurons to better understand their behavior. Later we wanted to extend this model to reproduce the functioning of other neurons and neuron-synapse combinations observed in nature. In particular, we wanted to investigate the information processing properties of these neuron-synapse combinations that we call syncoders. A syncoder (figure 1) is made of two units, the encoder, or cell body model, and the synapse model. The encoder generates a train of pulses at its output in response to a voltage applied at its input; the synapse converts pulse trains to voltages. In our model, the voltage output of a synapse is internally connected to the voltage input of an encoder.

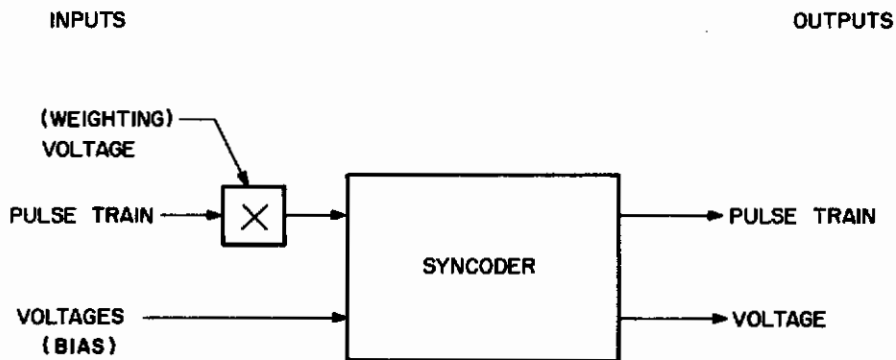


Figure 1. Syncoder Inputs and Outputs

The encoder is a thresholding element whose threshold exponentially decays with time after each output pulse. Therefore, it is more sensitive to small inputs if a long time has elapsed since the last output pulse occurred. The encoder has one input for analog signals in which the information is contained in the amplitude of the applied voltage. This input is encoded into a train of identical 1-millisecond pulses, in which the information is contained in the interpulse interval. The interpulse interval, t , is related to the input voltage, V , by

$$t = -K \ln \frac{V}{B}$$

where B and K are constants and V is always between $-B$ and $+B$.

The synapse section may be considered to have three functions: (1) it sums all voltages brought to its input, (2) it changes incoming pulses into a special analog wave form before summing, (3) a gain control or weighting function is carried out on pulse inputs. The first two functions are performed by a summing amplifier with RC feedback impedance; the third function is performed by a separate element, the synapse button. Voltages to the summing junction may be constant, adding a constant value to synapse output sum; these constant input values will be designated as "bias" values to distinguish them. The bias inputs may be used to vary the level which the exponential threshold approaches in the attached encoder. Analog voltages within the limits of ± 10 volts dc to 50 Hz may be brought to the summing junction;

the RC feedback impedance of the summing amplifier determines the frequency response characteristics of the synapse circuit. Conversion of pulses into analog signal is a special case of the latter consideration. The rise time of the synapse circuit is longer than the duration of input pulses. Thus, pulse inputs are converted to an output voltage that rises exponentially toward the weighting voltage during a pulse and decays exponentially with the same time constant toward zero. The value or weighting of individual input pulses can be changed by an external voltage source called the weighting voltage. Each pulse input must be connected to a weighting voltage, but a single voltage source may serve as the weighting voltage for a number of pulse inputs. The synapse amplifier inverts the input signals, so that positive input voltages produce negative outputs to the encoder section that follows. Negative input voltages produce positive output voltages and an output pulse train from the attached encoder.

The processing performed between the pulse input of a syncoder and its pulse output is called the syncing operation. The voltage output of a synapse is an intermediate result.

A block diagram of an encoder is shown in figure 2. The input voltage, V_s , is compared with the exponentially decaying reference voltage, V_r , and the pulse generator is triggered when V_s equals V_r . The pulse generator produces pulses of 24 volts amplitude and 1 millisecond duration. The voltage at the pulse output terminal is -12 volts when no pulse is present and rises to 12 volts for duration of pulse. At the completion of the pulse, V_r is 12 volts and thereafter decays exponentially to 0 volts with a 10 millisecond time-constant. Therefore, $V_r = 12 e^{-kt}$ where $K = \frac{1}{0.01}$. V_s is limited between 12 and -12 volts. A pulse is produced when:

$$V_s = V_r = 12 e^{-kt}$$

taking the logarithm of both sides:

$$\ln V_s = -kt + \ln 12$$

or

$$\frac{1}{K} \ln \frac{V_s}{12} = -t$$

which becomes

$$-0.01 \ln \frac{V_s}{12} = +t$$

where t is the interval from the end of one pulse to the beginning of the next. Since V_s lies between 12 and -12 volts, we are taking the logarithm of a number between -1 and 1. The logarithm of a negative number is undefined; thus no pulses are produced. The logarithm of a number between 0 and 1 is negative, resulting in positive values for t . Thus, the interpulse interval is directly proportional to the logarithm of the value of the input voltage at the time at which the second pulse is produced. A typical performance characteristic for an encoder is shown in figure 3. This curve demonstrates that the encoder apparently follows the equations quite closely over a 40 dB range of input voltages; the departure from linearity is due to a combination of noise and hysteresis in the comparator amplifier.

The synapse junction and button comprise the synapse section of the syncoder and will be discussed together. Figure 4 is a functional diagram of the synapse junction and button elements. The synapse junction is composed of the transistor operational amplifier and a parallel RC feedback impedance. The built-in time constant is 3.3 milliseconds, which may be increased by adding parallel capacitors. Current coming into the summing junction is balanced by current from the output of the amplifier, which results in a change in the output voltage of the circuit due to

Contrails

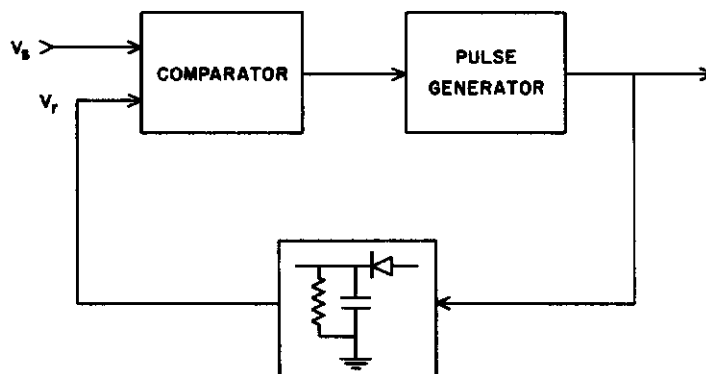


Figure 2. Encoder Block Diagram

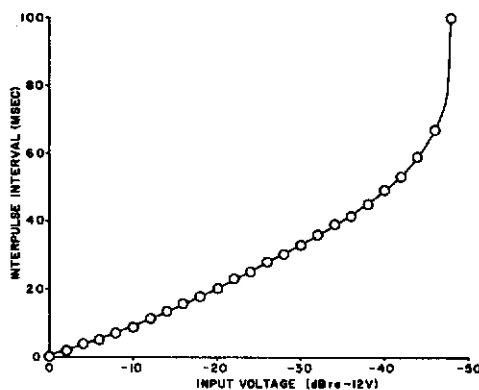


Figure 3. Encoder Performance Characteristic

the feedback impedance. The external voltage source and bias resistor determine the steady-state value of the output of the synapse section. The button transistor acts as a switch that is normally closed but opens when there is an input pulse to inject a current, whose value is determined by the external weighting voltage source, into the summing junction of the operational amplifier. The value of each of the two resistors in each button circuit is exactly one-half that of the feedback resistor of the operational amplifier. The RC feedback acts as an integrator and the output voltage begins to rise exponentially toward the weighting voltage. Since the input pulse is less than one-third as long as the time constant of the feedback impedance, the output is an exponential charging curve whose final value does not reach the weighting voltage, but is determined by it. When the feedback capacitance is increased, the final charging value reached during a pulse becomes proportionately less for the same weighting voltage since time constant of feedback impedance is increased. At the end of the pulse, the output of the synapse begins an exponential decay toward the steady-state bias value.

The output of the synapse circuit is connected to the patch panel and to the input of an encoder. The button circuits and the bias resistors are in patch cords for ease in programming the networks of these elements on a patch panel. The patch panel has eight holes for the summing junction of each syncoder and eight holes for the operational amplifier output of each syncoder, as well as enough holes to connect two blocks of buttons to the pulse output of each syncoder. The actual circuit diagram and description of encoder circuit operation are given in the appendix.

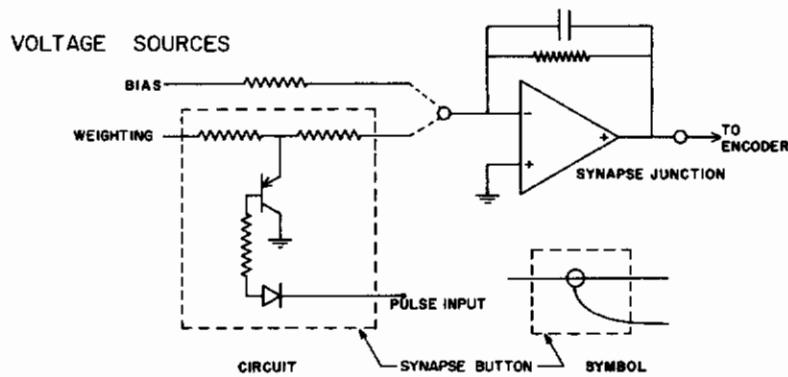


Figure 4. Synapse Block Diagram

For convenience in programming networks of syncoders, the symbols shown in figure 5 have been adopted to represent syncoders, synapse buttons, and voltage sources. The symbol resembling a triangle with two curved sides is used to represent a syncoder.

The number inside the syncoder symbol denotes the actual unit used. The number outside and to the right of the symbol denotes the value of the feedback capacitor (C) in microfarads. The upper point on the symbol is the output terminal of the operational amplifier. It may also be used as a voltage source, and is capable of supplying up to 25 synapse buttons with weighting

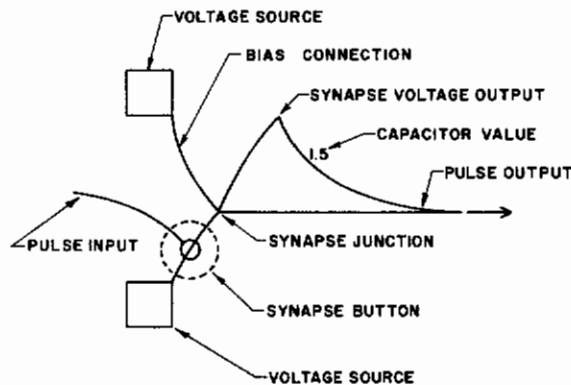


Figure 5. Syncoder Symbols

voltage. The lower lefthand point on the symbol is the summing junction of the operational amplifier. The lower righthand point is the pulse output of the syncoder which is the pulse input to synapse buttons. The square box represents a voltage source; the number inside identifies the voltage source used. The synapse button is represented by the two lines and the circle; the line that terminates on the circle is the pulse input connection. The line that runs through the circle is the input current path from voltage source to summing junction of the operational amplifier; the ends of this line are interchangeable.

If a line is connected from a voltage source (box) to the summing junction input of the syncoder without passing through a synapse button symbol, it represents a bias input and is a resistor equal in value to the feedback resistor.

Section III.

LOCATION AND DESCRIPTION OF CONTROLS

On the far left of the front panel (figure 6) of Root C is the patch panel, which contains 240 holes and will be described in detail in a later section. Immediately below the patch panel are, from left to right, the power indicator, the switch for the power supplies, and a switch marked FCN, the function switch connected to the patch panel, which will be described in the same section as the patch panel.

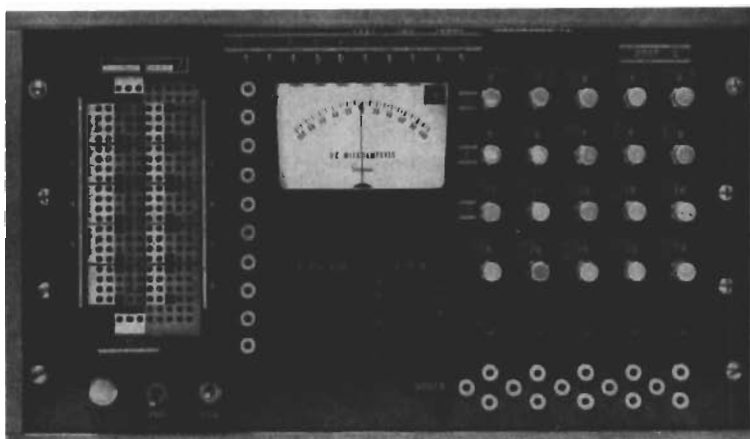


Figure 6. Root C Front Panel

The vertical row of jacks immediately to the right of the patch panel connect to the outputs of the operational amplifiers in each of the syncoders. Syncoder 0 is at the top with syncoder 9 at the bottom.

The operational amplifier on each syncoder can deliver 5 milliamps into an external load at ± 10 volts maximum with an output impedance of approximately 0 ohm.

The lights running from left to right across the top of the panel just above the panel meter are neon bulb indicators that flash each time the corresponding syncoder gives an output pulse. At the higher rates, it is not possible to distinguish individual pulses, but the brightness is approximately proportional to the firing rate of the syncoder.

Immediately below the neon lights is the panel meter. It is a zero-center meter calibrated over the range -100 to $+100$ microamperes and is connected in series with a 100 K resistor. Therefore, the range of the meter is from -10 volts to $+10$ volts. The movement is taut-band so there is no stiction problem. Negative is to the left and positive is to the right. The meter is connected to the appropriate point within the simulator by means of the two rotary switches immediately below it. The output of this pair of switches is also connected directly to the scope jack. The switch on the left is the function switch and is connected to separate decks of the switch on the right, which is the unit switch. Although the function switch has five positions, only four are used. The one most counter-clockwise is labeled J and corresponds to the operational amplifier output jacks of the syncoders. The next position is L, which is connected to the line inputs to the simulator. The middle position for the switch is the P0 position which connects the meter to the upper two rows of potentiometers, and the P10 position connects it to the lower two rows.

Contrails

The unit switch is labeled 0 through 9. To connect to potentiometer 7 (as an example), one would set the function switch to P0 and the unit switch to 7. To connect to potentiometer 18, one would set the function switch to P10 and the unit switch to 8.

In the upper right area of the front panel are the 20 potentiometers that are connected between the ± 12 volt power supplies in the simulator. The wiper arms on these potentiometers are connected to the patch panel and also to the meter switch as previously described.

In the lower right area of the front panel are 10 line jacks (light blue) and 5 ground jacks (light green). The ground jacks are connected to the common bus within the unit and the line jacks are connected to holes on the patch panel. The scope jack is dark blue.

Inside the top cover of the simulator is a small panel (figure 7) containing 11 five-way binding posts. The ten black ones are connected to the neon bulb outputs of each of the syncoders and are appropriately labeled. One row has the odd numbers 1, 3, 5, 7 and 9, and the other row has the even numbers 0, 2, 4, 6 and 8. The red post connects to an output circuit that consists of a diode, resistor, and capacitor, which then feeds the cable on the rear of the unit labeled "150 volts." This cable and output circuit are appropriately designed to drive the "+ GATE" input of the PDP-1 computer directly. This was originally used with the Roger's Grumpy Group Program. In order to use the output cable, one must connect a jumper from any one, BUT ONLY ONE, of the black posts to the red post. If nothing is connected to the red post, the output cable will be dead.

From the rear, (figure 8) the card file containing all of the printed circuit cards is on the top and the chassis containing the power supply is below it. The two cards to the left of the



Figure 7. Patch Panel Inside Top Cover

Contrails

center post are buffer stages to match the output pulses from the syncoders to the input circuitry of the synapse buttons. Each of the buffer cards has eight identical circuits. Two on the left card and all eight on the right card are used. The syncoder cards to the right of the center post are individually numbered 0 through 9 to indicate which circuit is connected to which set of holes on the patch panel. On the power supply chassis, going from left to right, are the ac line cord and 3 amp slow blow fuse, a plug marked "Control" that connects the power switch and pilot light on the front panel to ac power within the power supply. The next octal socket is a power output socket; the third socket is unwired. The power supply itself puts out ± 12 volts, ± 15 volts, and $+ 150$ volts to drive the neon lights. The 12- and 15-volt supplies are zener diode regulated; the neon supply is unregulated.

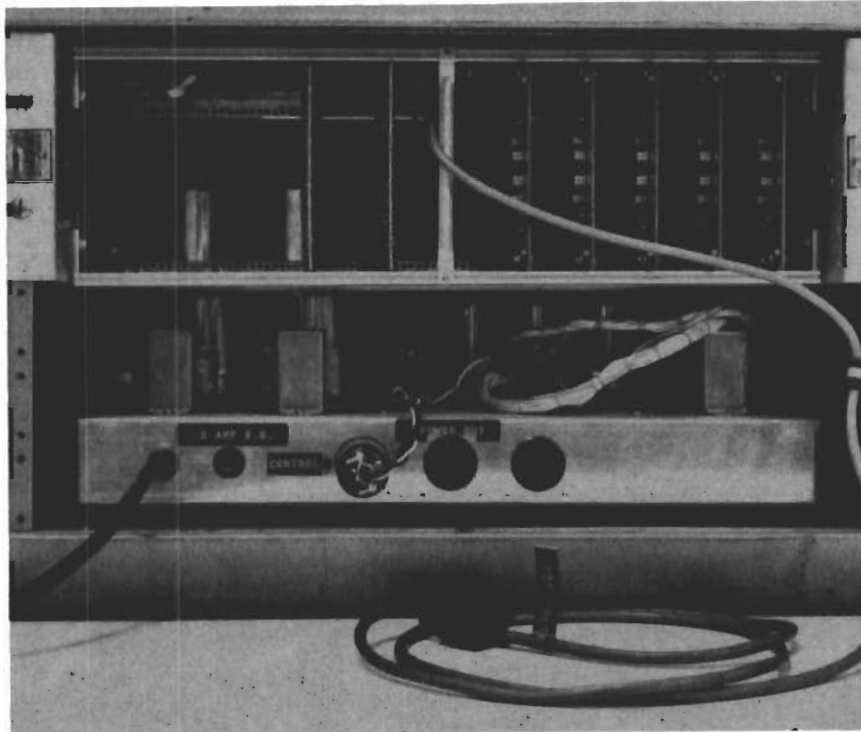


Figure 8. Rear View

Section IV.

PATCH PANEL LAYOUT

The patch panel (figure 9) is a 240-hole patch panel made by Amp, Inc, and is mounted with rows of 10 holes horizontally and 24 holes vertically. The color coding of the patch panel is as follows: the summing junction input to the syncoder operational amplifiers is yellow; the operational amplifier output is orange; the pulse output that drives the synapse buttons is purple; ground is black; the two sections of input lines, which are blue jacks in the lower right corner of the main panel, are red on the patch panel; the potentiometers are blue and also split up into two sections; the function switch is white.

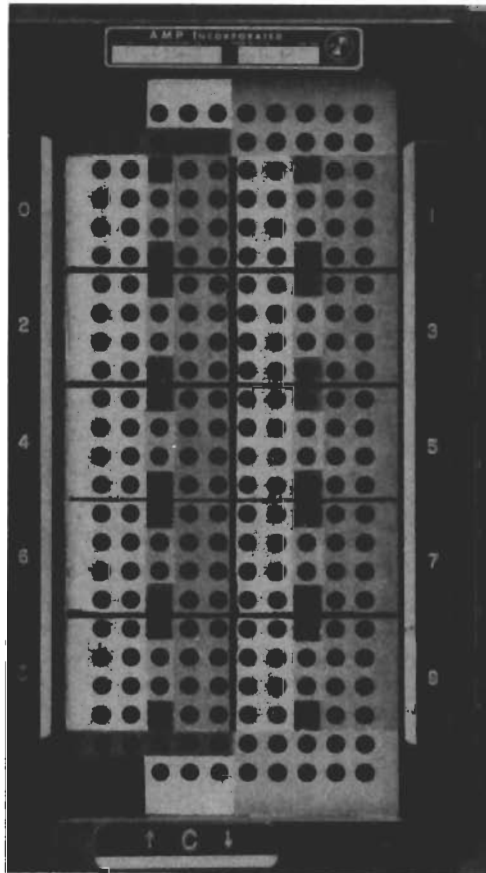


Figure 9. Patch Panel

The center hole of each of the white function switch sections is connected to the arm of the switch. When the handle of the switch is up, the hole on the left is connected to the center hole and when the switch is down, the hole on the right is connected to the center hole. The switch has a center off position and is double pole; each white area is connected to one pole.

The upper blue area on the patch panel corresponds to the upper two rows of pots; the lower area is connected to the lower two rows. The upper red area on the patch panel corresponds to the upper row of line jacks; the lower red area is connected to the lower row of line jacks.

Section V.

PATCH PANEL PLUG-IN ELEMENTS

There are three basic categories of plug-in elements (figure 10) for the patch panel: (1) plain wires; (2) wires with resistors and/or capacitors inserted; and (3) synapse blocks.

The plain wires are used for direct interconnections, such as a connection from an operational amplifier output to a line.

The wires with resistors (100 K $\pm 1\%$) are yellow with either a white or black piece of tubing in the middle. These are used as bias resistors and may be connected from a voltage source, such as a line input, a potentiometer, or an operational amplifier output, to the summing junction input of a syncoder.

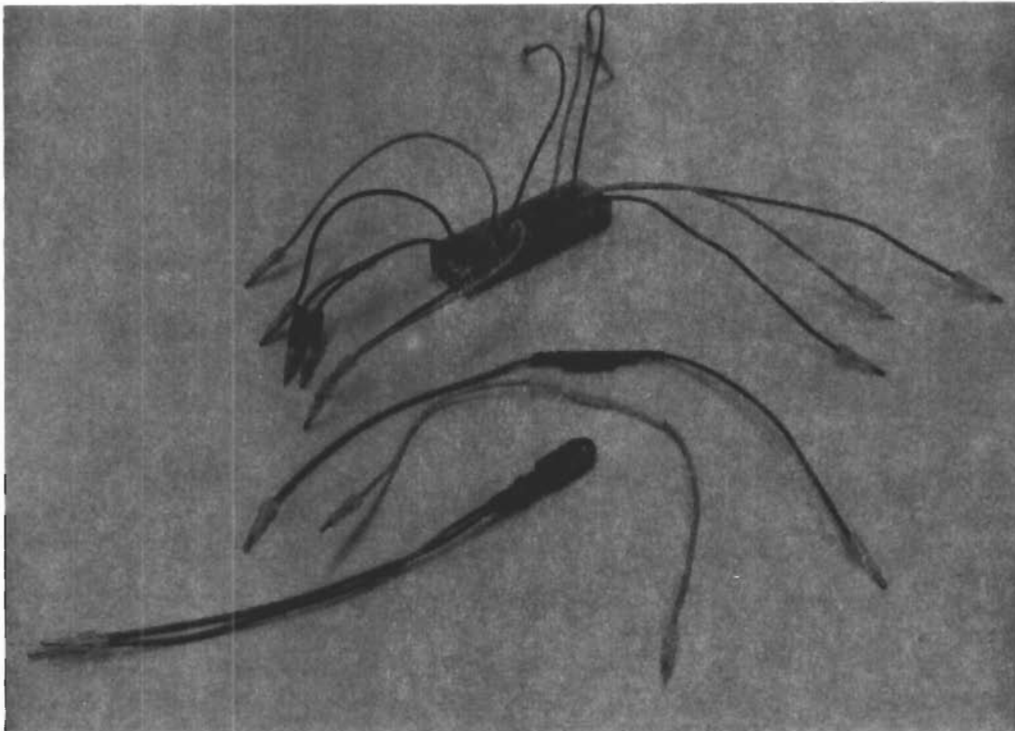


Figure 10. Plug-In Elements

The wires with capacitors are connected from the output to the summing junction input of the same operational amplifier. They should not be connected from one amplifier to another. The yellow wires with red tubing contain 1.5 microfarad nonpolarized capacitors; the yellow wires with blue tubing, 0.75 microfarad nonpolarized capacitors.

The green wire with red tubing contains an R-C network to permit use of a syncoder as a repeater, or interface, between the PDP-1 and Root C. In operation, it is connected from a line from the PDP-1 digital to analog converter, to the summing junction input of a syncoder.

The synapse blocks are epoxy encapsulated; each contains six synapse buttons driven by a common pulse input. To use a synapse block, the double plug is inserted into a pair of holes on

the patch panel so that the pulses from the panel are connected to the purple pin of the block and the patch panel ground is connected to the other pin. Each pair of wires (denoted by the same wire color approximately the same distance from the pulse input) connects to a button. One wire of each pair is connected to a summing junction input and the other connects to a voltage source, such as a line input, a potentiometer, or an operational amplifier output.

The restrictions on use of plug-in elements are summarized in the following table:

TABLE I. PERMITTED INTERCONNECTIONS

<i>Patch Panel Color</i>	<i>Yellow</i>	<i>Orange</i>	<i>Purple</i>	<i>Blue</i>	<i>Red</i>	<i>White</i>
Yellow	NO Capacitors*					
Orange	Resistors Synapse	NO				
Purple	Synapse Pulse	NO	NO			
Blue	Resistors Synapse Resistors	NO	NO	NO		
Red	Interface Synapse Resistors	Any	Any	Any [^]	Any	
White	Synapse Wire	Any	Any	Any [^]	Any	Any

Notes: *Only on same syncoder; not from one syncoder to another.

[^]Shorting the blue hole to ground will burn out the potentiometer.

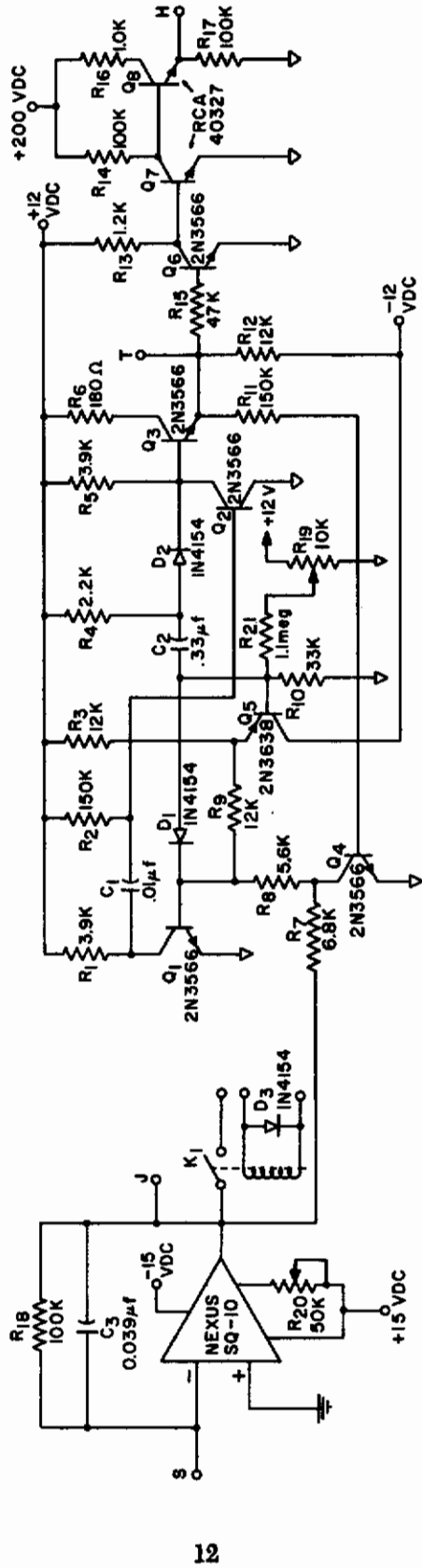


Figure 11. Encoder Circuit

Appendix

DESCRIPTION OF THE SYNCODER CIRCUIT

ENCODER

The neuron, or encoder, section of the syncoder performs the operation of conversion of an analog signal (voltage) into a train of identical, 1-millisecond duration, pulses.

In the encoder circuit shown in the accompanying illustration (figure 11), Q_1 is the threshold detector and is normally (no pulse) biased so that the collector current is zero. R_7 , R_8 , R_9 sum the exponential from R_{10} , R_{21} , C_2 , buffered by emitter follower Q_6 , with the input from "J." Q_4 is normally nonconducting, except during a pulse, at that time it locks-out the input signal to prevent shortening of the pulse length.

When the voltage at the base of Q_1 exceeds the base-emitter voltage, Q_1 conducts, thus turning off Q_2 by means of C_1 . The collector of Q_2 goes to 12 volts, as does the emitter of Q_3 and "T," which saturates Q_6 , which saturates Q_7 , which produces a positive 200-volt output pulse at "H," the emitter of Q_8 . During this same pulse, whose length is determined principally by R_2 , C_1 , C_2 charges primarily through D_1 and R_4 . By the end of the pulse, the voltage across C_2 is approximately 12 volts, which is the value from which the negative exponential starts at the end of a pulse (B). The final value toward which this exponential decays is determined by R_{10} , R_{21} , and the setting of R_{16} ; under normal conditions, this value is approximately zero. R_6 , and R_{16} are protection resistors inserted to protect the output transistors, Q_3 and Q_8 .

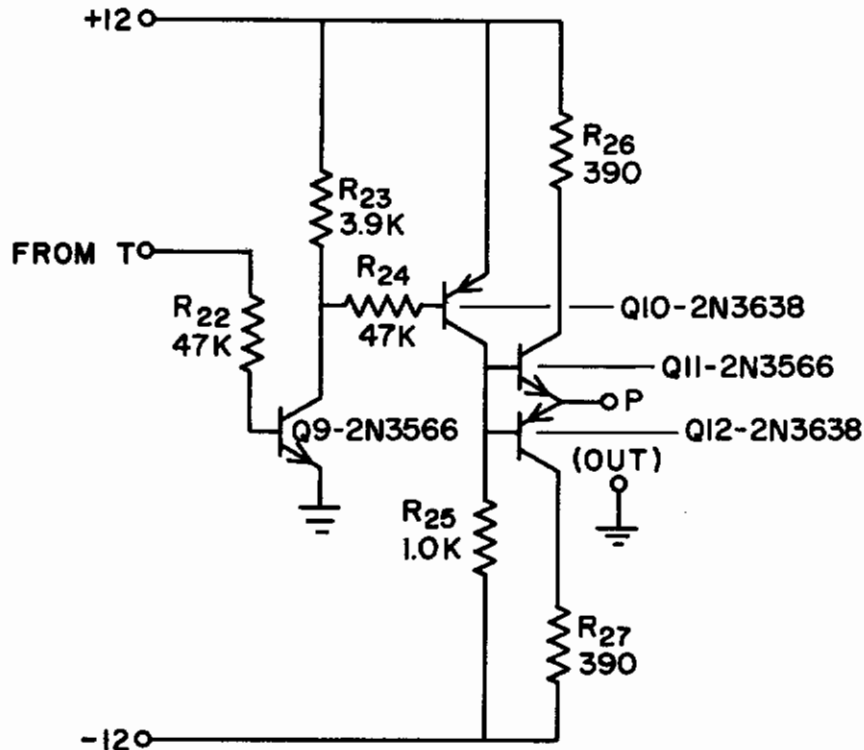


Figure 12. Buffer Circuit

BUFFER

The buffer circuit (figure 12) converts the zero to 12 volt pulses from "T" on the encoder to -12- to 12-volt pulses at P. The output current capabilities of emitter-followers Q₁₁ and Q₁₂, are adequate to drive several synapse blocks.

When T is at 0 volts, Q₉ and Q₁₀ are off and the output is at -12 volts. During a pulse, T rises to 12 volts; Q₉ saturates; Q₁₀ saturates; and the output at P is 12 volts. R₂₆ and R₂₇ are protection resistors used to limit the output current to a safe value.

SYNAPSE

The synapse section of a syncoder provides the transformation from pulses to an analog voltage which may be further processed in subsequent encoders. The synapse consists of two elements, one of which is the synapse junction composed of C₈, R₁₈, and the Nexus SQ-10 operational amplifier shown on the syncoder diagram. The other main element is a synapse button — its schematic is shown here:

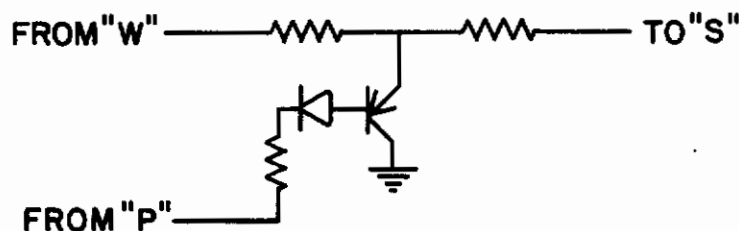


Figure 13. Schematic of Synapse Button

The transistor in the button is used as a switch, and is normally saturated. During a pulse, current flows from "W" to "S" — "W" here is any voltage source, including the "J" output of any syncoder. The feedback impedance of R₁₈ C₈ produces a waveform at "J" for a pulse, as shown in the diagram.

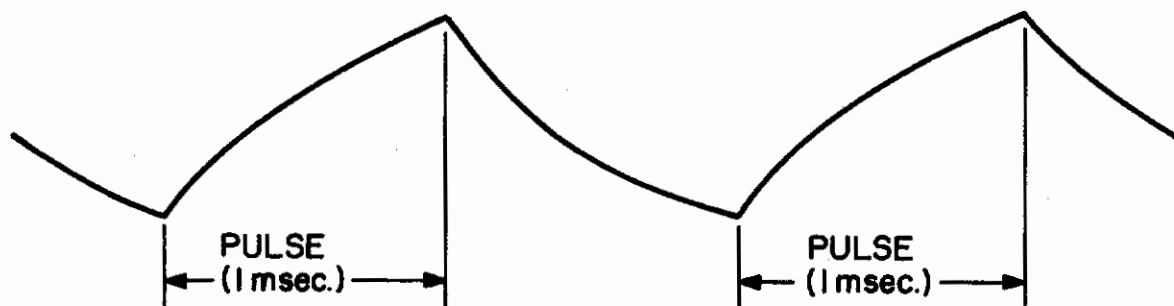


Figure 14. Diagram of Waveform Produced by Pulse Input

By controlling the magnitude and sign of "W," the effective weighting of each pulse may be changed at will, and the construction of self-adjusting networks made of these components can now be considered.

Contrails

<i>Component</i>	<i>Value</i>	<i>Tolerance</i>
A	Nexus SQ-10	
C ₁	0.01 mF	10%
C ₂	0.33 mF	5%
C ₃	0.039 mF	10%
D ₁₋₃	1N4154	
Q ₁₋₄	2N3566	
Q ₅	2N3638	
Q ₆	2N3566	
Q _{7, 8}	RCA 40327	
Q ₉	2N3566	
Q ₁₀	2N3638	
Q ₁₁	2N3566	
Q ₁₂	2N3638	
R ₁	3.9K	10%
R ₂	150K	10%
R ₃	12K	10%
R ₄	2.2K	10%
R ₅	3.9K	10%
R ₆	180	10%
R ₇	6.8K	5%
R ₈	5.6K	5%
R ₉	12K	5%
R ₁₀	33K	5%
R ₁₁	150K	10%
R ₁₂	12K	10%
R ₁₃	1.2K	10%
R ₁₄	100K	10%
R ₁₅	47K	10%
R ₁₆	1.0K	10%
R ₁₇	100K	10%
R ₁₈	100K	1%
R ₁₉	10K Trimpot	
R ₂₀	50K Trimpot	
R ₂₁	1.1 Meg	10%
R ₂₂	47K	10%
R ₂₃	3.9K	10%
R ₂₄	47K	10%
R ₂₅	1.0K	10%
R ₂₆	390	10%
R ₂₇	390	10%

Contrails

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) Aerospace Medical Research Laboratories Aerospace Medical Div., Air Force Systems Command Wright-Patterson Air Force Base, Ohio 45433		2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	
		2b. GROUP N/A	
3. REPORT TITLE DESIGN AND OPERATION OF ROOT C, A SMALL SYNCODER NETWORK SIMULATOR			
4. DESCRIPTIVE NOTES (Type of report and inclusive dates) Final Report, October 1964 - January 1967			
5. AUTHOR(S) (First name, middle initial, last name) Roger A. Gruenke, Captain, USAF J. Ryland Mundie, MD			
6. REPORT DATE May 1968	7a. TOTAL NO. OF PAGES 15	7b. NO. OF REFS 0	
8a. CONTRACT OR GRANT NO.		9a. ORIGINATOR'S REPORT NUMBER(S) AMRL-TR-67-236	
b. PROJECT NO. 7233			
c. Task No. 723303		9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)	
d.			
10. DISTRIBUTION STATEMENT Distribution of this document is unlimited. It may be released to the Clearinghouse, Department of Commerce, for sale to the general public.			
11. SUPPLEMENTARY NOTES		12. SPONSORING MILITARY ACTIVITY Aerospace Medical Research Laboratories Aerospace Medical Div., AF Force Systems Command, Wright-Patterson AFB, OH 45433	
13. ABSTRACT A syncoder is an electronic model of some of the information processing properties of nerve cells. This report describes the equations of operation of a single syncoder and serves as an instruction manual for the programming and operation of a network simulator containing 10 syncoders. The network simulator, called "Root C," also contains a patch panel, voltage sources, a meter, and the necessary input-output lines to permit the simulation of small networks of syncoders. An appendix contains a complete circuit description of a single syncoder.			

DD FORM 1473
1 NOV 65

Security Classification

Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Bionics Neuron model Neural network simulator Hybrid computer Neural computer Neural logic						

Security Classification