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# FOREWORD

This investigation was accomplished by Battelle Memorial Institute, Columbus, Ohio under Contract No. AF 33(616)-6375 sponsored by the 6570th Aerospace Medical Research Laboratories. Mr. R.G. Cameron of the Simulation Techniques Branch, Training Research Division of the Behavioral Sciences Laboratory served as contract monitor. This contract was initiated in support of Project 6114, "Simulation Techniques for Aerospace Crew Training" and Task 611408, "Simulation Computers."

The results are the culmination of a program begun in April 1959 and completed in April 1963.

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ABSTRACT

This report describes the development of fabrication techniques for construction of a silicon Hall effect element with characteristics suitable for application in an analog multiplier. The relative merits of various semiconductor materials are considered, and the reasons for the selection of silicon are outlined. The considerations necessary for the design of the element package structure are developed, and the tests required to characterize the Hall element in terms of electronic design parameters are also developed.

Approximately 24 successful silicon elements were processed, and three pairs were mounted in suitable magnetic structures so as to obtain complete element packages. Experimental transistorized circuitry was constructed for use with these element packages in order to exhibit the ability of the silicon Hall device to multiply.

PUBLICATION REVIEW

This technical documentary report has been reviewed and is approved.

Walter F. Grether
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Technical Director
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## EXPLANATION OF TERMS

| | |
|---|---|
| $V_H$ | Hall voltage, volts |
| $R_H$ | Hall coefficient, $cm^3$/coulomb |
| I | Current in element, amperes |
| B | Magnetic field, guass |
| a | Hall-element length |
| b | Hall-element width |
| t | Hall-element thickness |
| r | Hall coefficient factor, dimensionless |
| n | Charge-carrier (or electron) concentration, $cm^{-3}$ |
| q | Charge on the electron, $1.6 \times 10^{-19}$ coulomb |
| $\rho$ | Resistivity, ohm-cm |
| $\mu$ | Charge-carrier mobility, $cm^2$/volt-sec |
| T | Temperature, degrees C |
| d | Hall tab length |
| $R_{input}$ | Hall-element input resistance |
| $R_{output}$ | Hall-element output resistance |
| $R_{tab}$ | Hall-element tab resistance |
| $V_m$ | Calculated potential difference between Hall tabs per mil of Hall tab misalignment with $2 \times 10^{-3}$ amp input current and zero magnetic field |
| $V_{mi}$ | Potential difference between Hall output terminals measured with $2 \times 10^{-3}$ amp input current and zero magnetic field before Hall tab adjustment |
| $V_{mo}$ | Potential difference between Hall output terminals measured with $2 \times 10^{-3}$ amp input current and zero magnetic field after Hall tab adjustment |
| $\delta$ | Specific contact resistance, ohm-$cm^2$ |
| $R_c$ | Contact resistance, ohms |



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| | |
|---|---|
| $I_2$ | Hall-element current in Element (2), amperes |
| $V_{H2}$ | Hall output voltage from Element (2), volts |
| $R_{H2}$ | Hall coefficient of element (2) |
| c | $10^{-8}/t$ a constant for a given element, $cm^{-1}$ |
| G | Proportionality factor B/input to power amplifier, gauss/volt |
| K | Thermal conductivity of Hall-element material, $\frac{watts}{cm\text{-}^\circ C}$ |
| A | Area of the element |
| P | Input power to the element |
| $K_1$ | Thermal conductivity of insulating material, watts/cm-°C |
| $\tau_1$ | Thickness of insulation, cm |
| $\sigma$ | Conductivity, $(ohm\text{-}cm)^{-1}$ |
| $\Lambda$ | Function of b/a |



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# DEVELOPMENT OF AN ANALOG MULTIPLIER, BASED ON THE HALL EFFECT

## INTRODUCTION

The multiplication of two quantities is a nonlinear operation, and therefore is one of the more difficult analog functions. Although a wide variety of multiplying methods have been suggested and devised during the past years, only a few are commonly used. One of today's commonly used methods is the potentiometer multiplier wherein one variable is introduced as the voltage across the potentiometer, the sliding arm is positioned proportional to the second variable, and the product is read out as the voltage of the moving arm. Various other methods employ nonlinear electronic elements interconnected in proper sequence to approximate the product. Finally, a train of pulses modulated in both width and amplitude may be used as the input to an integrating circuit whose output is the desired product. The majority of these methods have been capable of multiplying within certain limits of accuracy and speed; however, difficulties of manufacture, complexities of maintenance, and excessive original equipment costs have led to the need for other methods.

The basic nonlinearity of analog multiplication precludes the use of feedback stabilization techniques and forces the designer of an analog multiplier to seek a basic physical phenomenon that naturally implements multiplication. The Hall effect in semiconductor materials is such a natural phenomenon. When exhibited in sufficient magnitude, this effect is attractive for multiplier application. Also, the Hall effect naturally provides a "four-quadrant" product since the algebraic sign of the output voltage is properly dependent on the signs of the inputs. This report describes an investigation of the application of the Hall effect for an analog multiplier.

## THE HALL EFFECT AND ITS APPLICATION TO ANALOG MULTIPLICATION

The Hall effect, discovered in 1879, has for many years been an important tool in research on the electrical properties of solids. It has been particularly useful in the study of semiconductors.*

The rudiments of the Hall effect may be understood with the aid of Figure 1 which depicts a parallelopiped sample of a solid electrical conductor. An electrical current I flows through the sample in a longitudinal direction. The sample is situated in a magnetic field B, normal to the direction of current flow. Under these conditions, an electric field $E_H$ (the Hall field) is developed between the edges of the sample in a direction normal to both I and B. The electric charge (comprising the current) moving in a magnetic field is deflected by Lorentz forces to one side of the sample. Charge is accumulated at the sides of the sample until the Hall field, $E_H$, which it creates, exactly opposes the Lorentz force on the moving charges.

* More detailed discussions of the Hall effect than that which follows may be found in numerous sources, e.g., References 1 and 2.

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The potential resulting from the Hall field is known as the Hall voltage and is given by

$$V_H = \frac{R_H \, I \, B \times 10^{-8}}{t} \text{ volts*}, \tag{1}$$

where

$R_H$ = Hall coefficient, $cm^3$/coulomb

$I$ = current, amperes

$B$ = magnetic field, gauss

$t$ = element thickness, cm.

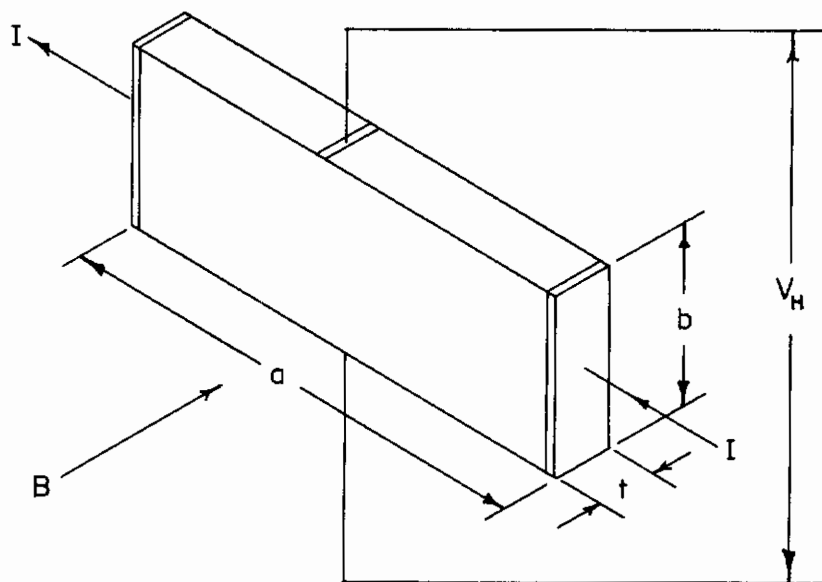


FIGURE 1. SKETCH OF A BASIC HALL ELEMENT

When one type of charge carrier (for example, electrons) dominates electrical conduction in the sample, the Hall coefficient is given by

$$R_H = r \frac{1}{nq}, \tag{2}$$

where

$r$ = dimensionless hall coefficient factor of the order of unity.

$n$ = electron concentration, $cm^{-3}$

$q$ = charge on the electron = $1.6 \times 10^{-19}$ coulomb.

* All symbols are defined in the Explanation of Terms at the beginning of the report.



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Equation (2) reveals that the Hall coefficient is inversely proportional to charge-carrier (electron) concentration.

Based on Equation (1) it can be shown how analog multiplication can be accomplished with the Hall effect. Of the parameters on the right-hand side of the equation, t is a constant in a given Hall element, and $R_H$ is related to the charge-carrier concentration in the Hall-element material and to its environment. Thus, if $R_H$ can be held invariant or if its variations can be compensated, then $V_H$ is proportional to the product of I and B, which are independent variables in Equation (1). With I and B, representing the multiplier and multiplicand, as electrical and magnetic inputs to the system, $V_H$ is an electrical output representing their instantaneous product.

Analog multiplication by the Hall effect in semiconductors has been the subject of several papers in recent years.[3-8]

## ERROR SOURCES IN HALL-EFFECT MULTIPLIERS*

There are several sources of potential errors in the Hall multiplication process. These involve Hall-element characteristics in which there is a dependence of $R_H$ in the Hall voltage expression on both the intensity of the magnetic field, B, and on the temperature of the element. Thus, the value of $R_H$ is not constant but is dependent on one of the input variables. To a much lesser degree, $R_H$ is also dependent on other element parameters, as will be discussed in a later section of the report.

Another source of error is the possible nonlinear relationship which may exist between the input variable, represented by the exciting current of the magnetic circuit, and the resulting flux density, B, in the element. This is brought about by the nonlinearities in the magnetic circuit.

All of these problems must be dealt with in the design of a precision Hall multiplier. In the sections of the report which follow, means are shown for reducing the errors created by these effects to a minimum.

As pointed out, if the two variables to be multiplied are represented by the Hall-element current, I, and the magnetic flux density, B, in the element, the Hall voltage, $V_H$, represents their product, since $R_H$ and t are relatively constant under ideal conditions. The major problems are: to design a Hall element in which $R_H$ is as nearly constant as possible over the operating range, to design excitation circuits which produce an element current and a magnetic field in the element which are linearly related to the two input variables to be multiplied and to design a readout circuit which delivers an output proportional to the Hall output voltage. These problems are considered in the following sections of the report.

*Means for error correction are discussed in Appendix F.



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## ENGINEERING INVESTIGATION

### Consideration of Materials for the Hall Multiplier Element

In this project, a survey was made of five semiconductor materials – silicon (Si), germanium (Ge), gallium arsenide (GaAs), indium antimonide (InSb), and indium arsenide (InAs) – to determine their suitability for the required Hall multiplier element. With one exception, these materials were selected for consideration because they could be prepared with reasonably well-controlled electrical properties, and because they were available commercially. Both factors are important if production is contemplated. At the time the initial survey and selection was made, GaAs fulfilled neither requirement. It was included for consideration because it seemed to offer some interesting potentiality and was the subject of extensive research effort.

It was further desirable that techniques for mechanically working and electrically contacting the candidate materials be in an advanced state of development.

Table 1 lists pertinent data from published and unpublished literature on the materials in question.* Included in the table are the quantities $R_H/\rho^{1/2}$ and $\mu^2$, which may be considered figures of merit for a Hall multiplier element operating respectively in the voltage-output mode and the power-output mode. They are useful for preliminary evaluations of one type of material relative to another in a given operating mode.

Specifications on the multiplier called for 1/2 per cent maximum error over the full range of current and magnetic field and operation in ambient temperatures ranging from 16 to 38 C. The properties of semiconductors are generally temperature dependent and often magnetic field dependent. Thus, it was important to give consideration to these factors. The last four columns in the table list the fractional changes in $R_H$ and $\rho$ per unit change in temperature and magnetic field.

### Selection of Material and Operating Mode

The requirements for a Hall multiplier element are that the material have a large figure of merit for the proper mode of operation and that the Hall coefficient and resistivity be as insensitive as possible to changes in temperature and magnetic flux density. Given the temperature range of 16 to 38 C and assuming a range of magnetic flux density, B, of 0 to 10 kilogauss, $\Delta R_H/(R_H \Delta B)$ must be less than $5 \times 10^{-7}$ gauss$^{-1}$; and $\Delta R_H/(R_H \Delta T)$ must be less than $2.3 \times 10^{-4}$ C$^{-1}$ if all of the allowable 1/2 per cent error is considered to result from the variation of the Hall coefficient with change in either magnetic flux density or temperature. The allowable variation of $\rho$ is not as evident, because most of the materials would produce a low-resistance element that would require an external fixed series resistor if the element were to be driven directly by the maximum specified 2-milliampere input current. In this case, the resistivity variations would exceed the tolerable level only for the high-resistivity silicon material. If the element current is to be supplied by an amplifier, however, as it would need to be

*The data in Table 1 do not cover the full range of properties that each material can exhibit. They are confined property ranges of potential suitability to the application.



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TABLE 1. HALL-ELEMENT MATERIALS CHARACTERISTICS[a]

| Material | $R_H$, $cm^3$/coulomb | $\mu$, $cm^2$/volt-sec | $\rho$, ohm-cm | n, $cm^{-3}$ | $R_H/\rho^{1/2}$[b] | $\mu^2$[c] | $\Delta R_H/R_H \Delta T$ | $\Delta R_H/R_H \Delta B$ | $\Delta\rho/\rho\Delta T$ | $\Delta\rho/\rho\Delta B$ |
|---|---|---|---|---|---|---|---|---|---|---|
| n-Si | $2.99 \times 10^5$ | 1,900 | 160 | $2.5 \times 10^{13}$ | 23,640 | $3.61 \times 10^6$ | L[d] | $3 \times 10^{-6}$ above 7 k gauss | $3 \times 10^{-3}$ | --[e] |
| n-Si | $4.7 \times 10^4$ | 1,770 | 27 | $1.6 \times 10^{14}$ | 9,050 | $3.50 \times 10^6$ | -- | (1/2 %) | -- | $4.8 \times 10^{-6}$ |
| n-Si | $3.3 \times 10^3$ | 1,750 | 1.9 | $2.2 \times 10^{15}$ | 2,400 | $3.06 \times 10^6$ | -- | L | -- | $2.8 \times 10^{-6}$ |
| n-Ge | $3.34 \times 10^4$ | 3,760 | 8.89 | $1.9 \times 10^{14}$ | 11,200 | $14 \times 10^6$ | -- | (1/4 %) | -- | $1.6 \times 10^{-5}$ |
| n-Ge | $4.47 \times 10^3$ | 3,000 | 1.58 | $1.6 \times 10^{15}$ | 3,600 | $9 \times 10^6$ | L | L | $2.2 \times 10^{-3}$ | $2 \times 10^{-5}$ |
| GaAs | $1.67 \times 10^3$ | 8,520 | 0.196 | $4.4 \times 10^{15}$ | 3,800 | $72.6 \times 10^6$ | $9 \times 10^{-4}$ | -- | $3 \times 10^{-3}$ | -- |
| GaAs | 15 | 3,300 | $4.5 \times 10^{-3}$ | $5 \times 10^{17}$ | 223 | $10.9 \times 10^6$ | $1.5 \times 10^{-4}$ | -- | -- | $7 \times 10^{-7}$ |
| InSb | 70 | 37,780 | $1.64 \times 10^{-3}$ | $1.1 \times 10^{17}$ | 1,729 | $1427 \times 10^6$ | -- | -- | L | -- |
| InSb | 19 | 32,700 | $6 \times 10^{-4}$ | $3.3 \times 10^{17}$ | 800 | $1069 \times 10^6$ | $3.3 \times 10^{-4}$ | $8.2 \times 10^{-7}$ | $1.6 \times 10^{-3}$ | -- |
| InAs | 62 | 27,000 | $2.3 \times 10^{-3}$ | $9 \times 10^{16}$ | 1,329 | $734 \times 10^6$ | $4.5 \times 10^{-5}$ | $3.5 \times 10^{-6}$ | $1.8 \times 10^{-3}$ | -- |

(a) All symbols are defined in the Explanation of Terms.
(b) Figure of merit for voltage-output mode.
(c) Figure of merit for power-output mode.
(d) L indicates too small to determine from available data.
(e) -- indicates that data were not available.



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for the high-mobility materials, the variations of $\rho$ with temperature and magnetic flux density would be subject to the same restriction as variations of $R_H$ as noted above. The data in Table 1 show that none of the materials studied are adequate, although InAs would be marginal if a smaller range of $\Delta B$ were used. Therefore, it is clear that compensation for the effects of variations of $\rho$ is required for a satisfactory multiplier. This is a result of the inherent temperature dependence of the mobility and charge-carrier density. In some cases, compensation would also be required for the effects of variations of $R_H$.

Assuming that these variations can be compensated, the best material for voltage output has the highest value of $R_H/\rho^{1/2}$ and, for power output, the highest value of $\mu^2$. The multiplier must operate into an operational amplifier at a sufficient voltage level to yield an adequate signal-to-noise ratio. In order to provide adequate signal-to-noise ratio in the multiplier output, a minimum value of 1/2 volt out is required when maximum values are applied to the multiplier inputs.

Hall voltages greater than 1/2 volt could easily be obtained with the best voltage-output materials and the maximum specified 2-milliampere input current, but these materials cannot supply the output current required in the multiplier specifications without an output amplifier. On the other hand, while the power-output materials could supply the current required, adequate voltage output can be achieved only with a very high input current so that an input amplifier would be required. For a given voltage output, the power-output materials must dissipate more power resulting from the input current than the voltage-output materials would, because of the considerably larger input current required. This increased power dissipation would result in added problems with respect to the variation of the Hall voltage output with temperature change.

Since an amplifier is required, regardless of the mode of operation, the voltage-output mode was chosen on the basis of increased stability with temperature. There is little difference between the temperature characteristics of silicon and germanium, so the choice of silicon is based mainly on the higher Hall coefficient of silicon. Gallium arsenide appears to have some promising characteristics, but too much development was thought to be required before it could be used in a device. In view of the above considerations, n-type silicon with a low carrier concentration was considered to be the logical choice for the Hall-element material.

## Design and Fabrication of Silicon Hall Elements

Initial efforts on multiplier design were directed towards the utilization of Hall elements 0.004 inch thick. In the course of developing such elements, it became apparent that their successful fabrication and utilization would require the solution of several surmountable but nevertheless very difficult technological problems. This initial work also revealed design deficiencies relating to output lead positioning and attachment on the elements. Subsequent work led to the use of a thicker Hall element of somewhat different design than initially conceived. It is this final design that is discussed in detail in the following sections.



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## Electrical and Geometrical Considerations

The electrical characteristics and the geometrical configuration of a Hall element are closely associated. Therefore, it is necessary to consider both factors simultaneously in the design of a Hall element to achieve a specified performance. For the Hall element in question, several specifications were assigned from which all other design factors were determined. These specifications were:

Maximum input current – $2 \times 10^{-3}$ ampere

Maximum magnetic field – 10,000 gauss

Input impedance – 16,500 ohms minimum

Output impedance – ~6,500 ohms

Output voltage ($V_H$) – 1.5 volts at maximum magnetic field and current

Output voltage with zero magnetic field and maximum input current – $13 \times 10^{-3}$ volts maximum

Hall element thickness – 8 to $12 \times 10^{-3}$ inch.

To minimize breakage from handling and to ease the difficulties associated with preparing good ohmic contacts to the element, a thickness of 0.012 inch was decided upon. The assigned element thickness then dictated the material requirements to achieve a Hall voltage output of 1.5 volts. A calculation shows that a silicon bulk resistivity of about 160 ohm-cm is required to give 1.5 volts output for the element thickness selected.

With the maximum output voltage fixed, the input impedance is related to the material resistivity and element dimensions. To obtain the desired value of input impedance, the element dimensions and configuration shown in Figure 2 were selected.

If the ratio of width to length in a Hall element (b/a in Figure 2) is too large, the input current contacts partially short the Hall electric field with the result that the Hall voltage is reduced below its theoretical value. With $b/a \leq 0.25$, the observed Hall voltage is at least 96 per cent of its theoretical value.* Thus, the final element dimensions were influenced by the required input impedance, the need for $b/a \leq 0.25$, and the desirability to keep the element area substantially less than the magnetic core cross-sectional area. The last requirement aids in the achievement of uniform flux density in the elements and provides room for gap-spacer mounting.

The Hall tab width was selected primarily for mechanical strength and ease of fabrication.

The output impedance specified for the element is not compatible with the other specifications, since it does not account for spreading resistance at the output terminals. As will be discussed later, output impedances in finished elements were 20,000 to 30,000 ohms. That these values are reasonable is shown by a calculation of the expected output impedance presented in Appendix A of this report.

*Löfgren[4] has carried out a quantitative analysis which, when applied to the present problem, confirms the suitability of $b/a = 0.25$.



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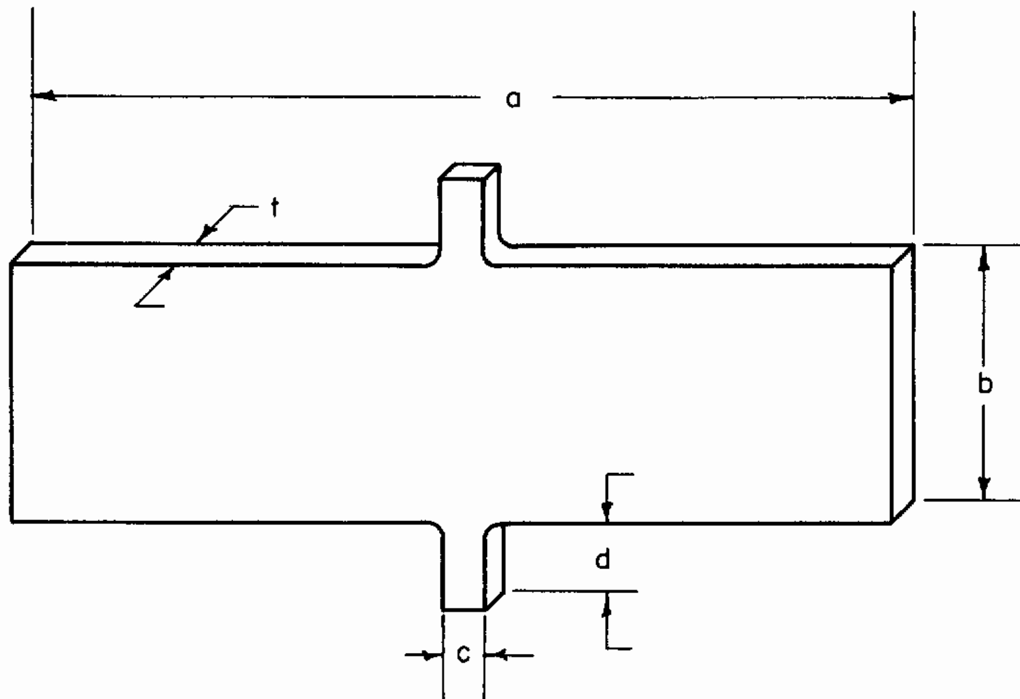


a = 0.625"
b = 0.1562"
c = 0.025"
d = 0.035"
t = 0.012"

Note: Drawing not to scale

FIGURE 2. CONFIGURATION AND DIMENSIONS USED FOR THE SILICON HALL MULTIPLIER ELEMENT



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Another factor that could influence the output impedance is the mechanical adjustment used to reduce any misalignment in the Hall tabs. A considerable variation in output impedance could arise between elements as a result of the mechanical adjustment method used. (This method is described in the fabrication procedure for Hall elements given in Appendix B.)

Important Bulk Properties of Single-Crystal Silicon Ingots

Multiplier design provides for the Hall element to operate in voltage-output mode. This calls for a high Hall coefficient, which in turn requires a low charge-carrier concentration. It is important that this be achieved with high-purity material having a single type of charge carrier dominant in order that the temperature and magnetic field stability of pertinent properties not be degraded.

Another important bulk property in the single-crystal silicon from which the elements are to be made is uniformity of charge-carrier concentration, both radially and longitudinally in the crystal. Radial carrier gradients could introduce a nonlinearity in the Hall voltage as well as increase the magnitude of the resistive component of voltage occurring at the Hall terminals at zero magnetic field. The latter voltage would be difficult to separate from the voltage developed through the misalignment of the Hall tabs unless the nature of the concentration gradient was known. Also, the input power dissipation could become heterogeneous, thereby compounding the above effects.

A longitudinal carrier concentration gradient could limit production yield of uniform elements. From the standpoint of reproducibility, a close tolerance must be maintained on the carrier concentration variations along the crystal.

To reduce the possibility of variations between elements, the silicon bulk material should be as strain-free as possible. The dislocation and oxygen density in silicon does not appear to play a major role in affecting the Hall-element operation. However, it was planned to make elements from a silicon crystal grown by the float-zone technique (having low oxygen content and high dislocation density) and from a crystal grown by the Czochralski technique (having high oxygen content and low dislocation density).

In the purchase of the silicon single crystals from the supplier*, the following specifications were set forth for both the float-zone and Czochralski-grown material:

Conductivity type – n-type

Resistivity – 160 ohm-cm ±5 per cent over several inches of crystal

Orientation – < 111>

Radial charge-carrier gradient – minimum

Crystal diameter – 0.75-inch minimum

Minority carrier lifetime – >100 microseconds.

*Dow Corning Corporation, Hyper-Pure Silicon Division, Hemlock, Michigan.



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The specifications given were more rigid than a supplier would normally expect for other device structures. The Hall-element length required that the ingot diameter be not less than about 0.75 inch.

Although the Hall-effect device is a majority carrier device, nevertheless a specification on the minority carrier lifetime was given for the purpose of obtaining the most perfect crystals possible. The lifetime value can be used to some extent as a means of denoting the quality of silicon, since the lifetime is sensitive to defect density.

Figure 3 is the resistivity profile for both the float-zone and Czochralski crystals. The profile shown for the float-zone crystal, designated as 02-0109, was determined at Battelle and was found to agree with the supplier's data. The profile shown for the Czochralski crystal, designated as H-145, was received from the supplier. In view of the close agreement between measurements on the float-zone crystal, it was felt that a remeasurement at the Battelle laboratories for this crystal would not be required.

Crystal 02-0109 met the resistivity specification set forth quite well, whereas the resistivity of Crystal H-145 was considerably higher and nonuniform.

Designated on the curves are the sections of each crystal used in the processing of Hall elements. Also shown is the section taken from H-145 for the preparation of a test specimen for contact-resistance measurements.

It was expected that Crystal 02-0109, having a flat resistivity profile over a reasonable length, would give a high yield of Hall elements having uniform characteristics. However, as will be shown later, a number of elements prepared from the center section of the ingot exhibited a high input resistance value. The cause of this effect is discussed in Appendix C. Crystal H-145 should yield higher Hall output voltages on the basis of its resistivity.

## Calculated Hall-Element Characteristics

To ascertain the expected characteristics of Hall elements prepared with the design features and material discussed above, the value of the Hall voltage, input impedance, output impedance (at zero output current), and the Hall tab misalignment voltage at zero magnetic field were calculated.

Table 2 summarizes the results for each silicon crystal. Three resistivity values are included in the calculations for Crystal H-145 because of its large resistivity gradient. (See Figure 3.)

The results indicate that Crystal 02-0109 would give the 1.5-volt Hall output required. The misalignment voltage shows that the Hall tabs must be aligned to within about 0.1 mil to meet the specifications of the 0.013 volt set forth. As can be seen, the misalignment voltage becomes greater with higher resistivities, making the precision correspondingly more critical.


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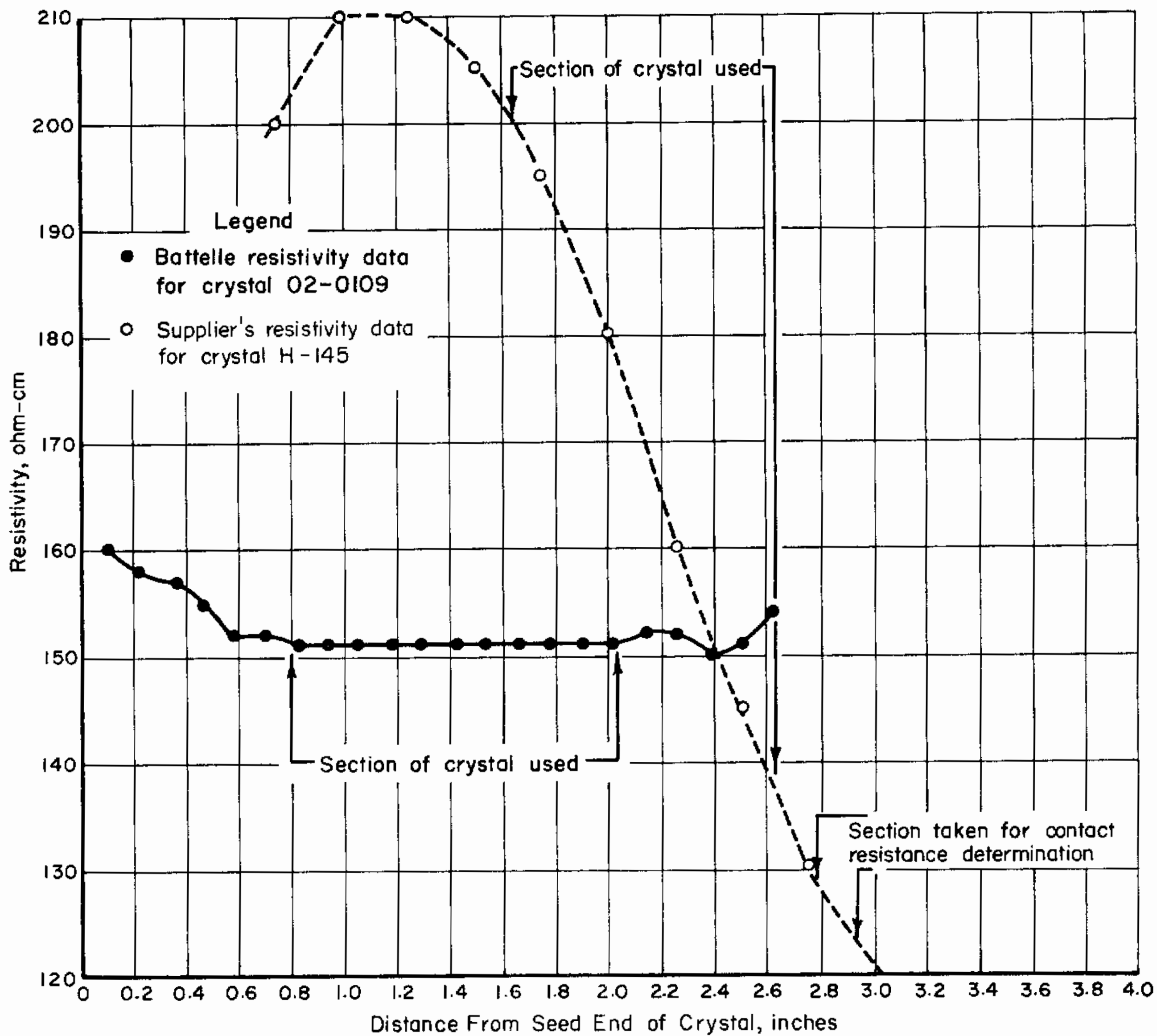


FIGURE 3. RESISTIVITY PROFILES FOR SILICON CRYSTALS USED IN HALL-ELEMENT FABRICATION



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TABLE 2. CALCULATED HALL-ELEMENT CHARACTERISTICS

| Crystal Designation | $\rho$(a), ohm-cm | $\mu$(b), $cm^2$/volt-sec | n(c), $cm^{-3}$ | $R_H$(d), $cm^3$/coulombs | $V_H$(e), volts | $R_{input}$(f), ohms | $R_{output}$(g), ohms | $V_{mi}$(h), volts/mil |
|---|---|---|---|---|---|---|---|---|
| H-145 (Czochralski) | 200 | ≈1530 | $2.0 \times 10^{13}$ | $3.67 \times 10^5$ | 2.42 | $26.0 \times 10^3$ | $36.4 \times 10^3$ | 0.083 |
| | 155 | ≈1520 | $2.63 \times 10^{13}$ | $2.37 \times 10^5$ | 1.55 | $20.5 \times 10^3$ | $28.2 \times 10^3$ | 0.065 |
| | 135 | ≈1500 | $3.07 \times 10^{13}$ | $2.02 \times 10^5$ | 1.32 | $17.8 \times 10^3$ | $23.5 \times 10^3$ | 0.057 |
| 02-0109 (Float zone) | 151 | ≈1510 | $2.74 \times 10^{13}$ | $2.26 \times 10^5$ | 1.48 | $19.8 \times 10^3$ | $27.4 \times 10^3$ | 0.064 |

(a) From silicon crystal resistivity profiles (see Figure 3).
(b) From Cronemeyer[9] using appropriate room-temperature resistivities.
(c) Calculated from $n = 1/(\rho q \mu)$.
(d) Calculated from Equation (2) with $r = 3\pi/8$.
(e) Calculated from Equation (1) with B = 10,000 gauss, $I = 2 \times 10^{-3}$ ampere.
(f) Calculated from $R_{input} = \rho a/bt$.
(g) Calculated from $R_{output} = 2.30\rho/t + 2 R_{tab}$ (see Appendix A).
(h) Output voltage expected per mil of Hall tab misalignment (if no other factors are considered) with 2.0 milliamperes input current and zero magnetic field.



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Hall-Element Fabrication

A series of Hall elements was fabricated from a portion (designated in Figure 3) of each silicon crystal. Details of the fabrication procedure are given in Appendix B. A study of the Hall-element contact resistance is discussed in Appendix D.

Electrical Properties of Fabricated Hall Elements

To obtain useful information on the Hall-element yield and uniformity, each element prepared from both silicon ingots was evaluated.

Table 3 is a tabulation of room-temperature d-c electrical data taken for Hall elements prepared from Crystal 02-0109 (float-zone silicon). The input and output resistance values were measured to the nearest 500 ohms. All output resistance values were determined after lead attachment and the misalignment adjustment operation (see Appendix B) except where otherwise noted. The input resistance values were measured before and after lead attachment and found to be consistent. Included in the table are the values of the misalignment voltage for each element before ($V_{mi}$) and after ($V_{mo}$) adjustment except where breakage prevented this measurement.

Table 4 is a similar tabulation for the Hall elements prepared from Crystal H-145 (Czochralski).

The data obtained on the Hall elements from each crystal reveal several significant factors that were not anticipated. These factors are discussed in the following:

(1) The most significant finding was the anomalous behavior of the input resistance found for Elements 25 through 40 prepared from Crystal 02-0109. A gradual increase in the resistance to a maximum value followed by a decrease to an apparently normal value was noted. Hall elements 41 to 46 showed a normal value of input resistance; however, the output resistance was somewhat higher than the values obtained for the remainder of the elements. The behavior of this group of elements was studied further and is discussed in Appendix C.

(2) The mechanical-adjustment method used to correct the misalignment Hall voltage (resistive zero magnetic field component) was not found to increase the input resistance significantly. This is demonstrated by comparing the output resistance data from those elements which were unadjusted with those which were adjusted.

(3) The input and output resistances for the Hall elements from Crystal H-145 were found to be considerably lower than expected. Considering the resistivity profile of the crystal, a gradual decrease in both parameters would be expected throughout the elements. On the basis of the data, it is concluded that the resistivity profile given by the supplier may have been in error. Only in elements prepared from the growth end of the crystal (~135 ohm-cm) would the input resistance values obtained be expected.



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TABLE 3. ROOM-TEMPERATURE D-C ELECTRICAL PROPERTIES OF HALL ELEMENTS PREPARED FROM CRYSTAL 02-0109

| Element | $V_{mi}$ mv | $V_{mo}$ mv | $R_{input}$, kilohms | $R_{output}$, kilohms | Remarks |
|---|---|---|---|---|---|
| 1 | 25.0 | -- | 20.0 | 26.0 | Hall tab chipped |
| 2 | 78.0 | -- | 22.0 | 27.0 | Hall tab chipped |
| 3 | 5.0 | 0.5 | 22.0 | 28.0 | |
| 4 | 50.0 | 0.6 | 22.0 | 28.0 | |
| 5 | -- | -- | -- | -- | Broken |
| 6 | 88.0 | 0.8 | 22.0 | 28.5 | |
| 7 | 96.0 | 0.6 | 22.0 | 28.0 | |
| 8[a] | 0.6 | 0.6 | 22.0 | 28.0 | |
| 9 | 38.0 | 0.4 | 20.0 | 26.5 | |
| 10 | 1.2 | 0.6 | 20.0 | 25.0 | |
| 11 | 25.0 | 0.5 | 20.5 | 26.0 | |
| 12 | -- | -- | -- | -- | Broken |
| 13 | 20.0 | -- | 20.5 | 26.0 | Broken |
| 14 | 88.0 | -- | 20.5 | -- | Broken |
| 15 | 68.0 | 1.0 | 20.0 | 26.0 | |
| 16 | 5.4 | 0.4 | 21.5 | 26.5 | |
| 17 | 45.0 | 1.5 | 20.0 | 29.0 | |
| 18 | 100.0 | 0.6 | 22.0 | 29.0 | |
| 19 | 33.0 | -- | 22.0 | 27.0 | Hall tab lead failure |
| 20[a] | 0.2 | 0.2 | 23.0 | 29.0 | |
| 21 | 7.0 | 0.6 | 23.0 | 30.0 | |
| 22[a] | 0.4 | 0.4 | 23.0 | 30.0 | |
| 23 | 5.0 | 0.4 | 24.0 | 34.0 | |
| 24 | 90.0 | 0.7 | 26.0 | 37.0 | |
| 25 | 80.0 | 0.6 | 30.0 | 42.0 | |
| 26 | -- | -- | 51.0 | -- | Elements 26 to 40 were not measured for $V_{mi}$ values. The appearance of a gradual increase of the input resistance to a maximum value followed by a decrease to a normal value of resistance indicated that the elements were defective in some unknown manner. |
| 27 | -- | -- | 90.0 | -- | |
| 28 | -- | -- | 165.0 | -- | |
| 29 | -- | -- | >200.0 | -- | |
| 30 | -- | -- | >200.0 | -- | |
| 31 | -- | -- | >200.0 | -- | |
| 32 | -- | -- | -- (Unfinished) | | |
| 33 | -- | -- | -- (Unfinished) | | |
| 34 | -- | -- | -- (Unfinished) | | |
| 35 | -- | -- | 104.0 | -- | |
| 36 | -- | -- | 58.0 | -- | |
| 37 | -- | -- | 44.0 | -- | |
| 38 | -- | -- | -- (Unfinished) | | |
| 39 | -- | -- | -- (Unfinished) | | |
| 40 | -- | -- | 28.0 | 50.0 | Elements having near normal $R_{in}$ but higher $R_{out}$ values than remainder of elements. |
| 41 | 40.0 | 0.6 | 24.0 | 45.0 | |
| 42 | 120.0 | 3.0 | 23.0 | 32.0 | |
| 43 | 80.0 | 0.5 | 24.0 | 34.0 | |
| 44 | 30.0 | 0.4 | 23.0 | 31.0 | |
| 45 | 60.0 | 0.3 | 23.0 | 30.0 | |



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TABLE 3. (Continued)

| Element | $V_{mi}$ mv | $V_{mo}$ mv | $R_{input}$, kilohms | $R_{output}$, kilohms | Remarks |
|---|---|---|---|---|---|
| 46 | 93.0 | 0.4 | 22.0 | 26.5 | |
| 47 | 16.0 | 0.9 | 22.0 | 26.5 | |
| 48 | 68.0 | 2.0 | 22.0 | 26.0 | |
| 49 | 40.0 | 0.6 | 21.5 | 25.5 | |
| 50 | 170.0 | 1.3 | 21.0 | 25.0 | |
| 51 | 17.0 | 0.6 | 24.0 | 24.0 | |
| 52 | 45.0 | 0.5 | 22.0 | 27.0 | |
| 53[a] | 27.0 | -- | 21.0 | 26.0 | |
| 54 | 150.0 | 0.5 | 21.0 | 27.0 | |
| 55 | 20.0 | 0.9 | 21.5 | 25.0 | |
| 56 | 54.0 | 0.3 | 22.0 | 27.0 | |
| 57[a] | 38.0 | -- | 22.0 | 27.0 | |
| 58[a] | 110.0 | -- | 21.0 | 28.0 | |
| 59[a] | 54.0 | -- | 21.0 | 40.0 | |
| 60[a] | 200.0 | -- | 22.0 | 35.0 | |

(a) Hall elements not supplied with current and Hall voltage leads.



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TABLE 4. ROOM-TEMPERATURE D-C ELECTRICAL PROPERTIES OF HALL ELEMENTS PREPARED FROM CRYSTAL H-145

| Element | $V_{mi}$ mv | $V_{mo}$ mv | $R_{input}$, kilohms | $R_{output}$, kilohms | Remarks |
|---|---|---|---|---|---|
| 1 | 23.0 | -- | 20.0 | 24.0 | Test sample |
| 2 | -- | -- | 20.0 | 24.0 | Current contact chipped |
| 3 | 98.0 | -- | 19.0 | 24.0 | Test sample |
| 4 | 130.0 | -- | 17.0 | 17.0 | Test sample |
| 5 | 64.0 | -- | 17.0 | 17.0 | |
| 6 | 74.0 | 2.0 | 17.0 | 17.0 | |
| 7 | 51.0 | 0.3 | 17.0 | 17.0 | |
| 8 | 1.5 | 0.2 | 17.0 | 18.0 | |
| 9 | 25.0 | 1.2 | 18.0 | 19.0 | |
| 10 | 26.0 | 1.2 | 17.0 | 17.0 | |
| 11[a] | 32.0 | -- | 17.0 | 17.0 | |
| 12 | 56.0 | 0.9 | 17.0 | 18.0 | |
| 13[a] | 54.0 | -- | 17.0 | 16.0 | |
| 14 | 19.0 | 0.9 | 18.0 | 18.0 | |
| 15 | 9.0 | 0.9 | 18.0 | 18.0 | |
| 16 | 4.0 | 0.3 | 17.0 | 18.0 | |
| 17 | 14.0 | 0.4 | 19.0 | 18.0 | |
| 18 | 35.0 | 2.5 | 17.0 | 17.5 | |
| 19[a] | 90.0 | -- | 17.0 | 17.0 | |
| 20 | 18.0 | 2.0 | 17.0 | 16.0 | |
| 21 | 28.0 | 1.5 | 17.0 | 18.0 | |
| 22 | 16.0 | 0.3 | 17.0 | 18.0 | |
| 23 | 12.0 | 1.2 | 16.5 | 17.0 | |
| 24[a] | 50.0 | -- | 16.0 | 16.0 | |
| 25 | 28.0 | 0.5 | 17.0 | 18.0 | |
| 26[a] | 60.0 | -- | 17.0 | 17.0 | |
| 27 | 34.0 | 0.2 | 17.0 | 17.0 | |
| 28 | 8.0 | 0.7 | 17.0 | 17.5 | |
| 29 | 11.0 | 0.5 | 18.0 | 17.0 | |
| 30[a] | 38.0 | -- | 17.0 | 15.0 | |
| 31[a] | 34.0 | -- | 16.5 | 15.0 | |
| 32 | 15.0 | 0.9 | 18.0 | 18.0 | |
| 33[a] | 94.00 | -- | 17.5 | 18.0 | |
| 34[a] | 32.0 | -- | 18.0 | 20.0 | |
| 35[a] | 58.0 | -- | 20.0 | 20.0 | |
| 36[a] | 70.0 | -- | 21.0 | 21.0 | |
| 37[a] | 115.0 | -- | 22.0 | 22.0 | |

(a) Hall elements not supplied with current and Hall voltage leads.



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(4) Except for several elements, the $V_{mi}$ values obtained for H-145 were somewhat lower and more consistent than those for elements prepared from 02-0109. On the basis of previous calculations (see Table 2), the Hall tab misalignment for some of the elements from each crystal would be greater than 1 mil. An optical comparator examination of all Hall elements showed the mechanical misalignment to be indeterminable. Therefore it was concluded that either nonuniform charge-carrier density, or the unknown effects of damage introduced by the ultrasonic cutting, or other unknown factors influenced the $V_{mi}$ values obtained.

## Hall-Element Output Voltage Characteristics

The Hall output voltage characteristics of eight elements prepared from Crystal 02-0109 were evaluated in a d-c magnetic field. The measurements were made at the maximum magnetic field and input current. The output voltage was determined for both polarities of the magnetic field to denote any effects related to the magnetic field direction.

Measurements were performed with a Pacific Electric Motor magnet having a 12-inch-diameter pole face and capable of being controlled to ±1.0 gauss. Tapered pole pieces terminating in a 2.0-inch-diameter pole face were inserted for the measurements performed. Each element was independently wax-mounted to a glass cover slide to prevent possible damage to the element. The slide and element assembly were remounted on a "paddle-type" holder to facilitate the positioning of the Hall element at the center of the pole faces and for an added support of the input and output leads to the element.

The Hall output voltage was measured with a digital voltmeter having a 1-millivolt resolution. The input current was supplied by dry cell batteries controlled through a voltage-divider network.

The linearity of the Hall voltage output with magnetic field and input current was determined for several elements of the same crystal group. Measurements of the Hall voltage output were made as the magnetic field was increased in increments of 2000 gauss to a maximum of 10,000 gauss. The Hall voltages were determined for each polarity of the field for each incremental field increase. For these measurements the input current was maintained constant at 2.0 milliamperes.

For evaluating the linearity of $V_H$ with input current, the current was increased in steps of 0.1 milliampere while the magnetic field was maintained constant at 10,000 gauss. During these measurements the magnetic field polarity was again reversed for each incremental step of input current.

Table 5 shows the tabulated values of the Hall output voltage measured at the maximum field and input current. A difference of 1 to 1.5 per cent in the output voltage for each element was found with magnetic field reversal. The spread in the output voltage between elements was found to be approximately 6.0 per cent.

Elements 3, 16, and 17 were used to determine the linearity of the Hall voltage with magnetic field and input current. The results of those measurements are shown in Figures 4 and 5. The linearity of the Hall voltage was found to be approximately ±0.12 per



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cent over full range of magnetic field and input current. The effect of magnetic field polarity appears to be more pronounced at the higher magnetic fields (>5000 gauss). This effect could be related to measurement error or an unknown secondary effort.

TABLE 5. HALL OUTPUT VOLTAGE MEASURED AT ±10.0 KILOGAUSS D-C MAGNETIC FIELD FOR SEVERAL ELEMENTS PREPARED FROM CRYSTAL 02-0109

| Element | Hall Voltage, volts at 2.0-ma input current | |
|---|---|---|
| | +10.0 Kilogauss | -10.0 Kilogauss |
| 3 | +1.720 | -1.700 |
| 4 | +1.709 | -1.710 |
| 6 | +1.700 | -1.675 |
| 7 | +1.720 | -1.701 |
| 8 | +1.750 | -1.751 |
| 9 | +1.645 | -1.642 |
| 10 | +1.636 | -1.632 |
| 16 | +1.650 | -- |
| 17 | +1.600 | -- |

The quality of the d-c magnetic field characteristics was quite gratifying, in that useful Hall elements were achieved. However, the values of the Hall voltage obtained was somewhat higher than expected. Previous calculations (see Table 2) showed that a Hall voltage in the order of 1.5 volts would be achieved for the material characteristics of crystal 02-0109. Since the input current, magnetic field, and element thickness were all reasonably well controlled, it is concluded that the Hall coefficients ($R_H$) used in the previous calculations were in error by approximately 12.0 per cent.

Considering the fact that the values of $\mu$, n, and $R_H$ used in the calculations were not measured on the crystals from which the elements were made, the agreement is very good. The results demonstrate the desirability of determining material properties precisely if Hall elements having good uniformity and yield are to be fabricated with characteristics matching design predictions.

### Temperature Effects

Power dissipation in a Hall element mounted by one surface with a thin electrically insulating material to a metallic substrate or a magnetic core face would cause a temperature difference between element and mounting material given by



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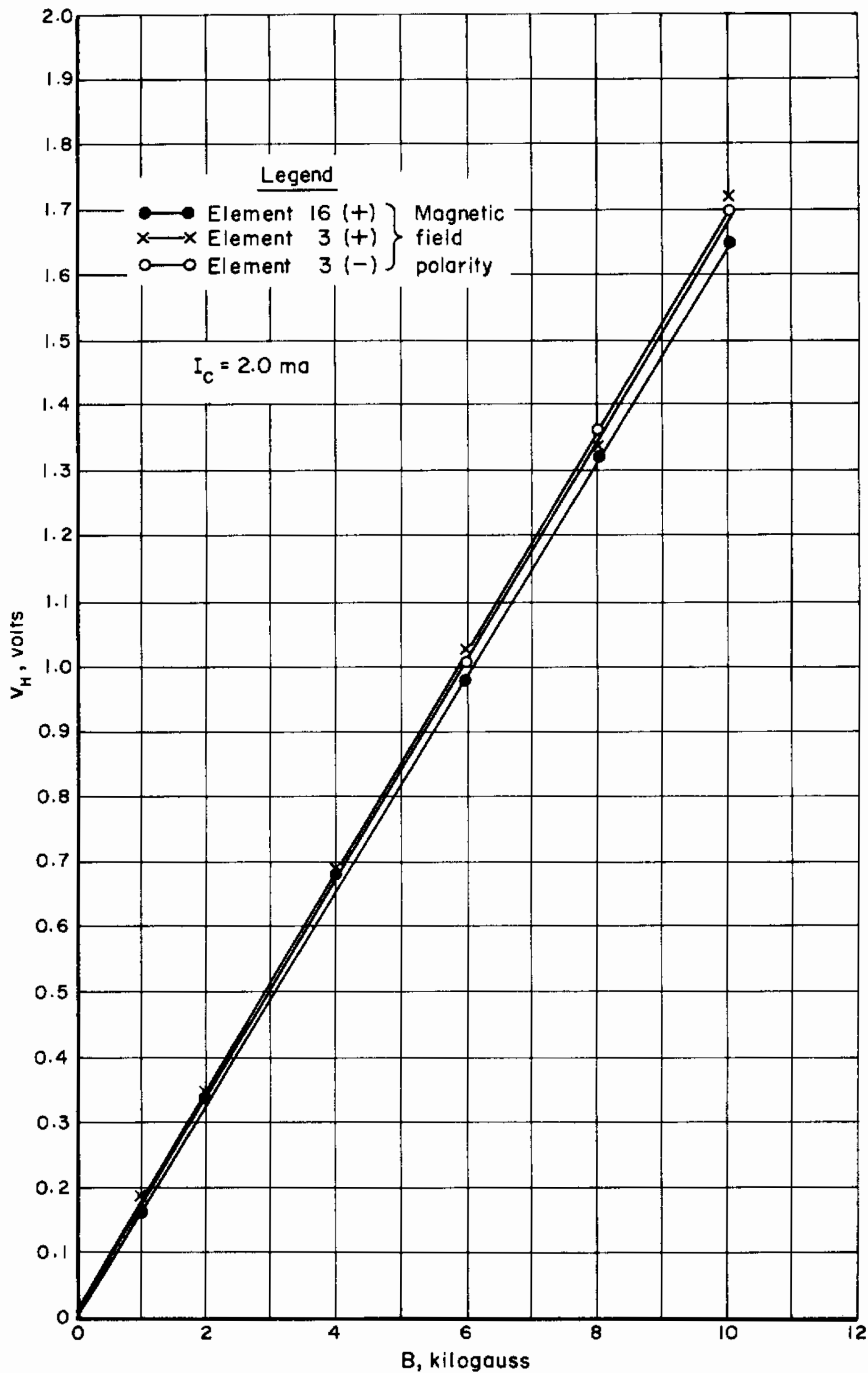


FIGURE 4. HALL OUTPUT VOLTAGE VERSUS D-C MAGNETIC FIELD WITH CONSTANT INPUT CURRENT



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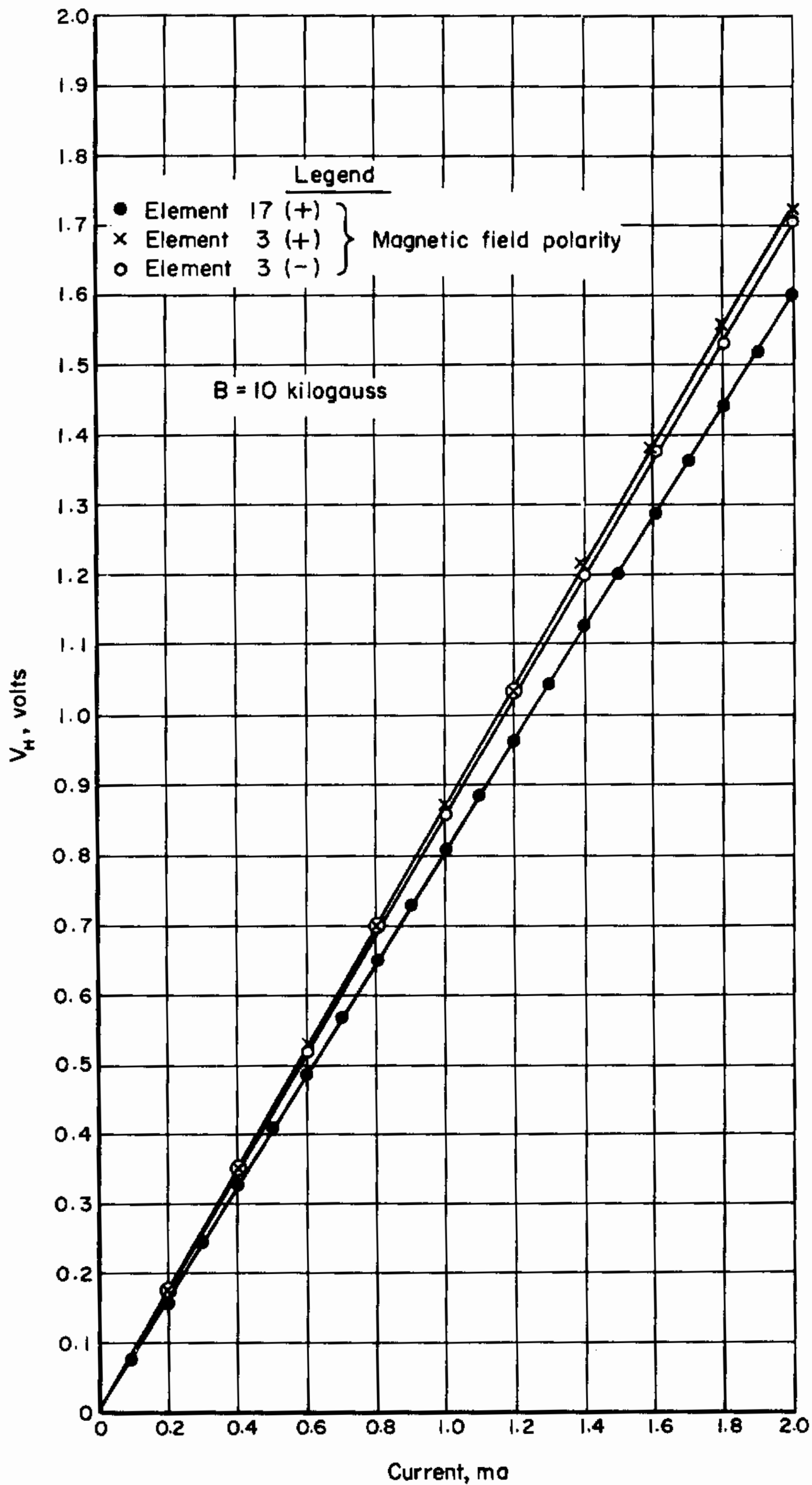


FIGURE 5. HALL OUTPUT VOLTAGE VERSUS INPUT CURRENT WITH CONSTANT D-C MAGNETIC FIELD



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$$\Delta T = \frac{t_1}{K_1} (P/ab) \left( 1 + \frac{K_1 t}{2Kt_1} \right), \tag{3}$$

where

$P$ = power, watts

$K$ = thermal conductivity of Hall element material, watt/cm C

$K_1$ = thermal conductivity of insulating material, watt/cm C

$t$ = thickness of Hall element, cm

$t_1$ = thickness of insulation, cm

$a, b$ = length and width of element, cm.

A calculation of $\Delta T$ from Equation (3) using the following numerical values, which are appropriate for the element and mounting method employed in this work, shows that $\Delta T$ = 0.31 C:*

$t$ = thickness of element = 0.03 cm

$t_1$ = thickness of mounting insulation = 0.0125 cm

$K$ = thermal conductivity of silicon - 1.0 watt/cm at room temp.

$K_1$ = thermal conductivity of insulation $5 \times 10^{-3}$ watt/cm C

$P$ = power input at maximum current of $2 \times 10^{-3}$ ampere = 0.08 watt

$A$ = area of element = 0.64 $cm^2$.

The temperature rise of 0.31 C indicates that no serious temperature effects should be encountered from Joule heat dissipation. However, a greater temperature rise could result from the power dissipated in the magnetic field winding and conducted via the core to the element; therefore heat sinks and the power requirements of the magnetic field winding should be considered.

The temperature difference, $\Delta T$, will produce a relative change in the Hall voltage ($V_H$) given by

$$\frac{\Delta V_H}{V_{H\,max}} = R_H^{-1} \left( \frac{dR_H}{dT} \right) \Delta T, \tag{4}$$

where

$\frac{dR_H}{dT}$ = Rate of change of $R_H$ with temperature, $\frac{cm^3}{coulomb - deg\ C}$.

*The mounting method and material insulation used are discussed in Appendix B.



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The relative change in the Hall voltage can be either positive or negative depending on the sign of $dR_H/dT$. In high-purity n-type silicon ($\approx 3.0 \times 10^{13}/cm^3$), the slope $dR_H/dT$ has been found to be positive between 100-300 K for experimental bulk samples measured in this laboratory.

An expression derived by Lofgren[4] for the heat power expressed in terms of $V_{H\,max}$ and $B_{max}$ is given as

$$P = \left( \frac{V_{H\,max}}{B_{max}} \right)^2 t\,(\Lambda^2 \sigma R_H{}^2\, b/a)^{-1} \times 10^{-8} \text{ watt.} \tag{5}$$

The maximum Hall voltage, $V_{H\,max}$, is then given as

$$V_{H\,max} = \frac{B_{max} \Lambda \sigma^{1/2} R_H\, b^{1/2}\, P^{1/2}}{(at)^{1/2}} \times 10^{-8} \text{ volt.} \tag{6}$$

Although Löfgren is not explicit in defining $V_{H\,max}$ and $B_{max}$, a close examination of his data indicates that he assumed $dR_H/dT$ to be negative and $d\sigma/dT$ to be negligible in the temperature range of interest. Contrary to this, high-purity n-type silicon has been found to have a positive $dR_H/dT$ and a negative $d\sigma/dT$ in this temperature range. The $B_{max}$ condition, it is assumed, is the maximum magnetic field that can be used without influencing or altering the material characteristics significantly at the maximum input power.

To determine the temperature dependence of $R_H$ and $\sigma$, one of the Hall elements prepared on the current project was measured over a 6 C temperature excursion from room temperature to ≈30 C. The results obtained showed the value of

$$\frac{\Delta R_H}{R_H\,\Delta T} \approx +0.1\%/\text{degree and of } \frac{1}{\sigma}\frac{\Delta\sigma}{T} \approx -1.4\%/\text{degree.}$$

These results verified that $dR_H/dT$ was positive. However, the value obtained for $d\sigma/dT$ was larger than expected.

From Equation (6) it is concluded, for the silicon used on this project, that the dominant factor affecting the temperature stability of $V_H$ would be in fact the $\sigma$ term and not $R_H$, as expected. For other materials or other values of $\sigma$ in silicon, $dR_H/dT$ and $d\sigma/dT$ would have to be determined to specify their effects on Hall element performance.

## Multiplier Package

Multiplier packages of several different designs, three of which are shown in Figure 6, were constructed and tested. The two arrangements shown in Figure 7, A and B, were found to be superior to all others tested.



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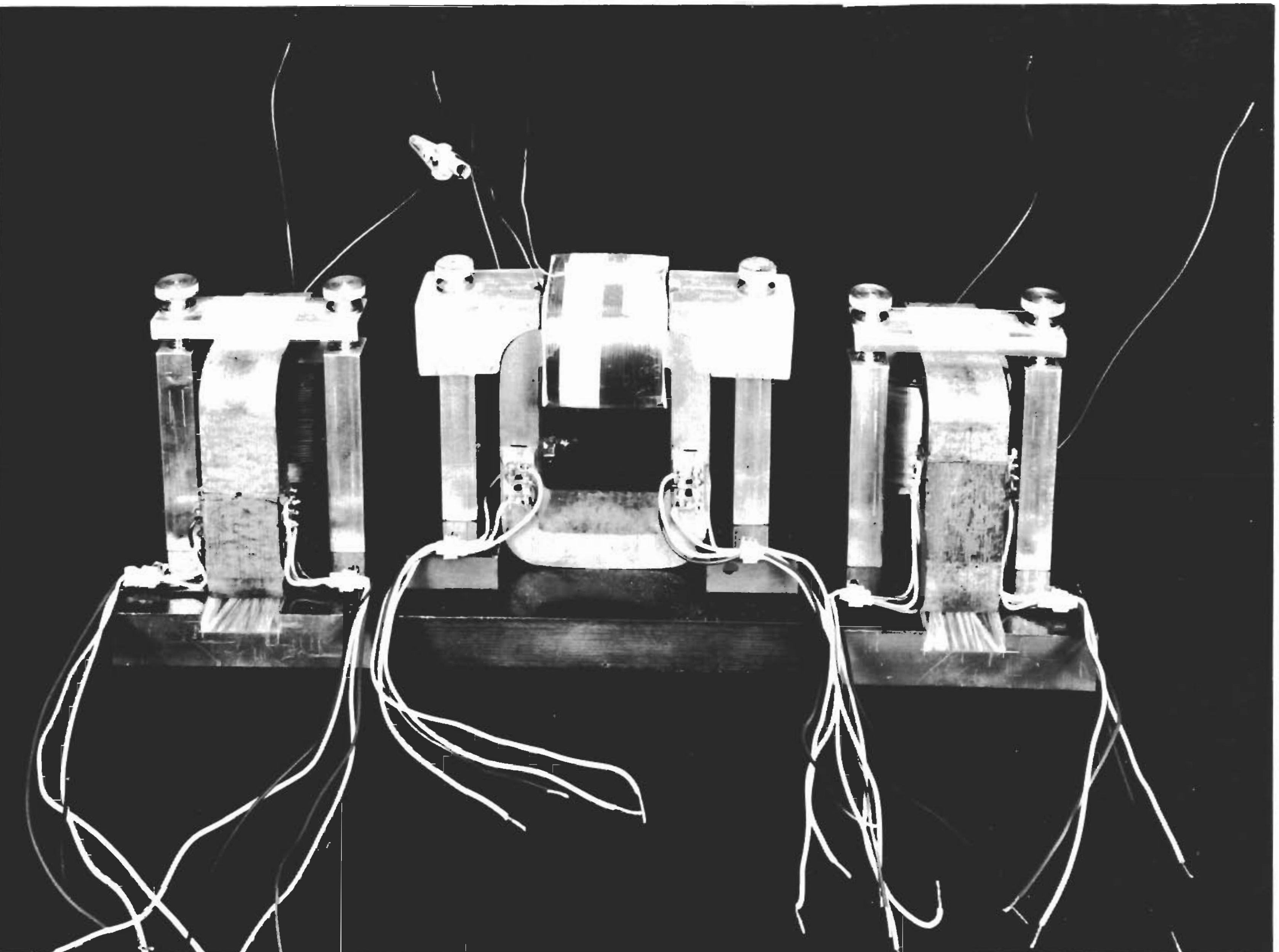

FIGURE 6. HALL MULTIPLIER PACKAGES



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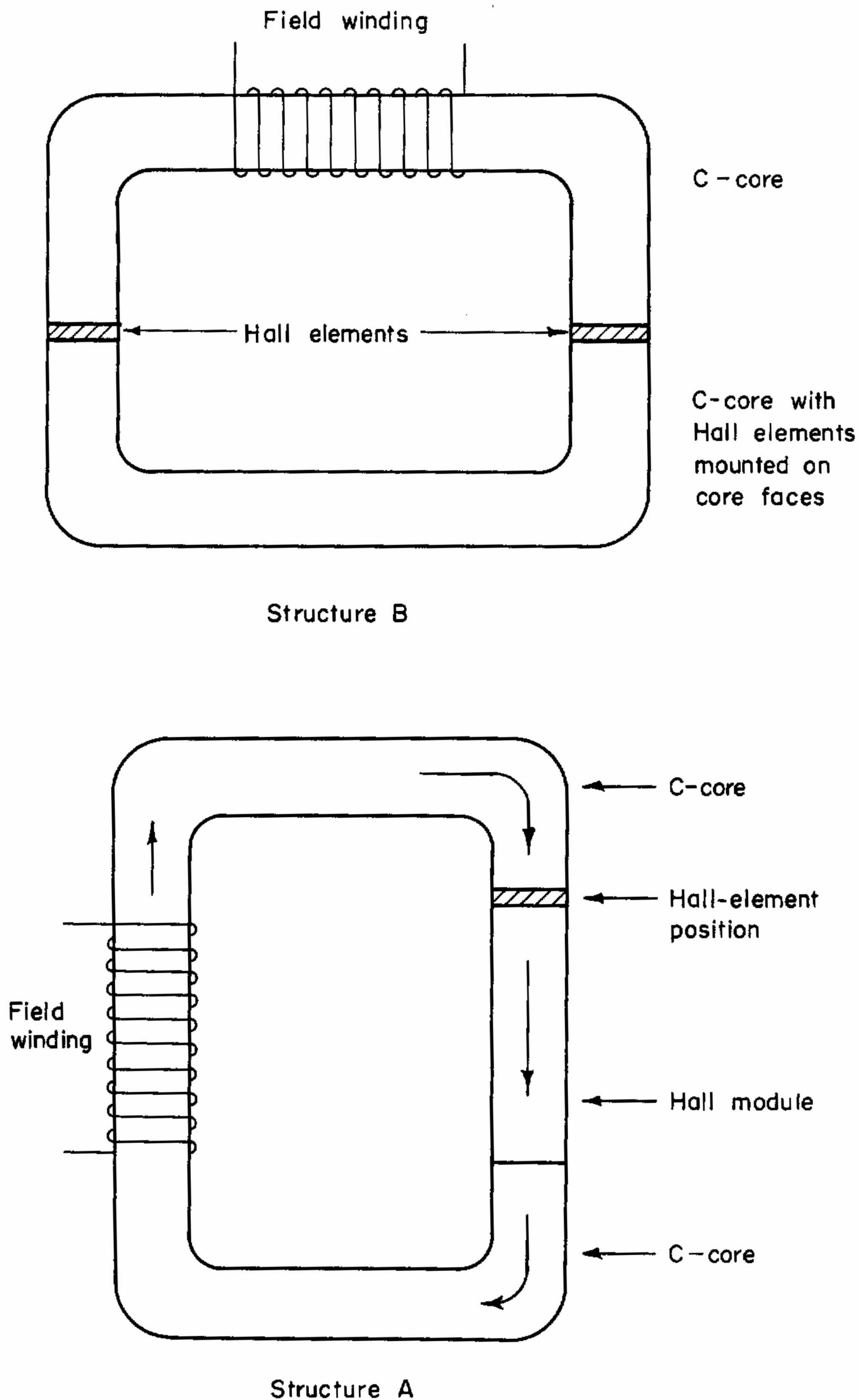


FIGURE 7. HALL MULTIPLIER MAGNETIC-CIRCUIT-TYPE STRUCTURES

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Two Hall elements electrically matched were positioned in each of the magnetic structures such that the same magnetic flux passed through each element. As will be explained in the section of the report on "Means for Error Correction", one element was used as the primary multiplier and the other for error correction. Figure 8 is a photograph of the Hall module used in the Type A core structure of Figure 7, while Figure 9 is a photograph of the Type B structure with one-half of the core structure removed to show the individual elements mounted on each core face. The principal mechanical requirements for this package may be summarized thus:

The elements must be held in a fixed position relative to the magnetic structure.

The means of holding the elements in place must not exert any mechanical stress on them.*

Each element must be electrically insulated from the other, and both elements must be electrically insulated from the magnetic structure.

To maintain magnetization efficiency, the dimensional tolerances of the air gaps must be held within ±0.5 mil.

It is desirable but not mandatory that it be possible to replace the entire package in the field by simply substituting one assembly for another.

Arnold Silectron C-cores were selected for the magnetic structure because of their uniform high quality, low magnetization requirements, and ready availability. A nonmagnetic shim is necessary to hold the dimension of the air gaps constant without causing stress in the elements. Four brass spacers, illustrated in Figure 10, accomplished this. These spacers form two grooves at right angles to each other and the elements are retained in position in these with Kel-F wax. The detailed description of the element mounting operation, given in Appendix B, applies to both types of core configurations.

Both of the structures shown operated satisfactorily, however Structure B eliminated the precise dimensional control required in sizing the core and Hall module of Structure A. In addition, Structure B has the advantage of a lower total magnetic reluctance in the magnetic circuit than does Structure A. If a large number of units are to be constructed, Structure B would be preferred. More details of the fabrication of the multiplier package are contained in Appendix B.

## Electrical Characteristics of the Hall-Element Package

### General

In order to determine the performance required from the associated electronics, the electrical characteristics of the Hall element are first defined in terms of the circuit

*Stress on the silicon Hall elements could change their electrical resistance as a result of the piezoresistance effect in the material. The consequence would be uncontrolled variation in their electrical properties and a degradation in multiplier accuracy.



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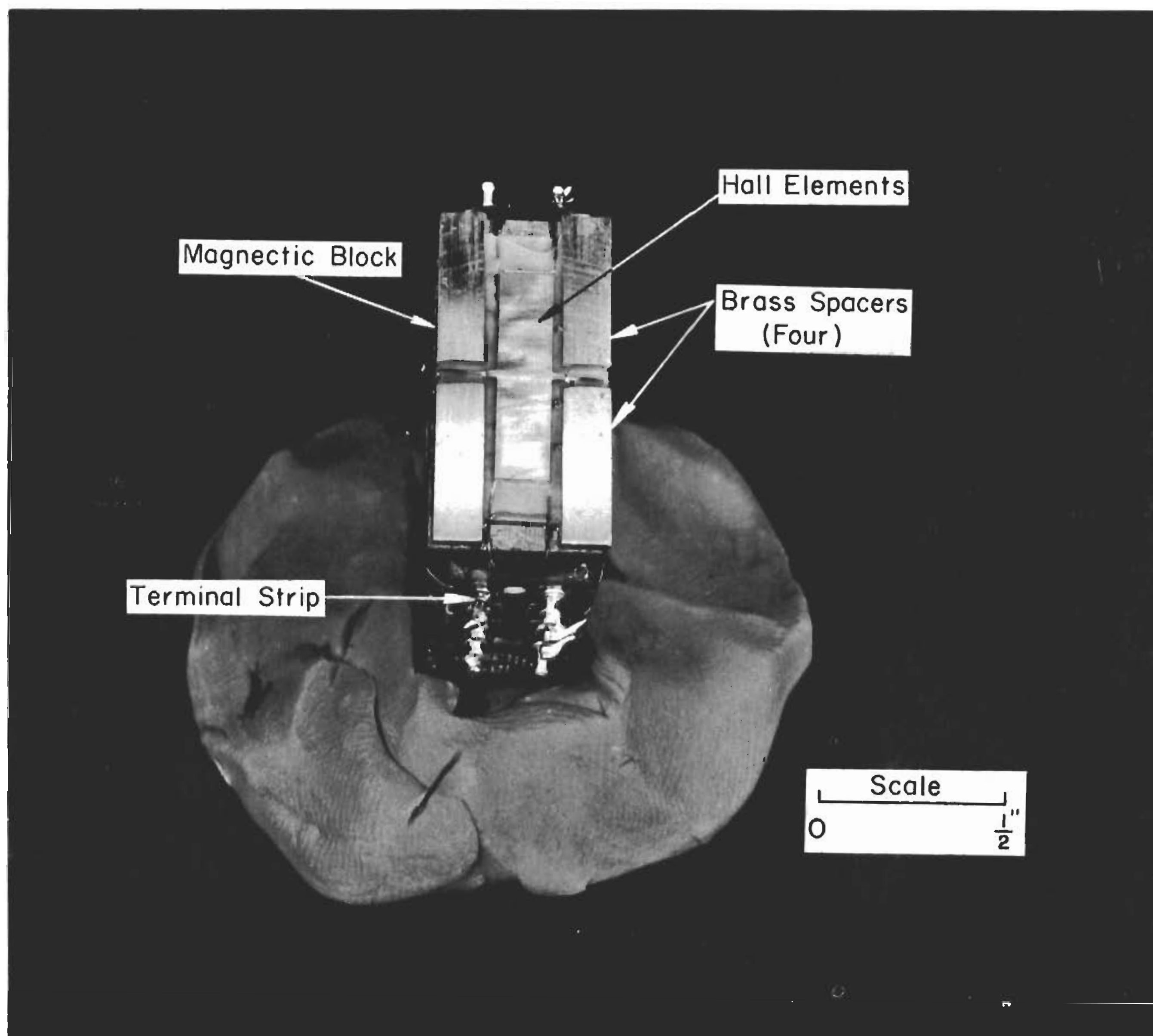


FIGURE 8. HALL MODULE ASSEMBLY


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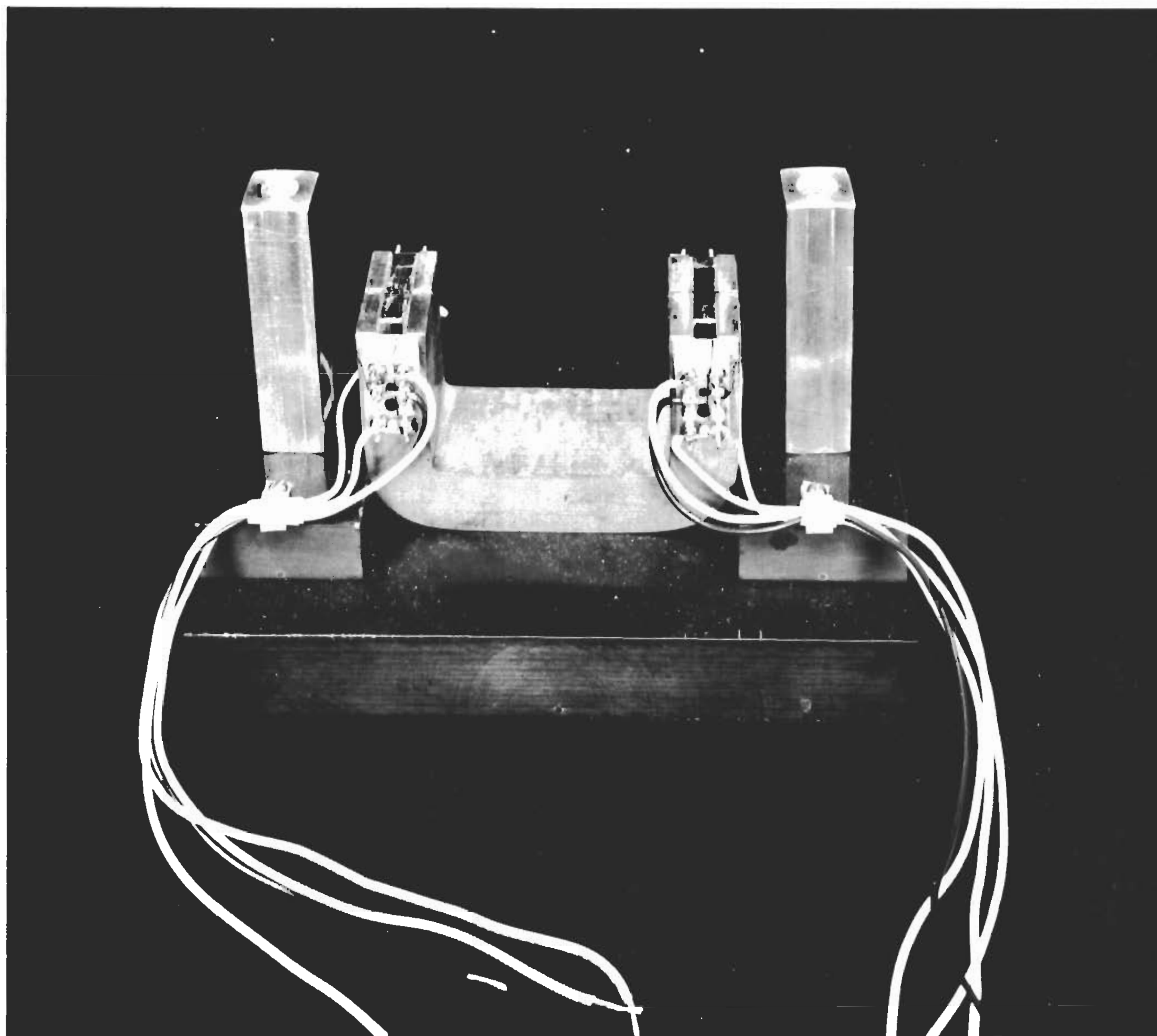

FIGURE 9. TYPE B STRUCTURE SHOWING INDIVIDUAL HALL ELEMENTS



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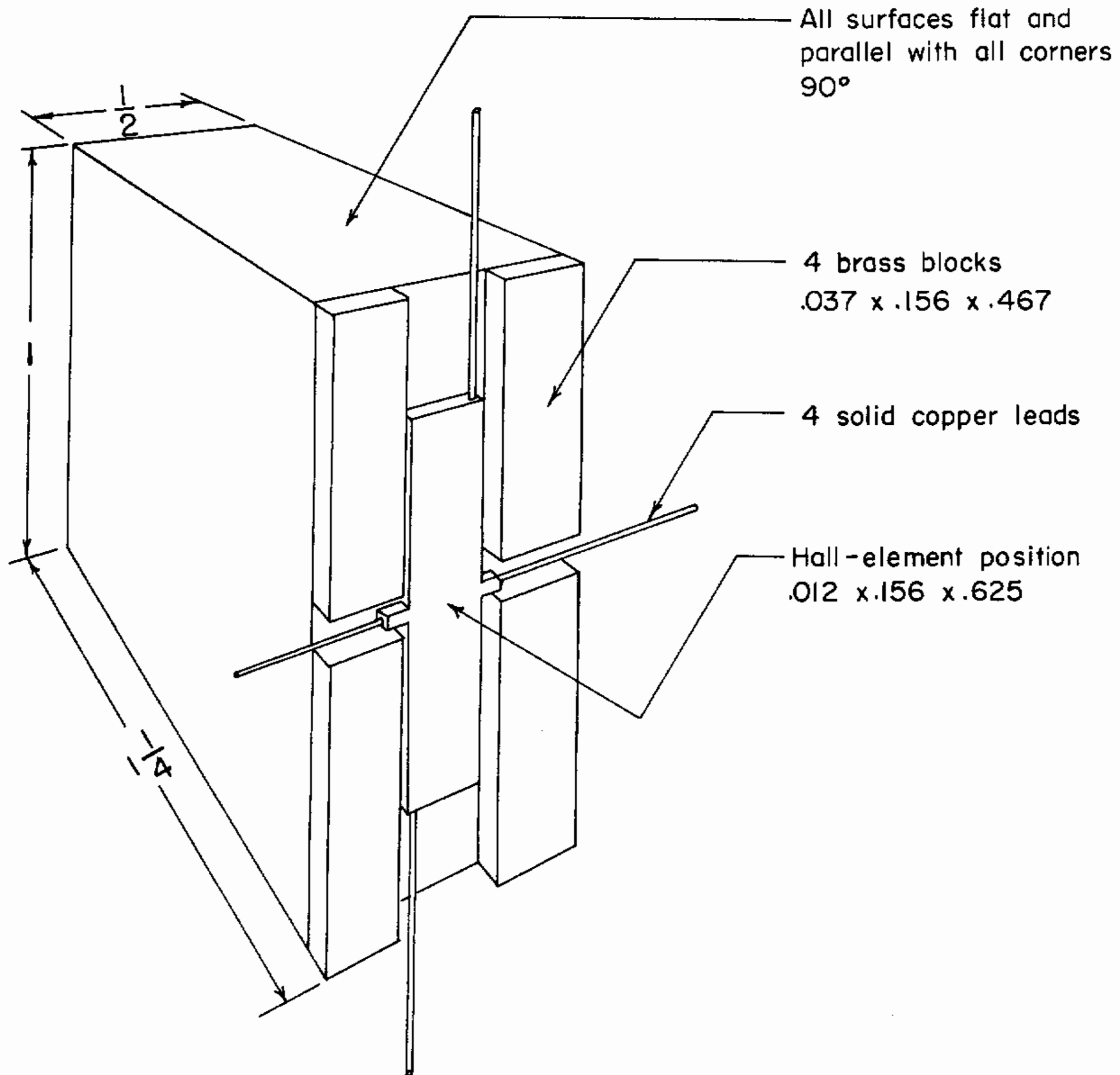


FIGURE 10. PERSPECTIVE LINE DRAWING OF THE HALL MODULE



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parameters. With its characteristics defined in this manner, the Hall element is considered as a voltage source having a series internal impedance, i.e., as a Thevenin generator, driving the input circuits of the output amplifier. Typical of the parameters necessary are the expected maximum and minimum values of the Hall voltage, the impedance level at the current drive terminals of the element, again both static and dynamic, and the usable dynamic ranges of the input quantities. The accurate definition of these dynamic ranges, especially at their lower extremes, requires data concerning the "noise" levels expected in the input circuits and, equally important, the "noise" level generated by the Hall element. All of these "noise" levels are to be considered over the operating frequency range.

## Linearities

The over-all accuracy of the multiplier system will have a first-order dependence upon the linearity of the Hall voltage defined with respect to both variable element drive current and variable flux density, each varied with the other held constant. In this instance, the linearity of the Hall voltage is not the linearity of the output voltage characteristic of the Hall element itself, as was measured on several elements prior to their being assembled into a multiplier package. Rather, linearity here concerns the linearity of the Hall voltage output of the multiplier package as a function of the multiplier input quantities, which are represented by the Hall-element current and the current into the existing coil of the magnetic structure.

When multiplying, the magnetic circuit of the multiplier package must establish a magnetic flux density in the Hall element, which is linearly proportional to the appropriate input variable. Since the intermediate electronic circuit between the input terminals for this variable and the circuit output current will be linear, the relationship between the current and the magnetic flux density produced also must be linear.

The flux density in a magnetic structure at d-c and at low frequencies is a linear function of the exciting ampere-turns, provided the reluctance of the magnetic path is a constant. Essentially this is so if the dominant reluctance in the magnetic circuit is the reluctance of the air gaps. Arnold Company's Silectron, the material from which the C-core is made, has a high magnetic permeability over the design range of flux density, hence the reluctance of the core used for this configuration should be only a few per cent of the total reluctance of the complete magnetic path. Since, once determined, the number of turns of wire on the exciting coil is a constant, the flux density in the magnetic structure of the package then becomes a linear function of the exciting current. However, from manufacturer's information on the material of the C-core, some saturation is evident at a flux density of 10 kilogauss, the maximum density for which this element has been designed. Therefore, it is evident that compensation will be necessary to correct for the nonlinearities introduced by the core where saturation effects appear. A solution to this problem is discussed later under "Hall Coefficient Compensation".

## Flux-Density Determination

It is more difficult to measure d-c magnetic flux accurately than it is to measure a-c flux. The measurement of the effects of flux fringing and leakage in the package



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magnetic structure was therefore made with 60-cycle a-c excitation of the magnetic circuit and with d-c current drive for the Hall element. The effective resistance of the magnetic circuit is low compared to its inductive reactance, hence the voltage drop across the coil is due almost entirely to inductive reactance. The ratio of inductive reactance to resistance is greater than 50 to 1, so any error introduced because of voltage drop due to resistance is negligible. The voltage drop across the coil, then, is a measure of the total magnetic flux through the coil of the structure. Since the cross-sectional area of the core, the number of turns on the coil, and the frequency of the exciting voltage all are known, the a-c flux density in the core may be determined.

A ten-turn search coil was wound directly over the air gap and a second ten-turn search coil was wound directly over the exciting coil winding. If there were no fringing and no leakage of magnetic flux, the ratio of the induced voltages in each search coil to the exciting coil voltage would be identical with the turns ratio of each search coil to the exciting coil. Also, because each search coil has the same number of turns, the induced voltages in each of them would be equal, and a properly polarized series connection of the two coils would produce cancellation or zero voltage output. The first check performed was to compare the voltage ratio, with respect to the exciting coil voltage, with the turns ratio for each search coil. The voltage ratio and the turns ratio were equal in the case of the search coil wound over the exciting coil, indicating no flux leakage; however, the voltage ratio for the search coil located over the gap was 10 per cent lower than the turns ratio, indicating there was flux fringing and leakage where the elements were located. Also, there was incomplete cancellation of induced voltages when the two search coils were connected in series bucking, and the magnitude of the residual voltage correlated with the 10 per cent leakage determined with the first test. This 10 per cent effective flux loss was measured at 10-kilogauss flux density, and the loss was found to decrease as the flux density was decreased, which shows that the magneitc circuit is nonlinear at high flux densities.

"Noise"

The voltage output leads connected to the Hall element form a single-turn loop which encloses a small part of the a-c magnetic field; consequently there may be an induced voltage in this loop which adds to or subtracts from the normal Hall voltage output. No attempt was made with the first mounted elements to minimize this voltage, which in this instance was between 80 to 100 millivolts; however, the geometry of the lead arrangement was altered in later mounted elements to minimize the inductive pickup in the leads. A lead from one Hall tab of each element was crossed underneath the element during mounting in a groove cut in the core. This put both leads in the same plane and reduced the induction pickup voltage from a-c magnetic fields. These later constructed element packages have induced a-c "noise" voltages of less than 10 millivolts, which is a considerable improvement. This level of voltage is sufficient to mask any other element "noise", however, it is well below the normal operating level of the multiplier and therefore can be neglected. This type of noise output would not be present in strictly d-c operation of the multiplier.

Impedance Levels

The impedance at the current input drive terminals of the element is resistive over the frequency band of interest. The value of this resistance was determined under



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static conditions as one of the checks performed on the unmounted element, and it averages approximately 20 kilohms. These static values were checked over the operating range of current using a resistance bridge and with no other input to the element. The Hall terminals were open circuited for these tests. In addition, the dynamic value of impedance was determined over the current range defined as the quotient of the voltage across the element divided by the current drive input while a constant-value magnetic field was applied. This value of dynamic impedance is the terminating impedance for the electronics of the element current drive input, and the dynamic value was found to be the same as the static value, averaging approximately 20 kilohms.

The value of dynamic impedance at the Hall voltage output terminals is necessary to complete the characterization of the element with respect to the associated electronics. The static value of this impedance was determined along with the rest of the measurements made on the unmounted Hall element, and was found to be approximately 15 to 20 kilohms. This is the ohmic value measured as before with no other inputs to the element. The dynamic value of impedance was determined under multiplier package operating conditions using the a-c test setup described for the measurement of flux fringing. The Hall output voltage, under conditions of full current drive and maximum magnetic field, was measured with an oscilloscope having a high input impedance of the order of 10 megohms. Then the Hall output voltage terminals were shunted with successively lower values of resistance until this Hall voltage was 0.9 of its open circuit value. Since the shunted resistor and the internal impedance of the Hall terminals form a simple series voltage divider for the open-circuit Hall voltage, the dynamic impedance, then, is 1/9 of the value of the shunted resistance across which 0.9 of the open circuit voltage is developed. The average value of this impedance, taken for several elements, is approximately 15 kilohms, which approximates the static value measured. However, to reduce the disturbance of the normal Hall potential to a minimum due to current in the Hall terminals, the input impedance of the readout electronics should be 1 megohm or greater over the frequency range of interest.

## Frequency Response

The product of two sine waves not of the same frequency is a sine wave of the higher frequency having an amplitude envelope which varies as a sine wave of the lower frequency. This is the familiar amplitude-modulation pattern, and when two sine waves having different frequencies are applied to the inputs of the multiplier package, the Hall voltage output will be an amplitude modulation pattern such as shown in Figure 11.

The frequency response of the magnetic flux density variable input is limited because of the large voltages required across the exciting coil to generate 10 kilogauss at the higher frequencies, so for the particular test structure the frequency range of this input variable was restricted to 60 cps or lower. However, there were no frequency limitations on the element current drive input variable other than those imposed by the frequency-response characteristic of the Hall element itself. An approximation of the upper limit of the Hall-element frequency response was made by increasing the frequency of the Hall-element current drive signal until the Hall voltage output decreased to 70.7 per cent of its low-frequency value. For this test the amplitudes of all inputs were held constant. There was no noticeable drop-off in response until the frequency of the element current drive input was above 10 kilocycles. The apparent



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70.7 per cent magnitude or 3-db down-point occurred at approximately 18 kilocycles. From these data it may be said that the frequency response of the particular elements exceeds 10 kilocycles and that there is no apparent change in linearity with frequency.

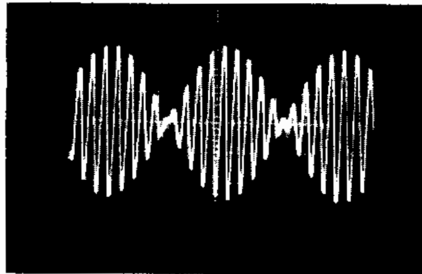

FIGURE 11. AMPLITUDE-MODULATION PATTERN

## Multiplier Circuitry

The Hall element, from a circuit point of view, is a 4-terminal device which cannot have any two terminals common. Therefore, either one of the input terminals can be at ground potential with the output read differentially, or one of the ouptup terminals at ground potential with the input driven differentially. If one of the input terminals is at ground potential the Hall voltage appears between the output terminals both of which vary from 0 to 20 volts above reference ground, depending upon the drive current.

The desired signal, the Hall output voltage, is the difference in potential between the two Hall output terminals. In the circuit of Figure F-1, Appendix F, both of these output terminals have a potential with respect to the zero reference even when the Hall output is zero. Therefore, a differential amplifier which responds only to the difference of potential between its two inputs and which has a common reference terminal at ground potential is required for the readout amplifier. Although, theoretically, a differential amplifier responds in this manner, all physically reliable amplifier circuits respond to some degree when both inputs are varied in the same sense; in other words, there may be a response to signals which create no difference in potential between the two inputs. This common mode response is usually greatly attenuated in comparison to the differential response, and the ability to maintain the attenuation of a common mode response over a dynamic range of several volts, while responding without attenuation to a differential input signal of the order of millivolts, is a figure of merit for differential amplifiers.

An impedance level of 1.5 megohms has been established for each input of the readout differential amplifier and must be maintained over the frequency range of interest. The input amplifier stage must be capable of absorbing at least 20 volts common mode input, since 20 volts is the expected excursion above ground of the Hall voltage. The readout amplifier of the first experimental multiplier setup, Figure 12, satisfied these requirements in performing sine-wave multiplication. The circuit was



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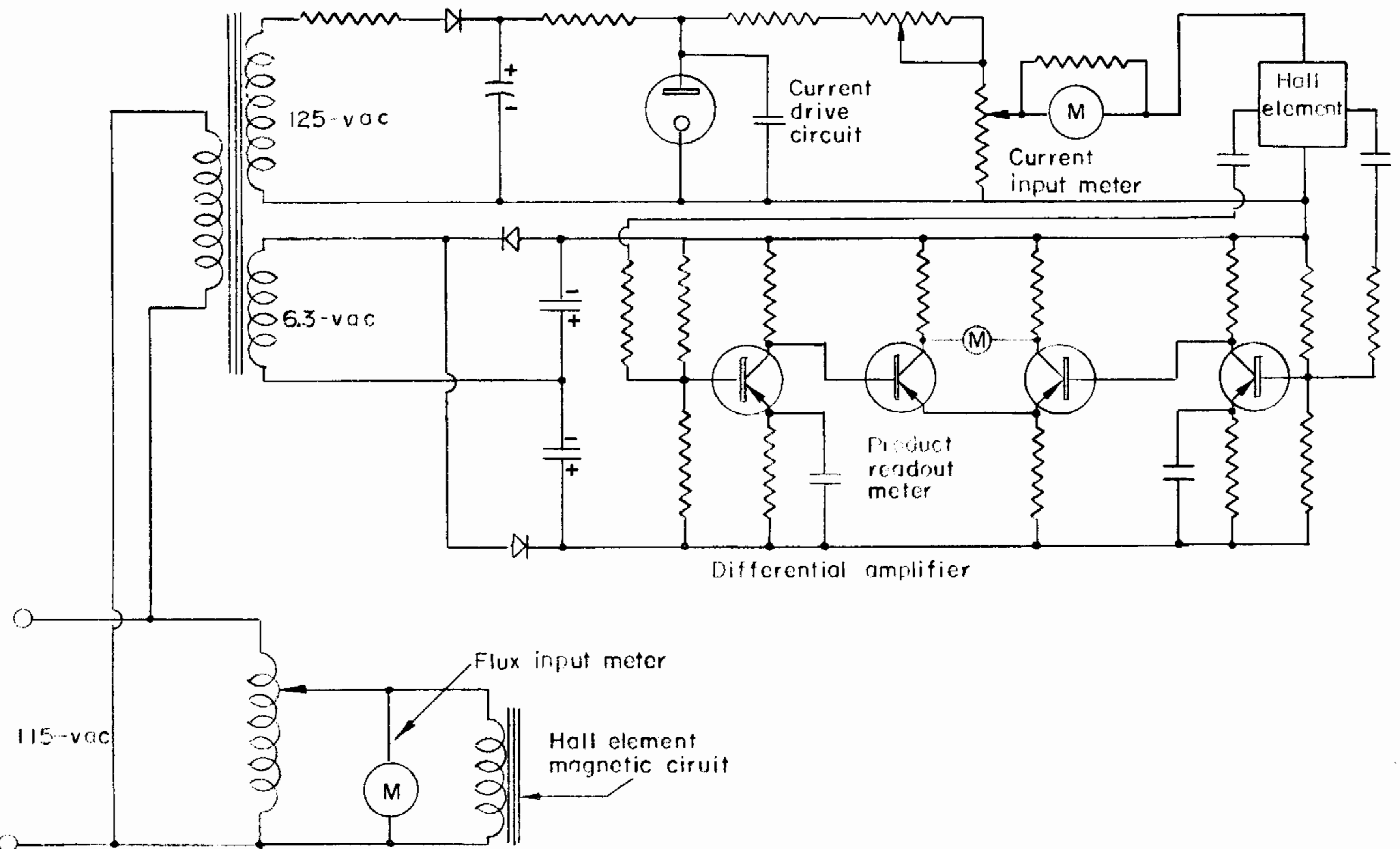


FIGURE 12. SIMPLIFIED MULTIPLIER CIRCUIT



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constructed to demonstrate the multiplying ability of the silicon Hall element. In order to keep the device simple, no circuit sophistication was attempted, that is, the input was not calibrated nor was there any d-c stabilization built into the circuit.

A multiplier as originally specified would be required to multiply variables ranging in frequency from d-c to five cycles per second. Because of the complexity of amplifiers handling d-c signals, it was decided to investigate the possibility of operation using a carrier system and a-c amplifier in which the stability problems would be very much reduced. Obviously, the output of the Hall element could be "chopped" and then amplified, thus permitting the use of a-c amplifiers in the output. However, in view of the problems in handling the wide range of the signal levels at the Hall-element output and the problem of determining the proper sense of the output signal, it was decided to investigate another type of operation.

The problems associated with the chopping function are very much reduced if, instead of chopping the Hall output signal, the currents representing the input variables are chopped at a high rate compared to the highest frequency existing in either variable-input signal. With this arrangement, chopping is accomplished at a higher current level and over a reduced range than if the Hall output were chopped directly. The Hall element output signal from such a system would consist of square waves whose period is that of the chopper and whose amplitudes are proportional to the instantaneous product of the two input variables. This output signal could then be amplified through stable a-c amplifiers and the product of the input variables determined.

Figure 13 is a block diagram of an elementary a-c system, as described above, which was constructed to demonstrate the feasibility of a-c operation. However, as mentioned earlier, because the frequency response of the magnetic circuit used for the laboratory demonstration is limited due to the restrictions caused by the particular magnetic structure, the circuit was driven directly from a current source the frequency of which was 60 cycles or below. The current drive for the element was chopped electronically with a multivibrator switch keyed by a relaxation oscillator operating between 2000-3000 cycles per second. This relaxation oscillator establishes a time base or carrier frequency for the system. Because the element current input is chopped, the Hall output voltage representing the instantaneous product of the two input variables is time variant regardless of the frequencies of the input variables, which conceivably could both be zero or d-c. The Hall voltage output is read by a differential amplifier having an appropriate input impedance and common mode rejection characteristics as described. A-c coupling is used between the differential amplifier and the Hall element.

As pointed out before, the output signal of the Hall element is a square wave whose repetition rate is the repetition rate of the time base and whose amplitude is proportional to the instantaneous product of the input variables. The polarity of the product signal appearing at the Hall-element output is dependent upon the combination of the polarities of the input variables; therefore, the product signal may be in any one of the four quadrants. However, polarity information is lost because of the type of coupling of the differential amplifiers. Therefore, a phase-detector arrangement is necessary. Polarity information restoration is accomplished in the phase detector by keying it synchronously with the keying of the element current drive input. Figure 14 is a schematic of the a-c multiplier circuitry.



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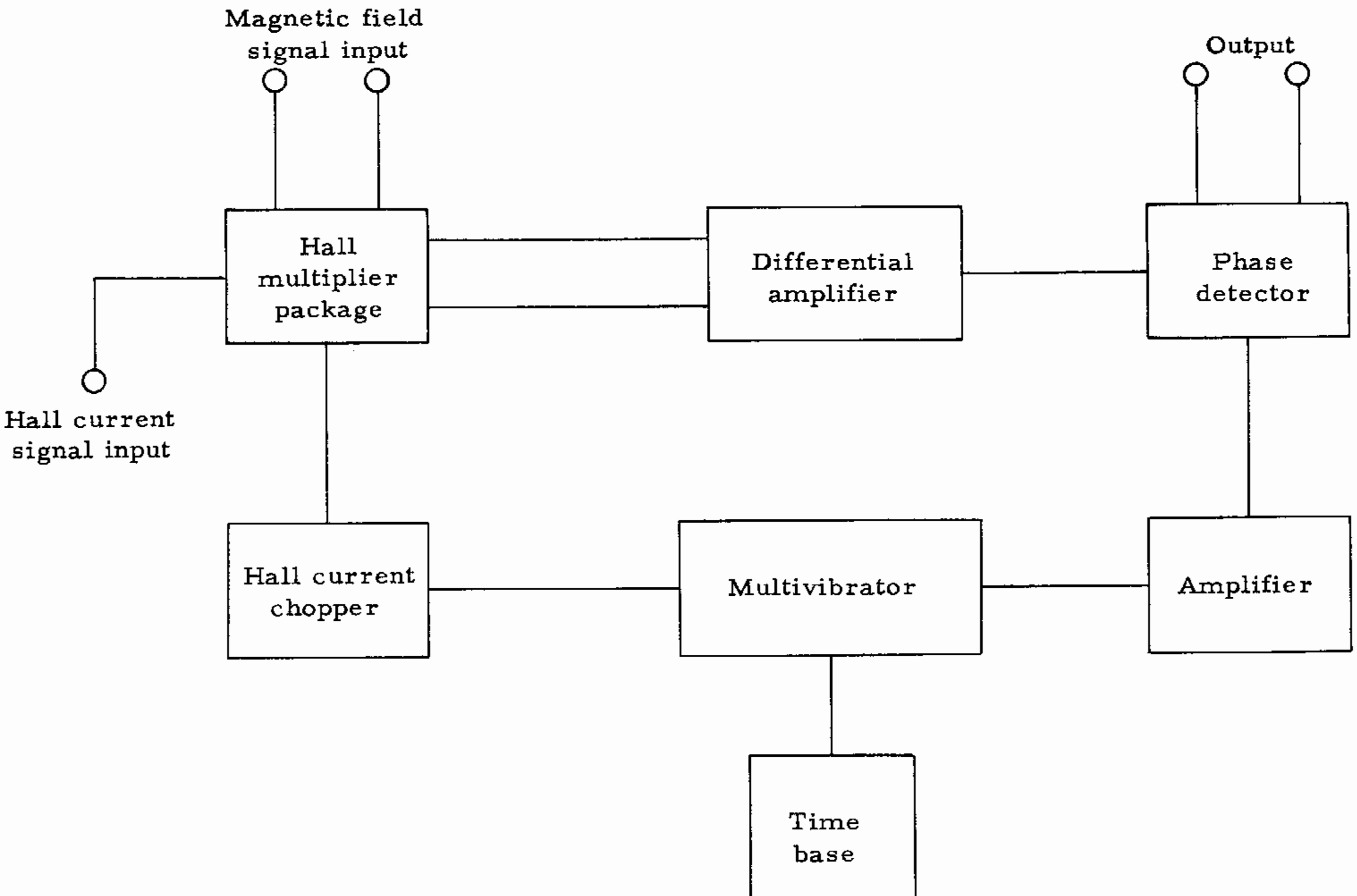


FIGURE 13. BLOCK DIAGRAM OF A-C SYSTEM



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FIGURE 14. SCHEMATIC OF A-C MULTIPLIER CIRCUITRY

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The various functions indicated in the block diagram of Figure 14 are performed by conventional circuits, as shown in the schematic diagram of Figure 14. The amplifiers for supplying the Hall-element current and the magnetic field current representing the two input variables are not shown. These would consist of conventional stabilized current amplifiers driven by the two input signals.

The Hall-element current is chopped, as previously discussed, by the transistor $T_1$. The chopping action is established by the base drive of $T_1$ from the output of the power amplifier composed of Transistors $T_6$ and $T_7$. The period of the chopper is established by the "time base" function in which the unijunction transistor, $T_2$, operates as a relaxation oscillator driving the buffer amplifier, $T_3$, which in turn triggers the multivibrator.

The period of oscillation is determined primarily by the product of R and C of the relaxation circuit. In the circuit shown, the frequency of oscillation is between 2000-3000 cycles per second.

The multivibrator consists of a conventional arrangement of transistors, $T_4$ and $T_5$. Its function is to convert the triggering pulses delivered to it by the buffer amplifier to square-wave pulses of a constant duration and amplitude, and to divide the trigger pulse frequency by two. These square-wave pulses are then amplified in the power amplifier, $T_6$ and $T_7$, and are impressed on the chopper, $T_1$, as well as on the "phase detector" composed of a balanced bridge circuit. The phase-bridge circuit consists of the two diodes (demodulators), $D_1$ and $D_2$, and resistors, $R_1$ and $R_2$, and a zero balancing potentiometer, $P_2$.

As explained previously, neither output terminal of the Hall element operates at the reference level (marked "0" volts in the schematic diagram). Hence, a differential amplifier is required to convert the differential output of the element to a proportional voltage referenced to "0" volts in the schematic.

The differential amplifier is made up of two transistors $T_{10}$ and $T_{11}$, which is driven by two cascaded amplifiers made up of transistors $T_8$ - $T_9$ and $T_{12}$ - $T_{13}$ respectively. The output of the differential amplifier is a voltage, with respect to ground, which is proportional to the Hall voltage output from the element.

Since the Hall output voltage may have either polarity with respect to the reference point and since polarity information is lost in the a-c differential amplifier, a means is required to regain the polarity information. The phase detector performs this function by comparing the instantaneous polarity of the amplified Hall output voltage wave with the polarity of the chopped exciting current in the element. The output of the phase detector is a square wave whose average value represents the magnitude and polarity of the Hall voltage output.

Potentiometer $P_1$ is provided for zero output adjustment to compensate for differences in gain of the amplifiers. $P_2$ provides adjustment compensation for differences in the diodes $D_1$ and $D_2$ and in the resistances $R_1$ and $R_2$.



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For precision multiplication of signals ranging in frequency from d-c upwards, the principles of this system would need to be extended. The Hall coefficient compensation circuits described previously would need to be incorporated, as would amplifier stabilization. In addition, means would have to be provided for chopping the magnetic field current source. This would consist of a current amplifier driven by the same chopping signal that drives the Hall element current chopper, Transistor $T_1$, in the schematic.

## SUMMARY AND CONCLUSIONS

From the results of this investigation, it can be concluded that a stable Hall multiplier of high precision is feasible, using the techniques developed. The degree of stability and precision possible is largely limited by the amount and the stability of the compensation applied.

A silicon Hall element was developed after a study of the suitability of a number of semiconductor materials. It exhibits a very high degree of linearity over a range of high output. The element also has an impedance compatible with the necessary associated circuitry. Fabrication techniques were established which are adaptable to the production of the elements.

Much of the nonlinearity in Hall multipliers can be attributed to problems related to the magnetic core and the energizing circuits. A circuit is described which will compensate for all normal nonlinearities between the magnetic field intensity in the element and the input variable which it represents. The circuit described also will compensate for nonlinearities which may be brought about by temperature effects in the Hall element.

The input variables to the multiplier may range in frequency from d-c to 5 cycles per second. The problems in achieving a high order of d-c stability in the amplifier circuitry associated with the multiplier are severe. However, the carrier system described permits a-c operation of amplifier circuitry, irrespective of the frequency of the input signals within the specified limits.



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# APPENDIX A

## DETERMINATION OF THE APPROXIMATE OUTPUT RESISTANCE AT THE HALL TABS WITH ZERO CURRENT AND MAGNETIC FIELD

The Hall-element configuration is shown in Figure A-1. We wish to determine the resistance between planes AB and A'B', which are assumed to be equipotential surfaces. For purposes of simplification, it is assumed that there is no curvature to the equipotentials in the tabs, so that they may be treated independently as a series resistance. It is also assumed that the material is isotropic. The problem is thus reduced to that of solving the two-dimensional Laplace equation for the geometry indicated in Figure A-2.

We have

$$\nabla^2 \Phi(x,y) = 0 \quad . \tag{1}$$

Assuming $\Phi(x,y) = X(x)\, Y(y)$, we obtain

$$\frac{1}{X}\frac{d^2X}{dx^2} = \frac{-1}{Y}\frac{d^2Y}{dy^2} = m^2 \quad , \tag{2}$$

where m is a constant yet to be determined. The solution of (2) is of the form

$$\Phi = XY = (A \cos my + B \sin my) \quad (C \cosh mx + D \sinh mx) \quad . \tag{3}$$

We require (3) to satisfy the boundary conditions

$$\Phi = 0 \qquad (x = b, \text{ independent of } y) \tag{4}$$

$$\Phi = V \qquad (x = o,\ o \leq y \leq w) \tag{5}$$

$$\frac{\partial \Phi}{\partial x} = 0 \qquad (x = o,\ w < y \leq a) \tag{6}$$

$$\frac{\partial \Phi}{\partial y} = 0 \qquad (y = a, \text{ independent of } x) \tag{7}$$

$$\frac{\partial \Phi}{\partial y} = 0 \qquad (y = o, \text{ independent of } x) \quad . \tag{8}$$

Conditions (4), (5), and (8) arise from considerations of symmetry in Figure A-1, while conditions (6) and (7) require no current flow across boundaries. Applying boundary conditions (4), (7), and (8), in that order, lead to the results $D = -C \coth mw$, $B = 0$, and $m = m_n = \frac{n\pi}{a}$ $(n = 0, 1, 2, \ldots\ldots)$. Thus $\Phi$ is of the form $[\alpha \cos my \,(\cosh mx - \coth mw \sinh mx)]$ where $\alpha = AC$. We know the use of $m = o$ leads to no useful result.



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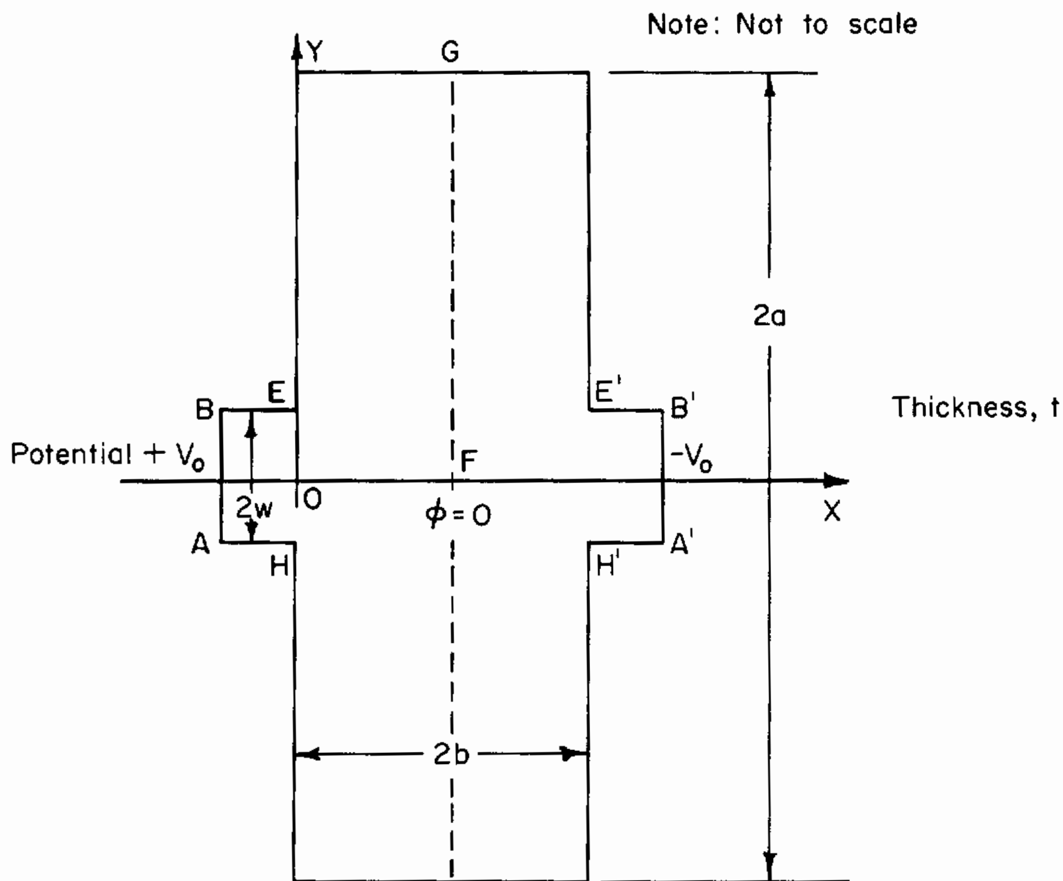


FIGURE A-1. HALL-ELEMENT CONFIGURATION

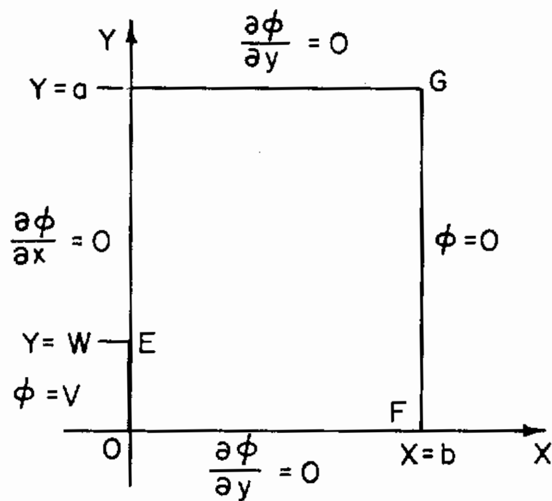


FIGURE A-2. HALL-ELEMENT GEOMETRY FOR USE IN SOLVING TWO-DIMENSIONAL LAPLACE EQUATIONS



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Furthermore, $\Phi$ must be expressed in a series

$$\Phi(x,y) = \sum_{n=1}^{\infty} \alpha_n \cos m_n y \,(\cosh m_n x - \coth m_n w \sinh m_n x) \quad , \tag{9}$$

so that all possible solutions of (1) are considered. It remains to determine a sufficient number of the coefficients $\alpha_n$; that is, $\alpha_1$, $\alpha_2$, .........., until the desired accuracy is obtained. The components of current density are:

$$J_x = -\sigma \frac{\partial \Phi}{\partial x} = -\sigma \sum_{n=1}^{\infty} m_n \alpha_n \cos m_n y \,(\sinh m_n x - \coth m_n w \cosh m_n x) \tag{10}$$

and

$$J_y = -\sigma \frac{\partial \Phi}{\partial y} = \sigma \sum_{n=1}^{\infty} m_n \alpha_n \sin m_n y \,(\cosh m_n x - \coth m_n w \sinh m_n x) \quad , \tag{11}$$

where $\sigma$ is the electrical conductivity.

From our assumption that the equipotential lines in the tabs are not curved, ($J_y = 0$ everywhere in the tab), we require $J_x$ to be constant at $x = o$ for $-w \leq y \leq w$. This arises from the consideration that

$$\nabla^2 \Phi = \nabla \cdot (J_x \, \underline{i} + J_y \, \underline{j}) \, j$$

is everywhere zero. Returning to Figure A-1, the total current through the tab is thus

$$I = 2wtJ_x \Big|_{\substack{x = o \\ y = o}} \quad , \tag{12}$$

where t is the thickness of the element. The resistance of the element (without tabs) is then

$$R = 2V/I = V/wtJ_x \Big|_{\substack{x = o \\ y = o}}$$

$$= V \Big/ wt\sigma \sum_{n=1}^{\infty} \frac{n\pi}{a} \alpha_n \coth \frac{n\pi}{a} w \quad . \tag{13}$$

The $\alpha_n$ can be determined by using the remaining two boundary conditions (5) and (6). If N points in the interval $o \leq y \leq w$ are used with Condition (5) and M points in the interval $w \leq y \leq a$ are used with Condition (6), then N + M simultaneous equations with N + M unknowns, $\alpha_1$, $\alpha_2$, .... $\alpha_{N+M}$ must be solved. A computer solution is desirable to attain a high degree of accuracy.



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For the present work, a manual solution was obtained using only four simultaneous equations. The results were: $R = 2.3\rho/t$, where $\rho$ is the resistivity (ohm-cm) and t is the element thickness (cm). The values $w = 0.032$ cm, $b = 0.20$ cm, and $a = 0.312'' \cong \pi/10$ (0.79 cm) were used. With $\rho = 150$ ohm-cm and $t = 0.030$ cm, the value of R is 11,500 ohms. The tab resistance was calculated separately as 7100 ohms. The total resistance is thus 25,700 ohms. Observed values on completed elements were most frequently in the range of 20,000 to 30,000 ohms. Considering that unknown resistivity and geometry variations must certainly occur, reasonable agreement with the calculated value is achieved.



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# APPENDIX B

## HALL-ELEMENT FABRICATION PROCEDURE

The fabrication procedure used in the preparation of the Hall elements is presented in chronological sequence. Included in the detailed description of each step are suggested refinements and additions felt necessary to achieve improved Hall-element uniformity and yield.

Figure B-1 is a block diagram of the steps in the process.

### Step 1. Silicon Crystal Characterization

Silicon crystals as received from a producer are supplied with resistivity, minority-carrier lifetime, and dislocation density values. The resistivity is determined by a gross measurement and as a consequence does not reveal variations of resistivity over small distances along the crystal. To predict Hall-element characteristics prior to fabrication, a more precise longitudinal resistivity profile measurement is made.

The resistivity is determined by a two-probe d-c method. Crystal ends are supplied with ohmic contacts prior to measurement. A probe spacing of 0.3 cm is used to obtain a more precise resistivity measurement.

Nickel contacts have been found in the past to be adequate for performing resistivity measurements. Nickel is applied to the ends of the crystal by an electroless nickel-plating bath having the following composition:

| | |
|---|---|
| $NiCl_2 \cdot 6H_2O$ | 30 g/liter |
| $NaH_2PO_2 \cdot H_2O$ | 10 g/liter |
| $NH_4Cl$ | 50 g/liter |
| $Na_3C_6H_5O_7 \cdot 2H_2O$ | 100 g/liter |
| Add $NH_4OH$ to give a pH value of 9.0 | |
| Bath temperature | 95 ±5 C |
| Plating time | 4.0 minutes |

The nickel-plated ends are tinned with a 60/40 tin/lead solder. Leads are attached following the tinning operation. The crystal is clamped in a holder of a two-probe resistivity apparatus to which a d-c current is supplied with a constant current power supply. Voltage probe measurements are taken with a high-input impedance electrometer voltmeter.



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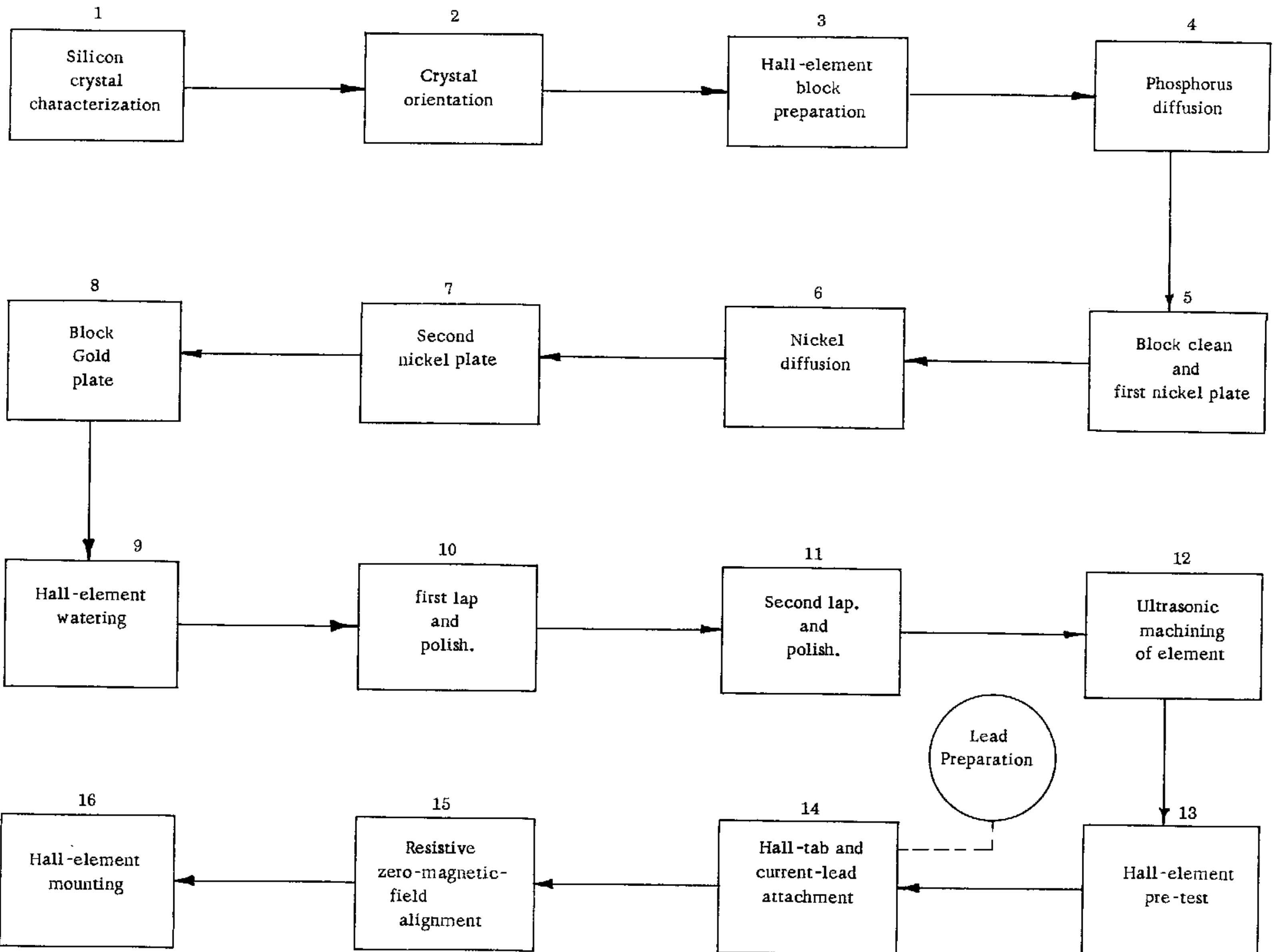


FIGURE B-1. CHRONOLOGICAL PROCESSING STEPS FOR THE FABRICATION OF SILICON HALL ELEMENTS



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The effects (such as anomalously high input impedance) encountered with the Hall elements prepared suggests that additional measurements should be performed on selected sections of a crystal prior to processing. These measurements should include the following:

(1) Several Hall specimens should be prepared from various portions of the crystal and a room-temperature determination of $R_H$ be made.

(2) A dislocation study on each end of the crystal should be included to determine the presence of lineage-type arrays.

(3) A radial resistivity determination should be included for a few selected portions of the crystal to denote the presence of carrier gradients.

## Step 2. Crystal Orientation

The silicon crystal is oriented to within 1° of the <111> plane prior to shaping into the Hall element "block". The orientation step was included primarily to minimize any possible influence of the crystal orientation on the Hall elements and to reduce possible scatter of characteristics between Hall elements.

The crystal is prepared for orientation by lapping the end surfaces flat with 600-grit silicon carbide, followed by etching in a "Nitrite" etchant (composition given below) for 10 minutes. The crystal is then cemented to a previously prepared steel mounting plate having precision-parallel surfaces. The mounted crystal is then placed on the goniometer* platform for the orientation operation.

Nitrite Etch

| | |
|---|---|
| NaOH | 100 g/liter |
| $NaNO_2$ | 150 g/liter |
| Temperature | 95 ±5 C |

## Step 3. Hall-Element "Block" Preparation

The oriented crystal mounted on the goniometer apparatus is transferred to a surface grinder for shaping the block to required dimensions. The grinding operation is carried out with a 180-grit diamond grinding wheel 0.5 inch thick. Because the block dimensions are critical, the surface grinding operation must be performed carefully.

The two Hall-element blocks prepared in the laboratory were controlled to less than a 0.5-mil run-out in the block length and width dimensions for crystal sections 2 inches in length.

*A goniometer manufactured by the Chemical and Metallurgical Division of the Sylvania Corporation was used for crystal orientation.



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Following the grinding operation, the Hall-element block is lightly sandblasted with a fine-grit abrasive. The sand-finished surface enhances the mechanical bond strength of the nickel-plated contacts.

### Step 4. Phosphorus Diffusion

The phosphorus diffusion method used for the silicon Hall-element block consisted of heating $P_2O_5$ at 200 C and carrying the resultant vapor over the block heated to 1230 C for 2 hours. The diffusion was carried out in an open-ended quartz tube furnace with argon used as a carrier gas for the $P_2O_5$ vapor flowing at a rate of 2000 cc/min. The Hall element blocks were maintained in a quartz carrier boat throughout the diffusion period.

To minimize the introduction of thermal strains, the silicon blocks were cooled slowly at 50°/hr from 1230 C to 450 C following the 2-hour diffusion period.

The diffusion time and temperature used results in an $n^+$ layer depth of nearly 0.2 mil for 150 ohm-cm material. The surface concentration is approximately $5 \times 10^{20}$ atoms/$cm^3$, which is a degenerate surface for applying low-resistance ohmic contacts.

### Step 5. Hall Block Cleaning and First Nickel Plate

During the phosphorus diffusion process, a phospho-silicate glass formation occurs at the surface of the silicon. This layer has a characteristically high resistance and must be removed prior to contacting. The technique used for the removal of the silicate glass does not effectively lower the phosphorus concentration at the surface prior to the application of the first nickel-plated layer. The steps in the cleaning and plating procedure are as follows:

(1) Hall-element block is soaked in concentrated HF (49 per cent) acid for 3.0 minutes

(2) Rinsed in hot (95 C) distilled water

(3) Etched in "Nitrite" etch for 30 seconds

(4) Rinsed in hot (95 C) distilled water for 15 seconds

(5) Rinsed in hot (95 C) deionized water for 30 seconds

(6) Placed into electroless nickel plating bath for 3.0 minutes

(7) Rinsed in hot (95 C) distilled water for 1.0 minute.

The plating time used results in a nickel layer approximately 0.04 mil thick.



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## Step 6. Nickel Diffusion

Nickel is diffused into the silicon block surface for the purpose of improving the contact bonding and electrical characteristics. The diffusion constant for nickel into silicon is between $10^{-5}$ to $10^{-7}$ $cm^2/sec$ for a temperature range of 700-1300 C; as a result, only a short diffusion period was required for the diffusion temperature used.

The diffusion is carried out in a quartz tube furnace for a period of 1/2 hour with "forming" gas (10 per cent $H_2$, 90 per cent $N_2$) flowing over the silicon blocks maintained at 750 C. Following the diffusion period, the furnace temperature is again slowly cooled at a 50 C/hr rate to 450 C.

## Step 7. Second Nickel Plate

A second nickel-plated layer is applied to the Hall-element block to obtain a good soldering surface. The procedure used is as follows:

(1) Nickel-diffused Hall-element blocks are soaked in HF (49 per cent) acid for 4.0 minutes

(2) Rinsed in hot (95 C) distilled water for 1.0 minute

(3) Rinsed in hot (95 C) deionized water for 30 seconds

(4) Nickel plated in the electroless nickel plating bath for 4.0 minutes

(5) Rinsed in hot (95 C) distilled water for 2.0 minutes

(6) Stored in 100 per cent ethyl alcohol.

## Step 8. Gold Plating

To maintain the nickel surface free of possible oxide formation during the storage period, the Hall block is plated with a thin gold layer. During soldering, the gold is taken into solution by the tin/lead solder, thus maintaining a clean nickel surface for the solder to achieve good wetting characteristics.

The gold plating step is carried out by an electroplating method using a standard gold plating solution*.

*"Sel-Rex" Standard Gold Plating Solution, manufactured by the Sel-Rex Corporation, Nutley, New Jersey.



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## Step 9. Hall-Element Wafering

The completed Hall element block is cemented to a precision "L" mounting block. The Hall block is sandwiched between two flat glass plates to eliminate chipping of the block edges during sawing. The Hall-element block and glass plate are cemented simultaneously to the "L" block with 70C cement*.

Hall-element wafers 0.017 inch thick are cut from the Hall-element block with a 0.015-inch-thick diamond saw. Figure B-2a is a photograph of Hall element wafer after the cutting operation. All cutting is completed prior to removing wafers from the mount for the purpose of maintaining identification of each individual element.

## Step 10. First Lap and Polish

Hall-element wafers are lapped and polished on one surface using the lapping fixture shown in Figure B-3a. This fixture can accommodate four Hall elements Ⓑ to reduce the polishing time. The Hall-element wafers are mounted to the insert section Ⓐ of the fixture with 70C cement. Pressure is applied to the elements to reduce the cement thickness, thus minimizing the possible beveling of elements. The insert is placed into the retainer section Ⓒ and set for 0.015 inch below the retainer surface. A 600-grit wet grind is first performed on the elements to remove material down to the retainer surface. Final polishing is completed with 0.1-micron diamond paste with a nylon cloth and kerosene lubricant.

Following polishing, the Hall elements are removed and cleaned in hot xylene.

## Step 11. Second Lap and Polish

To achieve a close tolerance on the thickness dimensions over the length of the Hall element, each previously polished wafer is independently lapped and polished with the polishing fixture shown in Figure B-3b. A tolerance of ±5 per cent is achieved over the element Ⓓ length by the use of the thick retainer section Ⓒ of the fixture.

The lapping and polishing is carried out in the same manner as described in Step 10. Figure B-2b shows a completed polished wafer. The insert section A of the final polishing fixture is preset to the required final Hall-element thickness of 0.012 inch from the retainer Ⓒ. The cement thickness is maintained in the order of 0.1 mil.

The procedure described above in Steps 10 and 11 for sizing the Hall element wafers is a slow operation. Improved lapping fixtures that would accommodate a larger number of elements would be necessary for large quantity production. Another possible scheme would be to employ a grinding operation using a diamond grinding wheel and a precision surface grinder.

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*Manufactured by the Hugh Courtright and Company, Chicago, Illinois.



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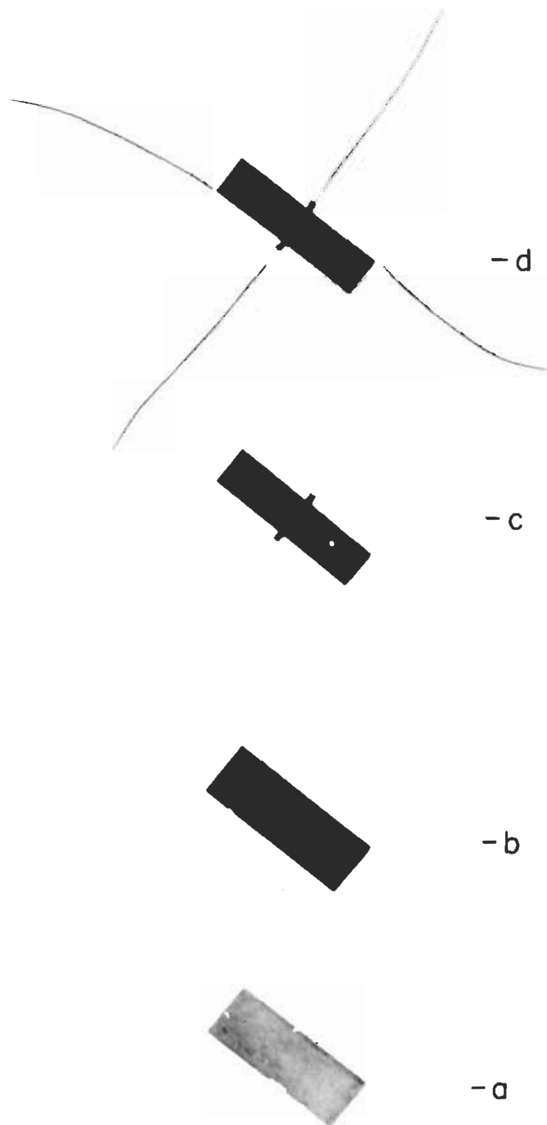


FIGURE B-2. STAGES IN THE FABRICATION OF HALL ELEMENTS



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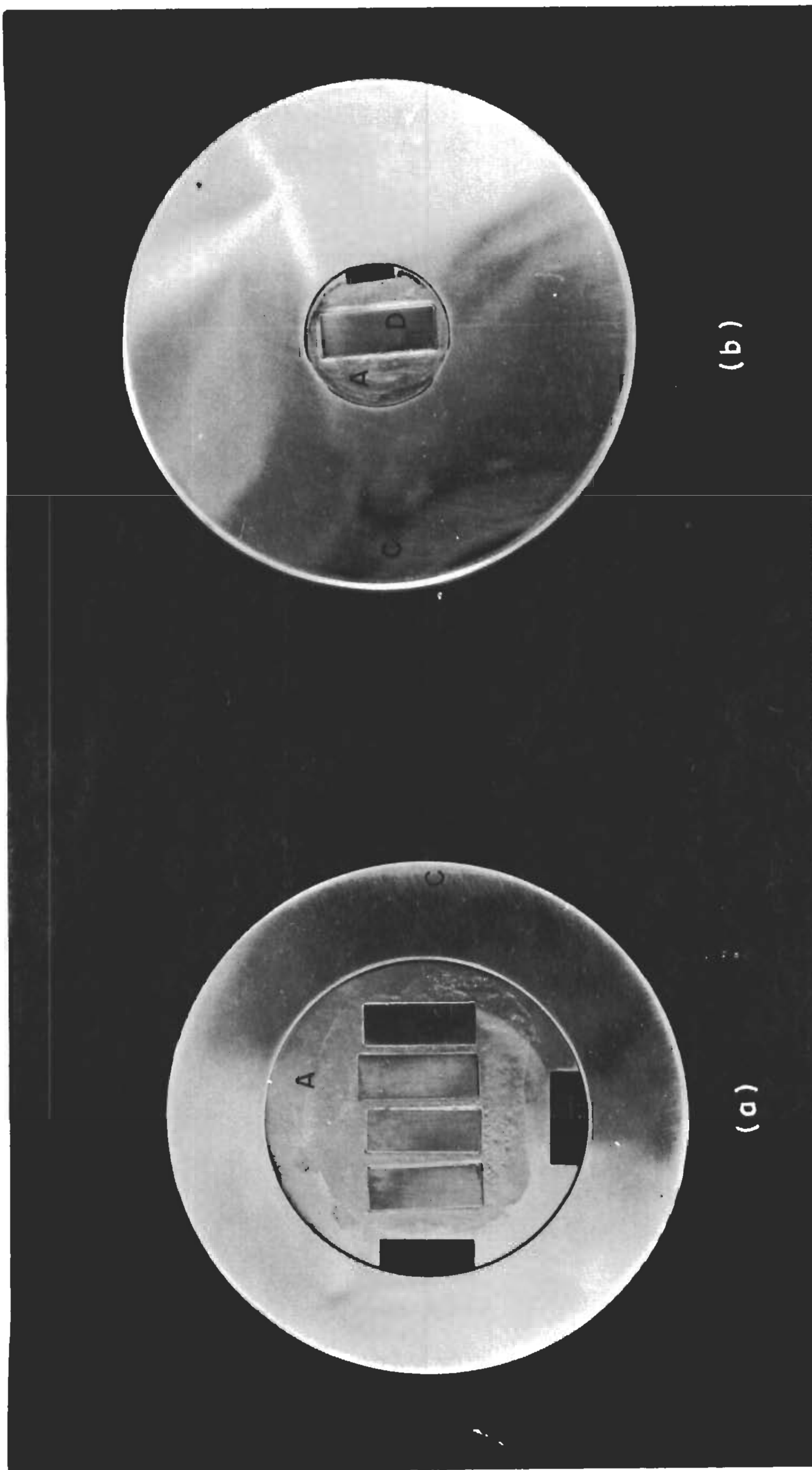


FIGURE B-3. LAPPING AND POLISHING FIXTURES USED IN PREPARING HALL ELEMENTS



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Step 12. Ultrasonic Cutting Operation

The Hall-element geometrical configuration is obtained by standard ultrasonic cutting techniques. To accomplish a reasonable control on the Hall tab alignment and dimensions, a special cutting tool was designed and constructed. Figure B-4 is a photograph of the ultrasonic cutting tool. Two such tools were constructed to allow dressing of tools used alternately in cutting elements. Figure B-2c shows a completed Hall element after cutting. The polished Hall elements were mounted on microscope slides with 70C cement. A thin cover glass was applied to prevent chipping of the element. Figure B-5a is a photograph of a mounted Hall element prepared for cutting. Figure B-5b shows a cut element prior to demounting and cleaning. To obtain alignment between the Hall-element wafer and the cutting tool, a stereoscopic microscope was used.

The Hall-element cutting operation was found to require approximately 15 minutes for each wafer. Most of the time was spent in the alignment of the wafer to the cutting tool. Cutting time required only a few minutes.

The cutting operation time could be easily reduced by the proper designing of alignment fixtures capable of indexing the cutting tool to the Hall-element wafer. Another possible method that could be developed is an optical projection of the mounted Hall element whereby an operator could easily align the cutting tool to the element.

Step 13. Hall-Element Pretest

Hall elements are pretested to eliminate all elements from further processing that do not meet the electrical specifications. The pretesting is performed with the Hall-element holding fixture shown in Figure B-6. The Lucite block Ⓐ contains recessed grooves that accommodate the Hall element width and Hall tab dimensions. The element is spring loaded against a fixed contact by the phosphor-bronze flat spring Ⓑ. The Hall tabs are contacted by the two offset phosphor-bronze flat springs Ⓒ and Ⓓ. A 2-milliampere current is supplied to the element by dry cell batteries through a voltage-divider network. The voltage drop between Hall output terminals at zero magnetic field, $V_{mi}$, is measured with a Kintell high-impedance zero center, multirange voltmeter.

The pretest d-c electrical measurements consisted of determining the misalignment Hall voltage ($V_{mi}$) at the maximum input current of 2.0 milliamperes, the input resistance, and the Hall terminal output resistance at zero current. Following these measurements, the Hall elements considered best suited were selected from each group for the attachment of input and Hall output leads. This was necessary prior to the mechanical adjustment of the misalignment voltage.

Step 14. Lead Attachment

The attachment of insulated copper leads to the current and Hall contact areas by standard soldering methods is the most critical step in the Hall-element fabrication procedure. The major problem encountered involved the prevention of solder buildup over the thickness dimension of the elements. This was finally resolved by tinning the



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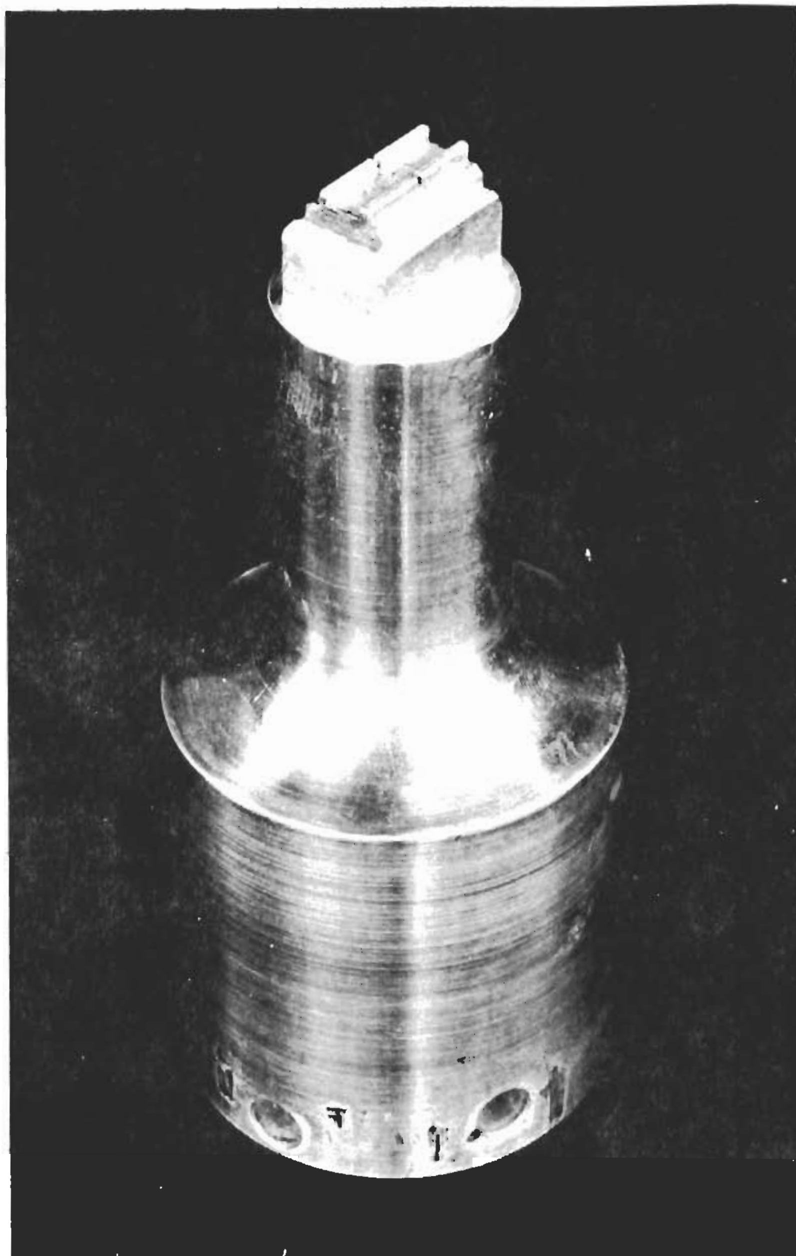

FIGURE B-4. ULTRASONIC CUTTING TOOL FOR CUTTING HALL ELEMENT CONFIGURATION



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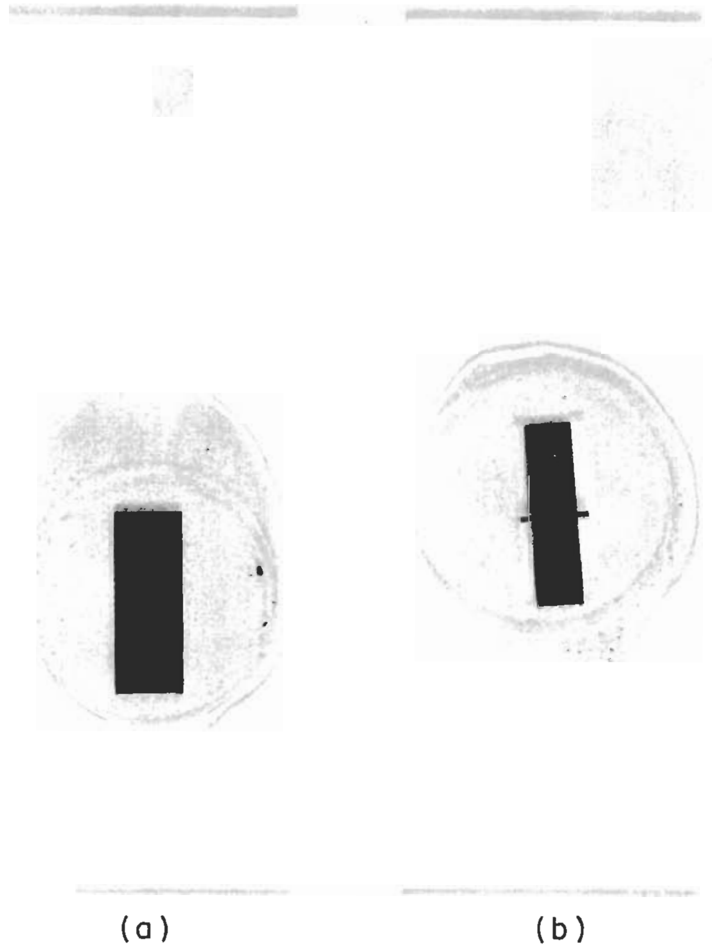

(a) (b)

FIGURE B-5. PHOTOGRAPH OF MOUNTED HALL ELEMENT WAFER BEFORE AND AFTER ULTRASONIC CUTTING OPERATION



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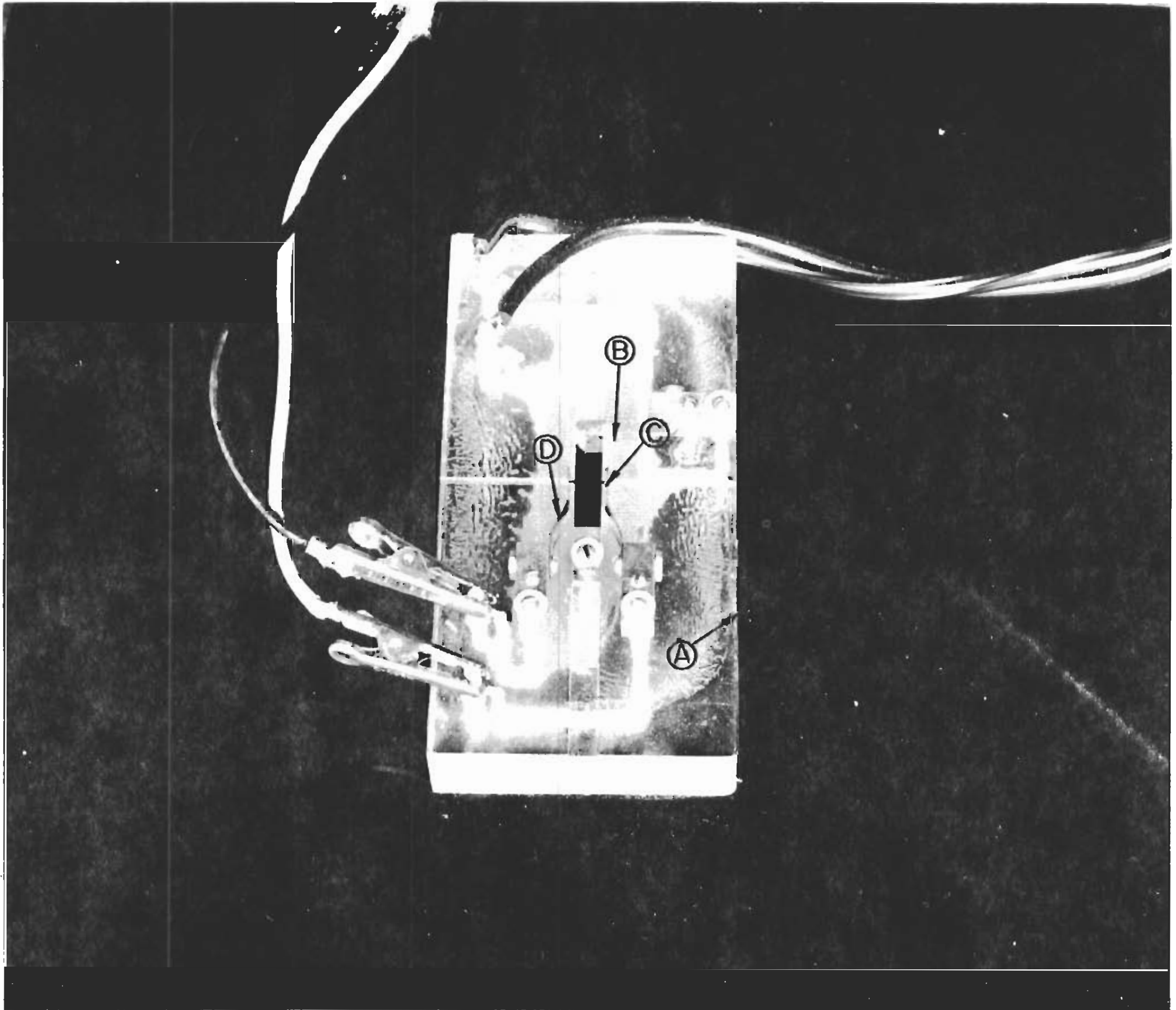


FIGURE B-6. HALL-ELEMENT PRETEST FIXTURE



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soldering areas prior to the attachment of the copper leads. The procedure and equipment used for the lead attachment operation is as follows:

## Lead Preparation

Leads were prepared from "Analac"* insulated magnet wire 0.007 inch in diameter. The Analac wire has the useful feature of being able to be tinned by solder-dipping methods without the need of mechanical abrasion. Insulation of the leads in the vicinity of the contacting areas of the Hall element is achieved with the Analac-type wire.

Leads are cut 2.5 inches long and tinned 0.125 inch on both ends by dipping into molten 60/40, tin/lead solder. Following tinning, the leads are again trimmed for proper tinned lengths to accommodate the current contact area and Hall tab ends.

## Soldering Operation

The lead soldering operation is performed with the apparatus shown in Figure B-7. The Hall element Ⓕ is placed in position on a polished stainless steel mount heated to within 10 degrees of the melting point of 60/40 tin/lead solder (172 C). Temperature control of the stainless steel mount is maintained by a temperature controller through a thermocouple Ⓑ mounted internally and in the vicinity of the Hall-element position. The Hall element is maintained in good thermal contact to the stainless steel mount by two phosphor-bronze springs designated as Ⓔ in the photograph. The copper lead Ⓑ is clamped to the extension arm of the micromanipulator Ⓓ by the phosphor-bronze spring Ⓒ. The tinned end of the lead wire is moved into soldering position by the manipulator observed by a stereomicroscope (not shown).

The Hall-element current areas and Hall tab ends are tinned prior to lead attachment. A micro soldering iron having a tip tapered to 0.015 inch is used for the tinning operation.

With a lead in the current contact area position, additional heat is applied with the micro soldering iron to accomplish soldering. Alpha 123** flux is used during soldering to insure good wetting.

For the Hall tab soldering, the lead is butt-ended to the contact area with the micromanipulator. Additional heat is again supplied by the microsoldering iron to the lead only. This allows solder from the tinned Hall tab to flow to the wire, thus achieving a convex meniscus with no solder overflow. The final appearance of completed Hall element with leads attached is shown in Figure B-2d.

## Remarks

The procedure presented appears to be time consuming as well as difficult; however, it was found that, after several trials, an operator could attach all four leads to the element in approximately 5 minutes. An improvement of the apparatus could be made to allow soldering of all four leads simultaneously.

*Manufactured by the Anaconda Wire and Cable Company.

**Rosin-base flux (noncorrosive) manufactured by Alpha Metals, Inc., New Jersey.



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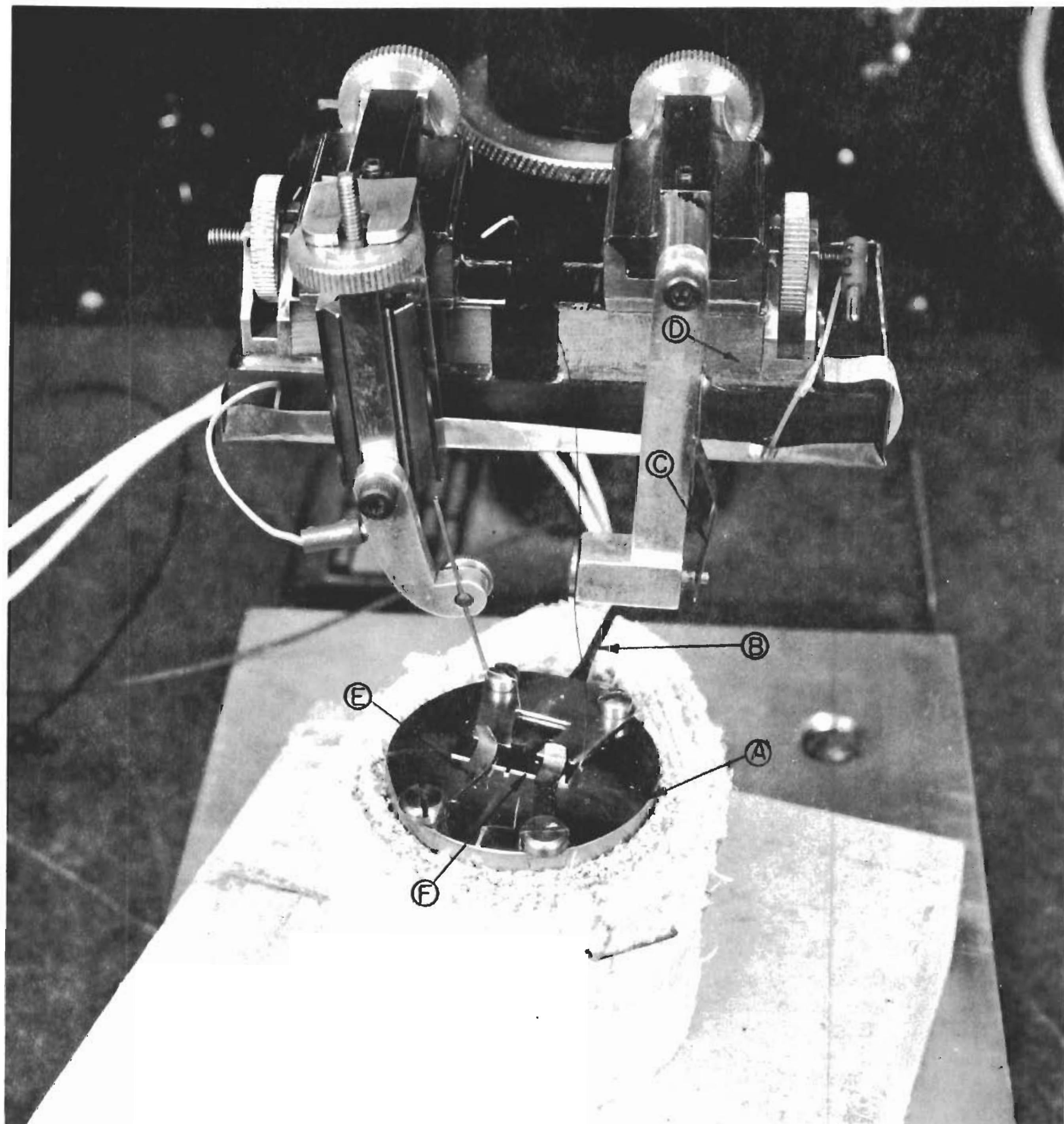


FIGURE B-7. HALL-ELEMENT LEAD ATTACHMENT APPARATUS



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The preheating of the element to a temperature near the solder melting point was found to be necessary to eliminate fracturing of elements from thermal stresses introduced by large temperature gradients. Attempts were made to solder several units without preheating; these all resulted in fractured units.

## Step 15. Hall Tab Alignment

Reduction of the resistive component of output voltage at the Hall terminals is accomplished by mechanical sawing on the Hall tab arm near its intersection with the body of the element.

A diamond-plated tungsten wire* 0.008 inch in diameter is used to adjust the misalignment voltage with maximum input current and zero magnetic field applied to the element. The apparatus used to perform the alignment operation is shown in Figure B-8. The Hall element is held in the fixture Ⓐ by a vacuum chuck arrangement. The voltage is read by the Kintell high-impedance multirange voltmeter Ⓑ. Current to the element is supplied by the dry cell battery supply Ⓒ. The mechanical sawing operation is observed through the stereomicroscope Ⓓ. The polarity of the misalignment voltage is used to indicate the Hall tab requiring the mechanical adjustment. Figure B-9 is a close-up view showing the Hall element in position for mechanical adjustment. Current input and Hall terminal voltage output leads are contacted by the phosphor-bronze spring contacts designated Ⓐ and Ⓑ, respectively. The Hall element is held in position without stress through the vacuum chuck arrangement Ⓒ. The diamond wire position is shown as Ⓓ.

### Remarks

The alignment by mechanical sawing was found to be very successful. However, it is necessary to carry out the operation with a minimum of light striking the Hall element. Under illumination, excess charge carriers are injected into silicon which alters the conductivity, thus introducing difficulties in obtaining a zero $V_{mo}$ value. As a result it was necessary to perform the adjustment under very dim light fields to achieve the lowest possible $V_{mo}$. The fixture as shown was not completed because of the pressing demands for completed Hall elements. It was necessary to perform the sawing operations manually for all elements produced. A holding fixture for driving the diamond wire should be constructed to obtain better control on the sawing operation without the need of bright light fields.

## Step 16. Hall-Element Mounting

The final step in the fabrication process involves the mounting of two matched Hall elements to the module package formerly described. A polytrifluorochloroethylene wax designated as Kel-F200** was used to mount elements in position. The properties of Kel-F200 are as follows:

*Manufactured by the Sample Marshal Laboratories, Inc., Lyndhurst, New Jersey.
**Manufactured by the Minnesota Mining and Manufacturing Company, Jersey City, New Jersey.



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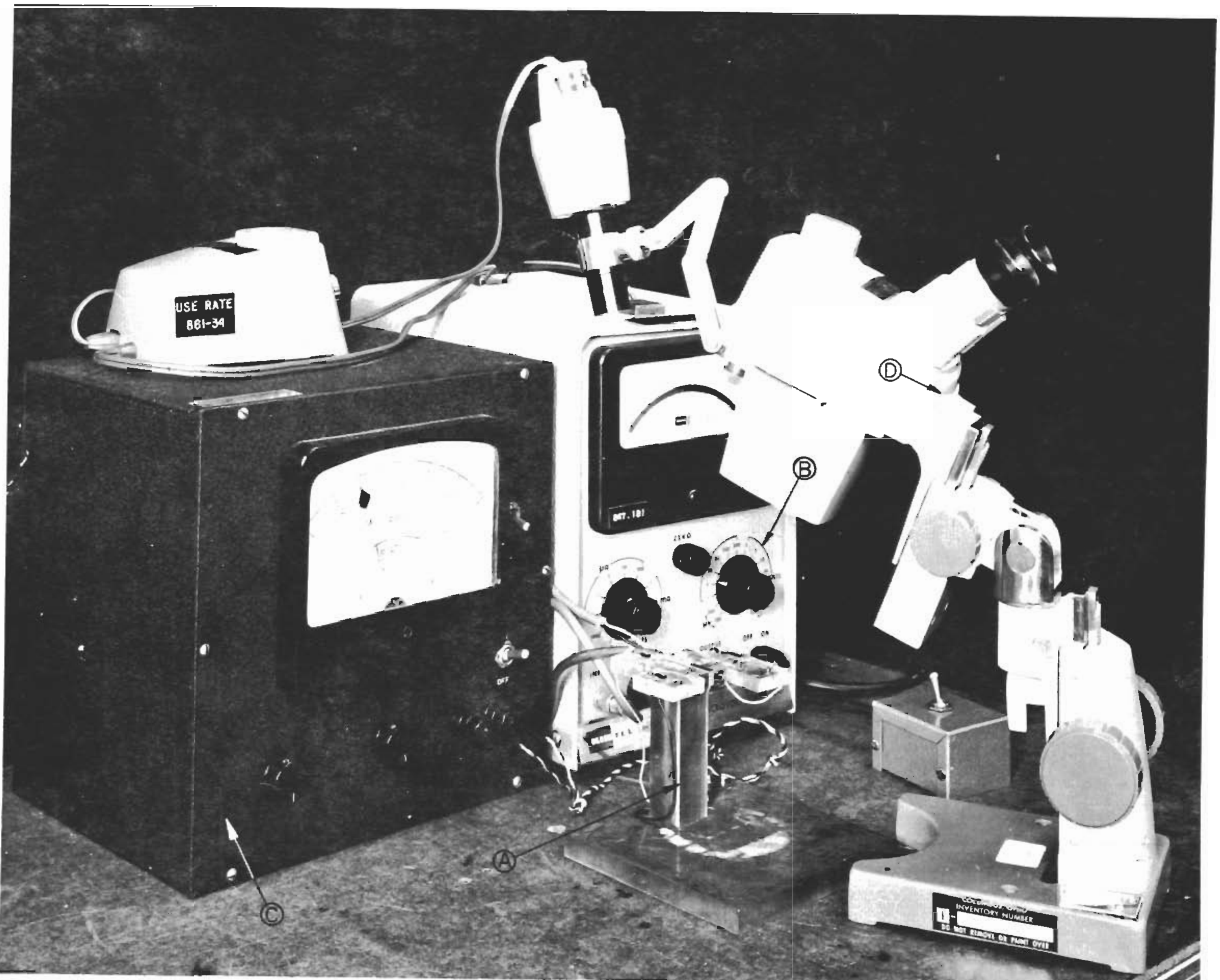


FIGURE B-8. RESISTIVE, ZERO-MAGNETIC-FIELD, HALL TERMINAL-ALIGNMENT APPARATUS



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FIGURE B-9. VIEW SHOWING POSITION OF HALL ELEMENT AND DIAMOND WIRE OF THE ALIGNMENT APPARATUS



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| | |
|---|---|
| Melting point | ~110 C |
| Thermal conductivity | ~5 x $10^{-3}$ watt/cm C |
| Resistivity | ~$10^{18}$ ohm-cm |
| Dielectric strength | ~500 volts/mil |
| Dissipation factor at 60 cycles | ~0.02 |
| Thermal coefficient of expansion | ~4.00 x $10^{-5}$/°F |

The procedure for mounting consists of controlled heating the module package uniformly to the melting point of the Kel-F200 wax. This is accomplished with a thermostatically controlled block heater.

Kel-F200 is applied in the area between the brass spacers of the module package. One element is then placed in position and coated with additional wax. The second element is placed atop the first element and additional wax applied. Pressure is applied to the elements after transferring module package to a cold block. Cellophane is placed over the Hall elements prior to applying pressure with a flat-surfaced block.

After the wax hardens, the Hall-element leads are bent away from surface, and excess wax is removed from brass spacer surface by passing the surface lightly over 600-grit metallographic paper.

The final operation involves the soldering of the current and Hall tab leads to properly coded terminals of the mounted terminal strip. This operation is quite simple and requires only standard soldering techniques.



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APPENDIX C

## ANOMALOUS BEHAVIOR OF THE INPUT RESISTANCE

The increase in the input resistance observed in a group of Hall elements made from Crystal 02-0109 was suspected to be related to microcracks introduced during the fabrication process. However, a microscopic examination of Elements 25 to 40 showed no evidence of such physical damage. Because the resistivity-profile data on Crystal 02-0109 (Figure 3) was extremely uniform, no explanation could be given for the anomalous behavior of the input resistance. As a result, it was decided to perform a dislocation density study by subjecting several elements to the "Sirtl" etch-pit solution.*

Examination of the etched elements revealed a high dislocation density (30,000/cm$^2$ estimated, which is not uncommon for float-zone grown silicon) and the presence of gross lineage** arrays oriented perpendicular to the current flow direction in the element.

Lineage arrays are known to introduce considerable variation in silicon-device characteristics. Impurities are easily precipitated at dislocation sites of the lineage variety. It is possible that such impurities can effectively increase the resistivity through carrier concentration at localized areas. However, it is not concluded here that this was the major factor causing the effects noted.

Figure C-1 shows photomicrographs of two elements having a high input resistance. They both exhibit lineage-type dislocations. Photomicrograph A is of Element 29 having the highest input resistance observed. Photomicrograph B is of Element 40, near the end of the high resistance distribution. It is noted that Element B does not contain a severe lineage, whereas Element A does reveal a strong lineage effect.

Another possible contributing factor in the affect observed could be related to localized carrier concentration in the center portion of the silicon crystal ingot. Time did not permit a resistivity profile determination of individual elements to verify this possibility. The efforts presented show that gross resistivity measurements performed on large-diameter crystals may or may not reveal the presence of resistivity gradients that lead to poor yield and poor quality control of devices.

*A modified "Sirtl" etch was used, which had a composition of one part concentrated HF (49 per cent) and two parts of a solution consisting of 50 grams $CrO_3$ dissolved in 100 ml deionized $H_2O$. Each element was etched for 10 minutes at room temperature. Silicon Hall elements were mounted on glass slides with Kel-F wax and polished with CP-4 type etch prior to "Sirtl" etch treatment.

**Lineage is defined as an array of dislocation etch pits that line up "peak-to-base" and are low-angle boundaries initiated by either impurity segregations or thermal defects during crystal growth.



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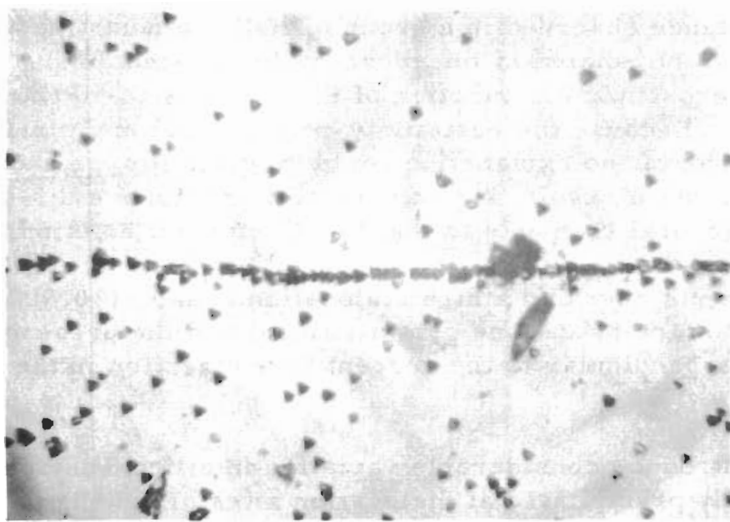
Current Flow

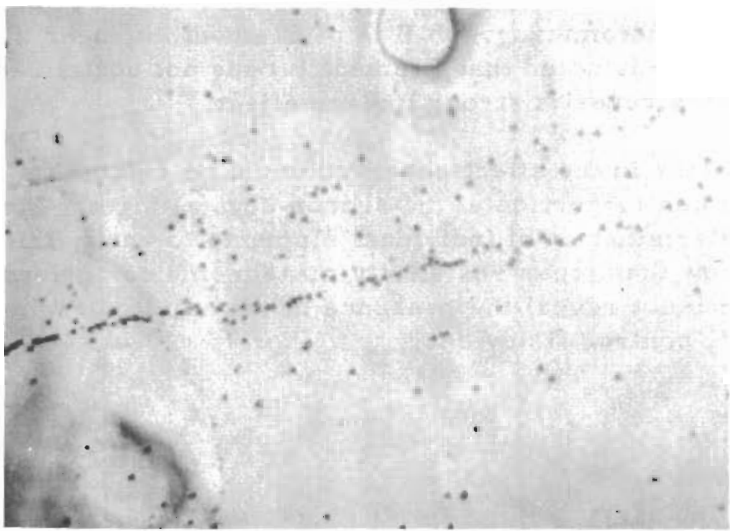


Lineage line

Hall output terminals

200X

Element (A)



Lineage line

200X

Element (B)

FIGURE C-1. PHOTOMICROGRAPHS OF TWO HALL ELEMENTS SHOWING THE PRESENCE OF LINEAGE TYPE DISLOCATION



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# APPENDIX D

## CONTACT-RESISTANCE DETERMINATION

The bonding of ohmic, low-resistance, electrical contacts to high-resistivity silicon is difficult. The Hall element contacts were therefore evaluated.

For mechanical strength, soldered contacts were used. The Hall elements would first be supplied with a plated contact to which individual leads could be readily soldered. In the soldering operation it is possible that this type of contact can be ruptured or damaged. As a consequence, it was decided to evaluate the specific contact resistance at the metal-silicon interface as a means of determining if such damage was introduced during soldering. This added information would also be useful in predicting a possible failure mechanism for Hall elements operated on a continuous basis.

The direct bonding of metal contacts by soldering, plating, etc., to high-resistivity silicon, for example, can result in a high value of contact resistance. To decrease the effective contact resistance in a high-resistivity material, the doping of the surface with the proper conductivity-type dopant by alloying or diffusion methods is required. The surface of the Hall-element current and Hall tab contacts were doped with phosphorus to near degeneracy by thermal diffusion methods. This surface is usually designated an n+ surface and is doped to a concentration level near $10^{20}$ atoms/cm$^3$.

### Test Specimen Preparation

The contact resistance test specimen was taken from the section of silicon crystal H-145 shown in Figure 3. The specimen was cut from the Hall-element block following the completion of block processing (see Appendix B). Copper blocks 0.5 cm long were applied to the ends of the specimen by soldering with a 60/40, tin/lead solder. The entire specimen was then lapped and polished to a uniform cross-sectional area. The over-all length of the specimen including the copper end blocks was 2.6 cm; the specimen was 1.6 cm long, 0.55 cm wide, and 0.22 cm thick.

### Test Procedure

An a-c method developed for evaluating the resistance at a metal-thermoelectric semiconductor contact[10] was used to determine the contact resistance between the metal-silicon interface. Briefly, the method involves longitudinal a-c potential probing along the specimen length from the metal-semiconductor interface. A 200-cycle a-c current signal is supplied to the specimen from a standard signal generator followed by power amplifier and impedance matching network. A wave analyzer is used to measure the input current to the specimen and the probe potential.



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To obtain a reference voltage, several potential measurements are made along the copper end block. The total resistance is calculated from the measured current and probe potential values. Several probe measurements are taken on the specimen to denote the quality of the contact and the reproducibility of the measurement. For Hall elements, a discontinuous contact at the current terminals, for example, could result in an increase in the magnitude of the zero magnetic field Hall terminal voltage by the channeling of current through localized regions.

## Results

Figure D-1 is a plot of resistance versus distance calculated from the potential measurements. As shown, the contact resistance ($R_c$) is difficult to interpret. An expanded plot revealed the value of $R_c$ to be $\approx 0.1$ ohm. This value was used to calculate the specific contact resistance (designated by the symbol $\delta$ on Figure D-1). The three series of measurements indicated that a good continuous contact was achieved.

Since an n+ layer was produced to a depth of 0.2 mils, the contact resistance also includes the added resistance of the graded layer.

Also shown on the curve is the resistivity value calculated from the resistance plot. The value of 106.0 ohm-cm was found to be in fair agreement with the value from the resistivity profile in Figure 3.

On the basis of the $\delta$ value determined, the total contact resistance for the input current contacts of the Hall element would be ~2.0 ohms. This amounts to 0.01 per cent of the total input resistance and is negligible. The total Hall terminal contact resistance is calculated to be ~12.3 ohms. This would account for 0.05 per cent of the Hall output resistance for a value of $R_{out}$ = 25,000 ohms.



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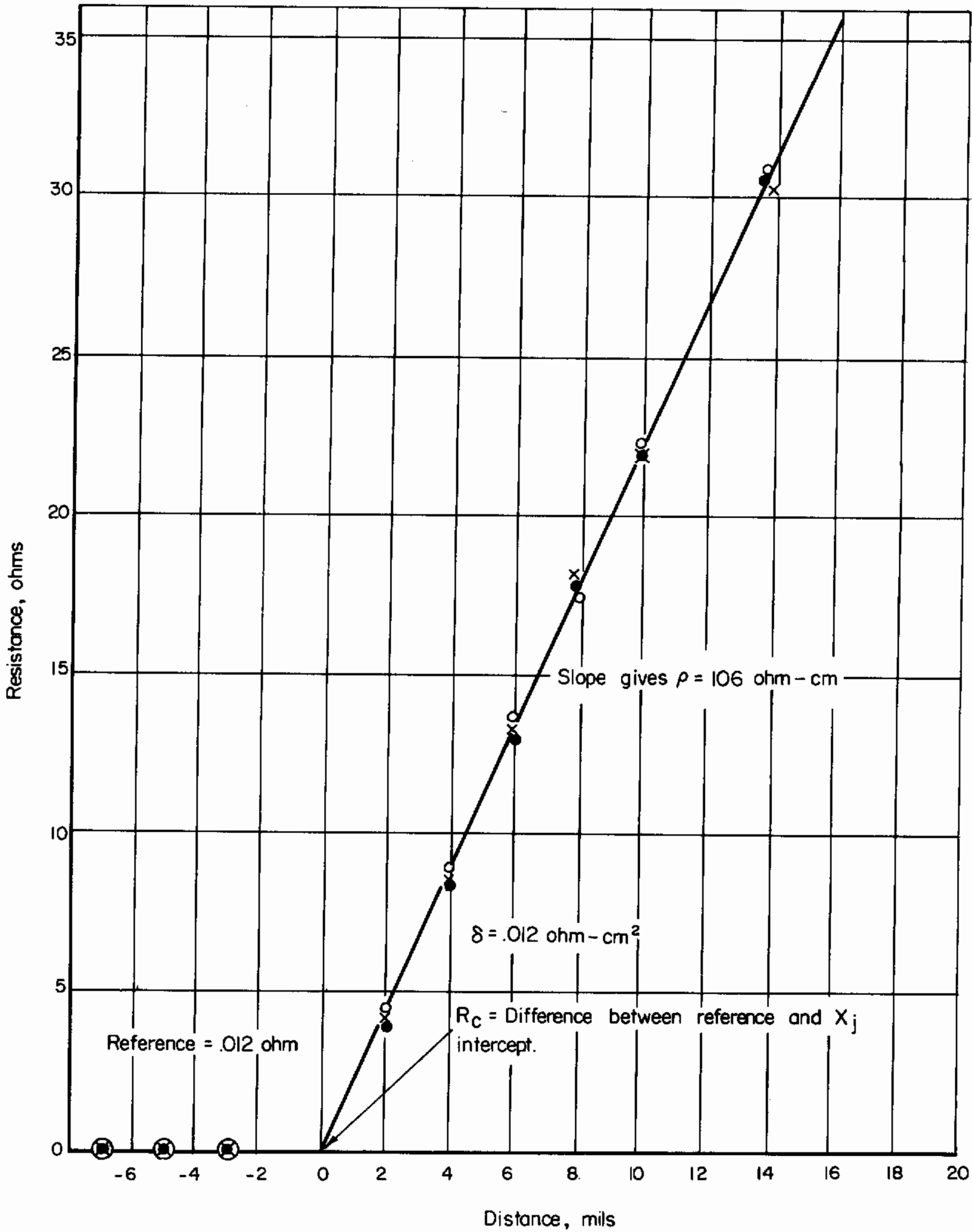


FIGURE D-1. RESISTANCE PLOT DETERMINED FROM THREE PROBE POTENTIAL EXCURSIONS PERFORMED ON THE CONTACT-RESISTANCE TEST SPECIMEN



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# APPENDIX E

## MULTIPLIER PACKAGE FABRICATION

### Module Construction

The module design feature consisted of two electrically matched Hall elements stacked together and wax mounted to the pole face of the magnetic core or pole piece. To eliminate the possibility of stress being applied to the Hall elements from the matching core pole face, a brass spacer scheme was used. This also served to maintain a close tolerance on the air gap between the pole faces of the adjacent magnetic circuit. The brass spacers were applied to the magnetic bar prior to mounting the Hall elements.

Figure E-1 is a dimensional perspective drawing of the module assembly. A Hall element is shown to indicate the position of the elements with respect to the magnetic bar dimensions. Figure 8 is a photograph of a module showing the various components comprising a complete unit.

The steps used in the fabrication of the module assembly are best described chronologically.

#### Step 1. Magnetic Bar Preparation

The magnetic bar sections as received from the supplier are not of uniform dimensions and do not contain flat and parallel pole faces; as a result, a grinding operation on the bar sections is necessary to shape the bars to the proper dimensions and to obtain parallel pole faces. The latter is essential to obtain close tolerance on the air gap following the attachment of the brass spacers.

The magnetic pole pieces were made from tape-wound core bar stock, Silectron, manufactured by the Arnold Engineering Company, Morengo, Illinois. This material is a laminated core structure prepared from iron laminates approximately 0.011 inch thick.

Five modules were fabricated from the tape-wound core material. The grinding operation on this material resulted in electrical shorting between the individual iron laminates. To remove the shorting effect, each surface was lapped and polished following the grinding operation. The surfaces were then etched with concentrated HCl acid for 10 minutes. Etching of surfaces was effective in removing a majority of shorts between the lamination. This was denoted by a change of the total resistance of the laminated structure from a few ohms resistance, after grinding, to several thousand ohms following etching.

#### Step 2. Brass Spacer Fabrication and Mounting

The application of the brass spacers to the magnetic bar requires three operations. First, a brass spacer subassembly, having a close dimensional tolerance, is machined into the configuration shown in the dimensional drawing of Figure E-1.


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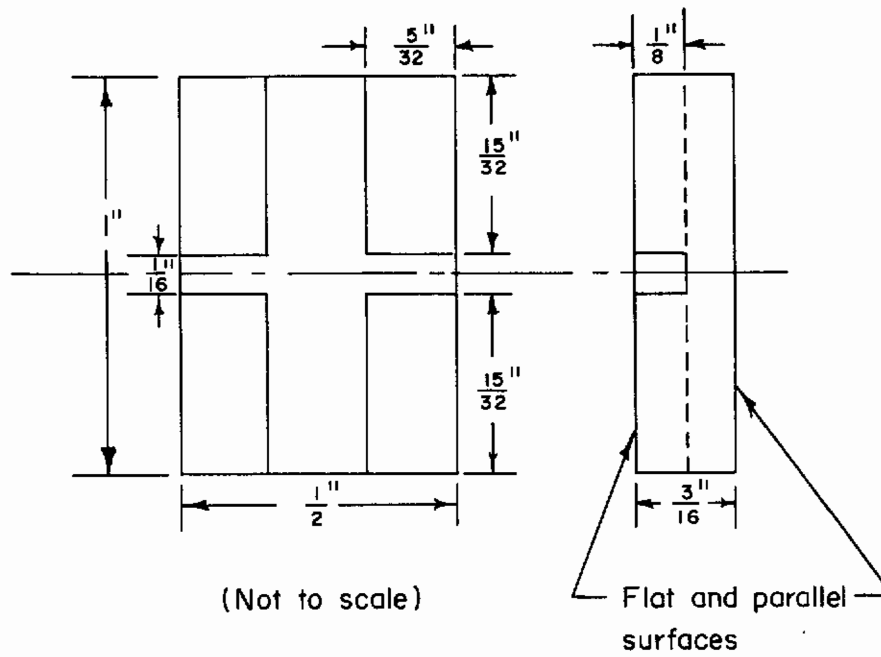


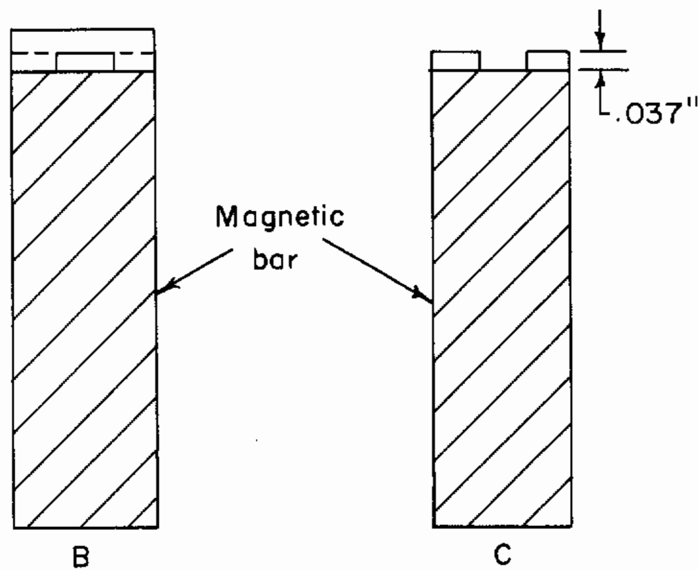


FIGURE E-1. DIMENSIONAL LINE DRAWING OF BRASS SUBASSEMBLY AND STEPS IN ATTACHMENT TO THE MAGNETIC BAR



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Second, the brass assembly is cemented to the magnetic bar surface as shown in the side-view drawing of Figure E-1. The third operation requires the removal of the excess brass by grinding to achieve the 0.037-inch thickness. This is demonstrated in Figure E-1.

The brass spacer subassembly was attached to several magnetic bars using a heat-cured structural adhesive, Type FM-47*. This adhesive is a thermosetting resin requiring various curing periods depending on the curing temperature and will withstand temperatures near 200 C without appreciable loss of bond strength; however, maintaining a close dimensional tolerance (adhesive thickness between brass and pole face) is somewhat cumbersome.

The FM-47 adhesive was abandoned in favor of Eastman 910 Adhesive**. Extremely thin layers (~0.2 mil) of Eastman 910 give high bond strength between the brass and bar face, and will easily withstand temperatures of 100 C for short periods without being adversely affected.

Eastman 910 is applied with a fine brush on the brass subassembly. The assembly is placed on the pole surface and clamped with slight pressure. After a 15-minute drying period, the bar assembly is ready for the final grinding operation.

## Step 3. Hall-Element Mounting

The Hall-element mounting procedure is described in the final step of the Hall-element fabrication procedure given in Appendix B.

## Step 4. Terminal Strip Attachment

Terminal strips prepared from GEC 500 Fiberglas material 1/16 inch thick are attached to each side of the magnetic bar with Eastman 910 adhesive following Step 3 above. Leads from the Hall tabs and input current contacts are soldered to the terminal pins of the terminal strip to complete the Hall module assembly.

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*Manufactured by the Bloomingdale Rubber Company, Aberdeen, Maryland.
**Marketed by the Armstrong Cork Company, Lancaster, Pennsylvania.



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# APPENDIX F

## ANALYSIS OF THE TWO-HALL-ELEMENT COMPENSATION CIRCUIT

Figure F-1 is the circuit of a compensation scheme that should accomplish the desired independence of the Hall product from temperature, core saturation effects, and changes in the Hall coefficient with flux density. It is shown that the product voltage, $V_H$, is independent of these variables if the following conditions are realized:

(1) The changes of element resistance with temperature and magnetic flux density variations for the two elements must be equal.

(2) The changes of element Hall coefficient with temperature and magnetic flux density variations for the two elements must be equal.

(3) The same flux must cut both elements.

(4) The gain of the amplifier is sufficiently high.

To obtain Conditions (1) and (2), it is necessary to make the elements as nearly identical as possible. By choosing two adjacent slices from a single crystal, it should be possible to closely approximate these conditions, therefore, to yield a high degree of compensation. Condition (3) can be closely approximated by the use of U-shaped cores for the magnetic structure with the elements placed in one or both of the gaps formed by the cores being fitted together.

Thus, satisfactory compensation for changes in the Hall coefficient and temperature effects may be accomplished with this circuit. In addition, the effects of the nonlinearities of the magnetic core can be reduced with this circuit to the point where they are negligible provided the amplifier gain is sufficiently high. It is therefore seen that this compensation circuit should permit the construction of a multiplier with a precision limited only by the degree of compensation introduced.

In Figure F-1, the diagram for the two-element compensation circuit, the difference between the Hall voltage output, $V_{H2}$, of reference Element 2, and the voltage, $V_x$, representing one of the input variables, is used to drive the power amplifier (assuming no gain in the differential amplifiers). The output of the amplifier excites the magnetic field in which both elements of the multiplier are located. Then

$$V_{H2} = \frac{R_{H2}\, I_2\, B}{t} \times 10^{-8} \text{ volt} \quad , \qquad \text{(F-1)}$$

where

$R_{H2}$ is the Hall coefficient of Element 2

$I_2$ is the current in Element 2 in amperes



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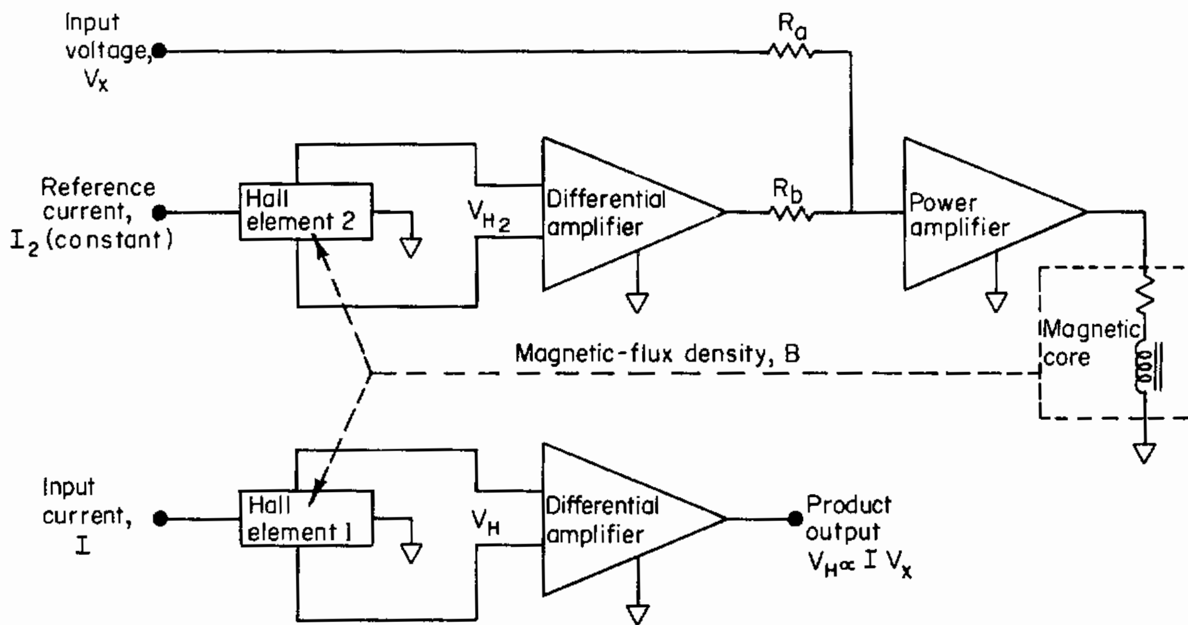


FIGURE F-1. TWO-ELEMENT COMPENSATION CIRCUIT



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B is the magnetic flux density in Element 2, which is assumed to be the same as the flux in Element 1, in gauss

t is the thickness of the Hall elements in cm.

The input drive to the power amplifier then is

$$V_x - V_{H2}$$

The flux density, B, in the core is proportional to the power amplifier drive and may be expressed as

$$B = G(V_x - V_{H2}) \quad , \tag{F-2}$$

or

$$V_{H2} = \frac{GV_x - B}{G} \quad , \tag{F-3}$$

where G is the proportionality factor.

Then, substituting Equation (F-3) in (F-1),

$$\frac{GV_x - B}{G} = cR_{H2}I_2B \quad , \tag{F-4}$$

where $c = 10^{-8}/t$.

Rearranging (F-4),

$$B = \frac{GV_x}{1 + cGR_{H2}I_2} \tag{F-5}$$

The desired product is the Hall voltage, $V_H$, of Element 1. Thus,

$$V_H = cR_HIB \quad , \tag{F-6}$$

where

$R_H$ is the Hall coefficient of Element 1

I is the current in Element 1, representing the second input variable.

Hence, substituting Equation (F-5) in (F-6),

$$V_H = \frac{cR_HIGV_x}{1 + cGR_{H2}I_2} \quad . \tag{F-7}$$

If $G \gg 1$

$$V_H \rightarrow \frac{R_HIV_x}{R_{H2}I_2} \quad . \tag{F-8}$$



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Since $I_2$ is held constant in Element 2 and $R_H$ and $R_{H2}$ are equal (elements cut from material having as near identical characteristics as possible), $V_H$ would approach being exactly proportional to $IV_x$. Thus

$$V_H \propto IV_x \tag{F-9}$$



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