AL TDR 64-187

# RESEARCH ON RADIATION-RESISTANT HIGH-TEMPERATURE THERMIONIC CIRCUITRY

TECHNICAL DOCUMENTARY REPORT NO. AL TDR 64-187

August, 1964

AF Avionics Laboratory
Research and Technology Division
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio

Project No. 4156, Task No. 415604

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The Tube Department, General Electric Company,
Owensboro, Kentucky)

# FOREWORD

This document reviews the development work performed and the results obtained during an applied research program, Contract AF 33(657)-11400, carried out by the Advanced Development Engineering Subsection, Tube Department, General Electric Company, Owensboro, Kentucky. This program was directed toward the development of radiation tolerant Thermionic Integrated MicroModule (TIMM) components and circuitry. The work was administered under the direction of the Electronic Technology Laboratory, Aeronautical Systems Division, Wright-Patterson Air Force Base, Dayton, Ohio; Mr. V. L. Cartmell, project monitor.

This report covers the period from the effective starting date of the contract, June 3, 1963 through May, 1964. Materials and processing investigation programs, individual circuit element development programs and integrated circuitry design and performance discussions are presented.

## ABSTRACT

This report covers the developmental work conducted during the contract period, June 3, 1963 through May, 1964, and discusses the progress made and problems encountered in designing and fabricating radiation tolerant, high temperature, Thermionic Integrated MicroModule (TIMM) circuit elements and functional circuitry.

The objectives of the program were to perform applied research toward the evaluation and processing of materials exhibiting stable and superior physiochemical characteristics over the temperature range up to 600°C, and to incorporate such materials into devices, modules and integrated circuits for reliable operation in severe mechanical, thermal and radiation environments.

Functional circuits, fabricated to demonstrate feasibility of the TIMM concept, have been designed to operate at 580°C. Performance characteristics of functional electronic circuits have been discussed in the interim reports of this program and are summarized herein.

Although many facets of the TIMM concept are still developmental, the results obtained thus far clearly demonstrate the feasibility of this approach.

This program has shown that many opportunities still exist for further size and weight reductions by the combination of individual circuit elements into multi-structure, functional elements. Further applied research is necessary to: (a) optimize performance characteristics of TIMM active circuit elements, (b) improve the high temperature properties and radiation tolerance of materials, and (c) broaden the application possibilities of this radiation hardened electronic system. Future work directed toward these objectives should lead to high reliability and high performance electronic components permitting the extension of the TIMM system to functional electronic circuits designed for RF and power applications as well as improved digital capability.

## PUBLICATION REVIEW

Publication of this technical documentary report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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# ACTIVE COMPONENTS

The results of this work are organized and reported under the following classifications:

1. Grid mesh processes other than photoetching.
2. Grid mesh configuration study.
3. Titanium-clad grid investigation.
4. Cathode refinement program.
5. Stable contact potential investigation.
6. Zero contact potential.
7. Tubes for circuit modules.

## GRID MESH PROCESSES OTHER THAN PHOTOETCHING

### Titanium Coating Thickness

A grid with strength greater than that of titanium foil is shown in Figure 1. The grid wires are composed of two different materials. The center or core of the wire is a refractory material such as molybdenum or tungsten to provide strength, and the outer surface or coating is of titanium for its desirable electrical characteristics.

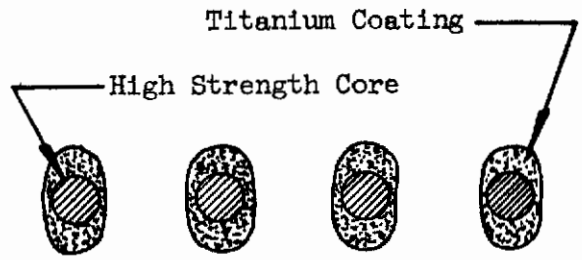


Fig. 1 Cross-Section of Titanium Coated Grid Wire

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These characteristics depend upon a pure titanium grid surface. This grid is subjected to breakdown products of the cathode and seal products during the sealing process and requires sufficient mass of titanium to getter these materials and remain clean.

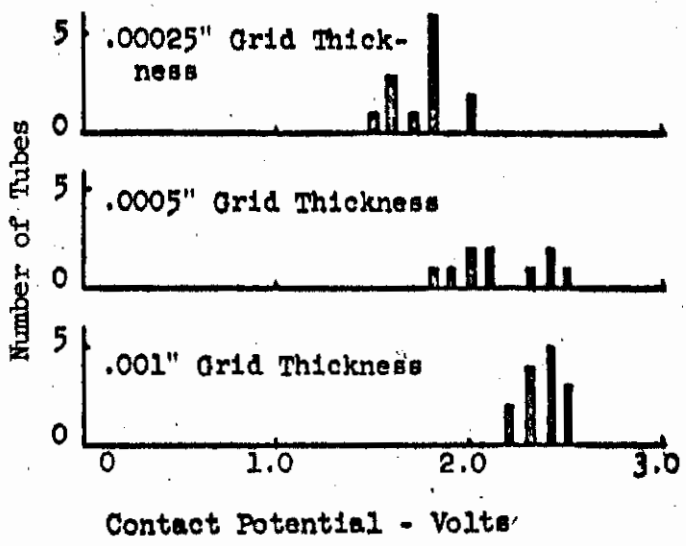
Experiments to determine the necessary titanium thickness were performed with titanium grids ranging in thicknesses from .00025" to .001". Data on these tests, Figure 2, indicate that grids thinner than .001" have a wider variation and a lower average contact potential than do the grids .001" thick. Life test data shown in Figures 3 and 4 indicate that the stability during life does not appear to depend upon grid thickness.

These data indicate that at least .0005" of titanium is required on each side of the grid to have the electrical characteristics of solid titanium, resulting in a minimum grid thickness .001" over the thickness of the strong metal core. This minimum diameter limits the grid turns-per-inch, which in turn limits the tube performance.

Titanium coatings on grids and diode anodes were tested and are described later in this report.

Molybdenum and Tungsten Grids

A TIMM triode was designed to evaluate tungsten and molybdenum grids. Tubes were built containing grids that were cleaned by several different processes, including electrocleaning, electroetching, hydrogen firing and vacuum firing, as well as several methods of degreasing. These tubes were life tested with the results shown in Figure 5. It may be noted that present processing methods for tungsten or molybdenum grids do not result in stable tube characteristics, the emission falling very quickly during life.



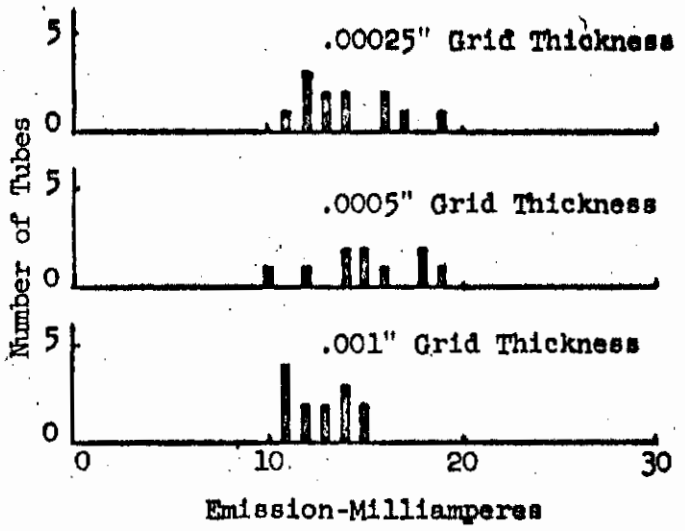
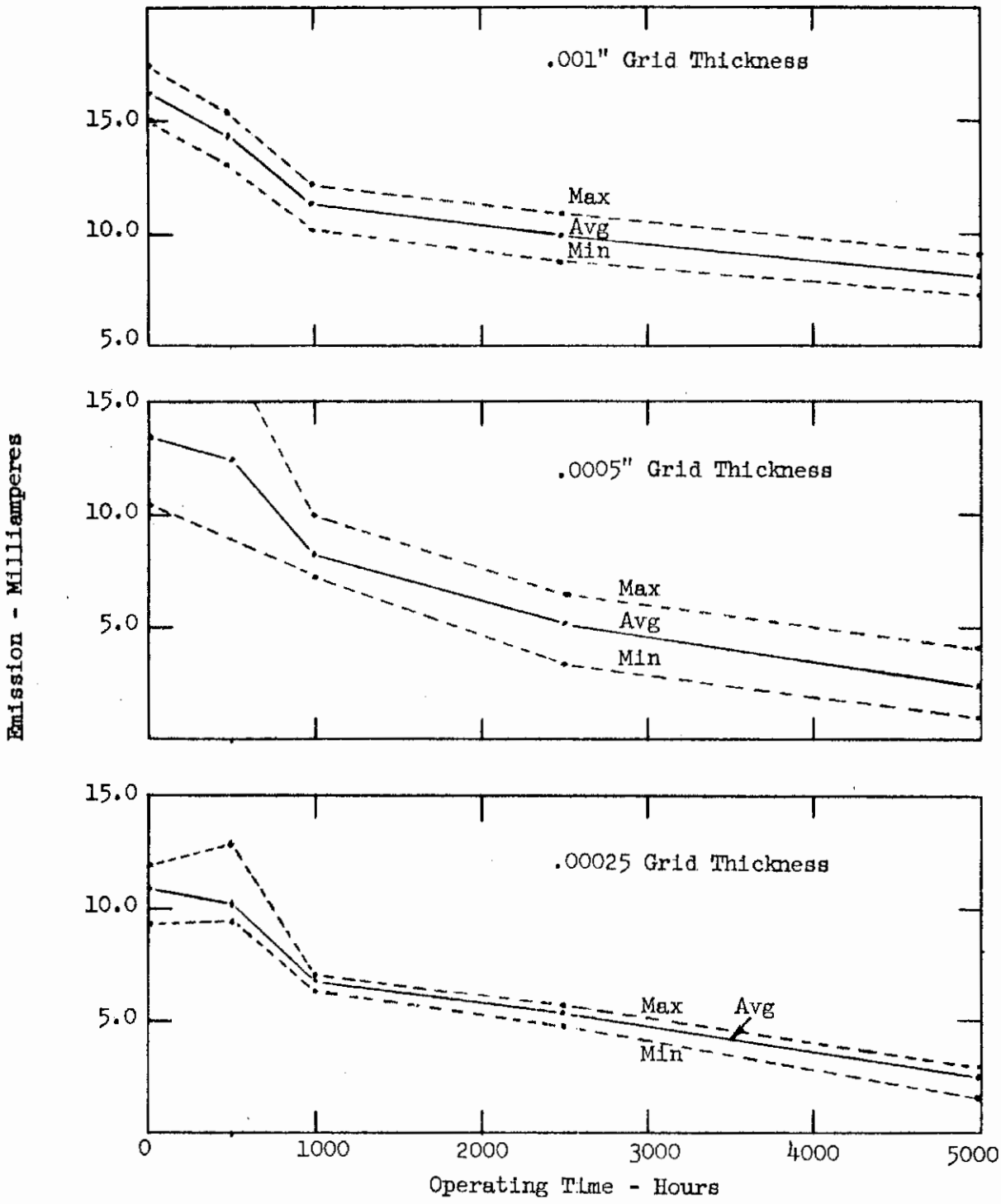



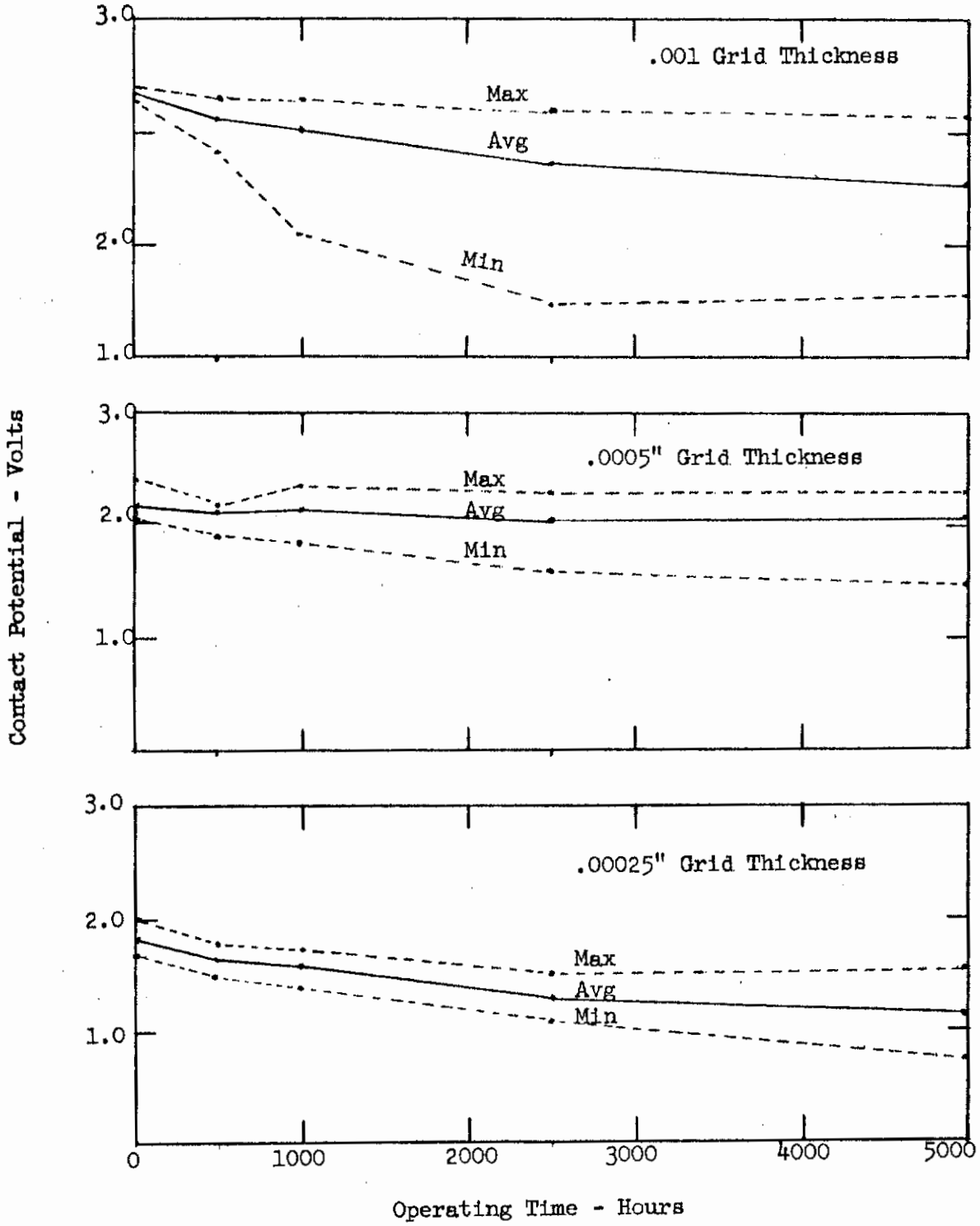

Fig. 2 Distribution of Grid-Cathode Contact Potential and Emission Vs Grid Thickness

XD-62 Triode
K-55611-W62D-3 Hexagonal Mesh Grid




| Operating Conditions: | Test Conditions: |
|---|---|
| Temperature = 580°C | Temperature = 580°C |
| $E_b$ = 15 V, $R_L$ = 1000 Ohms | $E_p$ = 35 V |
| $E_c$ = 15 V, $R_g$ = 1000K Ohms | $E_c$ = 35 V, $R_g$ = 22K Ohms |

Fig. 3 Average Emission Vs Operating Time
XD-62 Triode



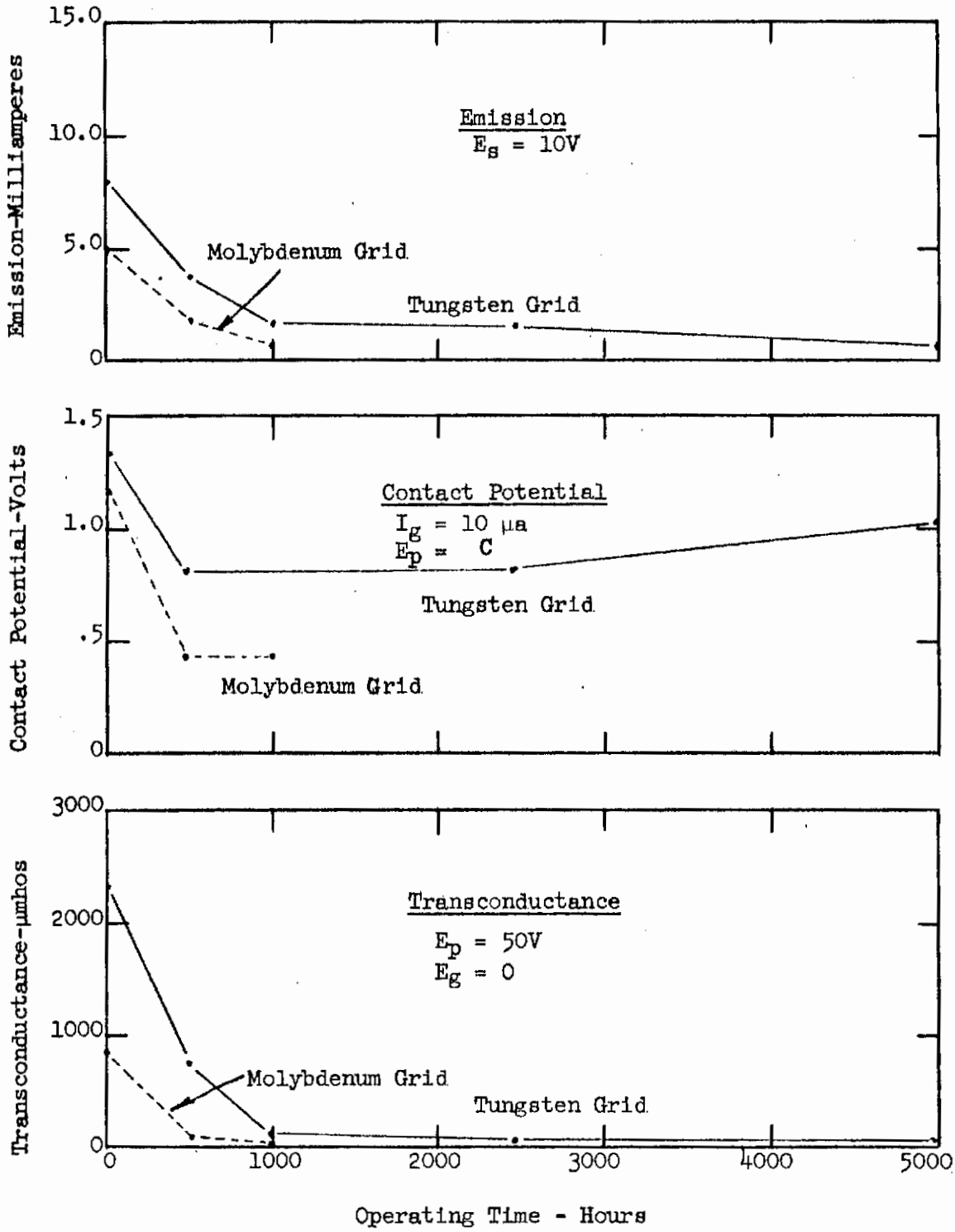

Operating Conditions:

Temperature = 580°C
$E_b$ = 15 V, $R_L$ = 1000 Ohms
$E_L$ = 15 V, $R_g$ = 100K Ohms

Test Conditions:

Temperature = 580°C
$E_p$ = 0
$I_g$ = 10 μa

Fig. 4 Average Contact Potential Vs Operating Time
XD-62 Triode




**Operating Conditions:**

Temperature = 580°C
$E_p$ = 50 V, $R_L$ = 1000 Ohms
$E_c$ = 0, $R_g$ = 22K Ohms

**Test Conditions:**

Temperature = 580°C
Molybdenum Grid Tubes Failed
After 1,000 Hours

Fig. 5 Average Emission, Contact Potential & Transconductance Vs Operating Time - TIMM Triode Comparing Grid Materials

Titanium Alloys

Two titanium alloys, 13V-11Cr-3Al containing 13% vanadium, 11% chromium, and 3% aluminum; and alloy GAl-4V containing 6% aluminum, 4% vanadium, were considered for grid material. These alloys are stronger than pure titanium. 13V-11Cr-3Al alloy does not exhibit distortion caused by crystal phase transition at high temperatures.

These alloys were first tested as diode anodes to determine the electrical effects on tube characteristics. These tubes were built as shown in Figure 6, and had only the anode stud fabricated from the material under test. The initial test data on these groups of tubes, shown below, indicate that pure titanium is superior to either alloy as an anode material:

| | Titanium | 13V-11Cr-3Al Alloy | GAl-4V Alloy |
|---|---|---|---|
| Emission | 15.1 ma | 7.0 ma | 9.5 ma |
| Contact Potential | 2.37 V | 2.32 V | 2.1 V |

It is believed that grids of these alloys would cause a lower emission and contact potential level in triodes. Life test data shown in Figures 7A and 7B indicate that there is no significant difference in stability between these groups of tubes.

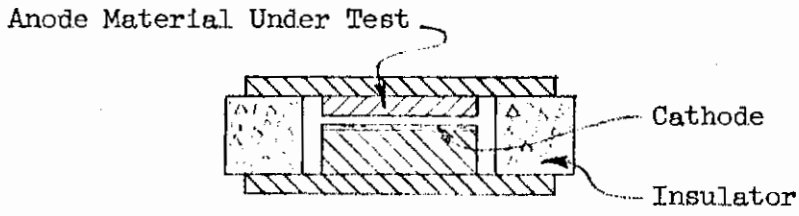
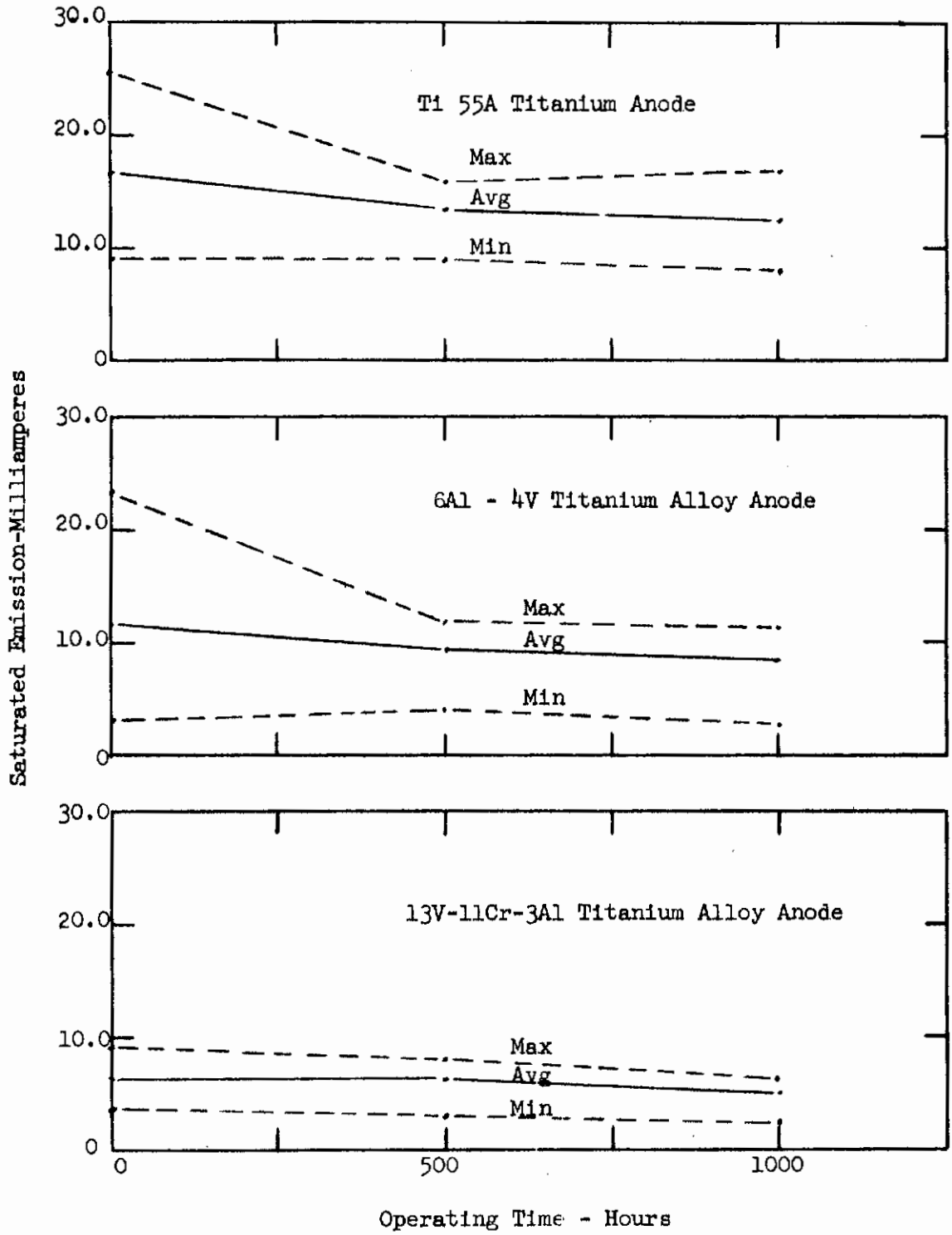



Fig. 6 Cross-Section of Test Diode



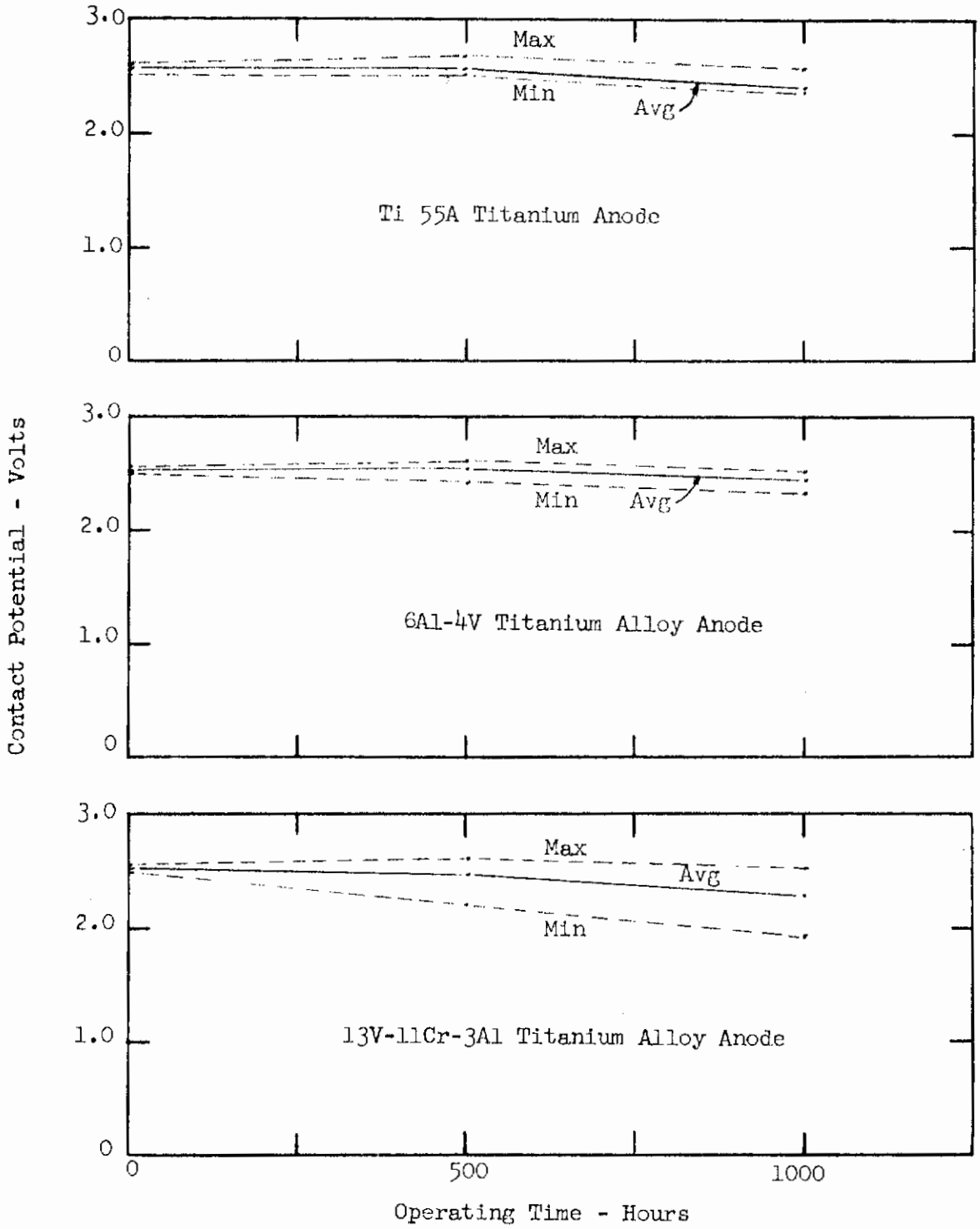

Operating Conditions:

Temperature = 580°C
$E_b$ = 10 V, $R_L$ = 1500 Ohms
$I_k \approx$ 4 Ma

Test Conditions:

Temperature = 580°C
$E_p$ = 10 V

Fig. 7A Average Emission Vs Operating Time
XD-61 Diode




Operating Conditions:

Temperature = 580°C
$E_b$ = 10 V, $R_L$ = 1500 Ohms
$I_k \approx$ 4 Ma

Test Conditions:

Temperature = 580°C
$I_p$ = 50 μa

Fig. 7B Average Contact Potential Vs Operating Time
XD-61 Diode

An attempt to draw the 13V-11Cr-3Al alloy down to a wire .001" in diameter for use in a wound grid was made. At this writing, .004" is the smallest diameter to which this material may be drawn without breaking. Previous attempts to roll this material to a suitable foil thickness for photoetched grids were also unsuccessful.

From the experiments performed, it was found that the titanium alloys degrade the emission level of the tube, and at least one of them is exceedingly difficult to fabricate into suitable sizes. Therefore, it is believed that tubes requiring a positive contact potential require pure titanium grids.

Wound Titanium Grids

The feasibility of fabricating grids by winding titanium or titanium alloy wire on a support was investigated. First experiments were performed by cementing the grid support ring onto a ceramic mandrel, winding the lateral wire over the ring, and then brazing the wire to the support ring. The wire could not be wound sufficiently tight without breaking to remain in contact with the ring, and it was found necessary to put a piece of ceramic on each side of this assembly with jig pressure during the vacuum brazing operation. Figure 8 shows the method of assembly.

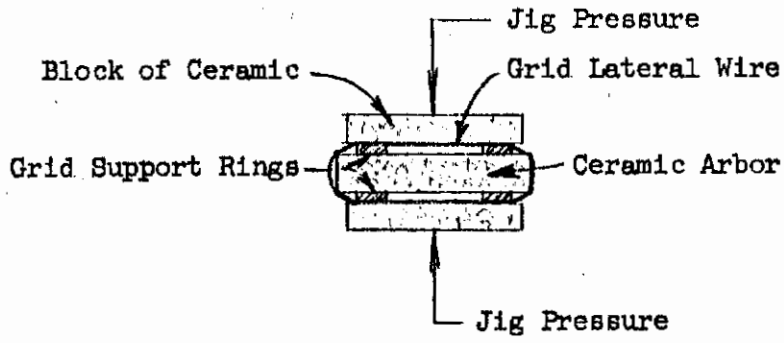



Fig. 8 Cross-Section of Grid Winding Mandrel

Two grid materials were tested - .001" diameter pure titanium wire obtained by etching .002" titanium wire, and .004" diameter 13V-11Cr-3Al titanium alloy wire. The support ring was fabricated from the same material as the wire.

The first consideration in selecting a brazing material was that it must not melt below the tube sealing temperature, approximately 1,000°C. Another requirement was that the brazing material must wet both the wire and the support without dissolving either. These two requirements eliminated many brazing materials commonly used in tube fabrication. The results of the brazing alloy tests are as follows:

1. Gold-Palladium - This alloy evaporated during the vacuum brazing step and made an unsatisfactory bond.
2. Thorium-Titanium - This alloy requires a high temperature, approximately 1,200°C, to braze. The grids with .004" diameter wire brazed very well but the grids with the .001" diameter titanium wire were wrinkled and distorted.
3. Gold - The phase diagram indicated that gold and titanium will not go into solution at normal sealing temperatures, making gold a satisfactory brazing material for tungsten wire on a tungsten support. Theoretically, a grid of these materials could subsequently be coated with titanium which would be compatible with the sealing temperatures. When an attempt was made to braze small diameter titanium wires with gold, the gold dissolved the wire completely during the brazing operation.

Neither titanium alloy nor pure titanium wound grids are feasible at the present state-of-the-art. It is believed that future developments could lead to a satisfactory grid of this type.

## GRID MESH CONFIGURATION STUDY

### Mesh Shape

The photoetched titanium foil grid is the only satisfactory grid tested to this date. Several different mesh patterns, square, rectangular, and hexagonal, each with inherent advantages and disadvantages, have been tested previously. Square grid patterns lost transparency because of corner radii. Rectangular patterns are weaker in one direction than another, allowing some grids to split when tensioned. Hexagonal mesh patterns have proved to be stronger and more uniformly tensioned. However, the photoetching master has round holes rather than hexagonal as specified because of loss of resolution during the photographic processes required to make an etching master. Figure 9 is a photograph of a thin molybdenum grid showing the shape of the grid holes. Titanium grids from this master have a similar appearance, and a representative section is shown in Figure 10.

Recently, the grid supplier made an improvement in the master fabricating techniques resulting in a master with holes more nearly hexagonally shaped. Figure 11 is a molybdenum grid from such a master. This grid was not designed for use in a tube but merely represents the state of the etching art. It is .003" thick with wires .001" wide at the narrowest point. Due to lack of time, titanium grids were not etched from this master.

Grids composed of lines that may be machine scribed do not have the photographic loss of resolution, but they are limited to patterns of continuous parallel straight lines, concentric circles, or combinations of these lines.

One possible technique to minimize the loss of transparency due to excessive corner radii is illustrated in Figure 12. Wires running one way

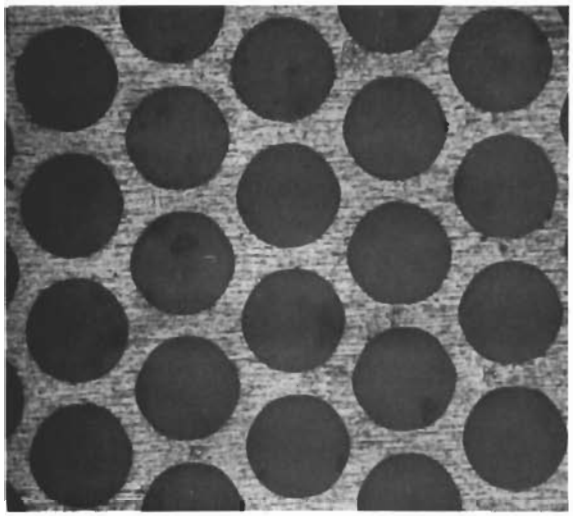


Fig. 9 Photoetched Molybdenum Grid Mesh Material Thickness .0005" (X120)

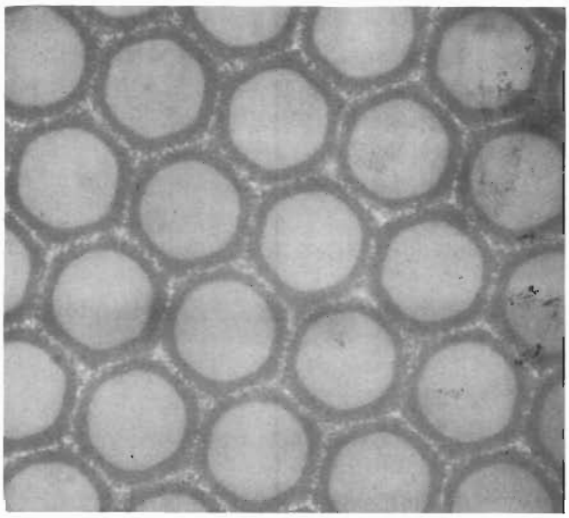


Fig. 10 Typical Photoetched Titanium Grid Mesh Material Thickness .001" (X120)

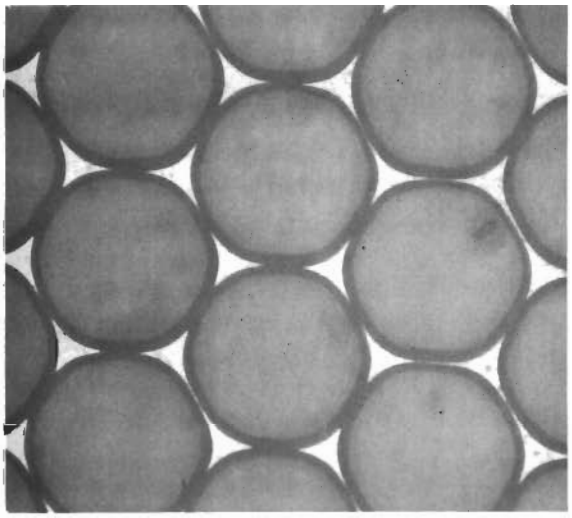


Fig. 11 Photoetched Molybdenum Mesh Material Thickness .003" Improved Master Process (X120)

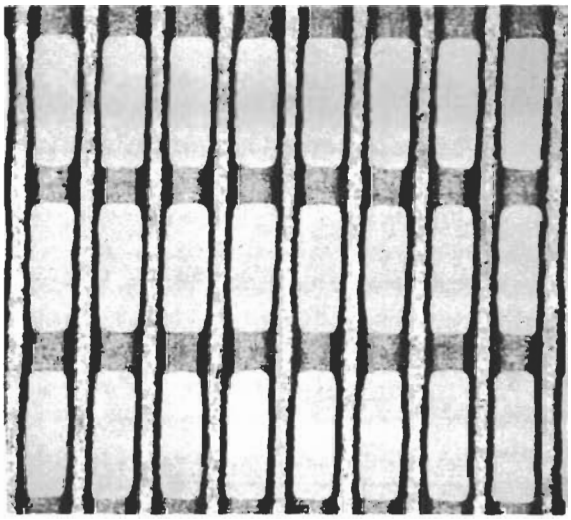


Fig. 12 Photograph of Titanium Mesh with Cross Wires Etched from Opposite Sides of the Foil. Material Thickness .001" (X52)

are etched from one side of the sheet while the cross wires are etched from the opposite side of the sheet. When this type of grid is etched from a sheet of titanium of normal thickness (.001"), the effective thickness of the control "wire" is only half that of the normal grid mesh. Past experience suggests that grids made from such thin material may be subject to more contact potential stability problems than those having thicker control electrodes.

The occasional breakage of wires or splitting of mesh when the grid is tensioned are reasons for grid failure. Titanium grid mesh may be stretched only a very little until it breaks. Slight variations in the force applied to the grids may be responsible for a complete lack of tensioning resulting in loose grids or over-tensioning which causes broken grids. The curved wire grid mesh pattern, Figure 13, suggested by V. Cartmell, is designed to have a greater stretching range in one direction than do straight wires. The wires in this grid mesh are curved when placed in the tube. As the grid is tensioned, the curved portions straighten, thereby allowing more expansion with no breakage. Tensioning would be dependent upon the stress retained in the deformed wires following the processing operations. (The wires could be curved in both directions, of course). Due to lack of time, this type of grid was not constructed.

Etched Grid Mounting

Figure 14 illustrates how lateral misalignment of electrodes observed in tubes will cause a grid to be poorly positioned. In an attempt to correct this problem, a new triode was designed utilizing insulators which fit very closely around the anode and cathode studs. These insulators also incorporate a solder trap groove next to the end electrodes to

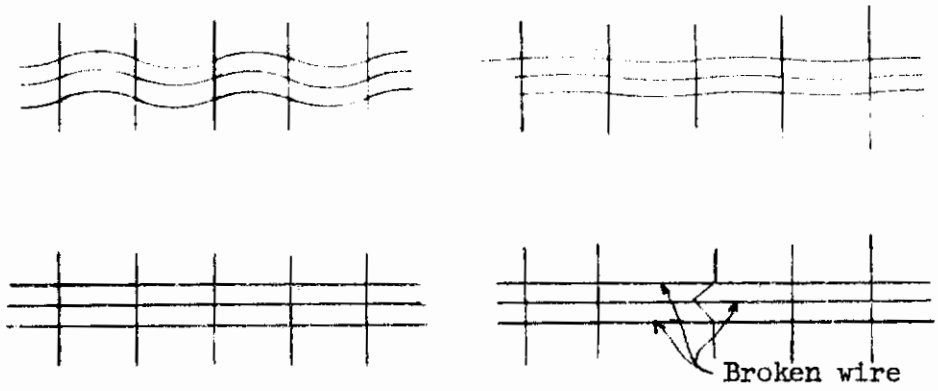



Fig. 13 Comparison of Curved Wire Grid to Straight Wire Grid When Tensioned

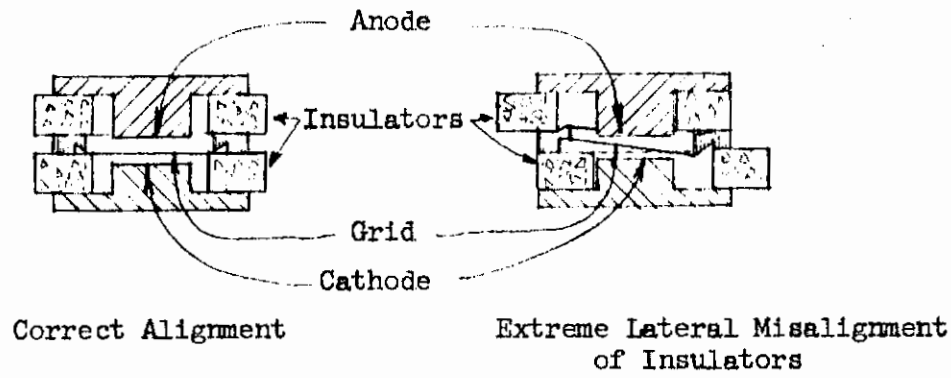



Fig. 14 Effect of Lateral Misalignment of Insulators on Triode Grid Position

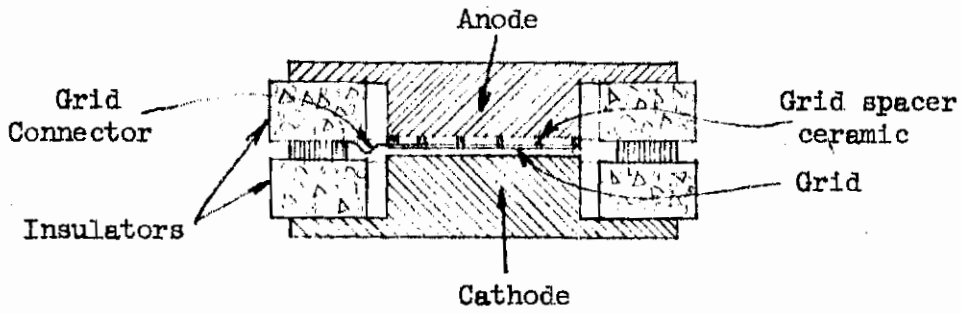
prevent brazing material from flowing up the side of the studs. This construction tolerated some electrode misalignment and improved the uniformity of grid tensioning. It was found necessary to modify the grid electrode to reduce the amount of grid tensioning to prevent grid breakage. Grids in tubes constructed in this manner were generally flat and had fewer shorts.

Since the titanium foil grid would not remain in tension after the tube was sealed, a support for the center of the grid was deemed necessary. A new design is shown in Figure 15. This design incorporated an insulator with perforations matching the grid openings brazed between the grid and the anode. Two materials were tested as a spacer. It was found that boron nitride could be cut the shape of the grid mesh but was too soft for an adequate braze. Forsterite could be brazed but was too hard to perforate. The thin titanium grid would dissolve instead of brazing.

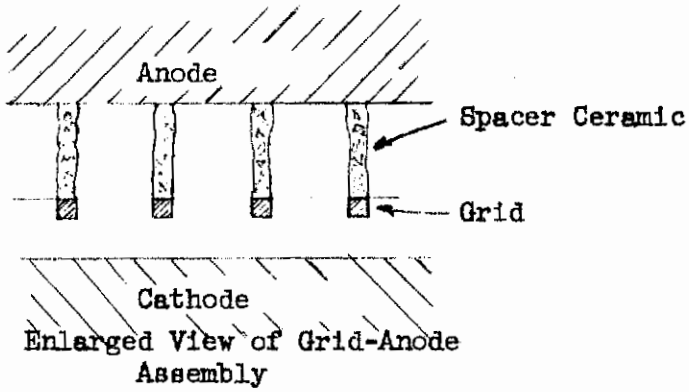
A new design with an adequate grid support is shown in Figure 16. This design utilizes ceramic posts in the center of the cathode and anode to clamp the grid in the proper location at the center. This design also utilizes the insulators which support the grid very close to the cathode and anode studs. Several methods of assembly were developed. Figure 17 shows a photograph of a tube cross-section built with the latest techniques.

An electrostatic stress between the grid and the anode was applied to test the strength of this construction. A low voltage was applied and then gradually raised until a current flowed indicating a short between the grid and the adjacent element as shown below:

| Center Grid Post | | No Grid Post | |
|---|---|---|---|
| No. | Volts | No. | Volts |
| 616 | 850 V | 651 | 220 V |
| 638 | 750 | 653 | 140 |
| 640 | 900 | 654 | 250 |
| 646 | 950 | 657 | 150 |
| 648 | 875 | 660 | 200 |
| Avg. | 855 | Avg. | 192 |




Tube Cross-section




Enlarged View of Grid-Anode Assembly

Fig. 15 Triode Design with Grid Mounted on Anode With Spacer Ceramic

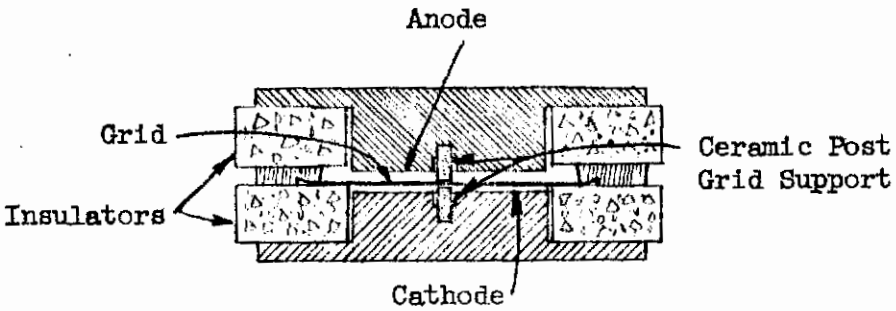
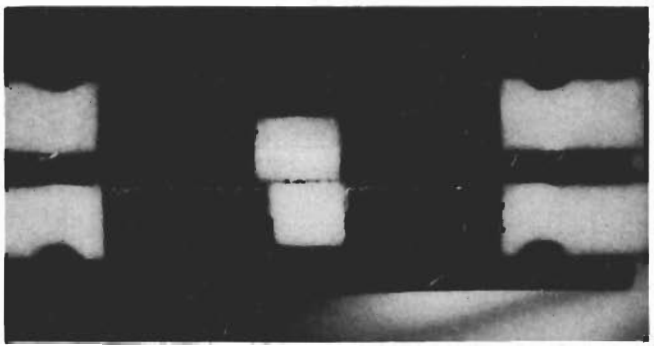



Fig. 16 Sketch of Cross-Section



Photograph of Cross-Section of Tube
Built in Development Laboratory

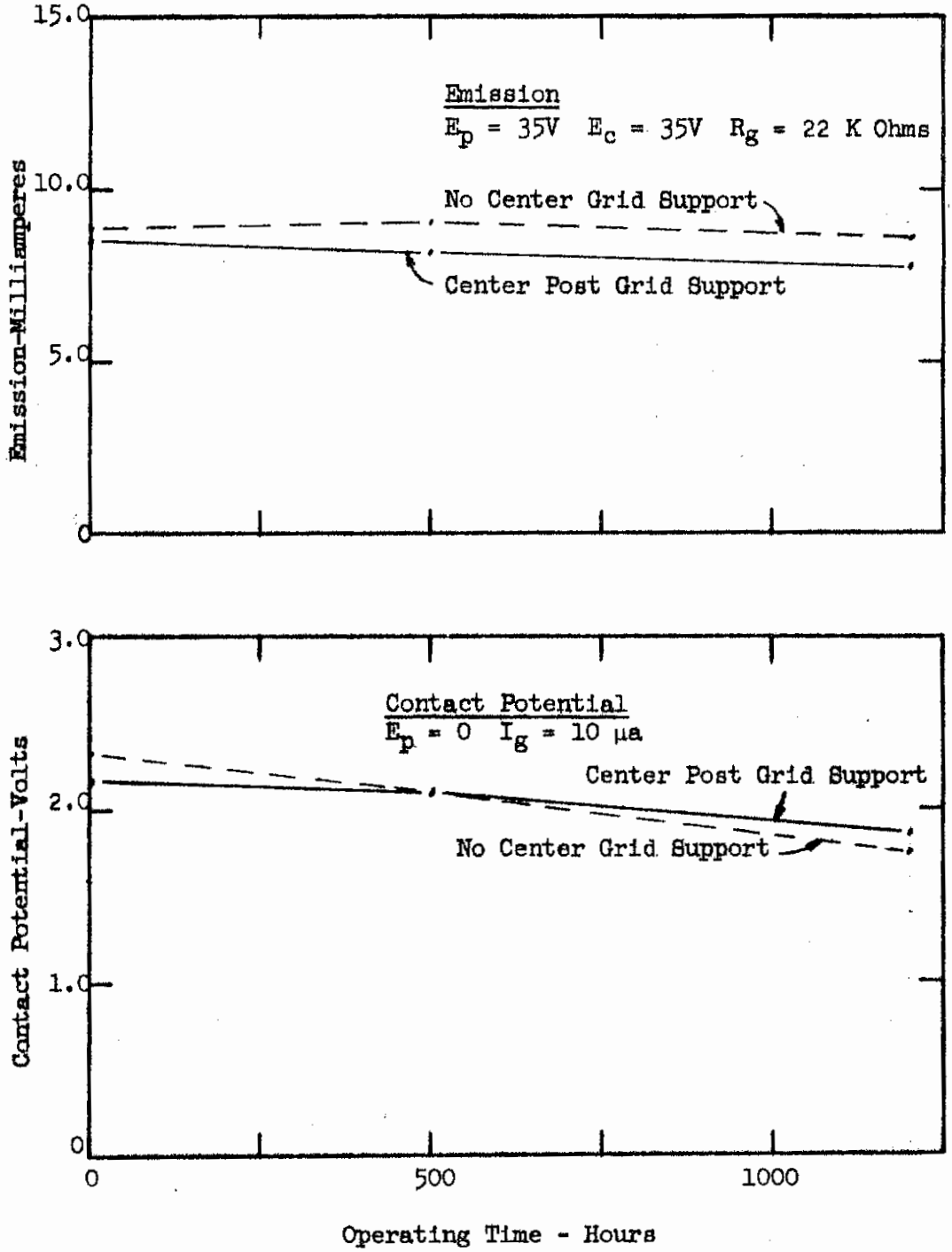
Fig. 17 Triode with Ceramic Post Grid Support

It may be noted that the post construction required four times the voltage that the unsupported construction required to cause a failure to occur. Subsequent analysis of the tubes showed that all the unsupported grids bowed and shorted while none of the post supported grids were mechanically disturbed.

Life test data of tubes with and without the grid support post are shown in Figure 18, and illustrate that the ceramic post has no effect on the electrical stability of the tubes.

Still another improved design is shown in Figure 19. This design stretches the grid over a ceramic cylinder placed closely around the cathode stud. Tubes built with this construction appeared to have uniform electrical characteristics. For ultimate ruggedness, this construction would also require the ceramic post grid support.

It was determined experimentally that the titanium alloy 13V-11Cr-3Al has a higher temperature coefficient of expansion than titanium. A new design using this material as a grid support ring to stretch the grid as




Operating Conditions:

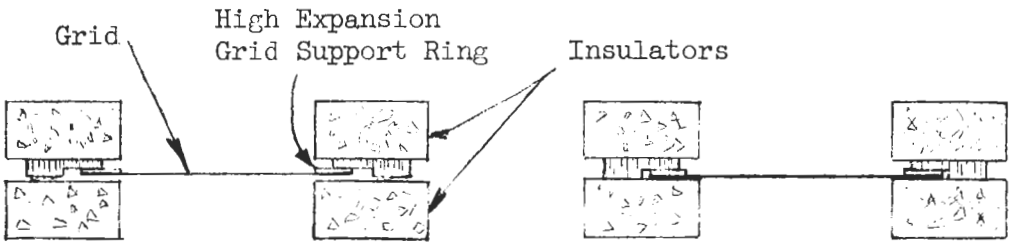
Temperature = 580°C
$E_b$ = 15 V, $R_L$ = 1000 Ohms
$E_c$ = 15 V, $R_g$ = 100K Ohms

Test Conditions:

Temperature = 580°C

Fig. 18 Average Contact Potential and Emission Vs Hours of Operation, XD-62 Triode


Fig. 19 Triode with Grid Stretched Over Ceramic Cylinder




The grid support ring is floating before and during the sealing operation. During the sealing process as the tube is heated, the high expansion ring expands more than the grid mesh thereby putting the grid mesh in tension. After sealing, the ring is held so that it can not move with respect to the body.

Fig. 20 Expansion Ring Grid Tensioning

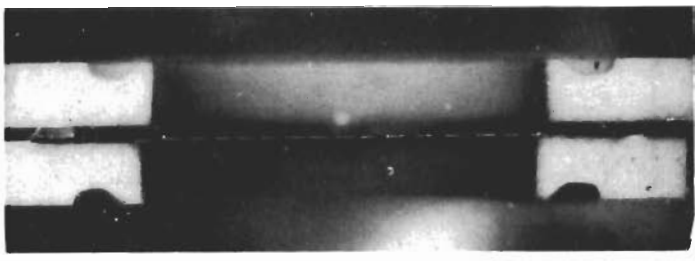


Fig. 21 Photograph of Grid Cross-Section Tensioned by High Expansion Support Ring

the tube is processed is shown in Figures 20 and 21. It was found that a grid ring of this material would stretch a grid and hold it flat during sealing unless a coated cathode was placed next to the mesh when it would bow. It is believed that this method of grid tensioning will work with suitable materials.

A planar grid lacks rigidity unless a high degree of tension can be maintained. A dome or conical shaped grid has some degree of rigidity because of its shape. An analysis was made to determine the optimum dome height for a TIMM triode with a .200" diameter grid. Other assumptions were necessary for a valid analysis and are discussed below:

1. It was determined that titanium may increase in size at least .2% when it is heated above the crystal phase change temperature and allowed to cool. It was assumed that the grid could "grow" .0005" from a .200" diameter during tube processing.
2. Lateral misalignment of planar electrodes does not affect the spacing but misalignment of dome-shaped electrodes causes spacing variation in proportion to the dome height. For the purpose of this analysis, .005" misalignment was assumed.

Figure 22 shows graphically each of these spacing effects for various dome heights and the sum effect of these defects, which indicates a dome height of .012" is optimum. This would allow a $\pm$ .00125" variation due to grid changing size and electrode misalignment which is too high in a close-spaced, high perveance tube.

Other Methods of Reducing Mesh Grids

The possibilities of electron beam or spark eroding machining were reviewed with the personnel at the General Electric Research Laboratory in Schenectady. Their experience with titanium indicates that the photoetching

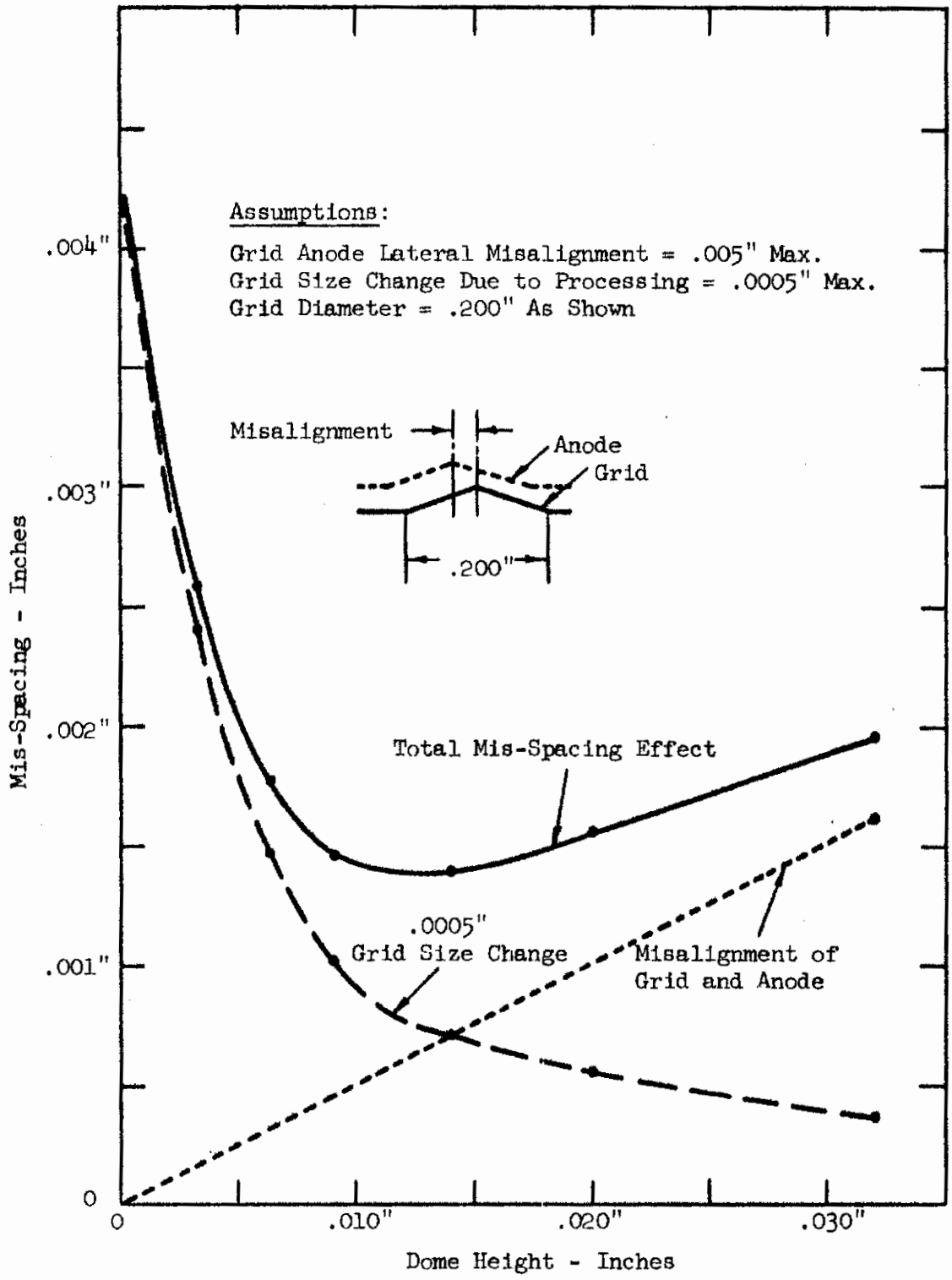



Fig. 22 Total Electrode Mis-Spacing Vs Dome Height

technique will produce more uniform and well defined openings than the discharge methods.

## TITANIUM CLAD GRID INVESTIGATION

### Titanium Coating Method

Prior to this contract, some titanium plating methods were investigated but none were found to be effective. Some preliminary vacuum coating tests were performed and found to be feasible. Diode anodes were covered with a .002" thick molybdenum disc and vacuum coated with titanium by means of the method illustrated in Figure 23. Metallurgical tests indicated that the titanium coating was over 95% pure and was almost .001" thick. These anodes were built into diodes and tested. Initial results are shown below and life test results are given in Figure 24:

| | Titanium | Titanium Coated Molybdenum |
|---|---|---|
| Average Emission | 13.5 Mu | 14.1 Mu |
| Average Contact Potential | 2.40 V | 2.38 V |

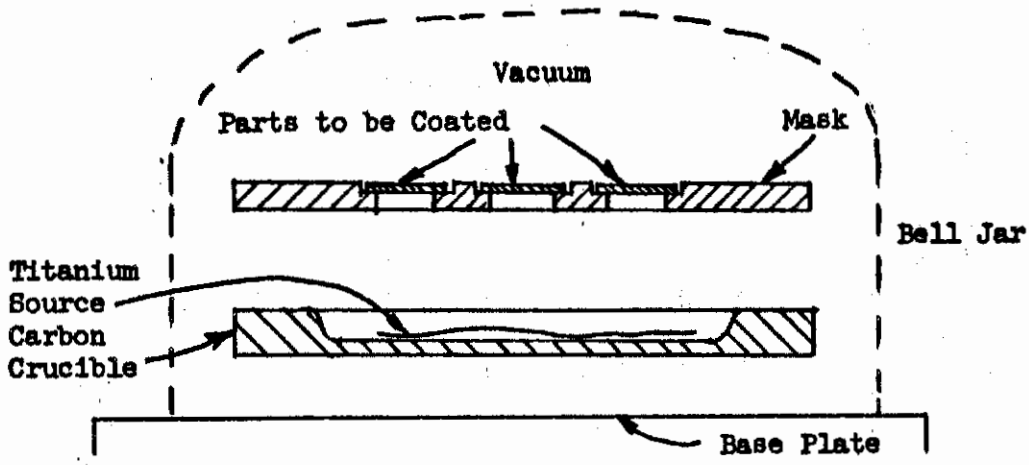
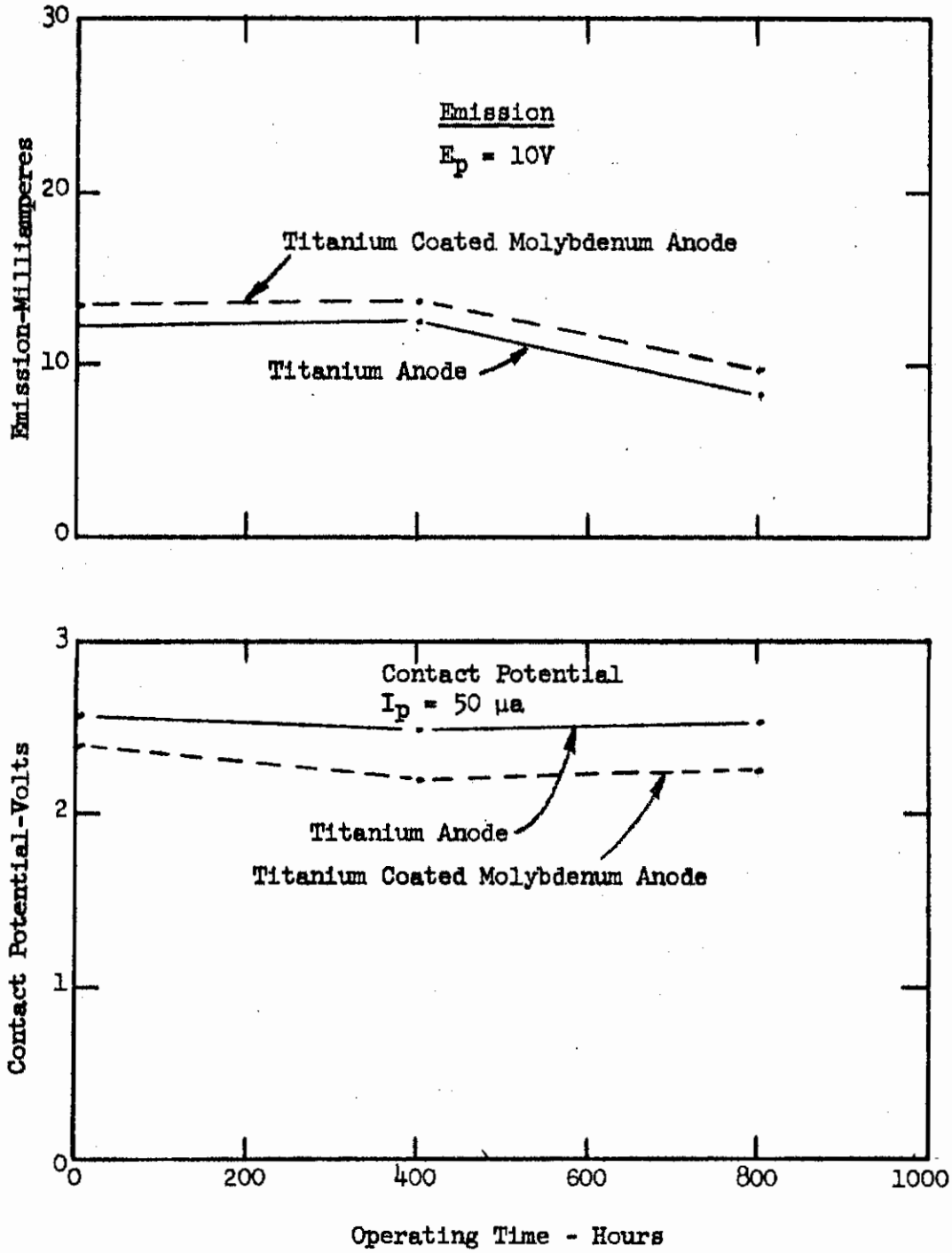



Fig. 23 Titanium Vacuum Coating Arrangement




Operating Conditions:

Temperature = 580°C
$E_b$ = 10 V, $R_L$ = 1500 Ohms
$I_k \approx$ 4 Ma

Test Conditions:

Temperature = 580°C

Fig. 24 Average Emission & Contact Potential Vs Operating Time
XD-61 Diode

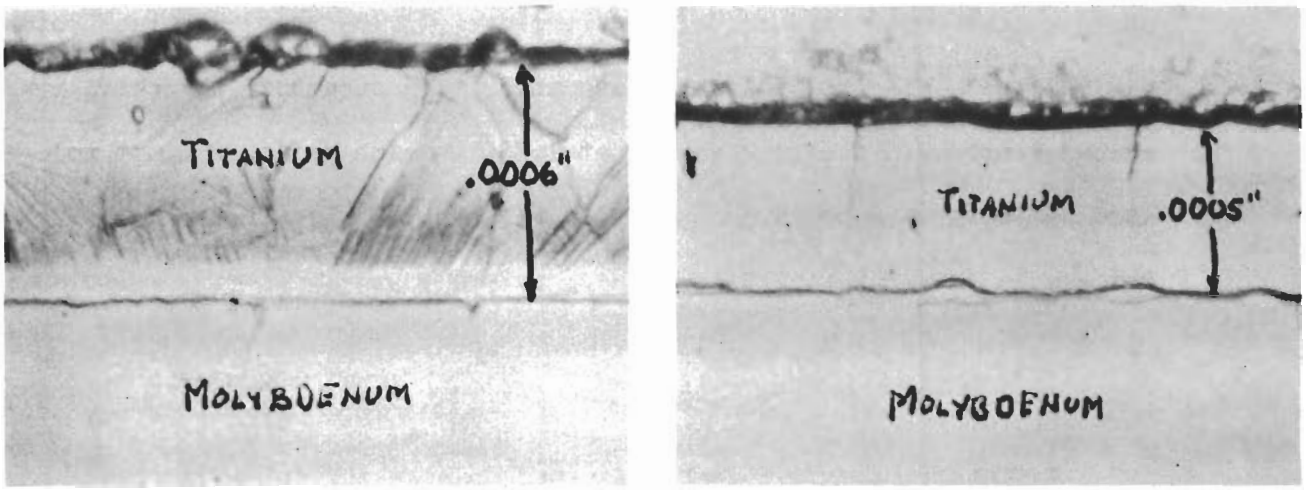
The electrical characteristics of these tubes appeared to depend, to some extent, on the temperature of the anode while being coated. Experiments in which this temperature was varied were conducted. Molybdenum strips were heated to the test temperature, then coated with titanium by evaporation. It was found that the titanium coating changed in structure quite radically when the molybdenum strip temperature was above 900°C. Above this temperature, the coating appeared to be a titanium molybdenum alloy instead of titanium. Figure 25 shows cross-sections of some of these samples.

A similar experiment was performed on titanium coated molybdenum anodes which were subsequently tested in tubes. The temperature during evaporation was varied by omitting or placing two different sized heat shields over the parts. It can be seen from the data below that the parts must be around 1,000°C while being coated for satisfactory tube characteristics:

| | Anode Temperature at Coating | | |
|---|---|---|---|
| | 80°C | 875°C | 1050°C |
| Average Emission | 12.5 Ma | 15.3 Ma | 14.2 Ma |
| Average Contact Potential | 1.37 V | 1.90 V | 2.31 V |

Titanium coating by evaporation was also applied to molybdenum grids, a cross-section of which is shown in Figure 26. Electrical results are shown below:

| | | Initial | | After $EOH_{25}$ Operation | |
|---|---|---|---|---|---|
| Tube No. | Grid Material | Contact Potential | Emission | Contact Potential | Emission |
| 191 | Ti Coated Moly | 2.0 V | 5.0 Ma | .75 V | 6.5 Ma |
| 192 | " " " | 2.3 | 6.0 | .7 | 5.0 |
| 193 | " " " | 2.25 | 5.5 | .9 | 5.0 |
| 196 | " " " | 2.45 | 4.5 | .85 | 5.5 |
| 197 | " " " | 2.48 | 4.5 | 1.1 | 5.5 |
| 198 | " " " | 2.4 | 5.5 | .85 | 5.5 |
| 195 | Bare Molybdenum | .25 | 8.0 | .2 | 3.0 |
| 200 | " " | .25 | 5.0 | .35 | 2.0 |




Coated at 650°C  Coated at 1,000°C

Fig. 25 Effect of Varying Molybdenum Temperature While Titanium Coating

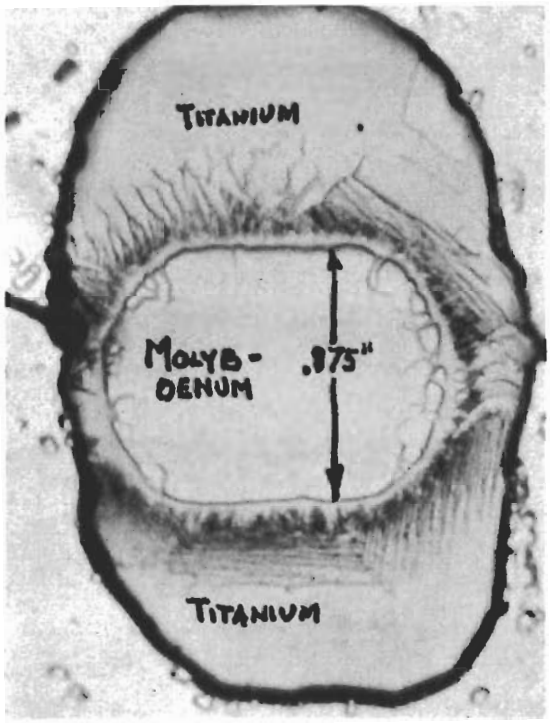



Fig. 26 Cross-Section of Titanium Coated Molybdenum Grid Wire X-1575

These data illustrate the usual drop in emission experienced with bare molybdenum grids as shown by tubes #195 and #200. The emission remained uniform in tubes with coated grids. However, grid-cathode contact potential dropped. The molybdenum anodes which were successfully coated received a hydrogen firing clean-up at 1,750°C which grids will not tolerate. It is believed that titanium coated grids are feasible if the cleaning process is improved.

Other Titanium Coating Methods

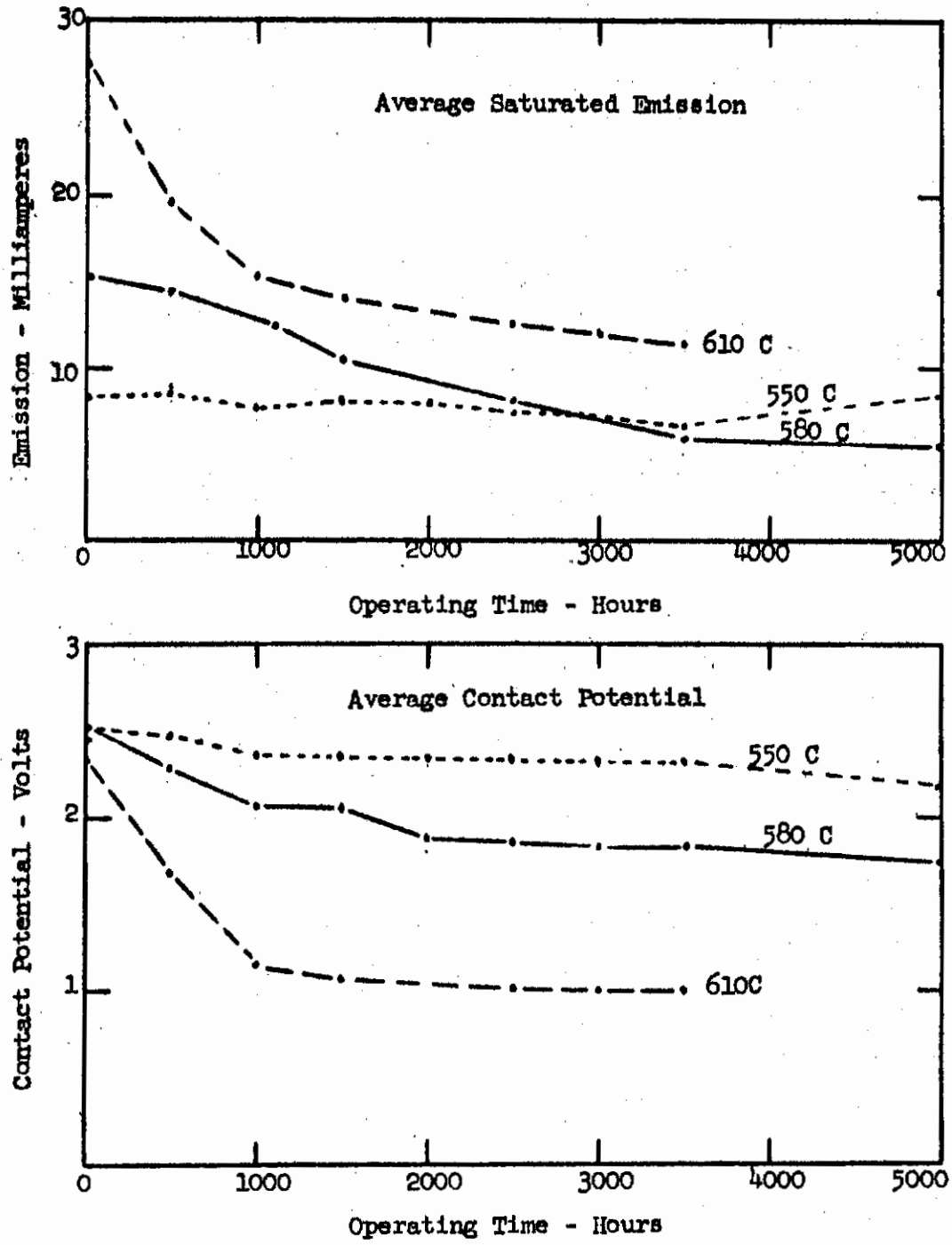
Titanium-clad molybdenum wire, .040" diameter, was previously tested for electrical characteristics and found satisfactory as a material in a TIMM tube. Efforts to draw this wire down to a size suitable for grids, however, have not yet been satisfactory.

## CATHODE REFINEMENT PROGRAM

Tube Characteristics are more stable during life if the operating temperature is reduced a few degrees. Figure 27 shows the life test results when diodes are operated at 550°C, 580°C, and 610°C.

A lower operating temperature reduces the emission level but a thicker cathode coating may raise the emission level. Tests were performed to determine the optimum coating thickness with respect to emission. Coating thickness was varied by adjusting the percent of cathode coating mix in acetone thinner. The initial test results, shown below, indicate that 25% coating operated at 560°C has characteristics of 15% coating operated at 580°C:

| Saturated Emission | | | Contact Potential | | |
|---|---|---|---|---|---|
| Cathode Coating | 560°C Test | 580°C Test | Cathode Coating | 560°C Test | 580°C Test |
| 15% | 12.3 Ma | 17.6 | 15% | 2.39 V | 2.35 V |
| 25% | 16.2 | 23.9 | 25% | 2.36 | 2.29 |
| 40% | 13.8 | 20.6 | 40% | 2.38 | 2.35 |




Operating Conditions:

Temperature = As Indicated On Curve

$E_b$ = 10 V, $R_L$ = 3300 Ohms

Test Conditions:

Temperature = As Indicated On Curve

Emission - $E_p$ = 10 V

Contact Potential - $I_p$ = 50 μa

Fig. 27 Emission & Contact Potential Vs Operating Time
Type XD-108 Diode

Repeat tests were performed with similar results, the 15% and 40% coating being lower in emission than the 25%. Life test data, Figures 28 and 29, indicate more stable characteristics at 560°C operation; however, tube characteristics may be slightly lower.

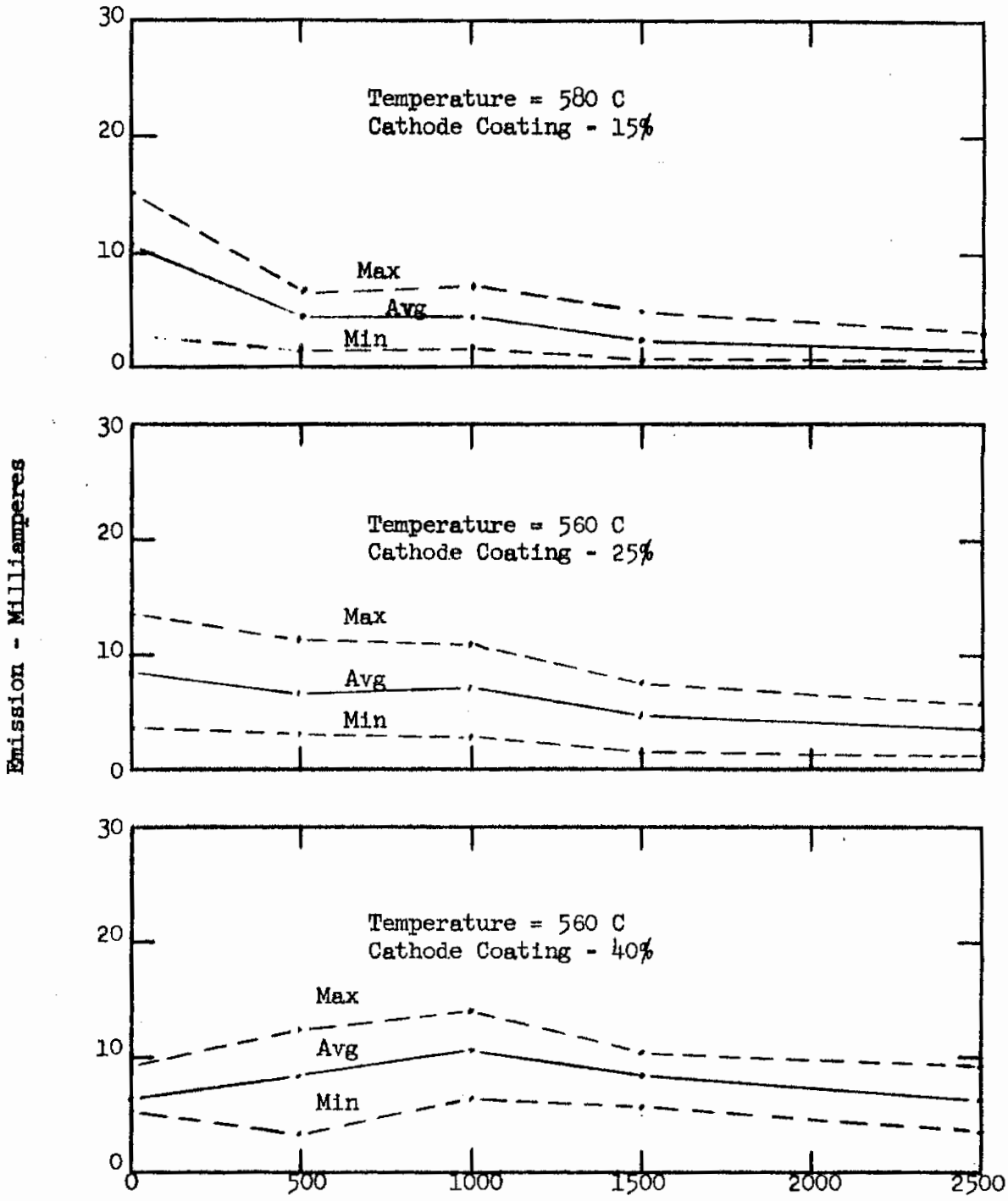
There has been some indication that emission level during life may be related to the thickness of the platinum cathode cover. Three groups of diodes having platinum cathode covers .001", .002", and .005" thick were built and life tested. Test results on these lots of tubes, Figure 30, were not significantly different. Metallurgical tests of the active portion of the cathode cover showed no trace of material migrating through from the titanium stud even on the thinnest cover .001" thick. This experiment shows that the platinum thickness may be chosen based on its mechanical properties. As a compromise between cost and ease of handling, .002" thick platinum is recommended.

The amount of nitrocellulose binder in the coating affects the coating uniformity and it was believed that it affected the emission. Two lots of diodes, one with 7 1/2% of the coating mix being binder and one with no binder, were constructed. There was only a little difference electrically between these two lots of tubes as shown below:

| | Average Emission | Average Contact Potential |
|---|---|---|
| Coating With No Binder | 6.6 Ma | 2.37 |
| Coating With 7 1/2% Binder | 8.31 | 2.37 |

A similar test comparing coating with 2% and 7.5% binders was performed on triodes with the same results and the life test data are shown in Figure 31.

Most TIMM cathodes have been coated by a printing method whereby a measured amount of coating mix is placed on the cathode and allowed to spread



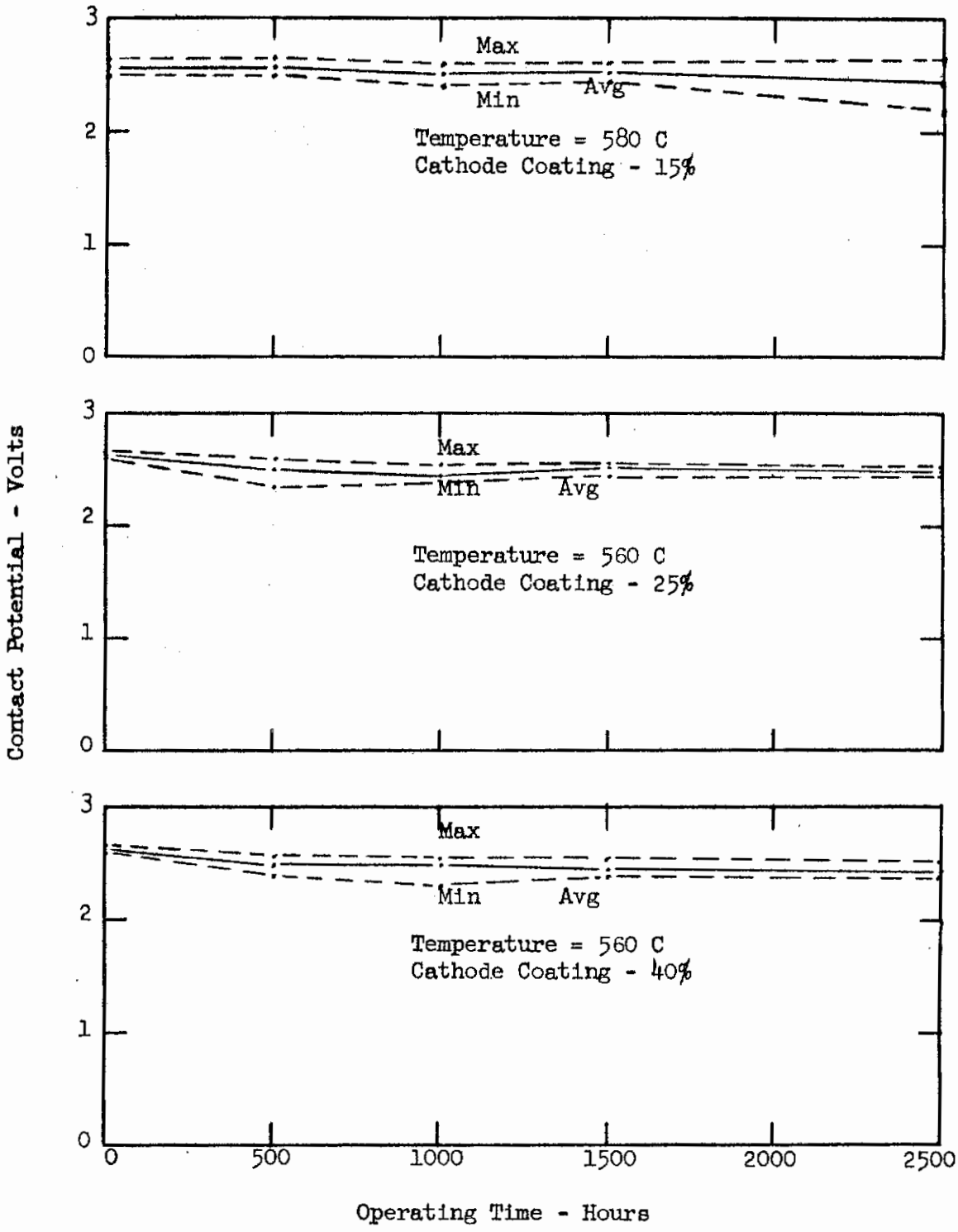

Operating Conditions:

Temperature = As Indicated
$E_b$ = 10 V, $R_L$ = 1500 Ohms
$I_k \approx$ 4 Ma

Test Conditions:

Temperature = As Indicated
$E_p$ = 10 V

Fig. 28 Average Saturated Emission Vs Operating Time
Type XD-61 Diode



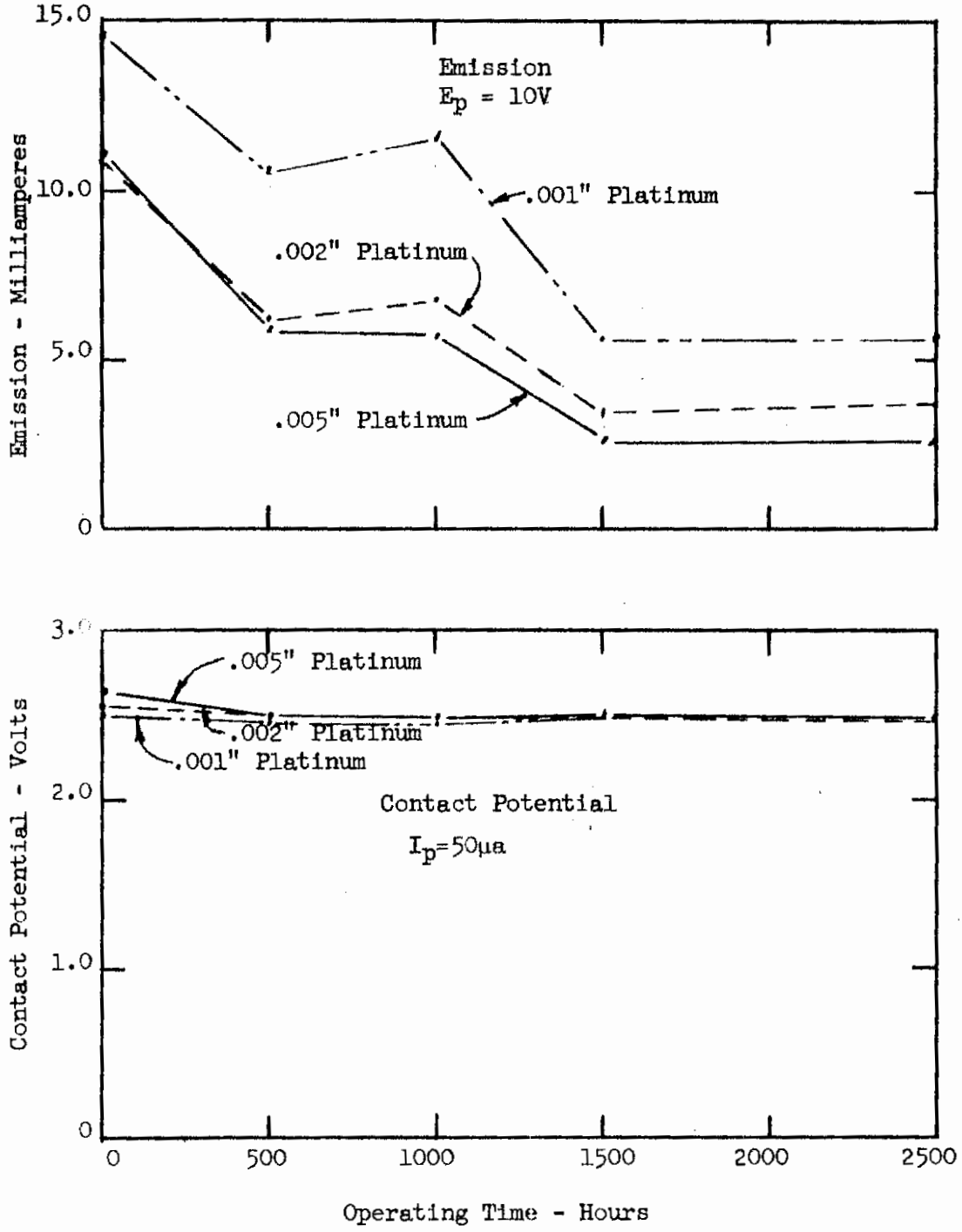

Operating Conditions:

Temperature = As Indicated
$E_b$ = 10 V, $R_L$ = 1500 Ohms
$I_k \approx$ 4 Ma

Test Conditions:

Temperature = As Indicated
$I_p$ = 50 μa

Fig. 29 Average Contact Potential Vs Operating Time
Type XD-61 Diode



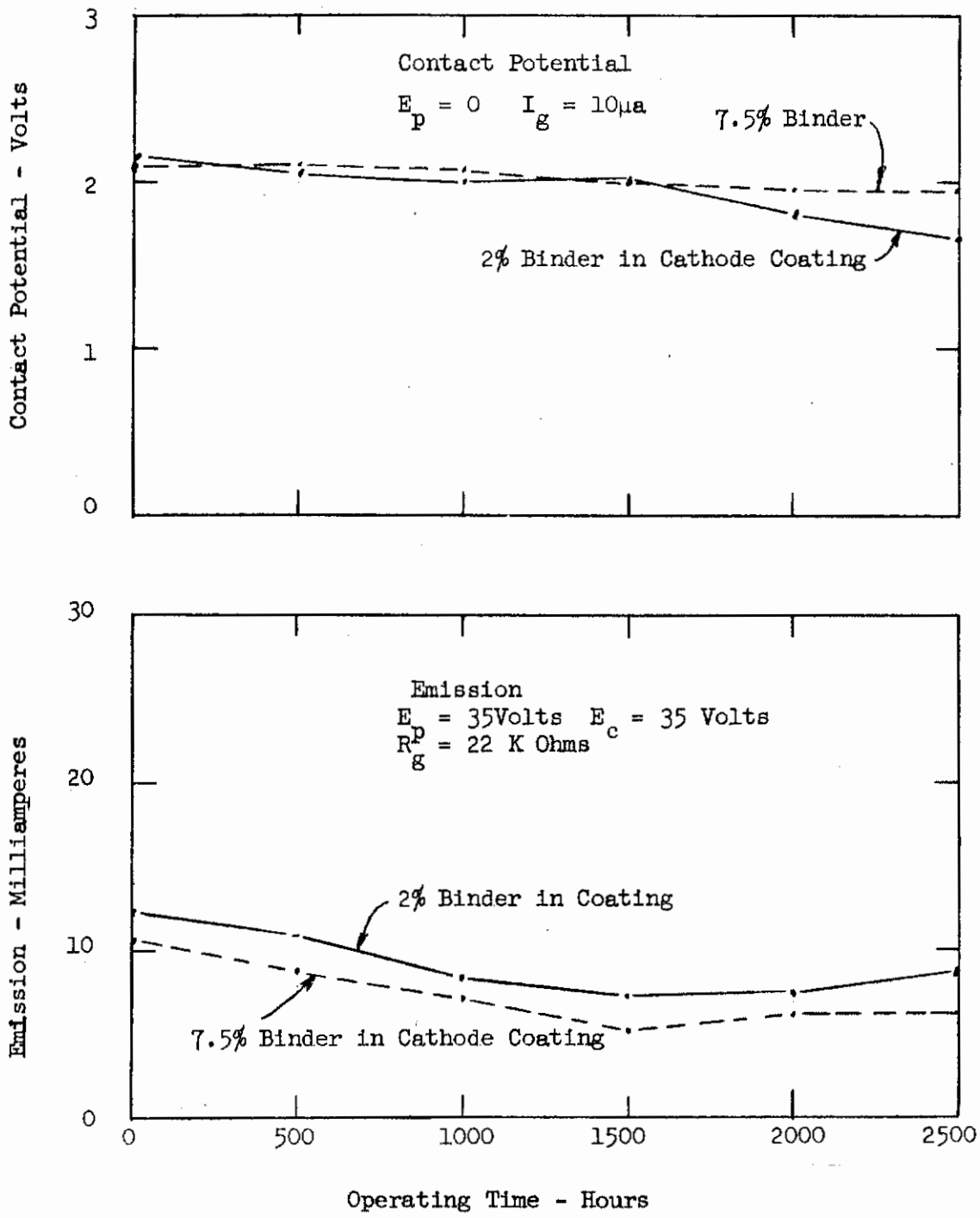

Operating Conditions:

Temperature = 580°C
$E_b$ = 15 V, $R_L$ = 1000 Ohms
$I_p \approx$ 4 Ma

Test Conditions:

Temperature = 580°C

Fig. 30 Average Emission & Contact Potential Vs Operating Time XD-108 Diode Comparing Three Platinum Cathode Thicknesses




Operating Conditions:

Temperature = 580°C
$E_b = E_c$ = 15 V, $R_L$ = 1000 Ohms
$R_g$ = 100K Ohms

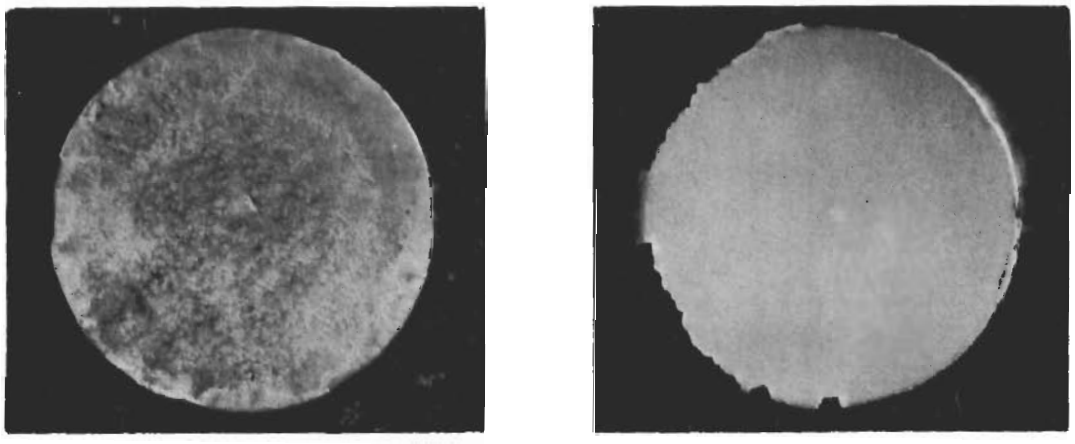
Test Conditions:

Temperature = 580°C

Fig. 31 Average Emission & Contact Potential Vs Operating Time
XD-62 Triode

and dry. Although this coating method has been successful, there are minor physical variations which may affect tube characteristics. One group of tubes was made with sprayed coating. Contact potential was reduced with no improvement in emission level. It is also difficult to prevent coating from spraying onto the titanium surface where only a very small amount will affect the tube characteristics.

A paper backing was covered with a uniform thickness of cathode coating impregnated with a special binder. When this coating is pressed against a cathode, it adheres to the cathode surface and detaches from the paper backing. This coating method if called "transfer tape method" and results in a very uniform cathode coating except for a small amount of tearing at the edge. Figure 32 shows a cathode coated with this method compared to one coated with the printing method. Electrical results have not been satisfactory as yet; the contact potential is satisfactory but the emission is very low. Neither the cathode processing to remove the binder nor the application method have been optimized, but it is believed that further efforts will result in a uniform, high emission cathode.



Printed Coating Transfer Tape Coating

Fig. 32 Appearance of Cathode Coating

## STABLE CONTACT POTENTIAL INVESTIGATION

Contact potential and, to a limited extent, emission are occasional problems. Many experiments were performed to determine the factors controlling these characteristics. These experiments are summarized:

### Grid-Cathode Spacing

During tube processing, the cathode coating gives off decomposed binder, carbon dioxide, carbon monoxide, and depending on the cathode base activity, a small amount of barium and strontium. Tubes were made with the spacing between the grid and cathode varied to see if the amount of cathode products absorbed by the grid was affected. The following data indicate that the grid-cathode contact potential and emission were not dependent upon the grid-cathode spacing:

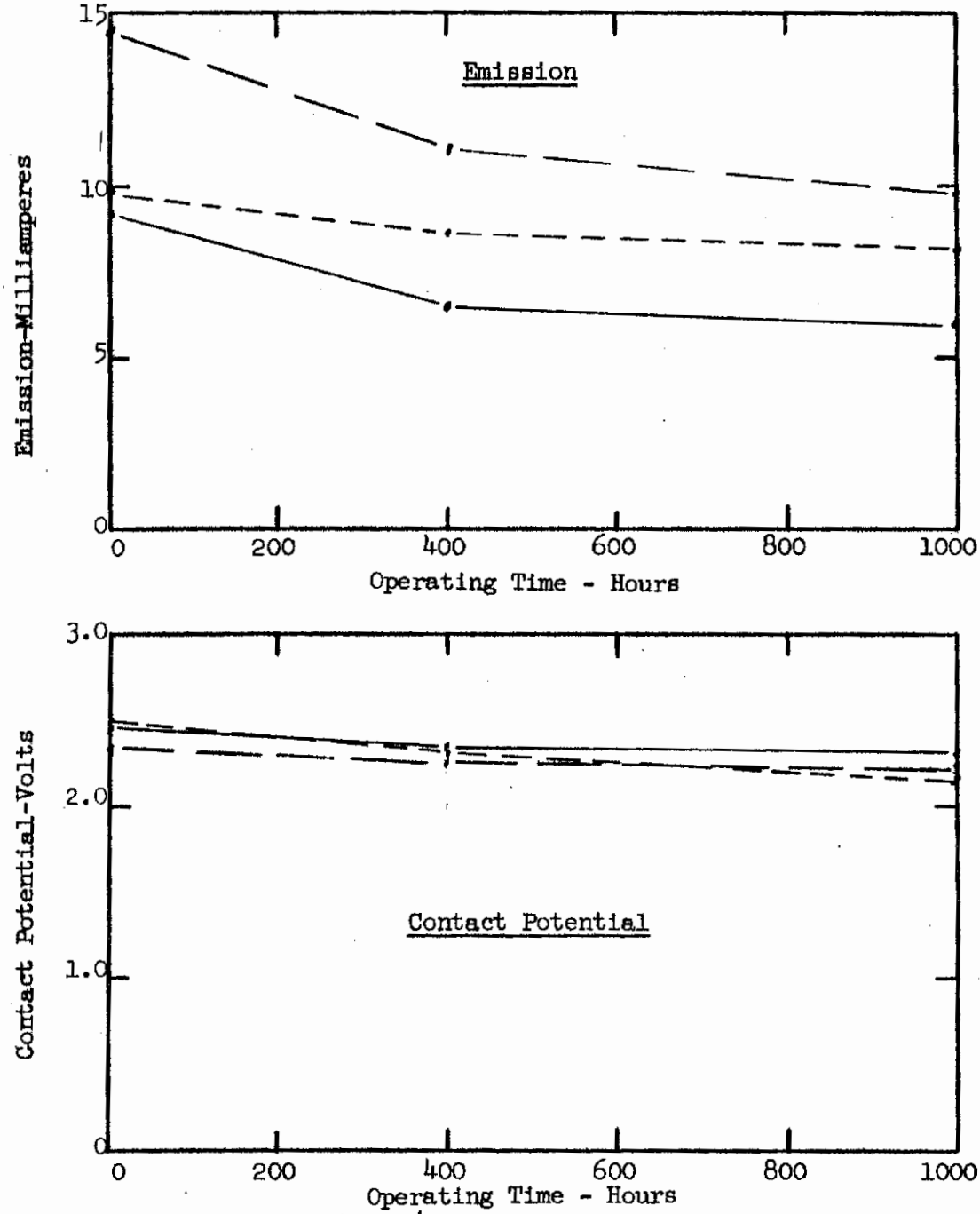
| | Grid-Cathode Spacing | | |
|---|---|---|---|
| | .001" | .0015" | .0025" |
| Lowest Contact Potential | 1.73 | 1.5 | 1.65 |
| Average Contact Potential | 2.12 | 2.12 | 2.09 |
| Highest Contact Potential | 2.42 | 2.36 | 2.32 |

### Cathode Coating Thickness

Three lots of triodes were built using three different coating amounts. These tubes were life tested at 560°C. This test data, Figure 33, indicated that heavier coating had a higher emission level but lighter coating was higher in contact potential.

### Temperature of Sealing

Triodes were sealed at several different temperatures. The test data were rather inconclusive because the higher sealing temperatures caused the grid to buckle and touch the cathode.




Cathode Coating % is Proportion by Volume of H1-1R-3 Cathode Coating Mix in Acetone

Operating Conditions:

Temperature = 560°C
$E_b = E_c = 15$ V, $R_L = 1000$ Ohms
$R_g = 100K$ Ohms

Test Conditions:

Temperature = 560°C
15% Coating* ————
20% Coating* --------
25% Coating* — — — —

Fig. 33 Average Emission & Contact Potential Vs Operating Time XD-62 Triode

Firing Temperature

Tests comparing titanium firing temperatures of 1,100°C and 1,250°C, ceramic air firing and vacuum firing indicated no significant difference in the characteristics of the final lots.

Ceramic Thickness

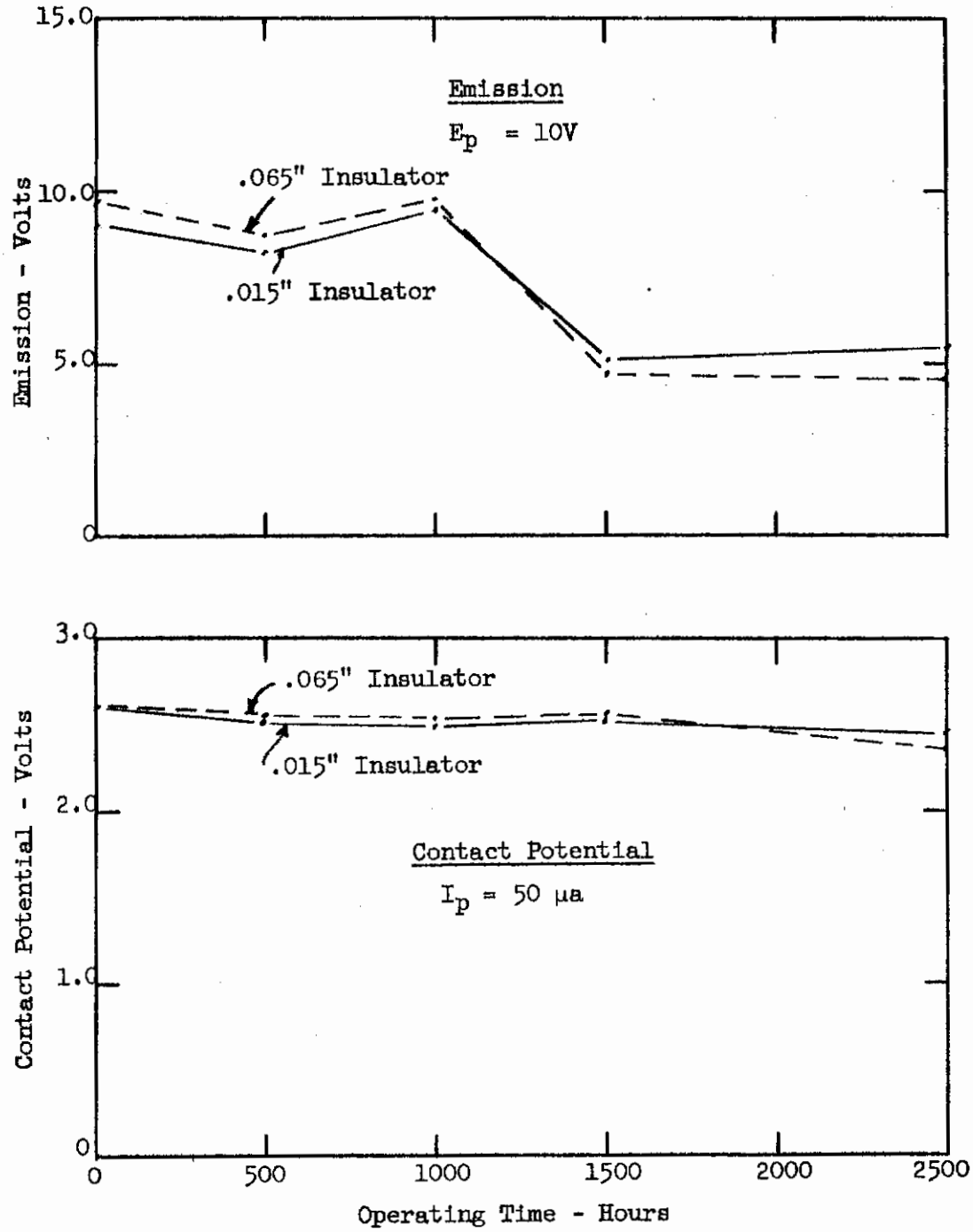
It has been noted that triodes usually had more contact potential problems than diodes. Although the grid is more prone to be contaminated than the diode anode, it was also considered that the larger internal area of the ceramic in the triode could possibly affect the tube characteristics. Three lots of diodes with the same cathode-anode spacing but with different thickness insulators were built and tested. The life test data, Figure 34, indicate that the ceramic area inside a tube has no effect on its characteristics.

Parts Analysis

A group of triode parts from which good tubes had been made were set aside as "standard" parts. Tubes were built from these parts and compared to tubes built from present parts to determine the source of contamination. Two tests from the many performed were significant. The following data indicated that one particular group of solder shims tested in diodes caused low emission:

| | Average Emission | Average Contact Potential |
|---|---|---|
| Clean Solder Shims | 18.5 Ma | 2.32 V |
| Slightly Contaminated Solder Shims | 9.8 Ma | 2.25 V |

The following data indicates that one group of anode studs tested in triodes caused low grid cathode contact potential:




Operating Conditions:

Temperature = 580°C
$E_b$ = 15 V, $R_L$ = 1500 Ohms
$I_k \approx$ 4 Ma

Test Conditions:

Temperature = 580°C

Fig. 34 Average Emission & Contact Potential Vs Operating Time XD-61 Diode Comparing Two Different Insulator Lengths

| Standard Triode Parts | | Contaminated Anode Stud | |
|---|---|---|---|
| Grid Contact Potential | Emission | Grid Contact Potential | Emission |
| 2.48 V | 15.0 Ma | 1.92 V | 1.5 Ma |
| 2.06 | 9.5 | 1.50 | 15.0 |
| 2.30 | 15.0 | 1.45 | 13.5 |
| 1.75 | 12.5 | 1.15 | 8.5 |
| 2.38 | 12.0 | | |
| Avg. 2.17 | 12.8 | 1.5 | 12.1 |

Metallurgical analysis on the solder rings causing low emission was performed but no trace of any unusual materials was found. This test is significant in that it illustrates that solder ring contamination below detectable levels may affect tube characteristics.

Analysis of the surface of these studs indicated traces of aluminum, lead and copper. Lack of time has prevented the tracing of the source of contamination and a positive method of eliminating it.

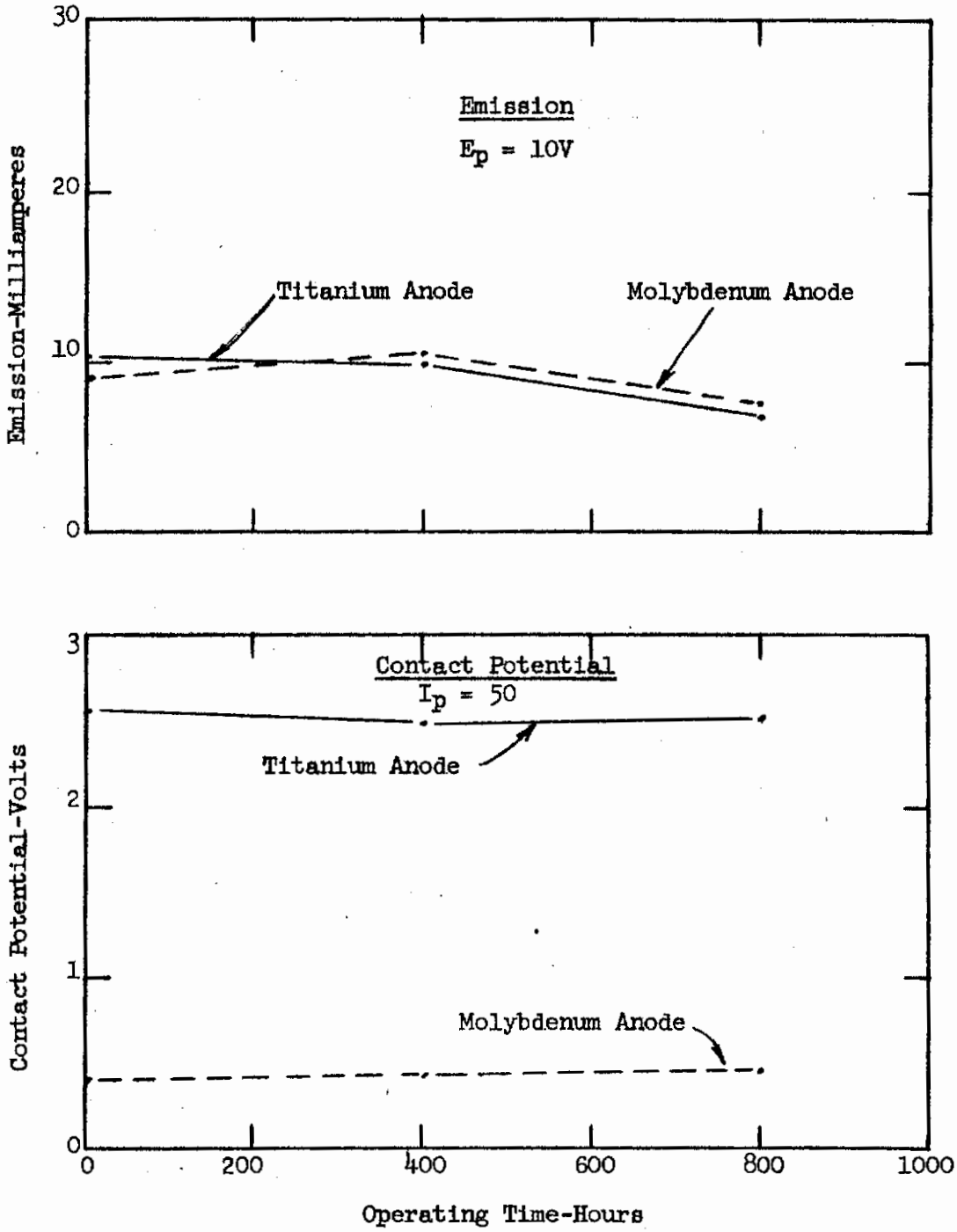
ZERO CONTACT POTENTIAL

Reducing the triode anode contact potential to zero has the same effect as raising the plate voltage by approximately 2 volts. This would be a significant advantage for low voltage operation.

Two anode materials have been tested for contact potential, tungsten and molybdenum. Both materials will reduce the anode contact potential to essentially zero after a few hours operation.

Tests have indicated that these materials must be extremely clean if emission deterioration is to be avoided during life. Data indicate that the anodes cleaned with present schedules are satisfactory for operation below 10 volts, but when operated around 40 volts, emission slumps rapidly.

Figure 35 shows the diode life test data comparing zero contact potential diodes with molybdenum anodes with conventional titanium anode diodes.




Operating Conditions:

Temperature = 580°C
$E_b$ = 10 V, $R_L$ = 1500 Ohms
$I_k \approx$ 4 Ma

Test Conditions:

Temperature = 580°C

Fig. 35 Average Emission & Contact Potential Vs Operating Time
XD-61 Diode

Figure 36 compares a conventional and a tungsten anode triode illustrating the advantage for low voltage operation. Figure 37 shows life test data on titanium, molybdenum, and tungsten anode triodes.

TUBES FOR CIRCUIT MODULES

A number of tube types was designed and built for circuit use. These tubes are summarized in Figure 38.

## CAPACITOR DEVELOPMENT

Capacitor development work was divided into three main efforts:

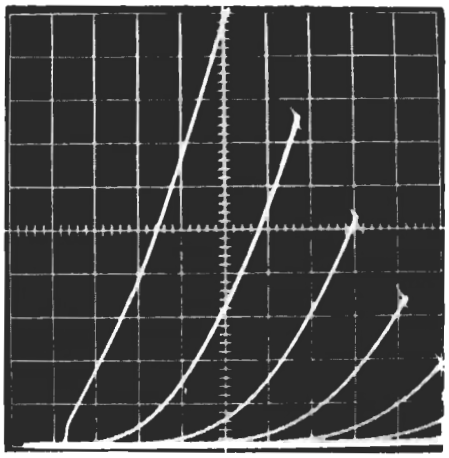
(1) Investigation of improved dielectrics and the elimination of polarization caused by ionic conduction.

(2) Development of a procedure to remove surface electrical leakage paths across the capacitor dielectric.

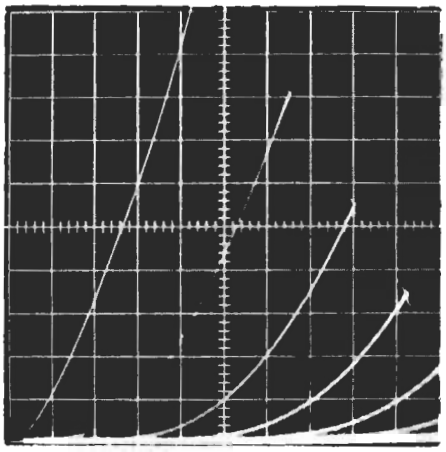
(3) Improvement of capacitor designs.

DIELECTRIC MATERIALS

The dielectric in use at the beginning of the contract period has our designation, OW-102. OW-102, a forsterite ceramic, was found to contain internal voids due to the ceramic processing and for this reason, OW-137, another forsterite ceramic in which such voids are minimized, was developed. The electrical characteristics of these two materials at 580°C are quite similar. A problem inherent in each of these two dielectric materials which make them undesirable in some capacitor applications is the presence of ionic conduction, presumably through a glassy phase, which causes an apparent electrolytic polarization of the capacitor. The results of our attempt to make a suitable "glass-free" dielectric material was a magnesia-spinel ceramic designated OW-133.



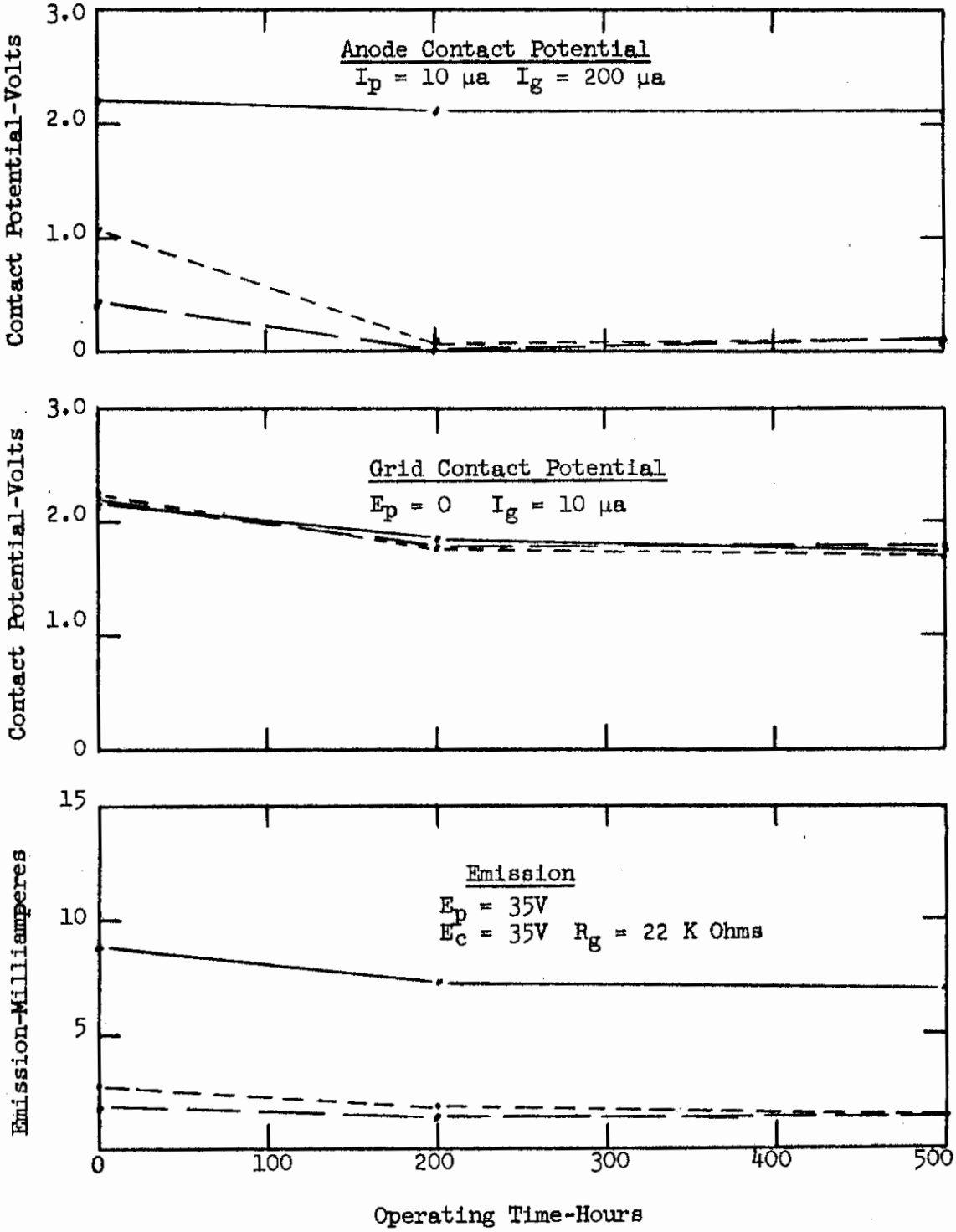
Titanium Anode
Tube #325



Tungsten Anode
Tube #332

Vertical Scale - Plate Current - 2 Milliamperes Full Scale
Horizontal Scale - Plate Voltage - 20 Volts Full Scale
Grid Step - 1/2 Volt Per Step - Top Line +2.5V $E_g$

Fig. 36 Comparison of Typical Plate Families of Triodes With Titanium and Tungsten Anodes




Operating Conditions:

Temperature = 580°C
$E_b$ = 40 V, $R_L$ = 1000 Ohms
$E_c$ = 0, $R_g$ = 100K Ohms

Test Conditions:

Temperature = 580°C
Titanium Anode ——————
Molybdenum Anode ----------
Tungsten Anode — — — —

Fig. 37 Contact Potential & Emission Vs Operating Time
XD-62 Triode - 3 Anode Materials

Diodes

Vertical Scale:
Plate Current-20 Ma Full Scale

Horizontal Scale:
Plate Voltage-20V Full Scale

Left Curve - Single Diode
Center Curve - Dual Series Diode
Right Curve - Triple Series Anode



High Perveance Triode

Vertical Scale:
Plate Current-2 Ma Full Scale

Horizontal Scale:
Plate Voltage-10V Full Scale

Grid Step:
1/2 Volt Per Step
Top Line = 2.5 Volts



High Mu Triode

Vertical Scale:
Plate Current-5 Ma Full Scale

Horizontal Scale:
Plate Voltage-100V Full Scale

Grid Step:
1/2 Volt Per Step
Top Line = 2.5 Volts

Fig. 38 Representative Characteristic Curves of Tubes Built for Circuit Modules

The original development work on OW-133 was done by J. P. Leschen of the General Electric Research Laboratory under Air Force contract No. AF 19(604)-5472. The object of the work was to develop a silica-free, titanium-matching ceramic and resulted in the issuance of patent No. 3,113, 846, entitled "Titanium Matching Composite Bodies."

Additional development work was performed under contract AF 33(657)-11400 to simplify the forming and firing procedure. This work was undertaken to provide a dry-pressing technique using 10,000 - 15,000 psi forming pressure rather than isostatic forming at high pressures or the hot pressing technique used in the original work. A second goal was to reduce the firing temperature of 1700°C or above used in the original work.

Two compositions were developed which can consistently be fired vacuum tight at a temperature of 1400°C using conventional "dry-press" forming methods. The raw material and nominal oxide compositions of these two bodies are essentially the same except that one (OW-133K) has a small amount of CaO added as a mineralizer. The compositions are as shown below:

| OW-133 Oxide | OW-133K Oxide |
|---|---|
| $Al_2O_3$ - 40.0 | $Al_2O_3$ - 39.8% |
| MgO - 60.0 | MgO - 59.6% |
| | CaO - 0.6% |

Processing steps are as follows:

(1) Weigh out materials into rubber lined mill containing approximately 50% by volume of alumina grinding media.

(2) Add necessary amount of distilled water for proper milling consistency.

(3) Mill 16 hours.

(4) Remove water by filtration using Buechner funnel.

(5) Dry.

(6) Calcine in air at 1150°C for one hour.

(7) Pulverize.

(8) Add 6% by weight of an aqueous solution contining water soluble wax.

(9) Granulate.

(10) Form into desired shape.

(11) Mature in air at 1400°C for two hours.

(12) Grind.*

(13) Clean.

(14) Air fire at 1150°C for one hour.

The following is a comparison of the known physical and electrical properties of OW-133 with those of OW-102 and OW-137:

Physical and Electrical Properties
of OW-133, OW-102 and OW-137

| Property | OW-133 & OW-133K | OW-102 | OW-137 |
|---|---|---|---|
| Density (gms/cc) | 3.55 | 3.10 | 3.10 |
| Transverse Strength (psi) | 20,000-25,000 | 18,000-22,000 | 18,000-22,000 |
| Porosity (Helium Mass Spectrometer) | Vacuum Tight | Vacuum Tight | Vacuum Tight |
| Color | White | Off White | Off White |
| Thermal Coefficient of Expansion (cm/cm/°C) 25° - 1,000°C | $10.3 \times 10^{-6}$ | $10.5 \times 10^{-6}$ | $10.5 \times 10^{-6}$ |
| Dielectric Constant (1 Mc): | | | |
| At 25°C | 9.7 | 7.4 | 7.4 |
| At 600°C | 10.5 | 8.1 | 8.2 |
| Loss Tangent (1 Mc)** | | | |
| At 25°C | < .0005 | < .0007 | < .0007 |
| At 600°C | .0033 | .0095 | .029 |
| Volume Resistivity(Ohm cm)*** | | | |
| At 25°C | $> 10^{14}$ | $> 10^{14}$ | $> 10^{14}$ |
| At 600°C | $10^{9}$ | $10^{8}$ | $10^{8}$ |

* See Following Page
** " " "
*** " " "

The electrical characteristics are reported above. It is important to note the improvement in dielectric constant, dissipation factor (Tan $\delta$), and bulk resistivity over the forsterite ceramics. Because of this extremely high value of resistivity, our test equipment was inadequate to observe electrolytic polarization phenomena, if any, present in this material. It can be said, however, that if polarization does exist in OW-133 and OW-133K, that it is much less than in the forsterite ceramics, OW-102 and OW-137.

Life tests on 20 TIMM capacitors with OW-133K dielectrics have progressed to 500 hours. These units are being operated with a 15 KC, 20 volt squarewave load applied. These results are shown in the appendix.

In addition to the development work outlined above, all of the capacitor needs of the contract for circuits, radiation studies, external (University of Dayton) evaluation and life tests were made using both stacked plate and mica roll techniques. Evaluation of life test data is presented in the appendix of this report.

DEVELOPMENT OF IMPROVED VACUUM INSULATION OF CAPACITOR DIELECTRIC

Early in the contract period, it was found during circuit tests at the General Electric Ordnance Department, that leakage paths developed

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* For thicknesses less than .015", a lapping technique is used to remove material. A Blanchard grinder with a diamond grinding disc is used for thicknesses over .015".

** Dielectric constant and loss factor (Tan $\delta$) were measured at 1 Mc using guarded ring techniques as described in ASTM D150-59T. The measuring equipment used was a Wayne-Kerr Radiofrequency Bridge, General Radio Type 1330-A Bridge Oscillator, and a Hewlett-Packard Model 400C V.T.V.M.

*** Bulk resistivity was measured using a four point technique. Voltage was supplied from a 300 volt battery, current and voltage were measured with a Keithly Model 410 micro-micrometer and a John Fluke Model 825A differential voltmeter, respectively.

across the capacitor dielectric when the capacitor was tested in vacuum environments at 580°C.

A series of 16 life tests was run at 580°C under various conditions to confirm these findings and to determine the cause of degradation. From these tests it has been concluded that the leakage is a surface rather than a bulk phenomenon and is caused by handling. It was also found that leakage paths were formed at 580°C on a clean capacitor by thermal breakdown of backstreaming oil vapors from an oil diffusion pump vacuum system. This fact was confirmed by testing clean (unhandled) capacitors in an ion pump system at 580°C and noting that not a single failure was observed due to surface leakage (Figure 39). It was found that an oil diffusion pump system could be used, however, if the capacitors under test were placed in a ceramic tube sealed off with a ceramic fiber insulation. This method proved quite satisfactory during a test run out to 300 hours.

Once the cause of surface leakage was defined, efforts were shifted toward finding a method of removing any surface film before testing. The tests below were all made in an oil diffusion pump vacuum system with the capacitors shielded from backstreaming oil vapors by a ceramic tube. The tests were run at 580°C for comparatively short times (96 hours), but it is felt that 96 hours is sufficiently long to give a good first approximation to the effectiveness of the cleaning procedure being tested. A clean capacitor will have a leakage resistance versus time curve similar to "A", Figure 39. Note the resistance climb due to polarization. If a capacitor under test did not show this climb due to polarization, it was assumed that the climb was offset by surface leakage and, therefore, when the polarization would reach a steady state value, the surface leakage would cause the capacitor to fail. It is for this reason that Curve "B", Figure 40, is considered a failure.

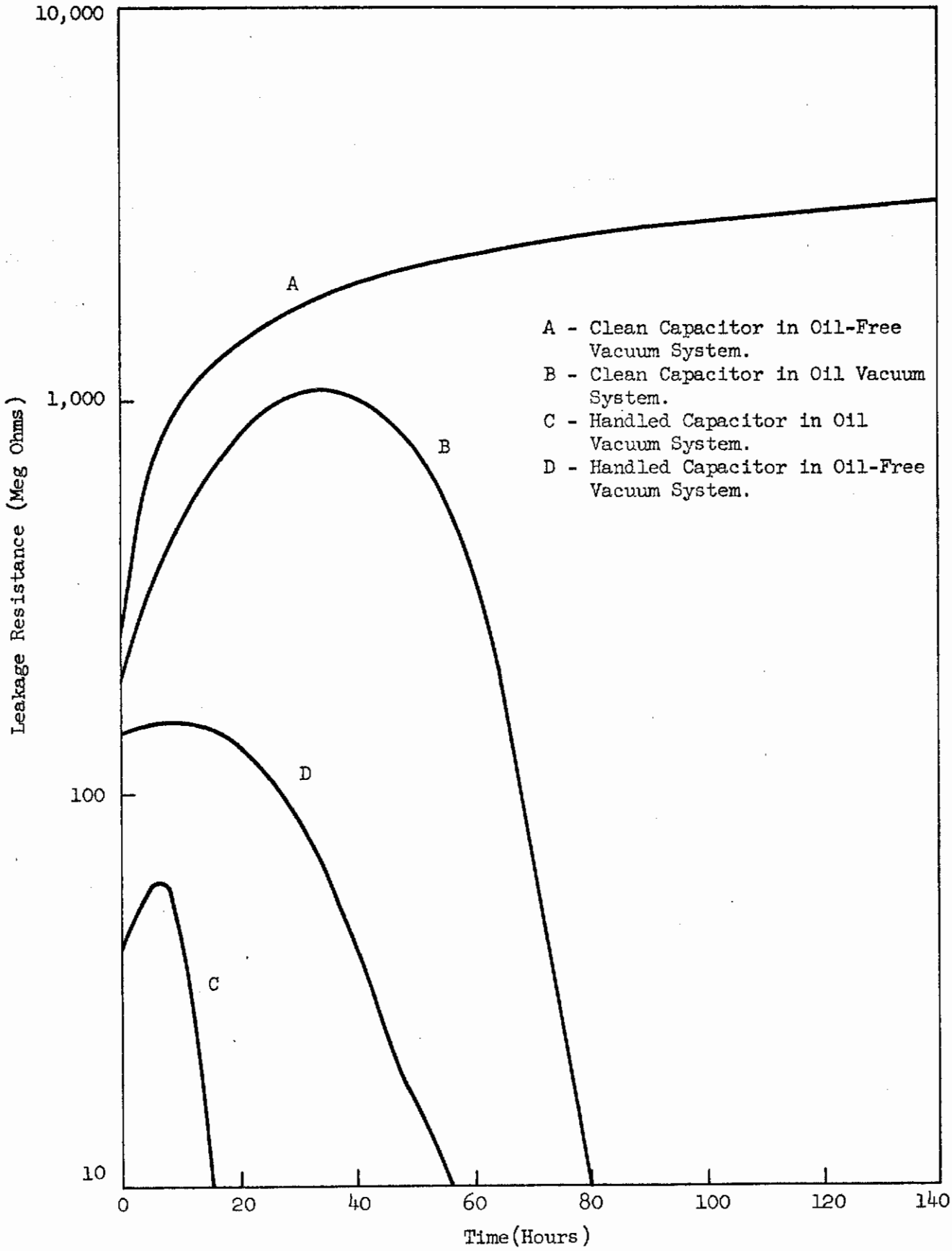



Fig. 39 TIMM Capacitor Leakage Resistance Versus Time Showing Oil Back-Streaming Effects

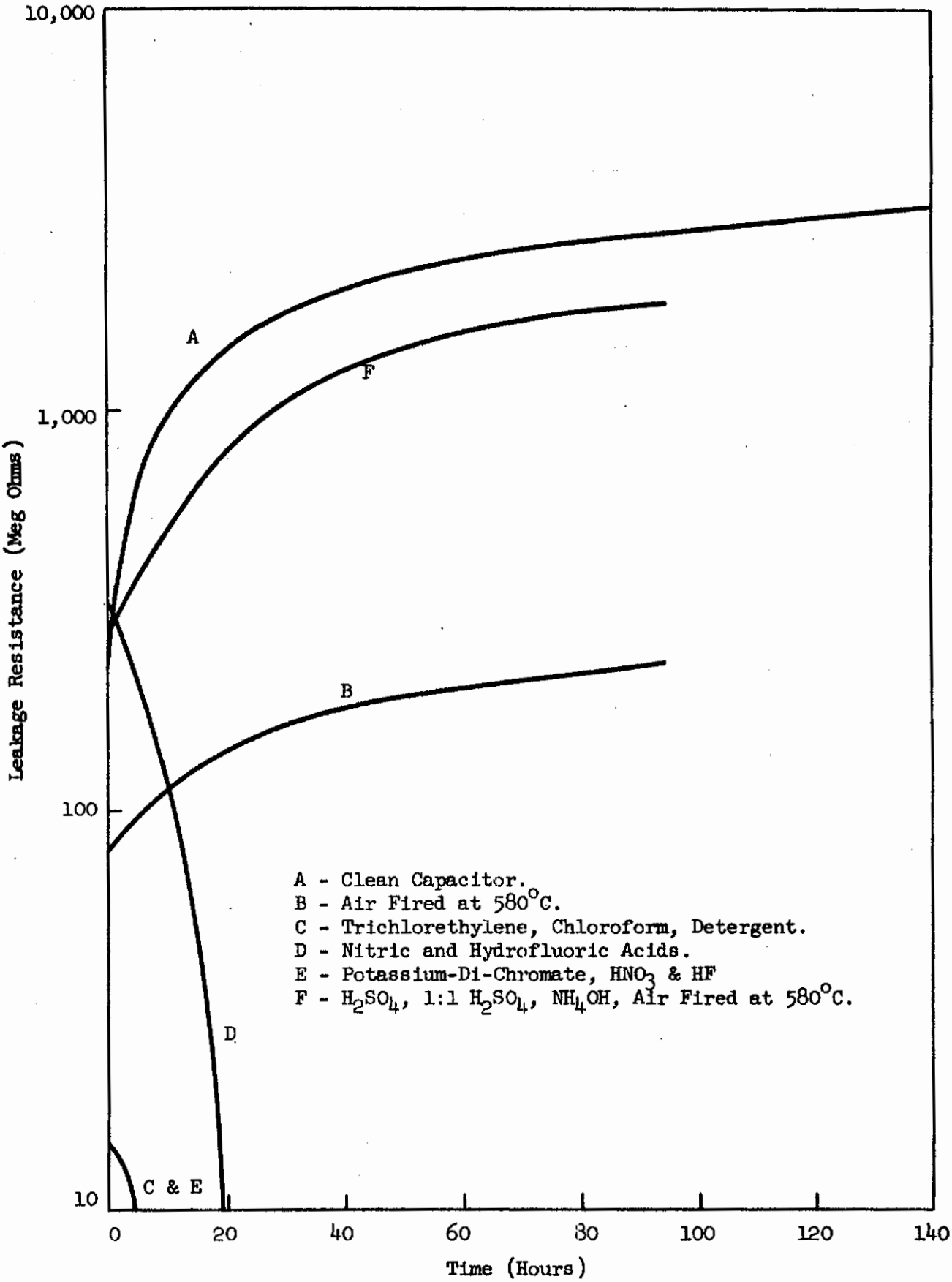



Fig. 40 TIMM Capacitor Leakage Resistance Versus Time for Various Cleaning Schedules

A series of cleaning procedures was performed on capacitor modules which had been purposely "dirtied" by handling with bare fingers. A number of cleaning procedures was found to be unsuccessful including air firing at 580°C; bathes in trichloroethylene, chloroform, and detergent; nitric and hydrofluoric acids; and potassium-Di-chromate nitric and hydrofluoric acids. A cleaning procedure which did prove successful is as follows: Dip in hot (100°C) conc. $H_2SO_4$ for two minutes, dip in hot 1:1 $H_2SO_4$, rinse in hot distilled $H_2O$, hot conc. $NH_4OH$ for two minutes, rinse, repeat each of the above for one minute, and then air fire at 580°C for at least one hour. The 1:1 $H_2SO_4$ dip was added to the procedure to act as a buffer between the conc. $H_2SO_4$ and distilled $H_2O$ to reduce thermal shock due to reaction.

The above results are graphically illustrated in Figure 40. Optical examination of a cross-section of a metal-ceramic seal subjected to the above procedure indicated no adverse effects to the seal area.

METALLIZED CERAMIC STACKED CAPACITOR

Very late in the contract period, a technique for making stacked capacitors with sprayed electrodes was developed. This method of making capacitors was reported earlier (Technical documentary report No. ASD-TDR-62-1039, December, 1962, Page 21, prepared under contract AF 33(616)-8096). However, the development of nickel-clad titanium powder made the fabrication more feasible.

The basic principle used in the design is schematically represented in Figure 41. The work done to date has been with ceramics slightly larger than the "standard" TIMM diameter of 0.323" because they were readily available. Figure 42 shows the dimensions of ceramic dielectric and the mask. Figure 43 is a photograph showing the size reduction that is possible using sprayed electrode techniques. Both capacitors have a capacitance of about 335 pf.

It was found necessary to place a 0.010" diameter nickel-clad titanium preform around the interconnecting pins to insure good electrical contact to the sprayed electrodes.

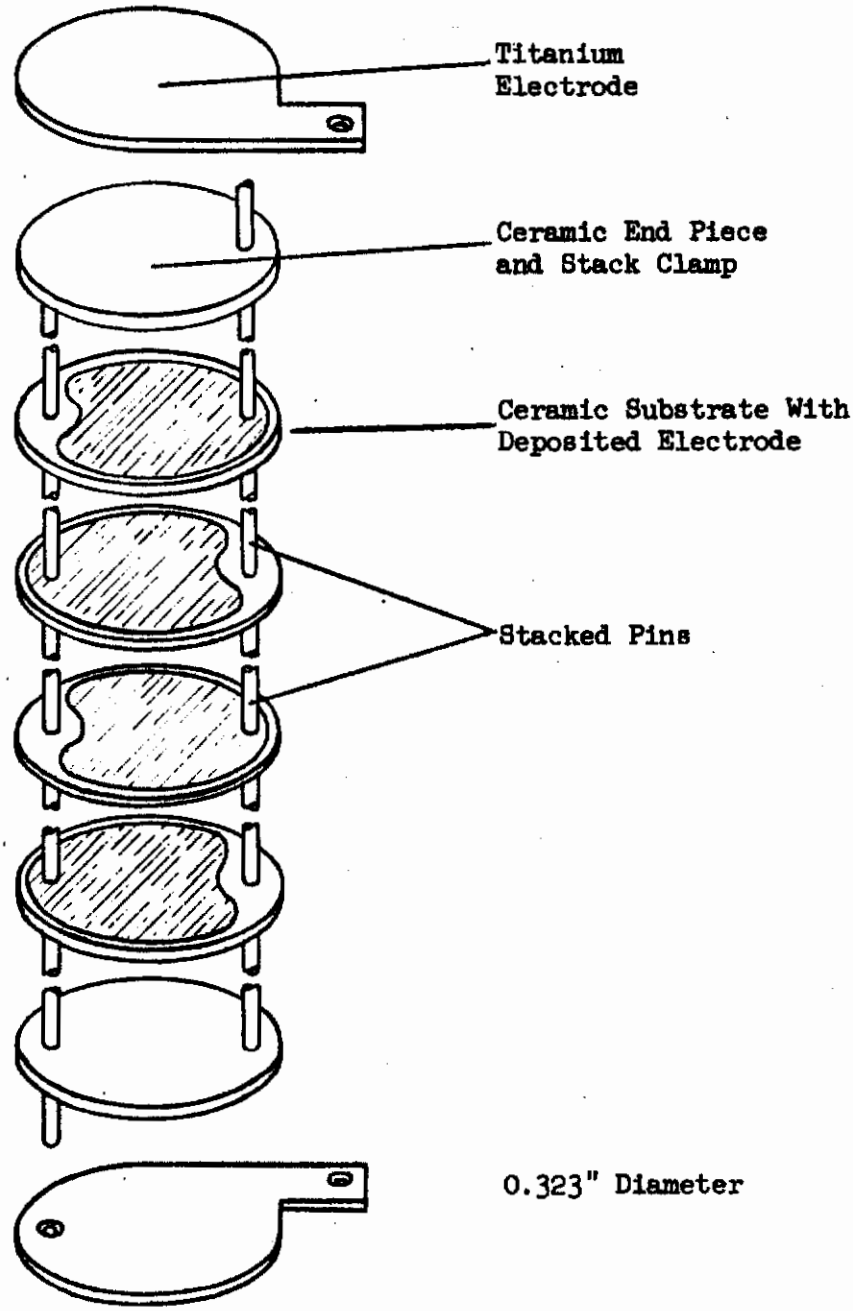



Fig. 41 TIMM Stack Capacitor-Proposed Design

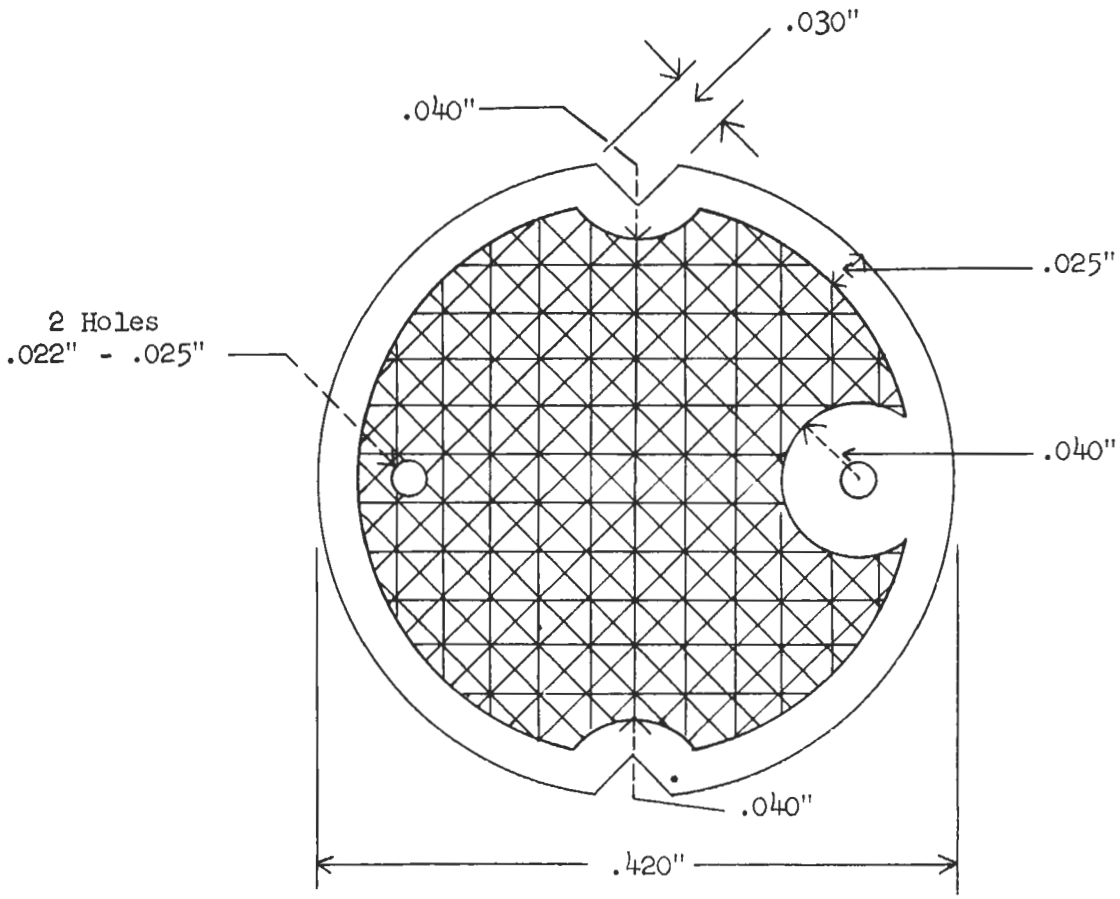



Fig. 42 Ceramic Dielectric and Mask

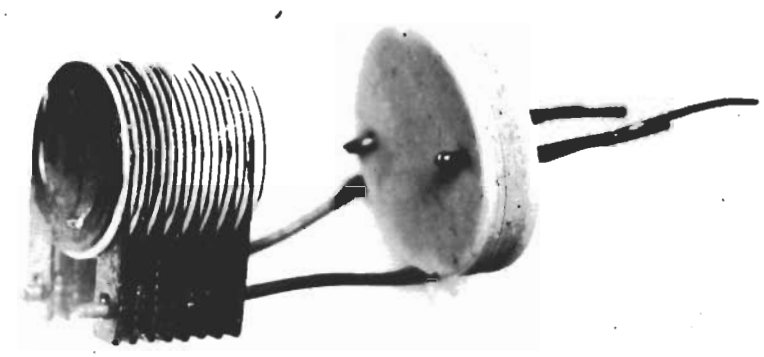


Fig. 43 Comparison Between Sprayed Electrode Capacitor and Conventional Stacked Ceramic Capacitor

Capacitors with values from 52 pf to 880 pf have been made and tested at 580°C in air. Dissipation factors (Tan δ ) have ranged between 0.00475 and 0.076. Capacitors have been subjected to 300 VDC with no adverse effects. D.C. resistance of a 335 pf unit (10 - 0.005" dielectrics) was measured at 580°C and found to be 22 megohms. No life test data is available at this time.

It should be stressed that this method of making capacitors is in the development stage and further work will be necessary before this type of capacitor can be adopted for use in TIMM circuits.

## RESISTOR DEVELOPMENT

To answer the need for high ohmic value TIMM resistors, a study was planned early in the contract to explore the effects of path length, width, thickness and spacing on resistance. By agreement with the project monitor, this work was deferred in favor of other programs.

## MODULE ASSEMBLY, INTERCONNECTION AND MOUNTING TECHNIQUES

### MODULE INTERCONNECT BRAZING

The Al:Cu:Ti brazing technique reported on contract AF 33(616)-8096 was found unsuitable due to deterioration of the metal powder composite on shelf life. An improved method was developed using a resistant braze technique.

Stainless steel wire, type 430, was plated with 0.0015" Ni and fired in a hydrogen atmosphere for five minutes at 800°C. This wire was placed into the holes of the titanium electrodes of the stacked module and crimped tight to the wire as shown in Figure 44. After this crimping operation the weld is made.

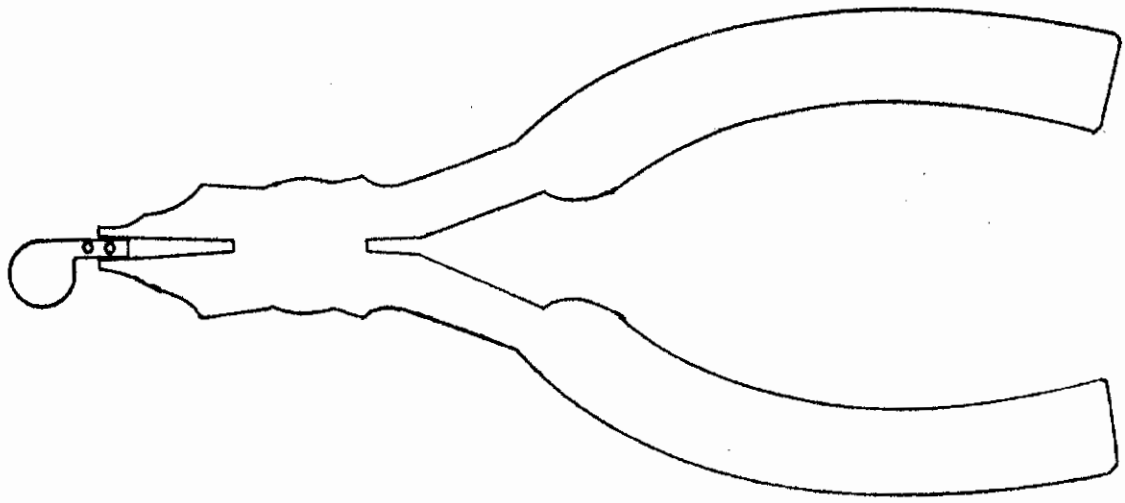


Fig. 44 Crimping Tool

The welder was equipped with specially shaped welding electrodes and electrode holders. The electrode holder directs a flow of inert gas, (Argon was used) into the weld area. Two additional jets of inert gas were used to enhance the inert atmosphere and prevent oxidation of the joint. To make reliable welds, the titanium tab should not be less than 0.015" thick. Figure 45 shows diagramatically the position of the welding electrodes prior to making the weld.

The general shape of the titanium electrode after weld is made is shown in Figure 46.

All circuits made under the contract except the diode matrix circuits have interconnects made as described herein. The diode matrix had been completed when this technique was developed.

METALLIZED INTERCONNECTS

The module boards required to satisfy the contract were made using techniques developed under Air Force contract AF 33(616)-8096. The module board

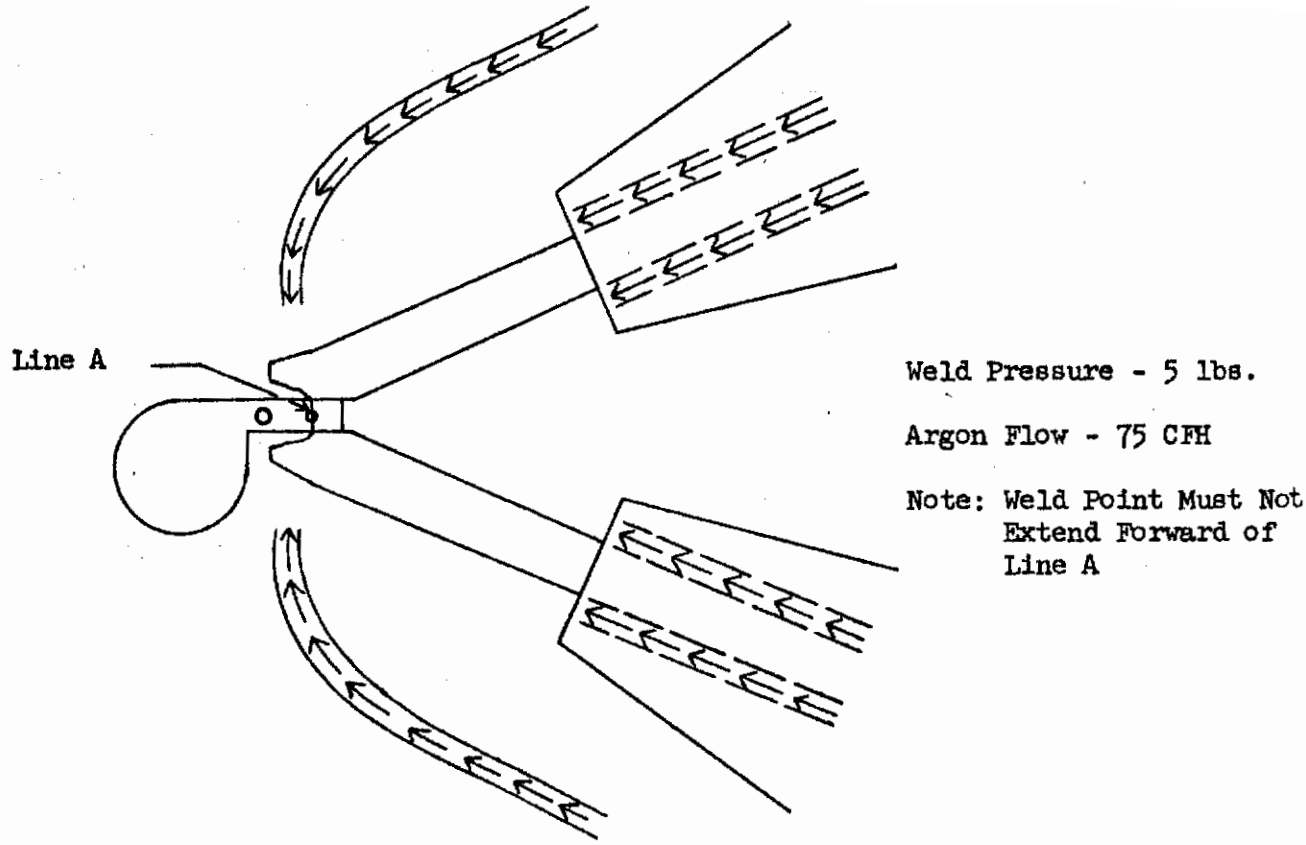



Fig. 45 Position of Points Prior to Making Weld

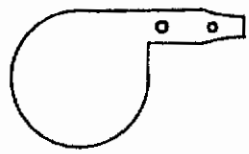


Fig. 46 Shape of Electrode After Making Weld

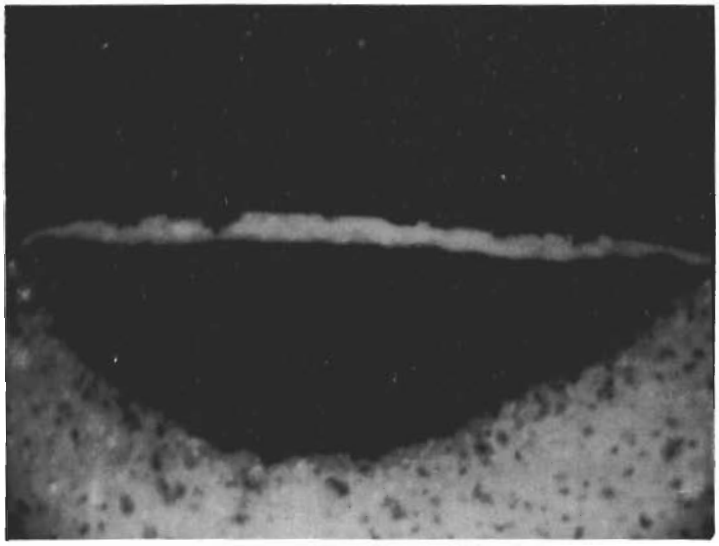
interconnect development did not materialize early enough to incorporate the new process for laying down metallized runs onto the module board. The long delivery period to obtain composite powders, necessitated the use of the tested and tried procedure for contract hardware.

Life tests on boards made under Air Force contract AF 33(616)-8096 after 10,200 hours at 580°C in air show that the oxidation of the metallized runs was insignificant compared to the bulk of the metallizing and that there was only minor change in D.C. resistance. See Figure 47. From these results it was deduced that a much smaller conductor cross-section would be satisfactory, such as silk screened or sprayed patterns.

Attempts were made to mix eutectic of Ni:Ti powder and Ni:$TiH_2$ powder for spraying on the ceramic board. Problems were encountered in trying to keep the mixture in suspension in the proper ratio. Also, the metal particles of the sprayed pattern did not make intimate contact to each other for good alloying. To obtain intimate contact and proper ratio of materials, a clad powder was investigated.

Sherritt Gordon Mines Limited, Alberta, Canada, coated -325 mesh titanium powder with nickel in eutectic porportions, 85% Ti, 15% Ni by weight. This composite powder provided very good bonding of metallizing with ceramic and alloying of the pattern. With a successful bonding and alloying technique, techniques were used which gave improved resolution of complex patterns.

The composite powder was dispersed in a fugitive organic binder for spraying or silk screen application. Module boards were masked and sprayed with the mixture. Vacuum processing of the board was done in the same way as previously reported. The conductive interconnects are 0.002" thick and approximately 0.020" wide. However, the thickness can be varied by adjusting the amount of powder sprayed on.




100X Polarized Light

Fig. 47 Cross-Section of Metallized Pin

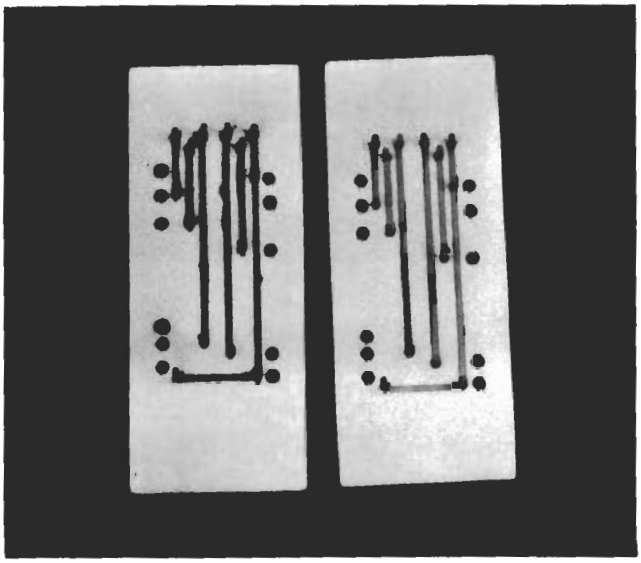
The composite powder was delivered late in the contract period and life test data is limited; however, since the metallized runs are the same alloy, there is good reason to believe that this type of module interconnect run would operate in air satisfactorily.

The time required in making a board by the new process would be cut in half. Figure 48 shows boards made by the old and new process.

MODULE MOUNTING

All modules delivered under the contract AF 33(657)-11400, except the diode matrix, were mounted to the board by welding the module lugs to sealed anchor pins. The diode matrix had been completed when this new mounting technique was developed.

A titanium post is sealed into the board using the active alloy technique. Module electrode lugs were aligned with the post and two nickel pins



Old Process New Process

Fig. 48 Comparison of Metallized Process

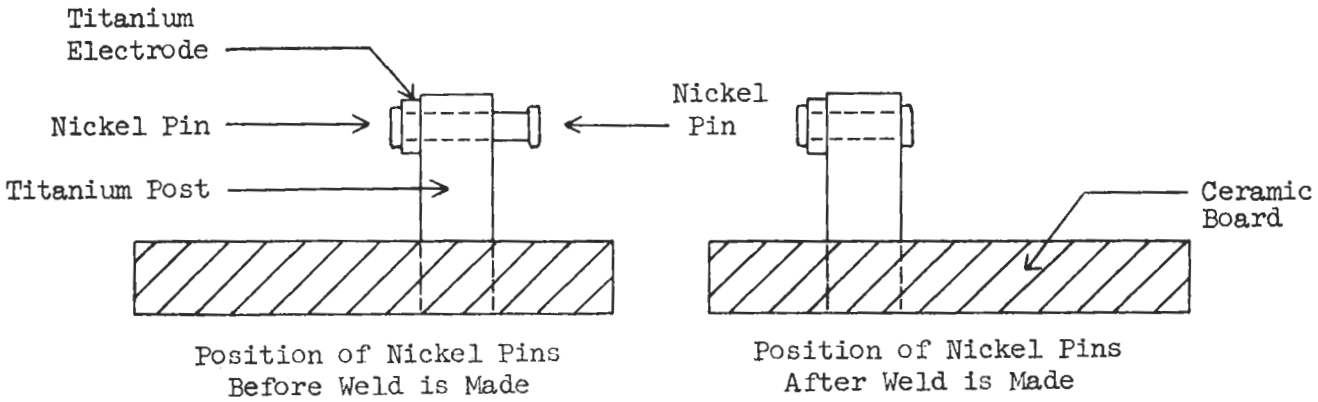



Fig. 49 Position of Nickel Pins Before and After Weld is Made

were brought together and upset welded in the hole of the titanium post as shown in Figure 49.

Metallographic inspection of the butt weld area showed good fusion of the two pins, see Figure 50.

MODULE SHOCK TESTS

A dummy module was mounted and shock tested on a Taft-Pierce high impact shock machine at room temperature. The board was rigidly mounted to the machine as shown in Figure 51.

The module was shocked in two directions in the plane of the board: (1) In a direction of the axis of the module, and (2) In a direction perpendicular to the axis of the module. The specimen was subjected to three shock waves in each direction at each level as shown on the following page:

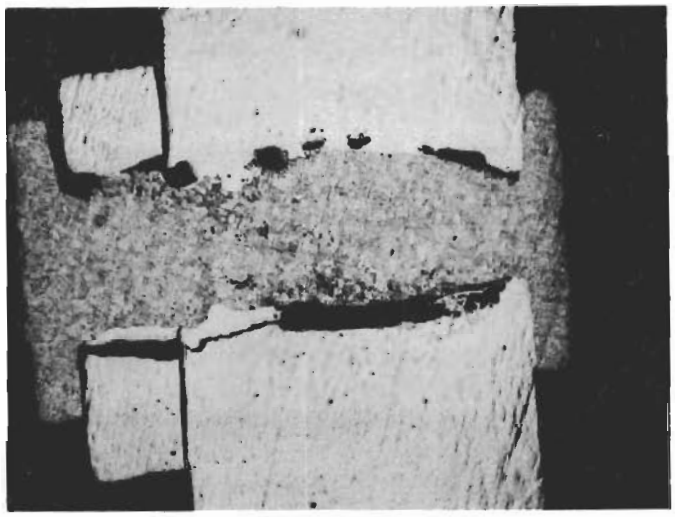


Fig. 50 Cross-Section of Pin-Electrode Assembly

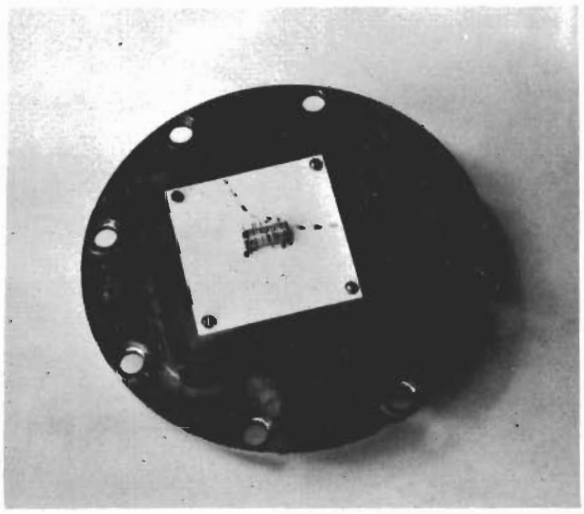


Fig. 51 Module Mounting Shock Test Assembly

| In the Direction of Axis | Perpendicular to Direction of Axis |
|---|---|
| 3 Tests at 300 G's | 3 Tests at 300 G's |
| 3 Tests at 400 G's | 3 Tests at 400 G's |
| 3 Tests at 500 G's | |

The board failed while being shocked at the 500 G level as shown by the dotted line in Figure 51. The welds which attached the electrode lugs to the titanium pins were not affected.

While time was devoted to designing shock tests at 580°C, no data was obtained at elevated temperatures. Any future work on TIMM should include shock test at elevated temperatures.

ISOSTATIC PRESSING OF BOARDS

After the final module design was established, module boards on which the TIMM circuits were to operate were isostatically pressed. The technique is described briefly.

Using a steel plate to divide a plastisol pressing bag in half, the bag was filled with ceramic material and evacuated with a small vacuum pump for 5 minutes. The bag was then placed in the isostatic chamber and pressed at 10,000 psi. After pressing, the two boards were removed and shaped to approximately 3" x 9" on a belt sander. The boards were then air fired at 1,100°C for one hour in an air fired box kiln. Using the proper templet to accommodate the proposed circuit, the holes for mounting pins and interconnection parts were drilled. These boards were then air fired at 1400°C for two hours in an electric heated kiln. The board underwent 18% shrinkage upon final firing. After this firing the boards were ground and finished to final dimensions.

MODULE BRAZING

As reported in AF 33(616)-8096, the technique for brazing TIMM components

into a modular stack involved the use of an aluminum-copper-titanium powder mixture (54% Al, 26% Cu, 20% Ti) suspended in an organic vehicle. Since the resultant paste could not be applied uniformly to the component titanium lugs, brazed seals were not reliable.

It was found that shims could be made from the same powder mixture by dry-pressing techniques. An isobutyl methacrylate-xylene binder was used to temporarily cement shims to components prior to brazing. Stacked modules were heated in vacuum at 300°C for five minutes to evolve the organic binder. This was followed by brazing at 600°C for fifteen minutes. This method of module brazing produced more reliable results, but it was thought that a further improvement could be made to achieve maximum strength in brazed module seals.

In earlier tests with the aluminum-copper-titanium powder, it was noted that there was limited flow at the brazing temperature. It appeared logical that an improvement in melting characteristics would increase bond strength by a greater degree of alloying and a subsequent reduction of voids within the braze. If it were possible to increase the strength of brazed seals by presintering the shims, there would be the added advantage of greater ease in handling the shims when stacking components in a module. Therefore, some tests were conducted with the braze powder mixture in an effort to improve its melting characteristics. It was thought that more intimate contact among the powder particles would cause the low melting (548°C) Al-Cu eutectic reaction to go more readily. Vacuum sintering was chosen as the method for agglomerating the powder particles. Powder sintered at 540°C for one-half hour showed no signs of agglomeration. However, samples of dry-pressed shims vacuum sintered at 540°C for one-half hour exhibited considerable particle agglomeration and a marked increase in strength. Sample titanium lugs were

then brazed with sintered shims, and others with as-pressed shims, at 600°C for fifteen minutes. There was no difference in the strength of the seals, either as-brazed or after 65 hours exposure at 580°C in air.

It was thought that shim forming pressure could have an effect on the melting characteristics of the braze. A set of dies was made for use with a hydraulic press to produce shims with 0.295" O.D. x 0.225" I.D. Preliminary tests indicated that the optimum shim thickness was 0.003". Sample shims were formed at 55,000, 65,000, 75,000 and 90,000 psi, and were subsequently used to braze sample titanium lugs. Although the results were erratic in some cases, all joints were approximately equal in strength, as-brazed and after 65 hours exposure at 580°C in air. None of the above shims were sintered since the test results indicated that seal strength is not related to shim forming pressure.

All titanium to titanium seals made with the dry-pressed shims showed randomly oriented areas where a greater degree of melting occurred. It was thought that aluminum-copper alloy of eutectic composition mixed with the brazing powder would result in more uniform melting of the shims during sealing.

An aluminum-copper mixture (70% Al, 30% Cu) was heated in vacuum at 675°C for five minutes. The resultant partially melted mixture was ground to -270 mesh and -325 mesh titanium powder was added in a 20% ratio. Shims formed from this mixture at 90,000 psi were used to braze sample titanium lugs at 600°C for fifteen minutes. As-brazed joints were not as strong as those made with the normal Al-Cu-Ti composite. There was also some sacrifice of flow within the braze.

In order to satisfy contract schedule commitments, no further tests were made with the module brazing powder. All modules made for this contract were brazed using dry-pressed shims. The shims were formed at 90,000

psi from the metal powder mixture containing 54% Al, 26% Cu, and 20% Ti. The brazing cycle used was that previously described: 5 minutes at 300°C and 15 minutes at 600°C in vacuum.

## CIRCUIT DEVELOPMENT

Circuit development work involved the design, fabrication and testing of two each of the following five different circuit functions:

1. Diode matrix.
2. 3-input NAND gate.
3. Set-reset flip-flop.
4. Cathode follower.
5. Phase shift oscillator.

This report will describe each circuit in detail, giving electrical and mechanical considerations and will present test data taken for each unit.

### DIODE MATRIX

The TIMM diode matrix is a simple array of twenty-four TIMM diodes. The array is arranged in such a way that it can be used to convert binary information into decimal information (see Figure 52). The binary bits and their complements are fed into the input side of the matrix. The matrix will accommodate three bit binary words so that for each of the eight arrangements of the three bits, a voltage appears on one and only one of the eight available output leads.

The diode matrix units constructed under the contract consist only of the diode array. The necessary voltage dropping resistors are to be supplied externally, although they could very well be included in the matrix package. Includion, however, would require one more lead to the package without

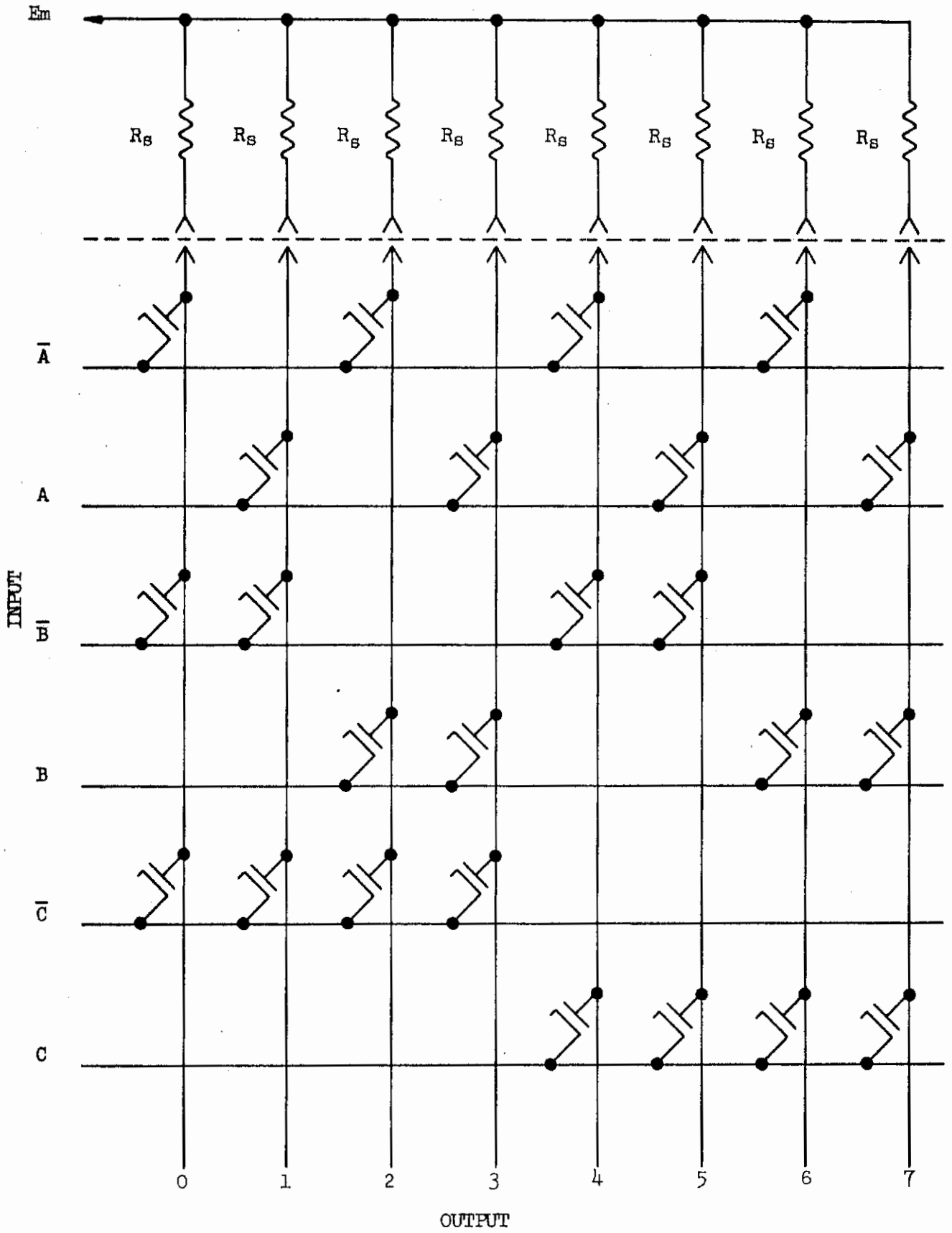


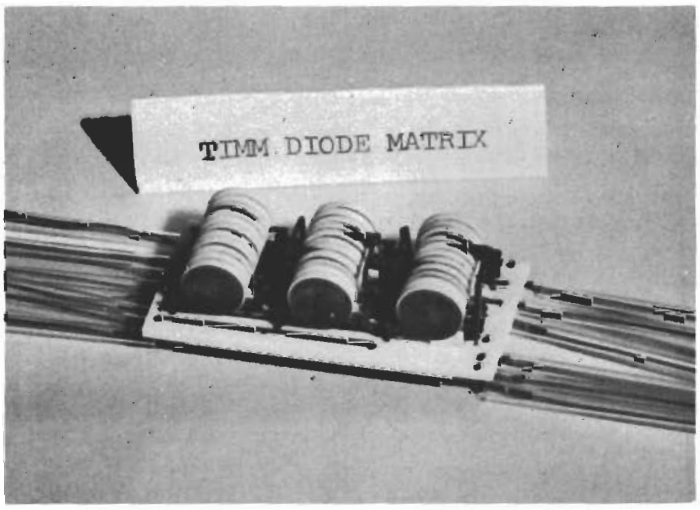

Fig. 52 3-Bit Diode Matrix B/D Converter

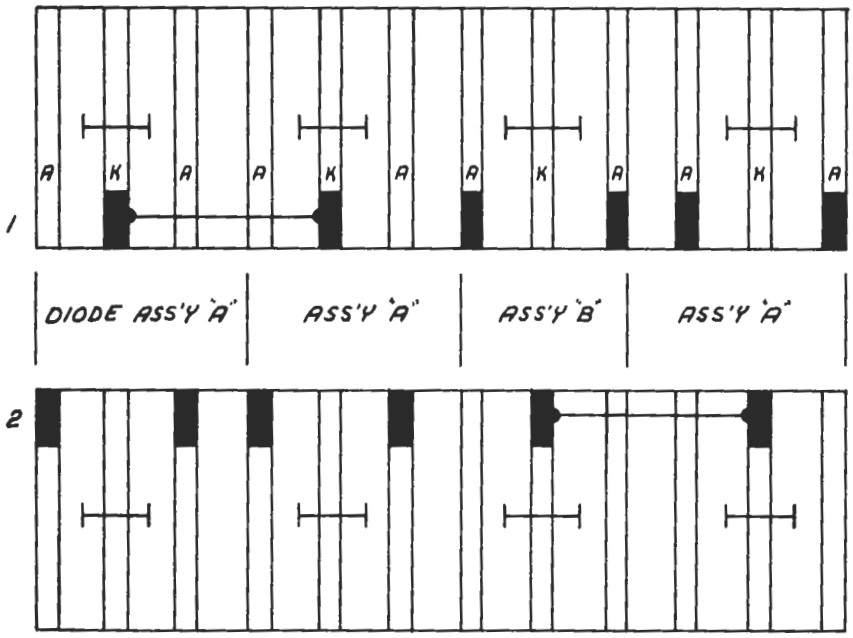
contributing to the demonstration of the versatility of TIMM. A second reason for not including the dropping resistors is that inclusion would make the matrix less flexible, since the value of the dropping resistance is a function of load requirements. Thus, the TIMM matrix can be used for a variety of load conditions depending upon the choice of dropping resistors. Data were taken on the units for several values of dropping resistors.

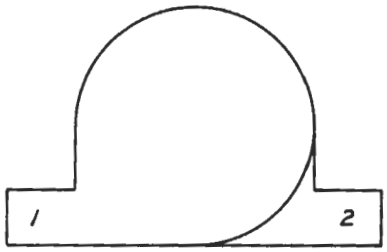
The completed diode matrix is shown in Figure 53. The matrix consists of three modules, each containing four dual, common cathode diodes. The module design and diode specifications are shown in Figures 54, 55, and 56. Figures 54 and 55 show the stacking and wiring arrangements for the modules. The modules are made up of diode subassembly units as shown to facilitate the stacking and sealing of the modules. Only the connection electrodes are shown in the figures.

Figure 56 is the circuit board layout for the diode matrix. The letters at the right are for the correct identification of the input terminals and the numbers at the left are for the output connections. Figure 56 is a bottom view of the board, i.e., the pin side view. Thus, the conductor runs on the top of the board are shown as parallel slotted lines. The single dotted lines show the module connection to the circuit board pins. The three vertical center lines on the drawings are lettered at the lower end to show the module number of the module in that position.

In order to test the finished diode matrix, a scale-of-eight counter circuit was constructed, with both outputs brought out from each counter flip-flop. The counter was designed to operate with the same characteristics as a low voltage (16 volts) TIMM flip-flop, with a "one" to "zero" differential of about six volts. The tests then demonstrate the compatibility of the TIMM diode matrix with a TIMM driving flip-flop.

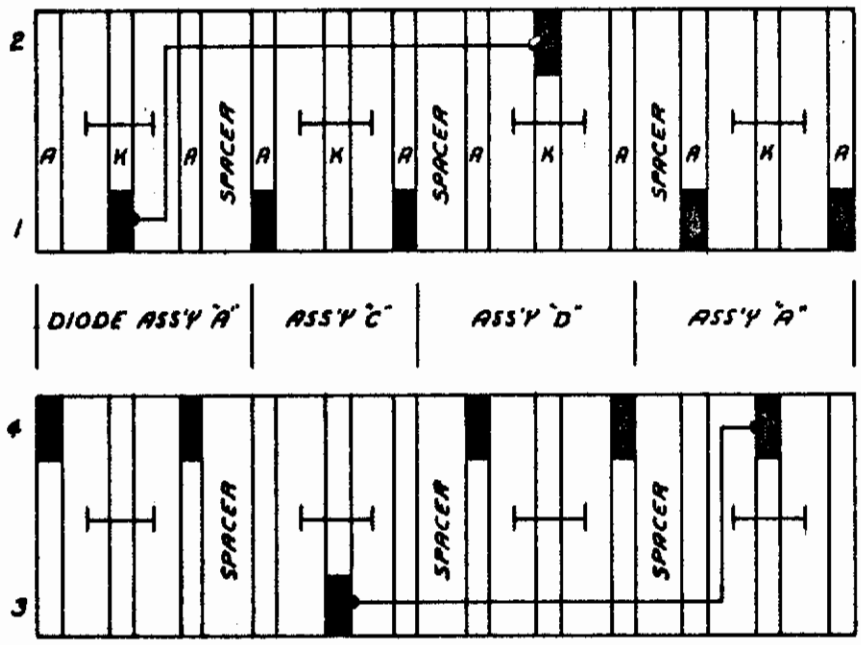


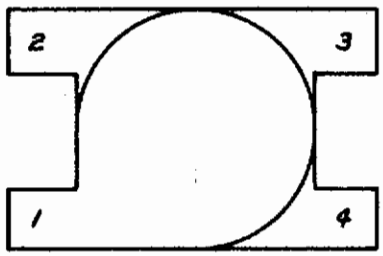




All Diodes Dual, Common K
Spec.; Each Section
$E_p \geq 2.3V$ at $I_p = 50\ \mu A$
$E_p \leq 3.0V$ at $I_p = 3\ mA$

Fig. 54 Diode B/D Converter Matrix, Module 3




All Diodes Dual, Common K
Spec.; Each Section

$E_p \geq 2.3V$ at $I_p = 50\ \mu A$

$E_p \leq 3.0V$ at $I_p = 3\ mA$

Fig. 55 Diode B/D Converter Matrix, Modules 1 and 2

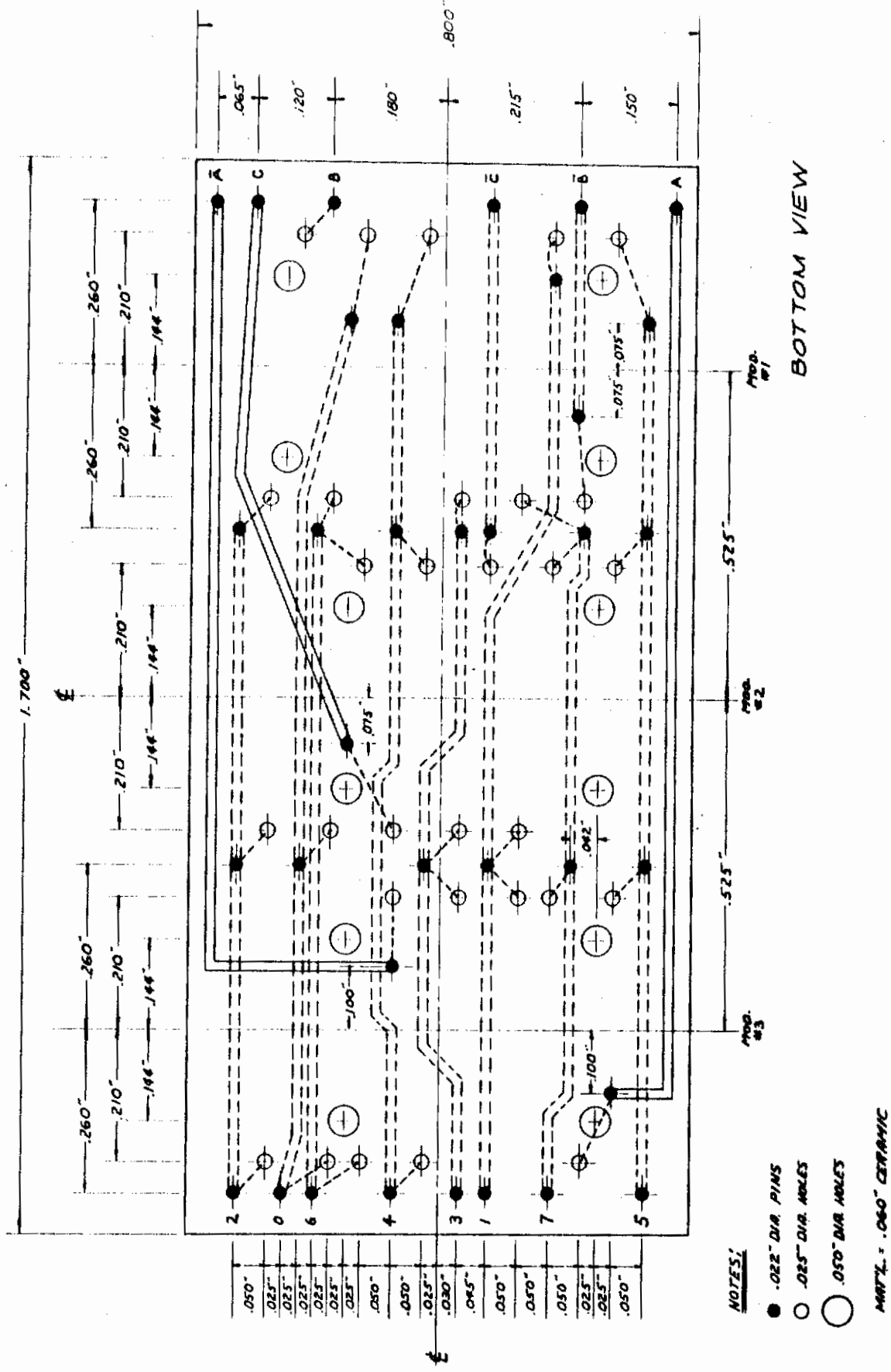



Fig. 56 Printed Circuit Board for Diode Matrix

The TIMM matrices were tested as follows. A recurring pulse was fed into the counter. The outputs of each flip-flop of the counter was fed into the inputs of the matrix. The output and complement of the "unit's" flip-flop were fed into terminals A and $\bar{A}$, respectively. The output and complement of the "two's" flip-flop were fed into the terminals B and $\bar{B}$. In the same manner the output and complement of the "eight's" flip-flop were fed into terminals C and $\bar{C}$. Thus, a three-bit binary word was entered into the matrix for each pulse of the driving generator. The binary words will include all possible combinations ranging from 000 to 111, the corresponding decimal output ranging from zero to seven. At the ninth count the matrix returned to the "zero" state and advanced to "one" at the tenth count.

Voltage measurements were made on each of the output leads for each state of the matrix while the matrix was driving an indicator circuit which presented a load of about 100K to each matrix output lead. The matrix current ($I_m$), i.e., the total current drawn from the matrix power supply was measured for each matrix state. The resulting data are tabulated below, along with the values of the input voltages: (See following pages).

NAND GATE

Two 3-input NAND gates were designed, fabricated and tested for this contract. The circuit diagram and logic for the NAND gates are shown in Figure 57. The circuit is designed for use with positive logic, i.e., a "one" is a positive voltage greater than 10 volts and a "zero" is a voltage less than 8.5 volts. The design supply voltage is +20 volts.

The completed NAND unit is shown in the photograph of Figure 58. The module stacking and wiring diagram and component specifications are shown in Figure 59. The ceramic circuit board for the NAND gates is shown in Figure 60. The board terminal pins in Figure 60 are labeled to designate the proper lead to the module with the letters A, B and C assigned to the 3 inputs.

TABLE I

DIODE MATRIX #1 PERFORMANCE DATA

| Binary | Input (Volts) | | | | | | Output (Volts) | | | | | | | | $I_m$ | $E_m$ | Rs |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| # | C | $\overline{C}$ | B | $\overline{B}$ | A | $\overline{A}$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | (Ma) | (Volts) | (Ohms) |
| 0 | 10 | 15 | 10 | 16 | 10.1 | 16 | 17.3 | 12.6 | 12.5 | 12.5 | 12.5 | 12.3 | 12.4 | 12.3 | 2.0 | 24.0 | 47K |
| 1 | 10 | 15 | 10 | 16 | 15.9 | 10 | 13.2 | 18.0 | 13.0 | 13.1 | 13.0 | 13.1 | 13.0 | 13.1 | | | |
| 2 | 10 | 15 | 16.5 | 10.5 | 10.1 | 16 | 13.0 | 13.0 | 17.7 | 13.0 | 12.9 | 13.0 | 12.9 | 13.0 | | | |
| 3 | 10 | 15 | 16.5 | 10.5 | 15.9 | 10 | 12.9 | 13.0 | 13.0 | 17.7 | 12.9 | 12.8 | 13.0 | 13.0 | | | |
| 4 | 15 | 10.2 | 10 | 16 | 10.1 | 16 | 13.0 | 13.0 | 13.0 | 13.0 | 17.8 | 13.0 | 13.0 | 13.1 | | | |
| 5 | 15 | 10.2 | 10 | 16 | 15.9 | 10 | 13.0 | 13.0 | 13.0 | 13.0 | 13.0 | 17.6 | 13.2 | 13.1 | | | |
| 6 | 15 | 10.2 | 16.5 | 10.5 | 10.1 | 16 | 13.0 | 13.0 | 13.0 | 12.9 | 13.0 | 13.0 | 17.6 | 13.0 | | | |
| 7 | 15 | 10.2 | 16.5 | 10.5 | 15.9 | 10 | 13.0 | 13.1 | 13.0 | 13.0 | 13.0 | 13.0 | 13.1 | 17.7 | | | |
| 0 | 10 | 15 | 9.6 | 16.0 | 10 | 16 | 18.0 | 12.6 | 13.0 | 13.0 | 12.9 | 12.2 | 12.8 | 12.2 | 2.0 | 35.0 | 100K |
| 1 | 10 | 15 | 9.6 | 16.0 | 16 | 10.5 | 12.8 | 17.8 | 12.7 | 12.5 | 12.6 | 12.5 | 12.2 | 12.5 | | | |
| 2 | 10 | 15 | 15.7 | 10 | 10 | 16 | 12.7 | 12.6 | 17.5 | 12.7 | 12.5 | 12.5 | 12.3 | 12.3 | | | |
| 3 | 10 | 15 | 15.7 | 10 | 16 | 10.5 | 12.7 | 12.9 | 12.7 | 17.8 | 12.4 | 12.5 | 12.3 | 12.5 | | | |
| 4 | 15 | 10 | 9.6 | 16 | 10 | 16 | 12.3 | 12.5 | 12.3 | 12.2 | 17.4 | 12.3 | 12.5 | 12.6 | | | |
| 5 | 15 | 10 | 9.6 | 16 | 16 | 10.5 | 12.8 | 12.4 | 12.7 | 12.4 | 12.4 | 17.8 | 12.6 | 12.8 | | | |
| 6 | 15 | 10 | 15.7 | 10 | 10 | 16 | 12.5 | 12.5 | 12.4 | 12.5 | 12.7 | 12.5 | 17.8 | 12.9 | | | |
| 7 | 15 | 10 | 15.7 | 10 | 16 | 10.5 | 12.9 | 12.8 | 12.9 | 12.8 | 12.8 | 12.9 | 13.0 | 17.8 | | | |
| 0 | 9.5 | 15.3 | 9.5 | 15.5 | 9.8 | 16 | 18.0 | 12.1 | 12.0 | 12.0 | 11.9 | 12.0 | 12.0 | 12.0 | 2.0 | 130.0 | 470K |
| 1 | 9.5 | 15.3 | 9.5 | 15.5 | 15.5 | 9.8 | 12.9 | 17.9 | 12.8 | 12.1 | 12.2 | 12.1 | 12.5 | 11.9 | | | |
| 2 | 9.5 | 15.3 | 16.1 | 10 | 9.8 | 16 | 12.9 | 12.1 | 18.5 | 12.2 | 12.0 | 12.2 | 12.3 | 12.0 | | | |
| 3 | 9.5 | 15.3 | 16.1 | 10 | 15.5 | 9.8 | 13.0 | 12.8 | 12.9 | 18.3 | 12.5 | 12.3 | 12.6 | 12.3 | | | |
| 4 | 15.9 | 10.1 | 9.5 | 15.5 | 9.8 | 16 | 12.9 | 12.9 | 12.9 | 12.8 | 18.3 | 12.7 | 13.0 | 12.9 | | | |
| 5 | 15.9 | 10.1 | 9.5 | 15.5 | 15.5 | 9.8 | 13.0 | 12.9 | 13.0 | 12.9 | 13.0 | 18.0 | 13.0 | 13.0 | | | |
| 6 | 15.9 | 10.1 | 16.1 | 10 | 9.8 | 16 | 12.9 | 12.8 | 12.9 | 12.8 | 12.9 | 12.6 | 18.4 | 13.0 | | | |
| 7 | 15.9 | 10.1 | 16.1 | 10 | 15.5 | 9.8 | 13.0 | 12.9 | 12.9 | 12.9 | 12.9 | 13.0 | 13.0 | 18.2 | | | |

TABLE II

DIODE MATRIX #2 PERFORMANCE DATA

| Binary | Input (Volts) | | | | | | Output (Volts) | | | | | | | | $I_m$ | $E_m$ | $R_s$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| # | C | $\overline{C}$ | B | $\overline{B}$ | A | $\overline{A}$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | (Ma) | (Volts) | (Ohms) |
| 0 | 10 | 17.5 | 10 | 18.5 | 10.1 | 18.5 | 20.0 | 12.6 | 12.6 | 12.6 | 12.2 | 12.3 | 12.2 | 12.3 | 2.0 | 125.0 | 470K |
| 1 | 10 | 17.5 | 10 | 18.5 | 18.5 | 10.1 | 12.8 | 20.0 | 12.8 | 12.7 | 12.1 | 12.1 | 12.2 | 12.1 | | | |
| 2 | 10 | 17.5 | 18.6 | 10 | 10.1 | 18.5 | 12.5 | 12.5 | 20.0 | 12.7 | 12.2 | 12.2 | 12.2 | 12.2 | | | |
| 3 | 10 | 17.5 | 18.6 | 10 | 18.5 | 10.1 | 12.8 | 12.6 | 12.8 | 20.0 | 12.2 | 12.2 | 12.2 | 12.2 | | | |
| 4 | 17.9 | 10 | 10 | 18.6 | 10.1 | 18.5 | 12.5 | 12.3 | 12.5 | 12.3 | 20.0 | 12.7 | 12.8 | 12.7 | | | |
| 5 | 17.9 | 10 | 10 | 18.6 | 18.5 | 10.1 | 12.5 | 12.7 | 12.5 | 12.6 | 13.0 | 20.0 | 12.9 | 13.0 | | | |
| 6 | 17.9 | 10 | 18.6 | 10 | 10.1 | 18.5 | 12.5 | 12.3 | 12.5 | 12.3 | 12.9 | 12.8 | 20.0 | 12.8 | | | |
| 7 | 17.9 | 10 | 18.6 | 10 | 18.5 | 10.1 | 12.6 | 12.7 | 12.6 | 12.7 | 13.0 | 12.8 | 13.0 | 20.0 | | | |
| 0 | 10 | 17.5 | 10 | 18.5 | 10 | 18.5 | 18.0 | 12.5 | 12.7 | 12.5 | 12.1 | 12.1 | 12.1 | 12.1 | 2.0 | 36.0 | 100K |
| 1 | 10 | 17.5 | 10 | 18.5 | 18.3 | 10 | 13.0 | 18.6 | 12.9 | 12.8 | 12.3 | 12.2 | 12.5 | 12.2 | | | |
| 2 | 10 | 17.5 | 18.5 | 10 | 10 | 18.5 | 12.7 | 12.7 | 18.5 | 12.8 | 12.5 | 12.2 | 12.4 | 12.3 | | | |
| 3 | 10 | 17.5 | 18.5 | 10 | 18.3 | 10 | 12.8 | 12.9 | 12.9 | 18.9 | 12.2 | 12.5 | 12.3 | 12.5 | | | |
| 4 | 17.9 | 10 | 10 | 18.5 | 10 | 18.5 | 12.5 | 12.5 | 12.5 | 12.5 | 18.5 | 12.7 | 12.8 | 12.8 | | | |
| 5 | 17.9 | 10 | 10 | 18.6 | 18.3 | 10 | 12.8 | 12.8 | 12.7 | 12.8 | 13.0 | 18.5 | 12.9 | 12.8 | | | |
| 6 | 17.9 | 10 | 18.5 | 10 | 10 | 18.5 | 12.5 | 12.4 | 12.5 | 12.5 | 12.8 | 12.6 | 18.5 | 12.8 | | | |
| 7 | 17.9 | 10 | 18.6 | 10 | 18.3 | 10 | 12.7 | 12.5 | 12.5 | 12.6 | 13.0 | 12.9 | 13.0 | 18.3 | | | |
| 0 | 10 | 17.5 | 10 | 18.5 | 10.1 | 18.5 | 17.6 | 12.9 | 13.0 | 13.0 | 12.8 | 12.7 | 12.8 | 12.8 | 2.0 | 24.0 | 47K |
| 1 | 10 | 17.5 | 10 | 18.5 | 18.4 | 10 | 13.1 | 17.6 | 13.0 | 13.0 | 12.9 | 12.9 | 12.9 | 12.9 | | | |
| 2 | 10 | 17.5 | 18.6 | 10 | 10.1 | 18.5 | 12.8 | 12.7 | 17.2 | 12.8 | 12.3 | 12.3 | 12.6 | 12.4 | | | |
| 3 | 10 | 17.5 | 18.6 | 10 | 18.4 | 10 | 12.8 | 12.8 | 13.0 | 17.1 | 12.5 | 12.6 | 12.5 | 12.8 | | | |
| 4 | 17.8 | 10 | 10 | 18.5 | 10.1 | 18.5 | 12.6 | 12.7 | 12.6 | 12.7 | 17.2 | 12.8 | 12.8 | 12.8 | | | |
| 5 | 17.8 | 10 | 10 | 18.5 | 18.4 | 10 | 12.8 | 12.7 | 12.7 | 12.8 | 13.0 | 17.0 | 12.9 | 13.0 | | | |
| 6 | 17.8 | 10 | 18.6 | 10 | 10.1 | 18.5 | 12.6 | 12.6 | 12.5 | 12.6 | 12.9 | 12.7 | 17.0 | 12.9 | | | |
| 7 | 17.8 | 10 | 18.6 | 10 | 18.4 | 10 | 12.7 | 12.7 | 12.7 | 12.7 | 12.9 | 13.0 | 13.0 | 17.1 | | | |

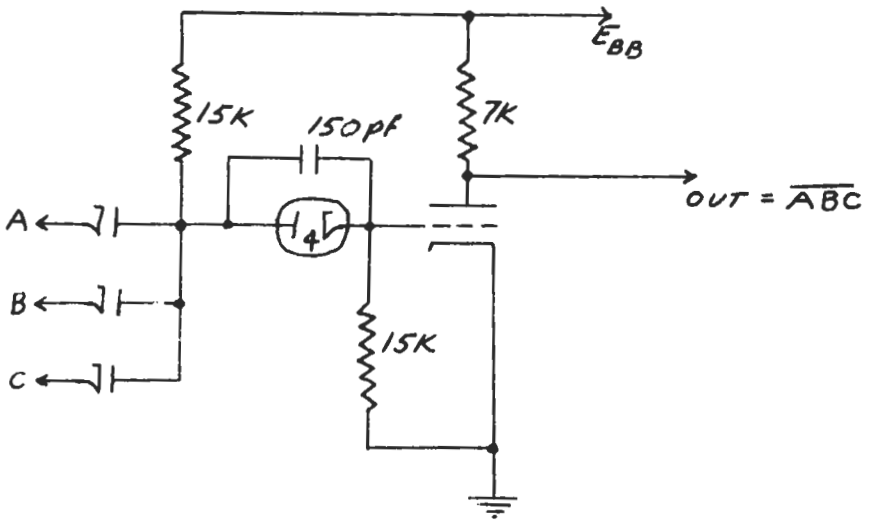



Fig. 57 TIMM 3-Input NAND Gate

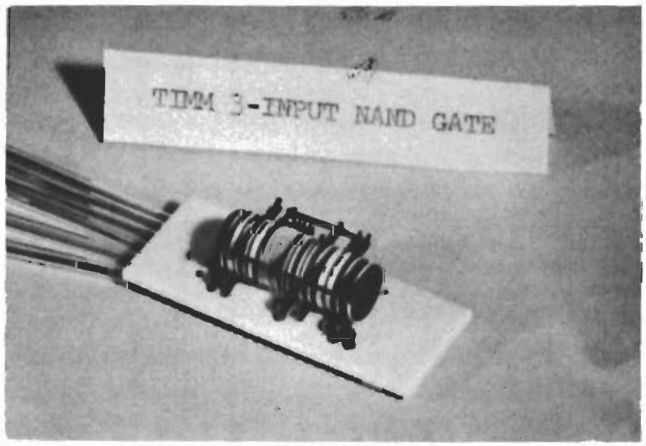
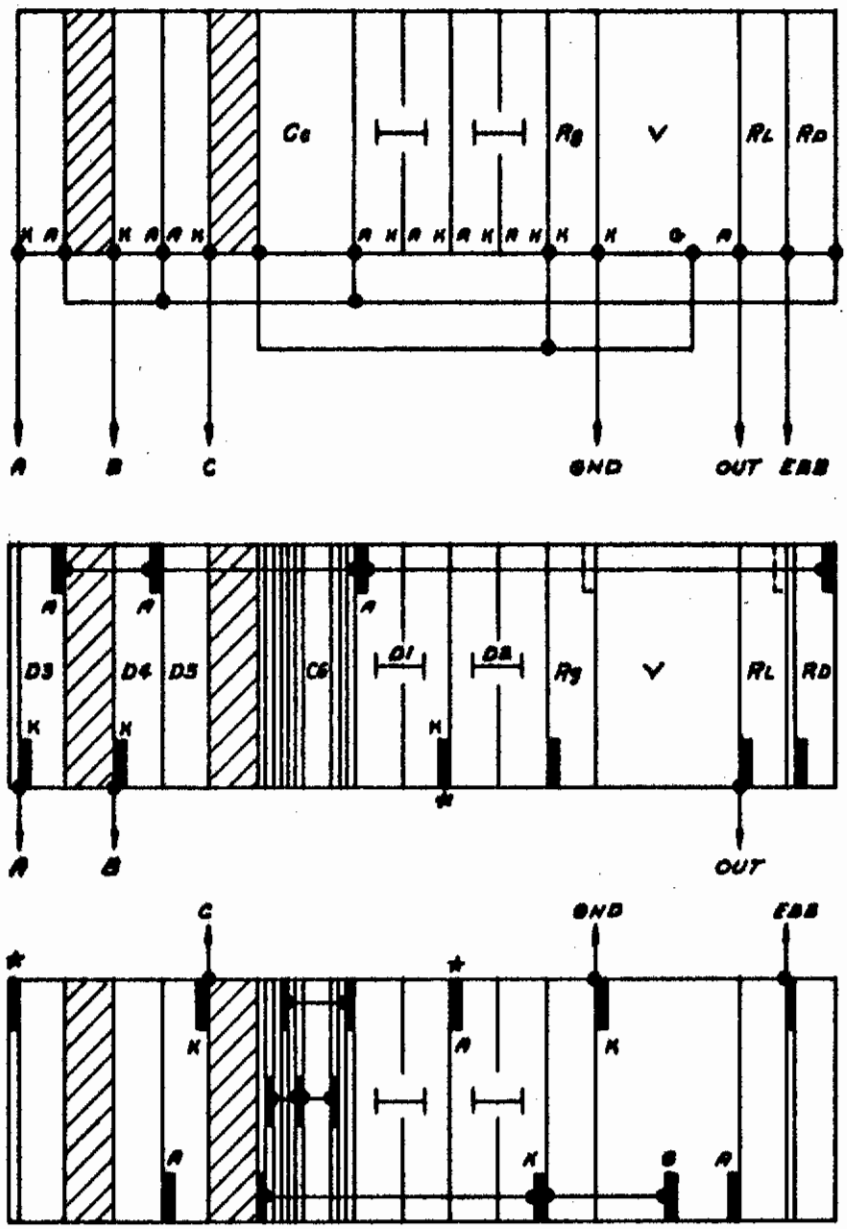



Fig. 58 TIMM 3-Input NAND Gate




Component Specifications:

V: TIMM Triode

$I_p \geq 2.0$ mA at $E_p$=7V, $E_g$=2.4V
$I_p \leq 200$ μA at $E_p$=10V, $E_g$=0V
$I_g \leq 300$ μA at $E_p$=7V, $E_g$=2.4V

$D_1$, $D_2$: TIMM Dual Series Diode

$E_p \geq 4.6$V at $I_p$=50 μA
$E_p \leq 6.0$V at $I$ = 1 mA

$D_3$, $D_4$, $D_5$: TIMM Diodes

$E_p \geq 2.3$V at $I_p$ = 50 μA
$E_p \leq 3.0$V at $I_p$ = 1 mA

$R_g$ 15 KΩ ± 10%
$R_L$ 7 KΩ ± 10%
$R_D$ 15 KΩ ± 10%

$C_c$ 170 pf Capacitor (9 Dielectrics)

[ ] Electrode Removed

★ Module Support Points

Total Length: 0.754"

All Spare Electrodes 0.010"

Fig. 59 Wiring and Stacking Diagram for TIMM 3-Input NAND Gate

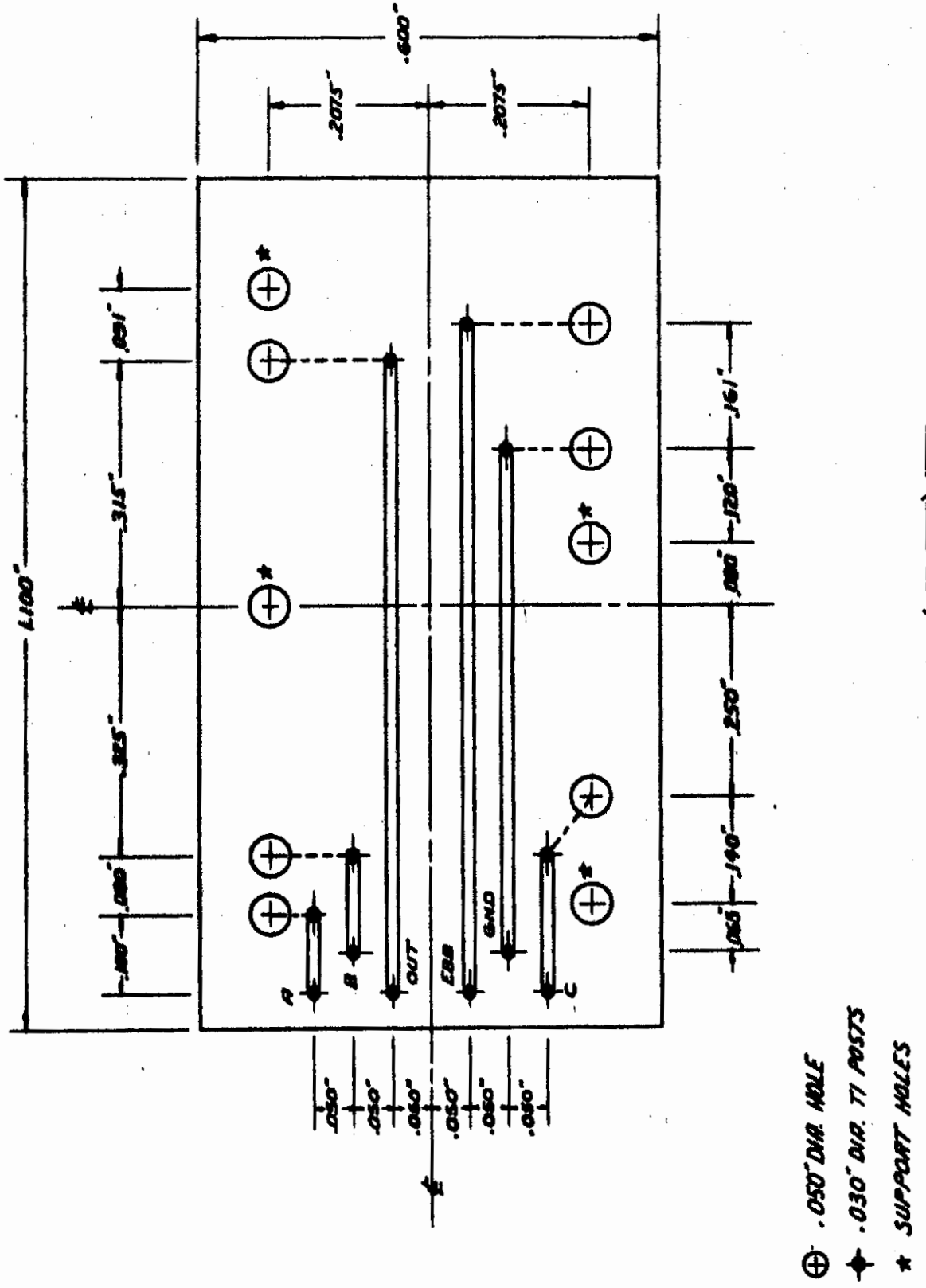



Fig. 60 Ceramic Print Board for TIMM NAND Gate

The operation of the NAND gate is best understood by viewing it as an AND gate and an inverter. If a positive voltage greater than 10 volts is applied to all three inputs, the anodes of the input diodes are raised in potential to a value 2.37 volts more positive than the lowest input voltage. This allows the voltage across the combination of the series diodes and the grid resistor $R_g$ to rise to a value sufficient to cause diode conduction and a consequent drop of about 2.5 volts across $R_g$. The voltage across $R_g$, of course, appears as a grid-to-cathode voltage for the inverter triode. Thus, when a positive voltage, greater than 10 volts, is applied to all three inputs, a positive voltage appears at the grid of the triode sufficient to cause maximum triode conduction.

If any one of the inputs has a voltage applied which is not greater than about +8.5 volts, then the potential across the series diode combination is insufficient to cause conduction, allowing the grid of the triode to remain essentially at the same potential as the cathode. Under those conditions the triode is non-conducting causing its anode potential to rise toward the plate supply voltage. Thus, the logic equation of the NAND gate is $E_o = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$.

The TIMM NAND gates were tested to determine loading capabilities and pulse performance. Figures 61 and 63 are plots of circuit output voltage as a function of input voltage (applied to all inputs simultaneously) for several loading conditions. When the NAND gate is used to drive several other NAND gates, the driving circuit is not loaded when a "one" appears as its output, since current is drawn from the driven circuits only when the cathodes of the driven diodes are at a low potential. For this reason the curves of Figures 61 and 63 are not truly functional since a constant load was used for each curve. The effect of the actual load variation of a NAND

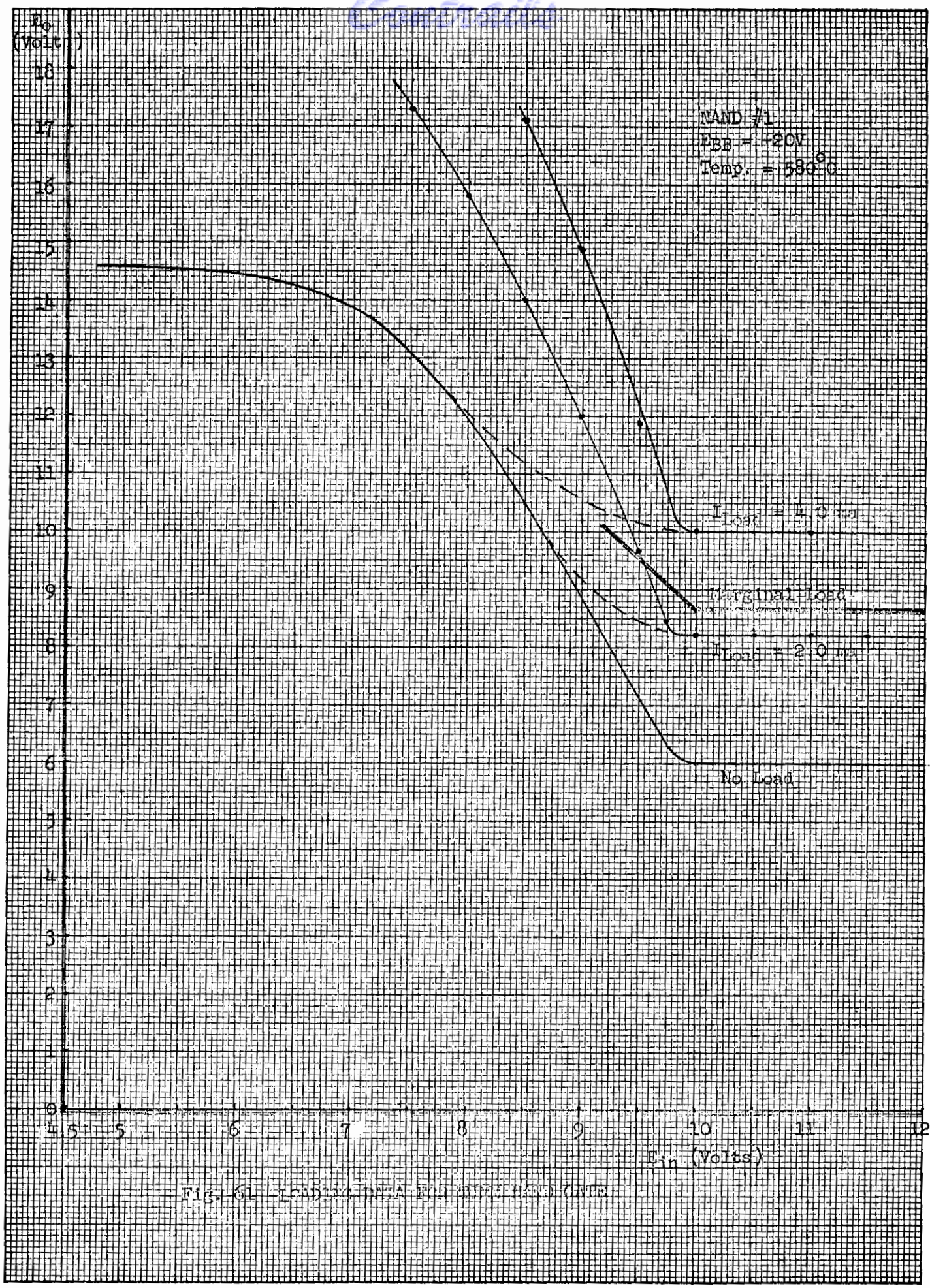



Fig. 61 - LOADING DATA FOR TYPICAL GATE

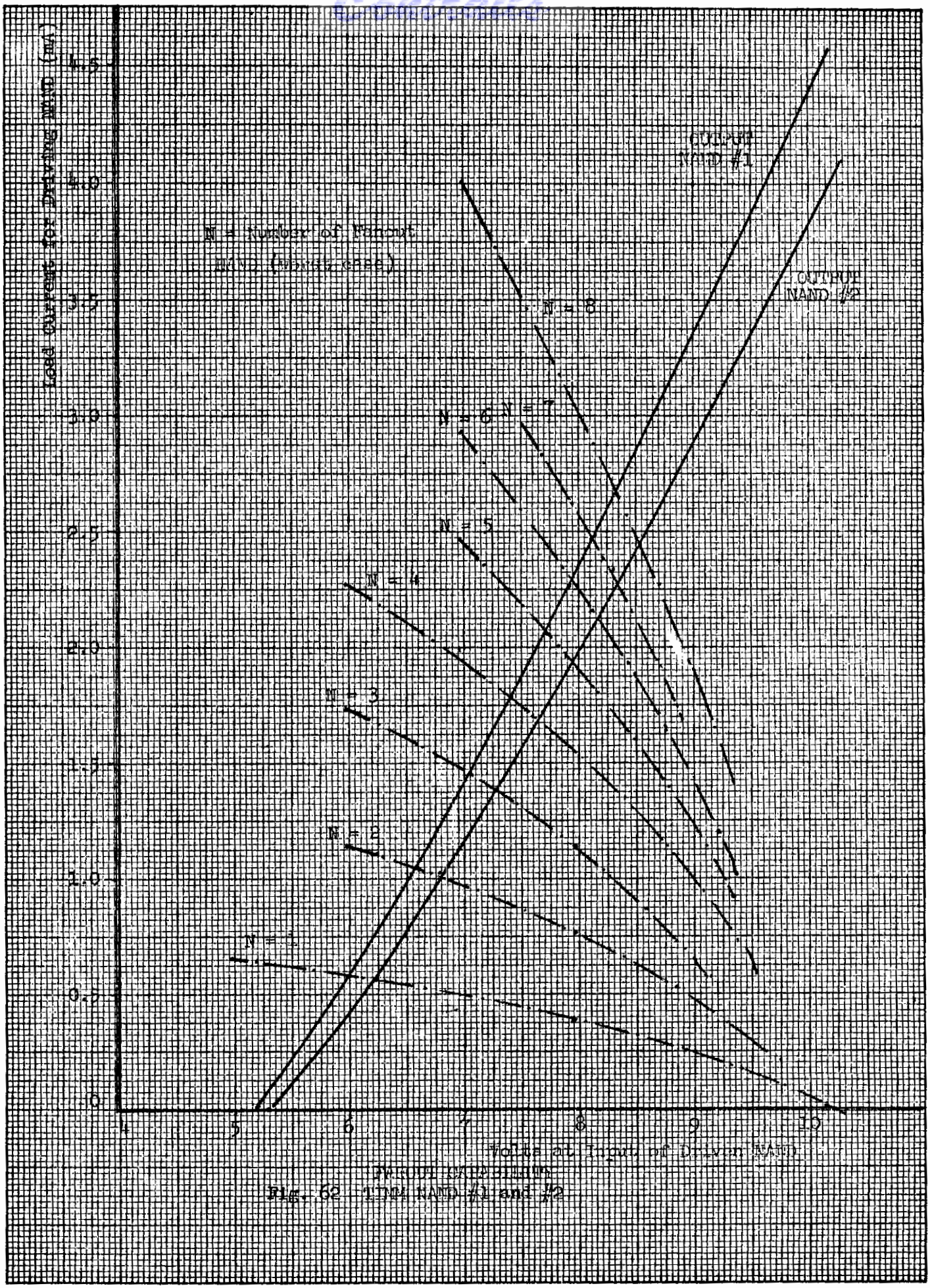



Fig. 62 1704, NAND #1 and #2

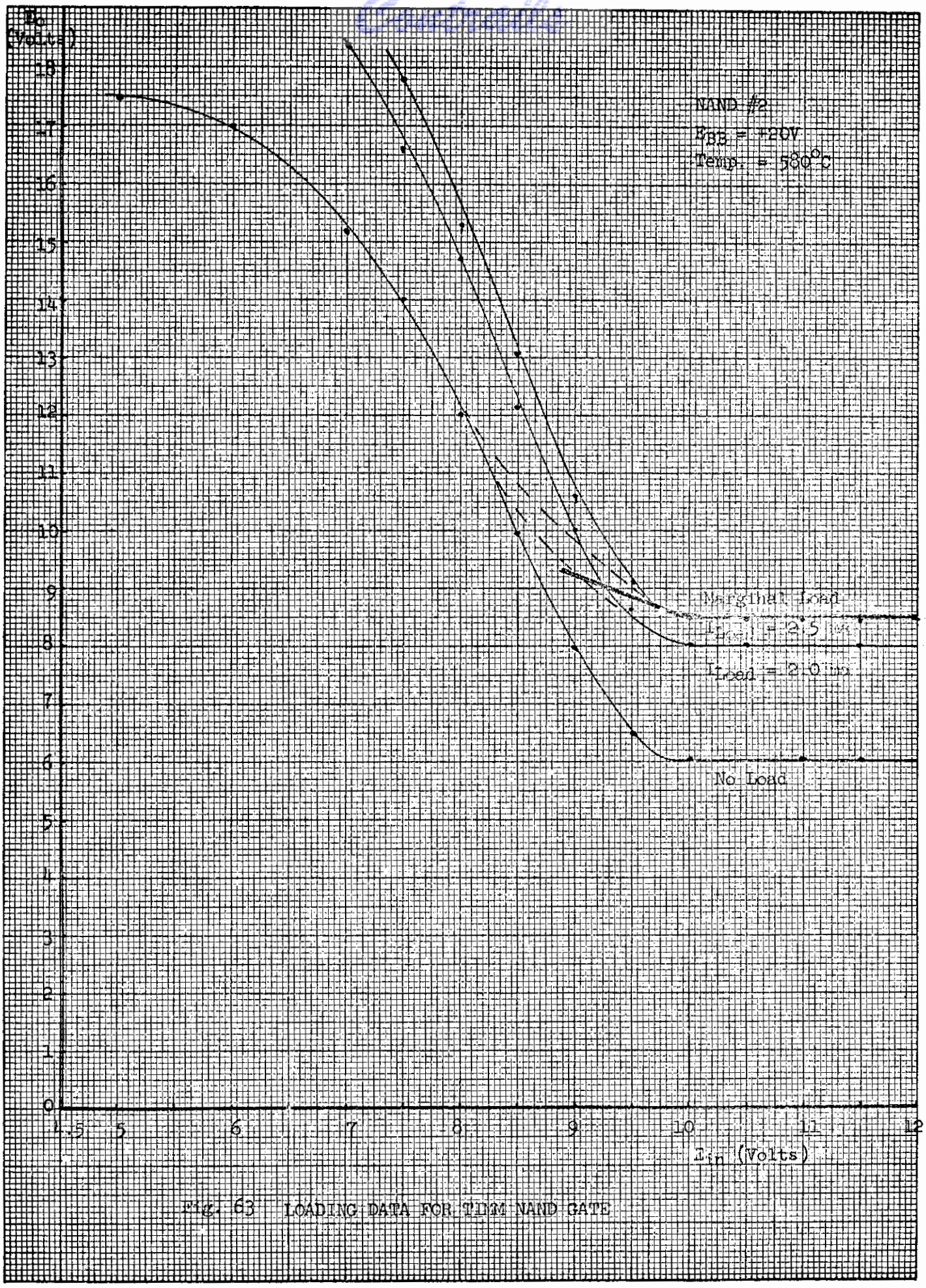



Fig. 63 LOADING DATA FOR TDM NAND GATE

driving a group of NANDs is shown in Figures 61 and 63 by the broken lines joining the loaded curves to the unloaded curve. Since enough NAND gates were not available to take load data under actual fanout conditions, the constant load data were taken and the actual load curves were estimated and are indicated in the figures by the broken lines.

In order to ascertain maximum loading for the NAND gate, the following considerations are made: The voltage value of the minimum logical "one" at the inputs must produce an output voltage which is not greater than a "zero" which, when applied to an input of an identical NAND, would produce an output voltage not less than that of the minimal "one". The minimal "one" can be determined by examining the load curves of Figures 61 and 63. There is a sharp knee in the curves at the point corresponding to an input of 10 volts. Any higher input voltage will have no effect on the output, so that the minimum input voltage for a logical "one" should be not less than +10 volts. The maximum voltage for a logical "zero" can be determined by finding the point on the no load curve which produces an output voltage of not less than 10 volts. For the curve of Figure 61, that point corresponds to a voltage of about 8.7 volts. For proper operation then, the NAND must not be loaded to the point where the output voltage at the knee of the loaded curve falls above an output voltage value greater than the maximum permissible "zero" (+8.7 volts for Figure 61). The heavy line in Figures 61 and 63 represent marginal load lines. The circuits will handle any load whose curve falls below the heavy line but will not handle greater loads.

NAND gates 1 and 2 were tested to ascertain loading capabilities and pulse performance. The curves of Figure 61 show that the NAND #1 can be loaded up to a value of about 2.7 Ma and still perform satisfactorily with a marginal "zero" of +8.7 volts and "one" of +10 volts. NAND #2 can be

loaded to about 2.5 Ma with a marginal "zero" of +8.5 volts and "one" of +10 volts.

To determine the drive current required by the circuits, the drive current at one input was measured for various levels of input voltage. The measurement at one input represents the worse case condition, i.e., with a "one" at two inputs and a "zero" at only one input. The following data were taken for input A on NAND #1 and #2 with +10.5 volts at inputs B and C. $E_{BB}$ = +20 volts, temperature = 580°C:

| $E_{IN}$ (Volts) | $I_{IN}$ (Ma) NAND #1 | $I_{IN}$ (Ma) NAND #2 |
|---|---|---|
| 5.0 | 0.65 | 0.68 |
| 6.0 | 0.59 | 0.60 |
| 6.5 | 0.55 | - |
| 7.0 | 0.50 | 0.50 |
| 7.5 | 0.45 | 0.44 |
| 8.0 | 0.39 | 0.36 |
| 8.5 | 0.34 | 0.30 |
| 9.0 | 0.26 | 0.22 |
| 10.0 | 0.03 | 0.00 |

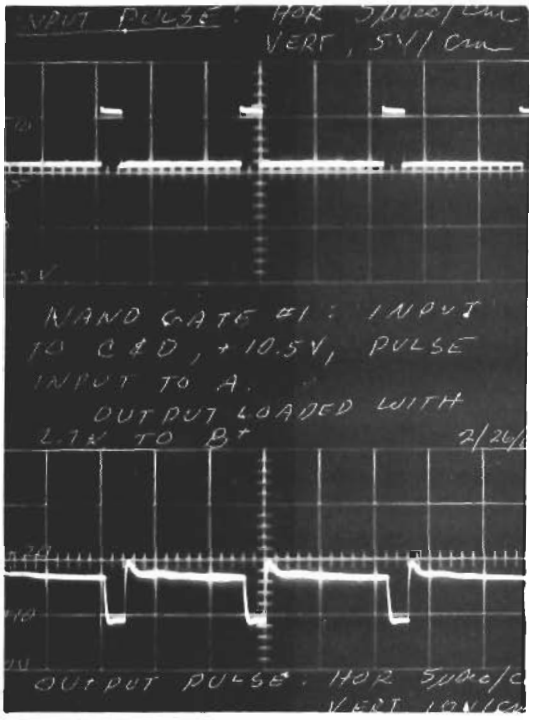
When the above data are plotted on the same graph as the graph of the output voltage of the driving NAND as a function of the load current, then the intersection of the two curves will yield the clamp point of the driving circuit. Assuming "N" identical NANDs in the fanout, the maximum fanout capability of the driving NAND can be determined by finding the highest value of "N" which will intersect the load curve of the driving NAND at a point where the output voltage is not greater than the maximum permissible value of a "zero". Such a graph is shown in Figure 62 for NANDs #1 and #2. Since for both TIMM NANDs the maximum voltage for a "zero" is +8.5 volts, it can be seen from the figure that either circuit can fanout to as many as eight other NAND gates and perform satisfactorily under worse case conditions. The following operational data were taken under the following conditions:

1. $E_{BB}$ = +20 volts, temperature = 580°C.
2. Circuits loaded with 2.5 Ma load for "zero" out, unloaded with "one" out.
3. "One" in, +12 volts, "zero" in, +8.5 volts.
4. Input current measured at input terminal "A".

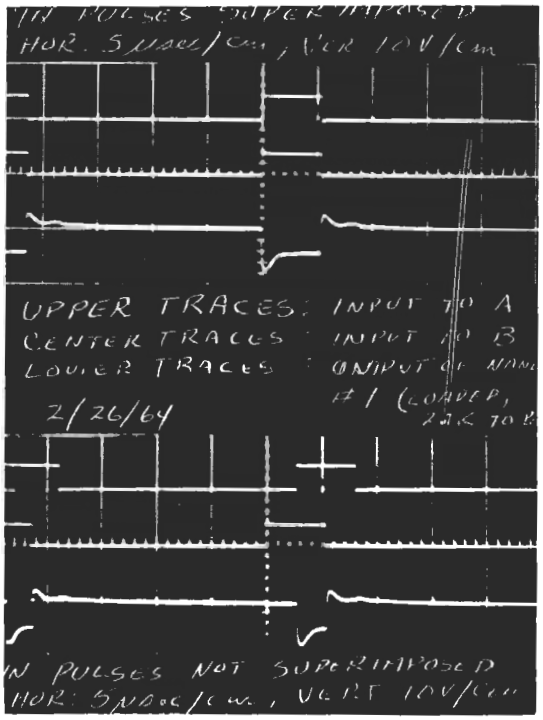
| Input | | | Output(Volts) | | $I_a$(Ma) | | $I_{BB}$(Ma) | |
|---|---|---|---|---|---|---|---|---|
| A | B | C | NAND #1 | NAND #2 | NAND #1 | NAND #2 | NAND #1 | NAND #2 |
| 1 | 1 | 1 | 8.5 | 8.5 | 0 | 0 | 4.6 | 4.38 |
| 0 | 1 | 1 | 11.5 | 12.5 | 0.35 | 0.34 | 1.5 | 1.51 |
| 0 | 1 | 0 | 13.5 | 14.2 | 0.18 | 0.24 | 1.3 | 1.35 |
| 0 | 0 | 0 | 13.5 | 15.0 | 0.18 | 0.14 | 1.3 | 1.3 |
| 1 | 0 | 1 | 11.5 | 12.5 | 0 | 0 | 1.5 | 1.31 |

Note that the output voltage in each case is within the limits for proper operation.

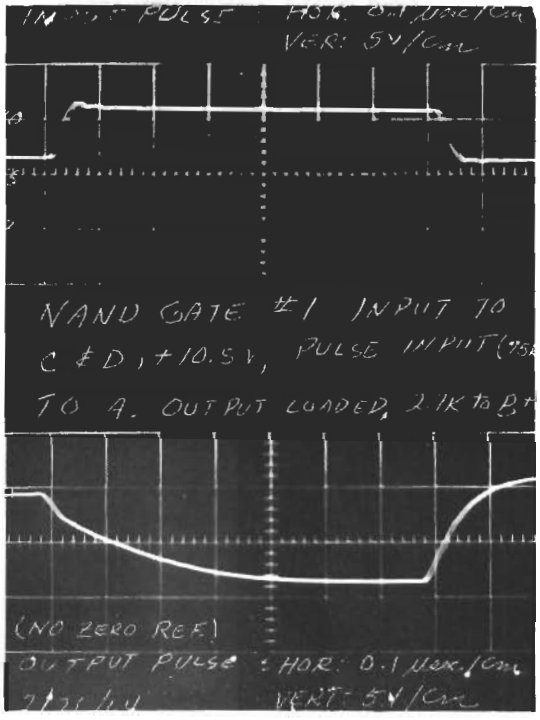
The pulse performance of the NAND gates was investigated next. The results of these tests are shown in the oscillographs of Figures 64 and 65. In both cases the plate supply voltage $E_{BB}$ was set at +20 volts and the oven temperature at 580°C and the NANDs were loaded with 2.7 K ohms to B+, approximating maximum load conditions. For oscillograph #1 in both figures, a steady state "one" of +10.5 volts was applied to inputs C and D, and a pulse with a +6 volts base line was applied to input A. This pulse is shown in the lower portion of the photos. In both cases the output pulse is ample to drive other NAND gates. Photograph #2 in Figures 64 and 65 was made with a pulse input on inputs A and B, and a steady state "one" at input C. The upper portion of the photographs shows the result of simultaneous "ones" at all inputs. The lower photograph shows the result of the input "ones" arriving at different times. Notice that there is very little feedthrough when the input pulses are not superimposed with respect to time. Photograph #2 of Figures 64 and 65 shows the rise time detriment of the loaded NAND. The upper portion of the photographs shows the input pulse at input A with steady state "one" at the other




Photograph #1

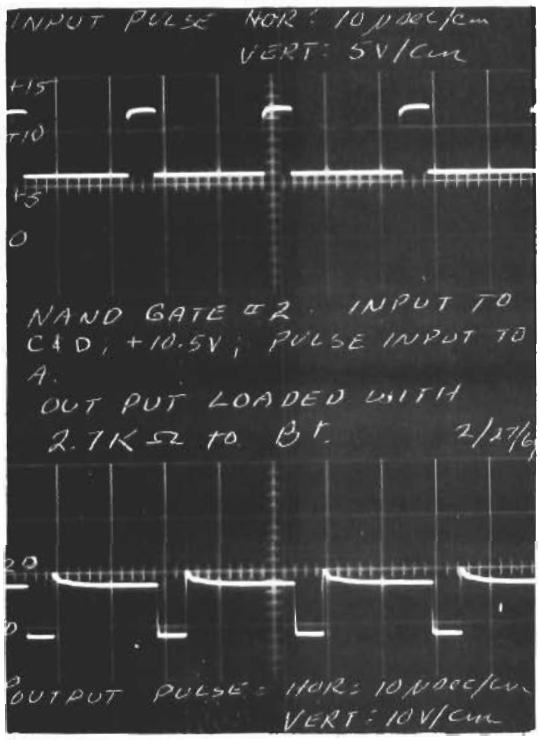



Input Pulses, +6 Volts Baseline
Photograph #2

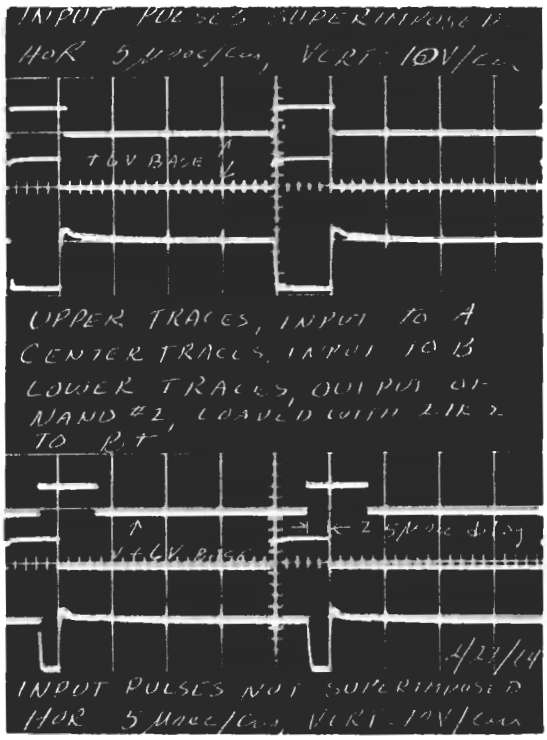



Photograph #3

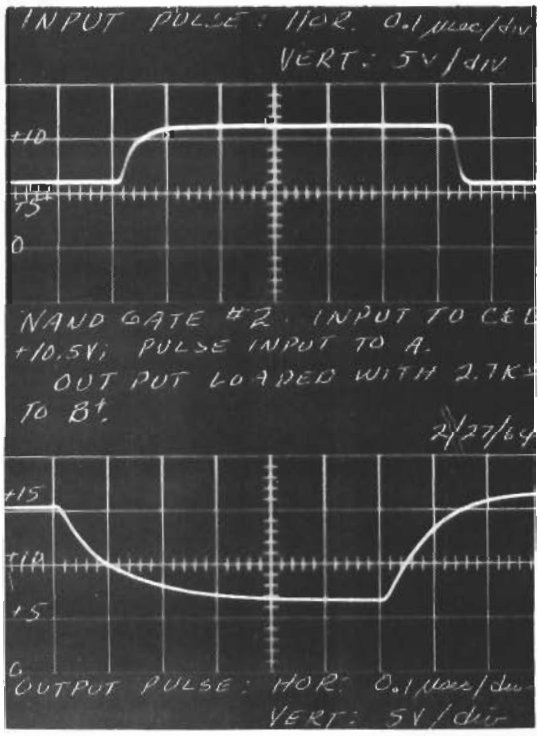
Fig. 64 Pulse Performance TIMM NAND #1




Photograph #1




Photograph #2




Photograph #3

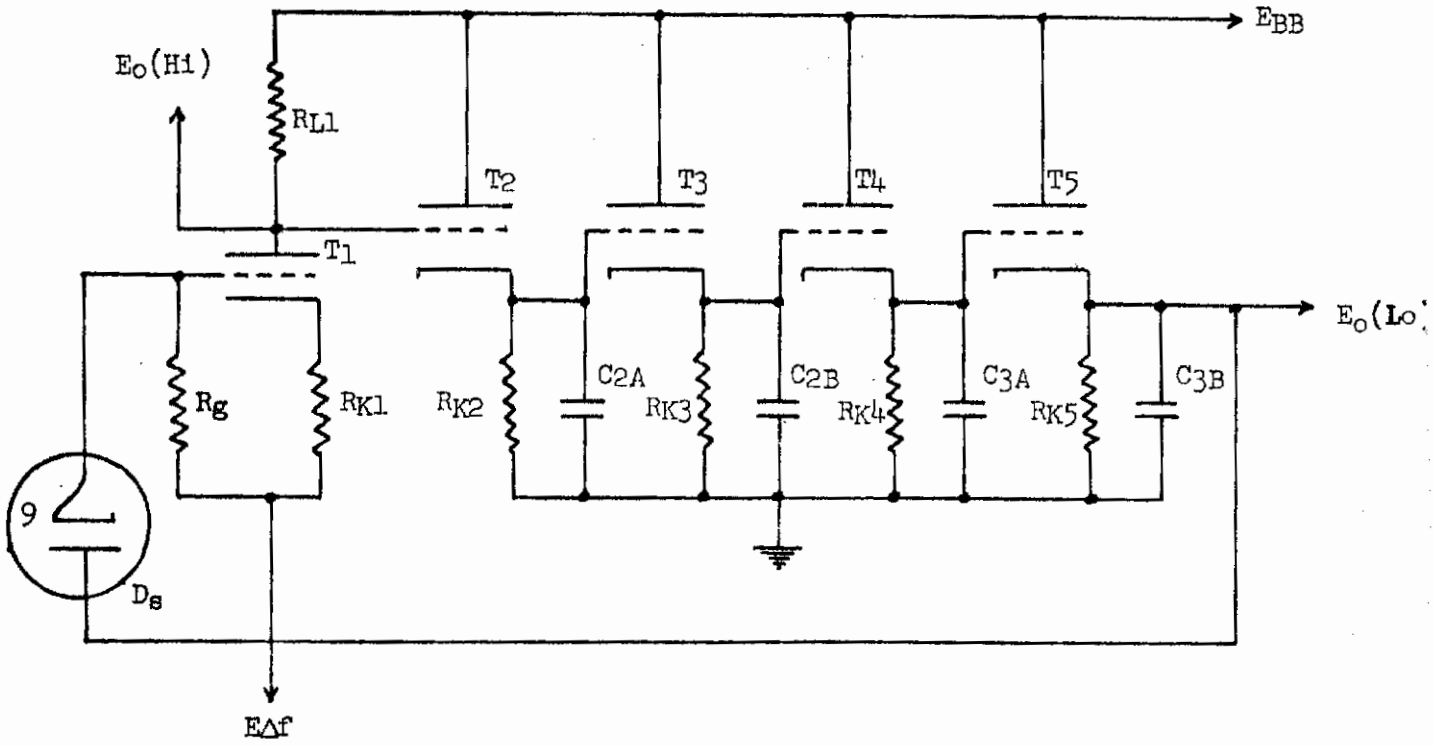
Fig. 65 Pulse Performance TIMM NAND #2

inputs. The lower portion of the photograph shows the rise and fall time of the output pulse on a 0.1 μsec per division scale. If rise time is defined as the time required for the pulse to rise from a value of $E_{min}$ + 0.1 ($E_{max}$ - $E_{min}$) to a value of $E_{min}$ + 9.9 ($E_{max}$ - $E_{min}$), then the rise time for the output pulse of NAND #1 is about 0.1 μsec and for NAND #2, about 0.18 μsec. The corresponding fall times are 0.3 μsec and 0.25 μsec, respectively.

PHASE SHIFT OSCILLATOR

Two TIMM phase shift oscillators were designed, fabricated and tested for the contract. A schematic diagram of the final design, along with component specifications, is shown in Figure 66. The module stacking and wiring diagram is shown in Figure 67. The circuit was stacked and sealed in one unit comprising a module of 2.015" length. This module is the longest TIMM module that has been stacked and experience with it has led to the conclusion that modules greater than about 1.5" in length should be avoided to avoid mechanical problems. The drawing of the circuit board layout is shown in Figure 68 and a photograph of a completed unit is shown in Figure 69.

The circuit consists of a voltage amplifier, $V_1$, and a series of four cascaded cathode followers. Each cathode follower is capacitive loaded by a 200 pf capacitor which causes a phase shift of 45° at the operating frequency of about 500 KC. Thus, the output signal from the voltage amplifier suffers a total phase shift of 180° through the four cathode followers. The output of the cathode followers is then fed back to the input of the voltage amplifier which completes the required 360° phase shift. The output from the fourth CF circuit is actually fed through a series arrangement of nine TIMM diodes. This arrangement allows the adjustment of the D.C. voltage at the grid of the voltage amplifier while offering minimal impedance to the fed-back A.C. voltage. The slope resistance of the diode units is less than




COMPONENTS SPECIFICATIONS:

$V_1$: 2.0 mA > $I_p$ > 1.5 mA
Grid $C_p$ > 2.0V at $E_p$ = 40V
$\mu$ > 14 $E_g$ = 0V

$R_{L1}$: 40K ± 10%
$R_g$ : 15K ± 10%
$R_{K1}$: 750 , ± 10%
$R_{K2}$, $R_{K3}$, $R_{K4}$, $R_{K5}$: 20K ± 10%

$V_2$, $V_3$, $V_4$, $V_5$: $I_p$ > 2.0 ma
Grid $C_p$ > 2.0V at $E_p$ = 40V
$\mu$ > 14, $g_m$ > 2500 µmho $E_g$ = 0V

$C_2C_2$: 2 section capacitor
200 pf per section

$C_3$: 2 section capacitor
200 pf per section

$D_s$: 3 triple series diodes
Each triple section
$E_p \geq 6.9$V at $I_p$ = 50 µA
$E_p \geq 9.0$V at $I_p$ = 1 mA

Fig. 66 TIMM Phase-Shift Oscillator

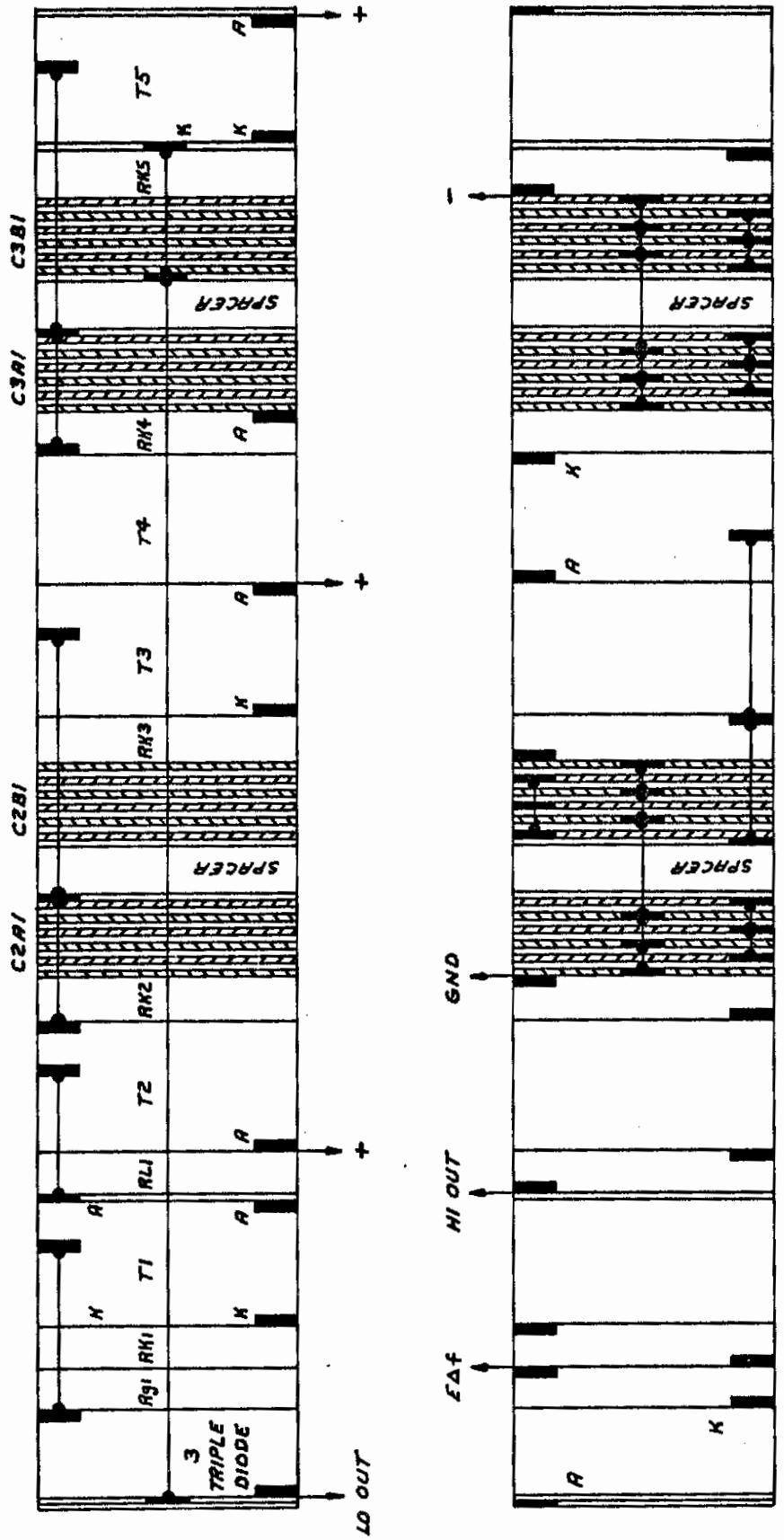



Fig. 67 Stacking and Wiring Diagram for TIMM Phase Shift Oscillator

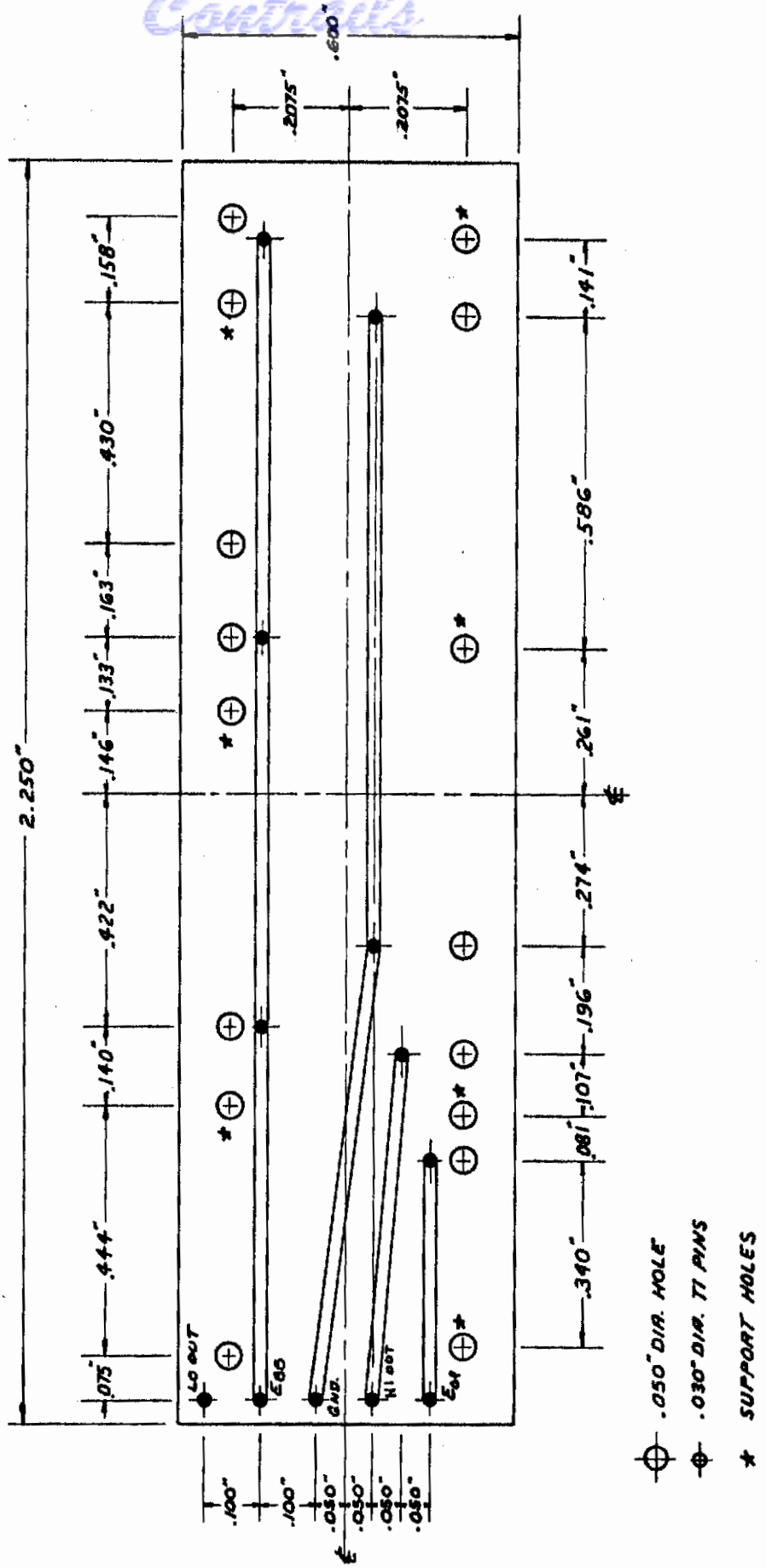



Fig. 68 Circuit Board Layout for TIMM P.S. Oscillator

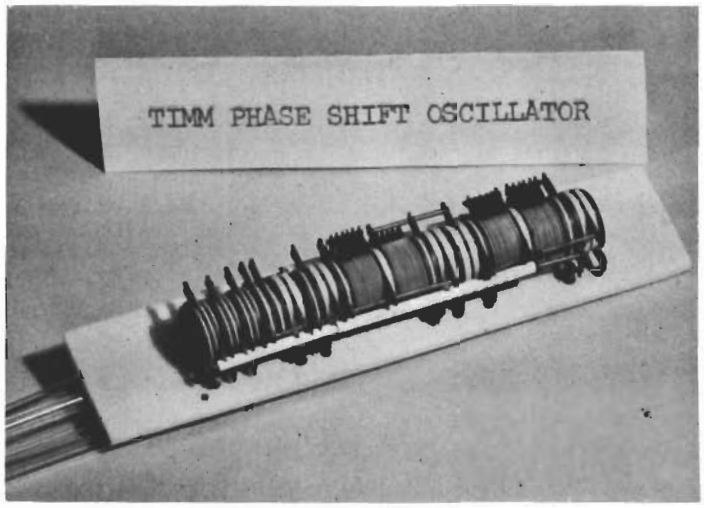



Fig. 69 TIMM Phase Shift Oscillator

400 ohms, thus the series impedance the A.C. sees is less than 3600 ohms in this circuit. Capacitor coupling could, of course, have been used but the diodes have the advantage of not being frequency sensitive and at the same time, the physical size of the nine diodes (3 triple series units) is less than that of the very large TIMM capacitor which would be required. The frequency dependency question is pertinent in this circuit because the oscillator is designed to be voltage tunable over a considerable range of frequencies.

Voltage tuning of the oscillator is possible because the amount of phase shift available in each CF stage is a function of the Gm of the tube in that stage. For a $45^{\circ}$ phase shift in a capacitively loaded cathode follower, the relationship $GmX_c = 1$ *(1) must hold so that when Gm is increased, $X_c$ must decrease to maintain the proper phase shift. That is accomplished, of course, by a rise in the operating frequency of the oscillator.

The operating frequency of the TIMM phase shift oscillator is varied by

varying the cathode. (1) This relationship is arrived at by finding the complex expression for the gain of the CF stage, $K = \frac{Gm^2 - jWC\,Gm}{Gm^2 + W^2C^2}$, $R_K \gg \frac{1}{R}$, $\mu \gg 1$. The phase shift then is $\Theta = \mathrm{Tan}^{-1}\left|\frac{WC}{Gm}\right|$. Thus, for $45^\circ$ phase shift $\frac{WC}{Gm} = 1$ or $GmX_C = 1$ voltage on the voltage amplifier. Since all stages of the oscillator are direct-coupled, the operating point, and hence the Gm of all CF stages [redacted] changed.

Data were taken on the two-phase shift oscillators to determine operating frequency range, output voltage amplitude, output impedance, and dependency of operation on plate supply voltage. Temperature dependency data were taken on oscillator frequency and $L_O$ terminal output voltage as a function of $E_{BB}$: temperature = $580^\circ C$:

| $E_{BB}$ | Frequency (KC) | | $E_{10}$ (PP Volts) | |
|---|---|---|---|---|
| (D.C. Volts) | P.S. Osc.#1 | P.S. Osc.#2 | P.S. Osc.#1 | P.S. Osc.#2 |
| 50 | 526.1 | 646.8 | 2.3 | 1.4 |
| 60 | 474.8 | 556.7 | 3.0 | 2.9 |
| 70 | 451.4 | 516.7 | 3.3 | 3.2 |
| 80 | 452.98 | 510.8 | 2.8 | 3.0 |
| 90 | 500.0 | 539.2 | 1.6 | 2.3 |
| 100 | ----------no oscillation---------- | | | |

With $E_{BB}$ = +80 volts, $E\Delta f$ = 0V, the output voltage, operating frequency and supply current were measured as a function of temperature for P.S. oscillator #1. The data are as follows:

| Temp.($^\circ C$) | Freq.(KC) | $I_{BB}$ (Ma) | $E_o$ (VPP) |
|---|---|---|---|
| 500 | 284.0 | 6.2 | 3.0 |
| 560 | 432.6 | 6.5 | 3.4 |
| 572 | 443.0 | 6.5 | 3.1 |
| 578 | 448.3 | 6.5 | 3.0 |
| 584 | 450.2 | 6.2 | 3.0 |
| 586 | 454.6 | 6.5 | 3.0 |

The following data were taken for both oscillators to determine the range of frequency control by a voltage at the $\Delta f$ terminal. Temperature in all cases is $580^\circ C$ and $E_{BB}$ = 70 volts:

| $E\Delta f$ | Frequency (KC) | | $I\Delta f$(Ma) | | $I_{BB}$(Ma) | | $E_{lo}$(PPV) | |
|---|---|---|---|---|---|---|---|---|
| (DCV) | Osc.#1 | Osc.#2 | Osc.#1 | Osc.#2 | Osc.#1 | Osc.#2 | Osc.#1 | Osc.#2 |
| +18 | 701.42 | 797.2 | 0.71 | 0.7 | 9.05 | 9.3 | 1.6 | 1.8 |
| +15 | 614.35 | 712.2 | 0.84 | 0.8 | 8.50 | 8.7 | 3.1 | 3.0 |
| +12 | 573.71 | 670.5 | 0.98 | 0.94 | 8.01 | 8.2 | 3.5 | 3.2 |
| + 9 | 528.43 | 633.0 | 1.15 | 1.05 | 7.5 | 7.65 | 3.6 | 3.4 |
| + 6 | 507.30 | 594.1 | 1.24 | 1.2 | 7.1 | 7.15 | 3.7 | 3.4 |
| + 3 | 479.27 | 553.4 | 1.39 | 1.31 | 6.6 | 6.6 | 3.6 | 3.4 |
| - 0 | 449.64 | 512.5 | 1.50 | 1.45 | 6.1 | 6.2 | 3.2 | 3.4 |
| - 3 | 421.26 | 474.4 | 1.65 | 1.59 | 5.6 | 5.62 | 2.8 | 3.0 |
| - 6 | 395.52 | 442.1 | 1.75 | 1.7 | 5.0 | 5.2 | 2.2 | 2.5 |
| - 9 | 373.40 | 408.1 | 1.85 | 1.8 | 4.5 | 4.7 | 1.4 | 2.0 |
| -12 | 362.13 | 377 | 1.95 | 1.9 | 4.0 | 4.2 | 0.4 | 1.3 |

Figures 70 and 71 show the oscillator frequency dependency on $E\Delta f$ for P.S. Osc. #1 and #2 respectively. Curves are plotted in the graphs for three values of $E_{BB}$. In both oscillators a supply voltage of +70 volts seems to be optimum for linearity and range. It can also be seen by the curves that a point exists where the operating frequency is relatively independent of supply voltage. In the case of Osc. #1, when $E\Delta f$ is about -2 volts, an over-all variation of only about 10 KC occurs as the supply voltage varies from +60 volts to +80 volts.

The TIMM oscillators are provided with two output terminals on the circuit board. One labeled $E_{lo}$ is a low impedance output from the fourth cathode follower. Another terminal labeled $E_{Hi}$ is provided for a higher voltage, high impedance output from the plate of the voltage amplifier stage. The voltage at $E_{Hi}$ is about four times that at $E_{lo}$.

The output impedance of both circuits was measured by the substitution or half-voltage method. The results of the measurements are as follows:

P.S. Osc. #1 — Lo Z Term; ZAC 1.4K at $E_{BB}$ = 70 V
Hi Z Term; ZAC 55 K at $E_{BB}$ = 70 V

P.S. Osc. #2 — Lo Z Term; ZAC 1.1K at $E_{BB}$ = 70 V
Hi Z Term; ZAC 30 K at $E_{BB}$ = 70 V

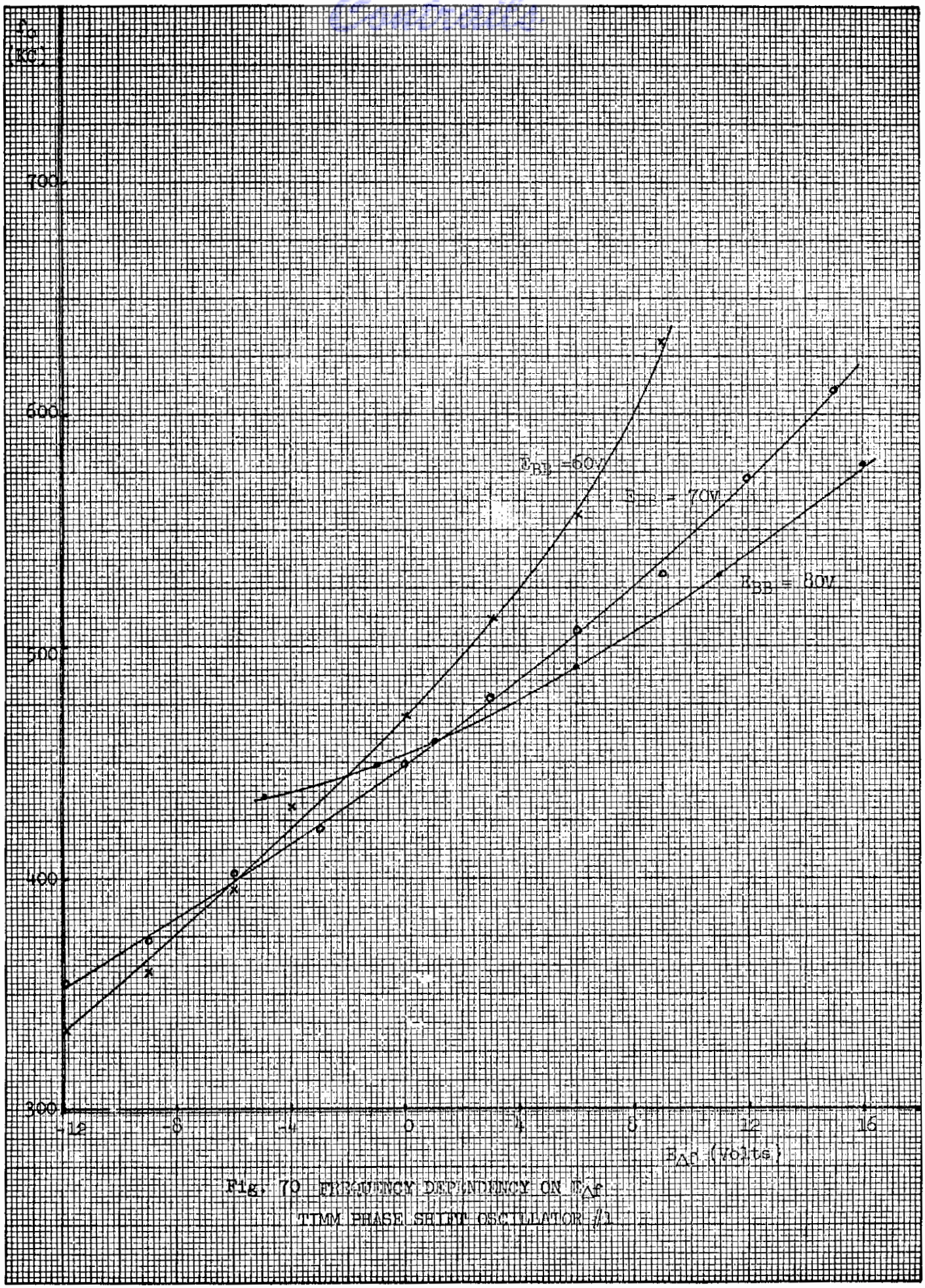



Fig. 70 FREQUENCY DEPENDENCY ON $E_{\Delta f}$
TIMM PHASE SHIFT OSCILLATOR #1

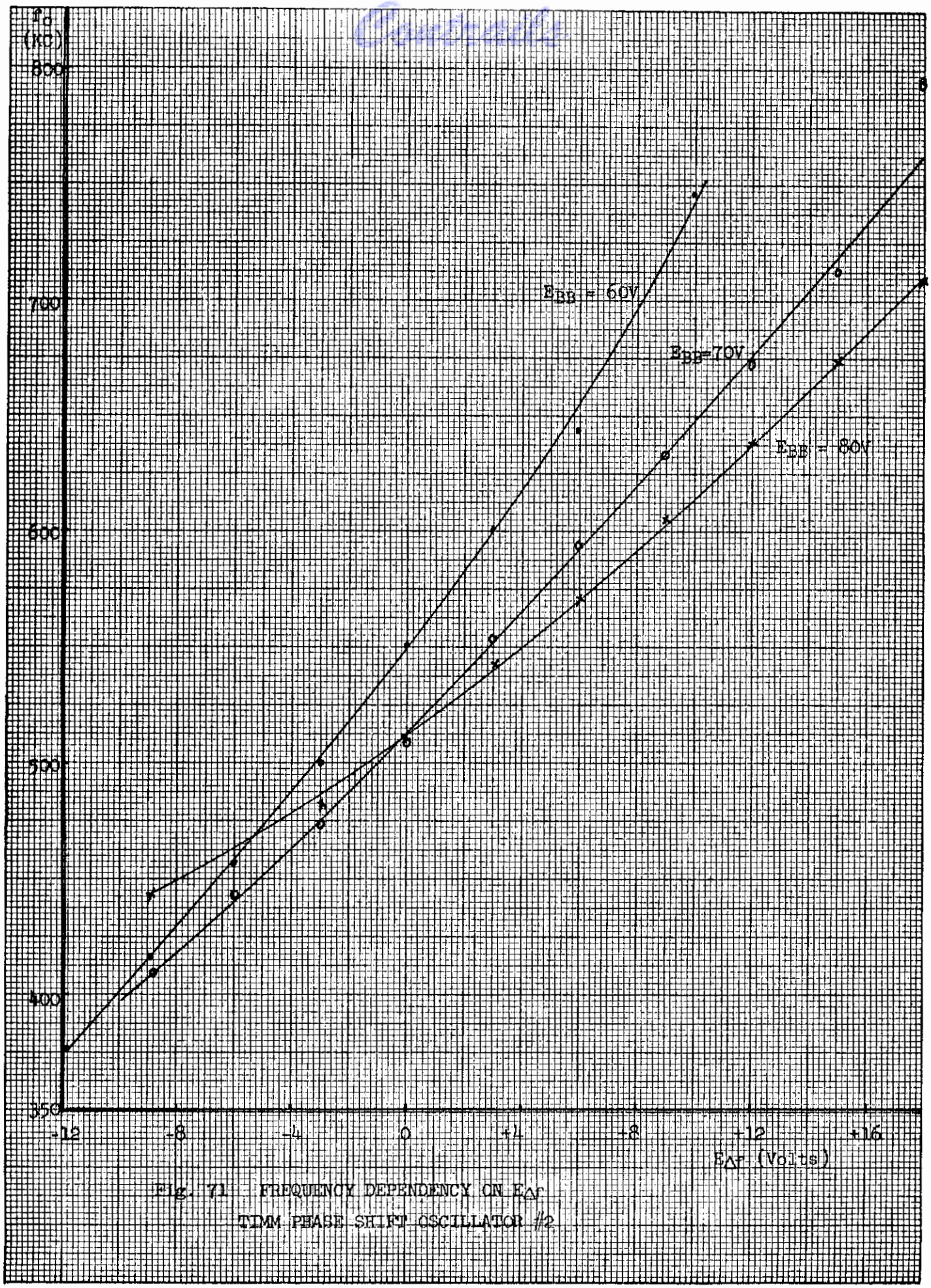



Fig. 71 FREQUENCY DEPENDENCY ON $E_{\Delta f}$

TIMM PHASE SHIFT OSCILLATOR #2

The frequency stability of both oscillators was found to be reasonably good over a period of several hours. No attempt was made to determine the stability, however. The oscillators are basic circuits which are not provided with stabilizing features; hence, stability was not considered a pertinent point when the data were taken. The oscillator is provided with degenerative D.C. feedback which could be optimized to provide good stability. The D.C. feedback is degenerative because there is, of course, no phase shift to the D.C. in the cathode followers.

The waveform of these oscillators is exceptionally good for a phase-shift circuit. If the voltage amplifier is biased toward one extreme of the operating range or the other, the waveform is a very good approximation of a sinusoid.

CATHODE FOLLOWER

Two TIMM cathode follower units were designed and constructed for the contract. The circuit diagrams for these circuits are shown in Figure 72. Figure 73 is a wiring and stacking drawing for a TIMM cathode-follower module complete with component specifications, and Figure 74 is the CF circuit board with all external pin connections identified. A photograph of a complete CF is shown in Figure 75.

The circuit is an ordinary cathode follower with the grid biased with a potential (with respect to ground) which is approximately one-half of the supply voltage. The grid was put at that high potential to extend the dynamic range of the input signal voltage so that a wide range in input signal amplitudes can be handled by the amplifiers. A blocking capacitor must be supplied at the input when testing this circuit. The TIMM cathode followers which were tested exhibited constant gain when driven by a low (600 ohms) impedance generator over a frequency range of from 100 cps to 500 KC. The gain will

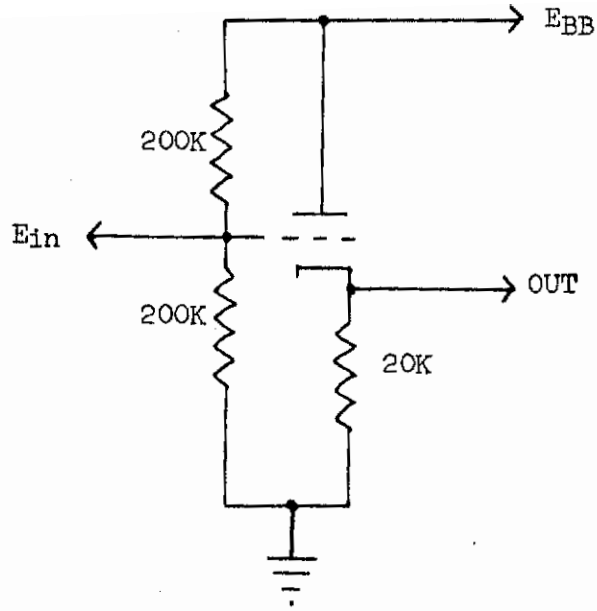
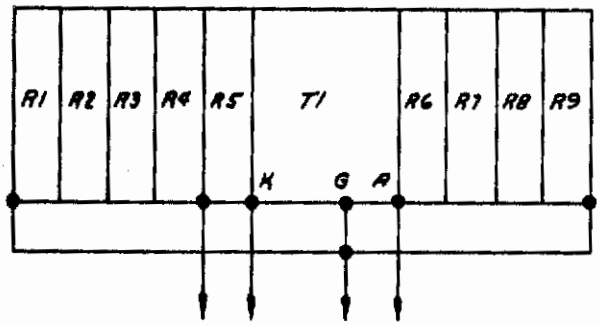
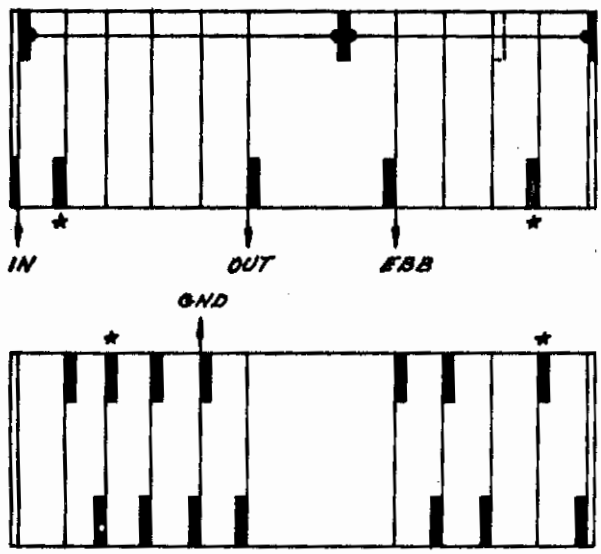



Fig. 72 TIMM Cathode Follower




Notes: ⁂ Electrodes Removed

★ Module Support Points

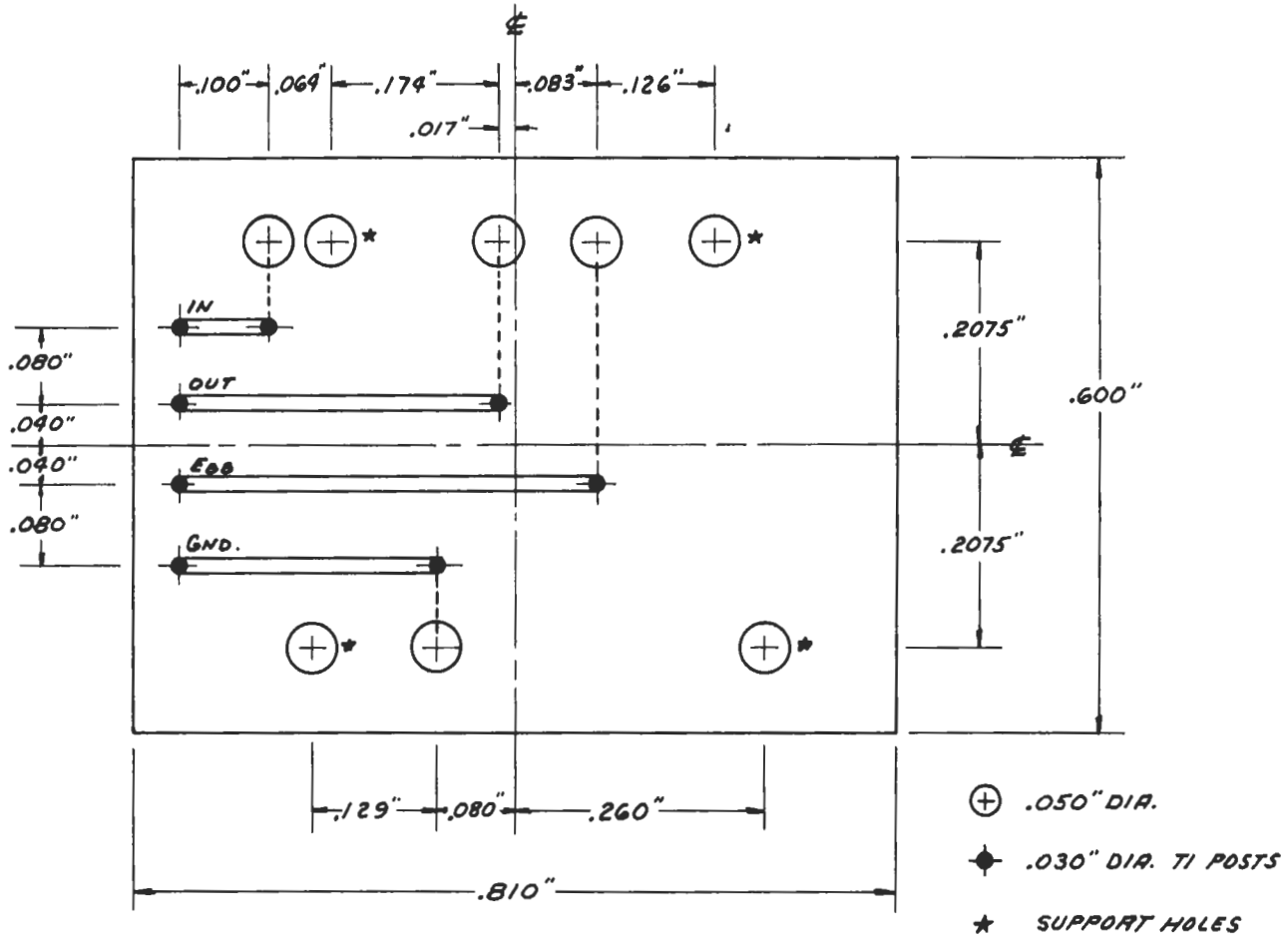
Component Specs:

$T_1$: $gm > 2000$, $\mu > 20$, $i_p > 2.0$ ma at $E_p = 60$ V, $E_g = +1.5$ V

$R_1=R_2=R_3=R_4=R_6=R_7=R_8=R_g=50K\pm10\%$

$R_5=20K\pm10\%$

Fig. 73 Wiring and Stacking Diagram for TIMM Cathode Follower




Bottom (Pin Side) View

Fig. 74 Ceramic Print Board for TIMM Cathode Follower

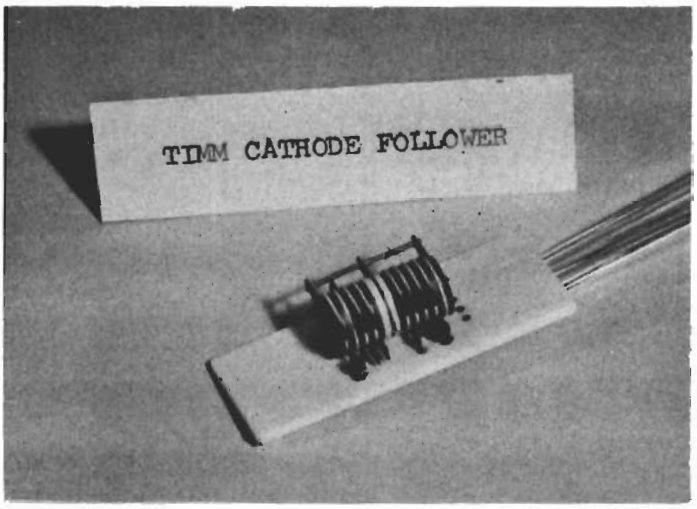



Fig. 75 TIMM Cathode Follower

roll off at the high frequency end when driven by a high impedance source due to shunt capacitances at the input. The grid voltage divider resistors were made up of eight TIMM resistors in series to minimize this reduction of input impedance at the higher frequencies. The magnitude of the input impedance of the CF circuits was measured as a function of frequency for both CF #1 and CF #2. The results are as follows: $E_{BB}$ = 100 volts, Temperature = 580°C, $e_{sig}$ = 1.0 volts rms.

| | \|Z\| in Ohms | |
|---|---|---|
| f(Kc) | CF #1 | CF #2 |
| 0.1 | 83K | 100K |
| 1.0 | 83K | 94K |
| 10 | 82K | 92K |
| 100 | 63K | 66K |
| 500 | 34K | 36K |

The dynamic output impedance of CF #1 was found to be 300 ohms, and that of CF #2, 220 ohms. When the circuits were loaded with resistors of those values (in series with 1.0 μf capacitors to block D.C.), it was found that the dynamic range was considerably narrowed so that distortion occurred with input signals exceeding 0.5 volts rms. This is normal and CF circuits generally are not loaded to that extent. Input signal levels as great as 35 volts rms can be handled by the circuits when they are lightly loaded. The gain of both circuits was constant over a wide range of input levels. CF #1 exhibits a gain of 0.95 with rms input voltages ranging from 0.5 volts to 30 volts. CF #2 exhibits a gain of 0.96 over the same range of input voltages.

SET-RESET FLIP-FLOP

Two set-reset flip flops were constructed for the contract. The circuit diagram of the circuits can be seen in Figure 76. The module wiring and stacking diagram is presented in Figure 77, along with component specifications. Figure 78 shows the circuit board with external connection pins designated to identify input leads. A photograph of a completed unit is shown in Figure 79.

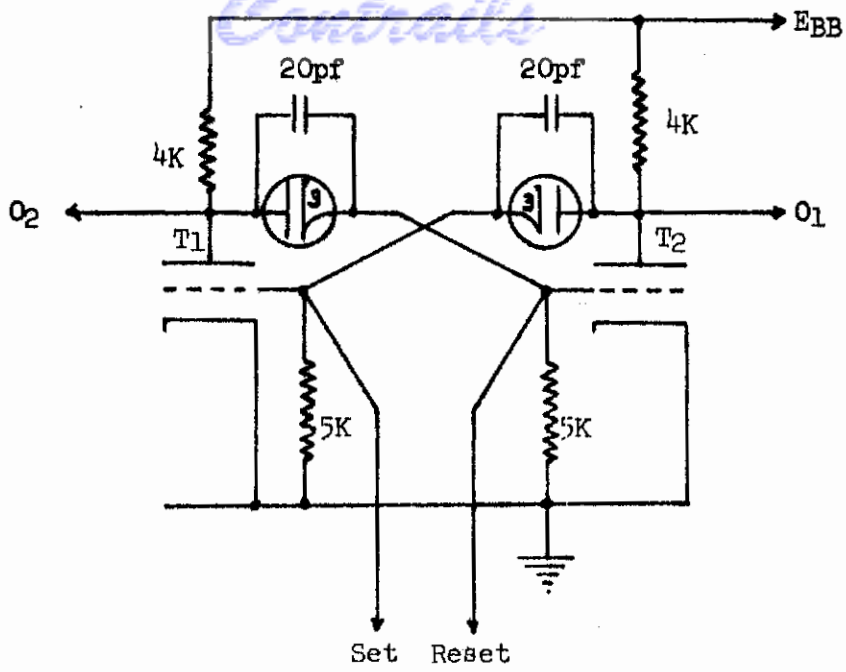
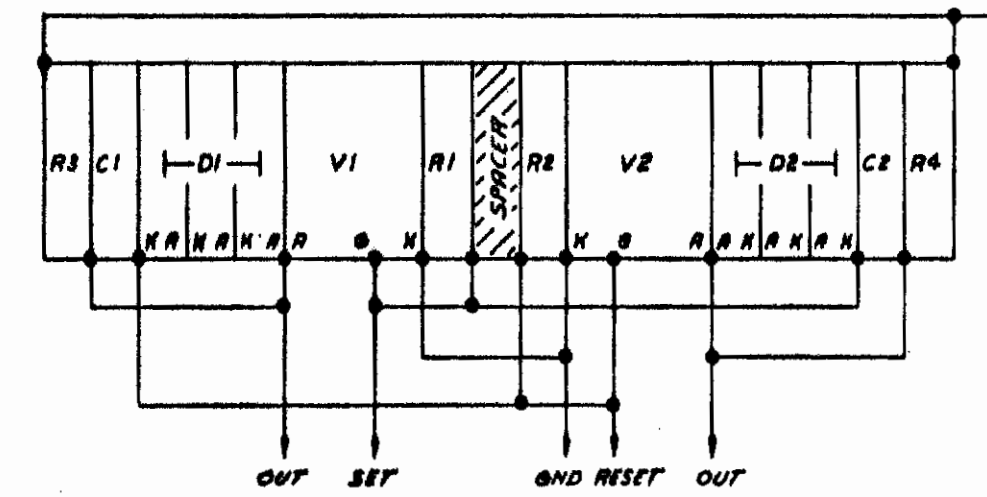



Fig. 76 TIMM Set-Reset Flip-Flop




Notes:

* Support Points
(N) 0.010 Ti Electrode

Component Specs:

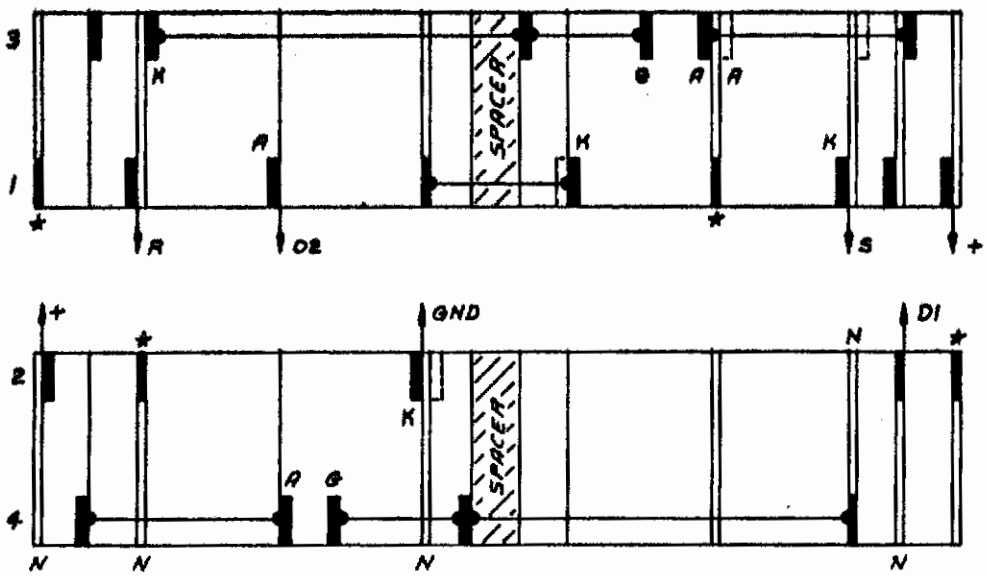
$V_1$ $V_2$: $I_p \geq 2.5$ mA at $E_p = 7$
$E_g = +2.4V$
$I_p \leq 100$ µA at $E_p = 1$
$E_g = 0V$
$I_g \leq 200$ µA at $E_p = 7$
$E_g = +2.3V$

$D_1D_2$: $E_p \geq 6.9V$ at $I_p = 50$ µ
$E_p \leq 9.0V$ at $I_p = 1$ mA

$C_1C_2$: 20 pf, ± 5%

$R_1R_2$: 5K ± 10%

$R_3R_4$: 4K ± 5%



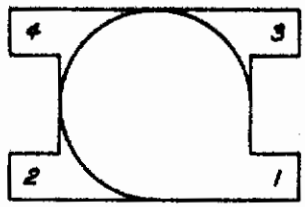
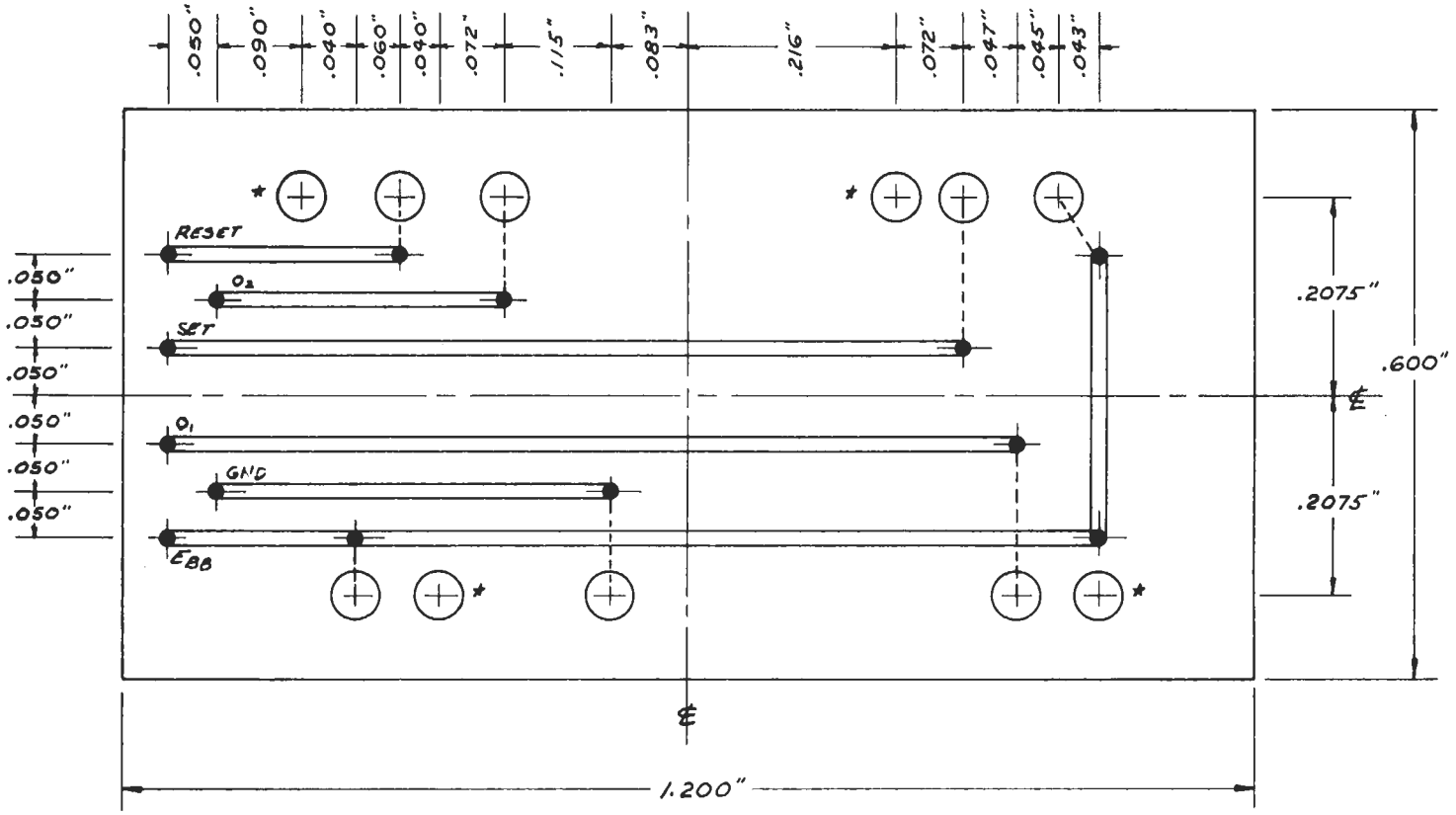




Fig. 77 Stacking and Wiring Diagram for TIMM S-R Flip-Flop




Bottom (Pin Side) View

Fig. 78 Ceramic Print Board for TIMM S-R Flip-Flop

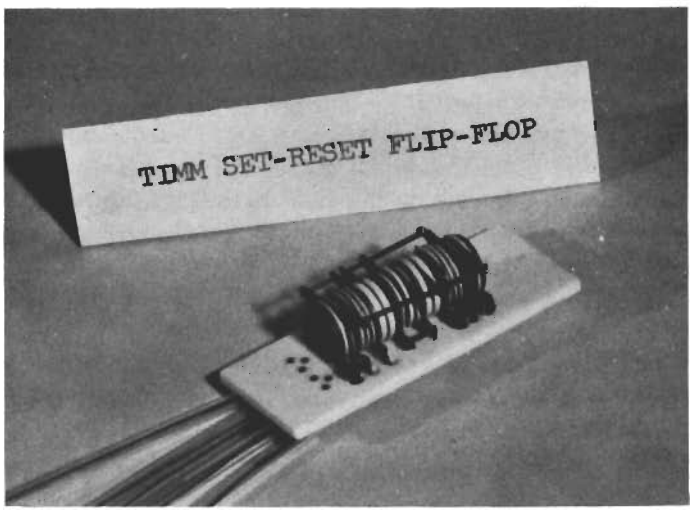



Fig. 79 TIMM Set-Reset Flip-Flop

The circuit is a basic TIMM bistable multivibrator with a trigger lead provided at each grid and an output lead at each plate. Since no isolation diodes are supplied in the input leads, they must be furnished externally if needed.

The flip-flops were tested by driving the trigger leads with pulses from two synchronized generators arranged so that one pulse could be time delayed with respect to the other. Data were taken to determine trigger sensitivity, minimum pulse spacing, output voltages and rise times and grid circuit voltages. Loading data were also taken. For all tests, $E_{BB}$ = +20 volts, Temperature = 580°C, unless otherwise stated. (See following pages).

The performance of SRFF #1 can be evaluated by examining the oscillographs of Figure 80. The photographs show the reset pulse and the resulting output from the plate of $V_1$. Photograph #1 shows the pulses for normal operating conditions of $E_{BB}$ = +20 volts, temperature = 580°C. Photograph #2 shows the performance at two different supply voltages, with temperature = 580°C in both cases. The upper portion of photograph #2 was taken with $E_{BB}$ = +15V and the lower portion with $E_{BB}$ = +25V. Note that there is very little difference in the performance of the circuit at the three voltages. Photograph #3 shows the effect of temperature changes on performance. The upper portion shows performance at normal operating conditions and the lower portion shows the result of lowering the module operating temperature to 535°C, a drop of 45°C. Note that there is some degradation of rise and fall time at reduced temperature.

The performance oscillographs of SRFF #2 are shown in Figure 81. Since these oscillographs were taken under the same conditions as for circuit #1, a description at this point is not necessary.

SRFF #1

1. Minimum Trigger:

   (a) Unloaded
   Grid $T_1$ (set) + 2.6v, 0.08μ sec. width.
   Grid $T_2$ (reset) + 2.4v, 0.08 μ sec. width.
   Minimum spacing with minimum triggers, 0.2 μ sec. with +3v triggers.
   0.12 μ sec.

   (b) Loaded with 10 K ohms from each output to B+
   Grid $T_1$(set) +2.7v, grid $T_2$ +2.6v (0.1 μ sec. width).

   (c) Loaded with 3.2 K ohms from each output to B+
   Grid $T_1$(set) +3.1v, grid $T_2$ (reset) +2.8v).

2. Plate Voltage Swing:

   (a) Unloaded

| | | |
|---|---|---|
| $E_{T_1}$ (max.) = +11.7v | $E_{T_1}$ (min.) = +5.4v | $\Delta E_{T_1}$ = 6.3v |
| $E_{T_2}$ (max.) = +11.7v | $E_{T_2}$ (min.) = +5.0v | $\Delta E_{T_2}$ = 6.7v |

   (b) Loaded with 10 K ohms from each output to B+

| | | |
|---|---|---|
| $E_{T_1}$ (max.) = +11.7v | $E_{T_1}$ (min.) = +6v | $\Delta E_{T_1}$ = 5.7v |
| $E_{T_2}$ (max.) = +12v | $E_{T_2}$ (min.) = +6v | $\Delta E_{T_2}$ = 6v |

   (c) Loaded with 3.2 K ohms from each output to B+

| | | |
|---|---|---|
| $E_{T_1}$ (max.) = +12.3v | $E_{T_1}$ (min.) = +7.4v | $\Delta E_{T_1}$ = 4.8v |
| $E_{T_2}$ (max.) = +12v | $E_{T_2}$ (min.) = +7v | $\Delta E_{T_2}$ = 5v |

3. Rise time, unloaded:

   $E_{T_1}$, tr = 0.07 μ sec. $E_{T_2}$, tr = 0.09 μ sec.

4. Fall time, unloaded:

   $E_{T_1}$, tf = 0.07 μ sec. $E_{T_2}$, tf = 0.1 μ sec.

5. Grid voltage swing, unloaded:

| | | |
|---|---|---|
| $E_{g_1}$ (max.) = +2.7v | $E_{g_1}$ (min.) = 0 | $\Delta E_{g_1}$ = 2.7v |
| $E_{g_2}$ (max.) = +2.6v | $E_{g_2}$ (min.) = 0 | $\Delta E_{g_2}$ = 2.6v |

SRFF #2

1. Minimum Trigger:

   (a) Unloaded
   Grid $T_1$ (set) +2.4v, 0.06 μ sec. width.
   Grid $T_2$ (reset) +2.4v, 0.08 μ sec. width.
   Minimum spacing 0.3 μ sec. with minimum triggers, 0.2 μ sec. with +3v triggers.

   (b) Loaded with 10 K ohm from each output to B+
   Grid $T_1$ (set), +2.5v, grid $T_2$ (reset), +2.5v, (0.1 μ sec. width).

   (c) Loaded with 3.2 K ohm from each output to B+
   Grid $T_1$ (set), +3.1v, grid $T_2$ (reset), +3.0v.

2. Plate Voltage Swing:
   (a) Unloaded

| | | |
|---|---|---|
| $E_{T_1}$ (max.) = +11.5v | $E_{T_1}$ (min.) = +5.5v | $\Delta E_{T_1}$ = 6v |
| $E_{T_2}$ (max.) = +11.7v | $E_{T_2}$ (min.) = +5.7v | $\Delta E_{T_2}$ = 6v |

   (b) Loaded with 10 K ohm from each output to B+

| | | |
|---|---|---|
| $E_{T_1}$ (max.) = +12v | $E_{T_1}$ (min.) = +6.3v | $\Delta E_{T_1}$ = 5.7v |
| $E_{T_2}$ (max.) = +13v | $E_{T_2}$ (min.) = +7v | $\Delta E_{T_2}$ = 6v |

   (c) Loaded with 3.2 K ohm from each output to B+

| | | |
|---|---|---|
| $E_{T_1}$ (max.) = +12.6v | $E_{T_1}$ (min.) = +8v | $\Delta E_{T_1}$ = 4.6v |
| $E_{T_2}$ (max.) = +13.0 | $E_{T_2}$ (min.) = +8v | $\Delta E_{T_2}$ = 5v |

3. Rise time, unloaded:

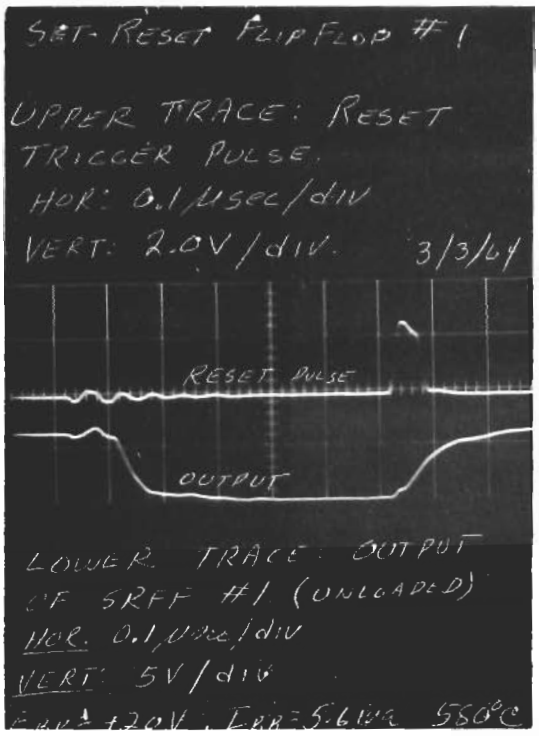
   $E_{T_1}$, tr = 0.08 μ sec., $E_{T_2}$, tr = 0.08 μ sec.

4. Fall time, unloaded:

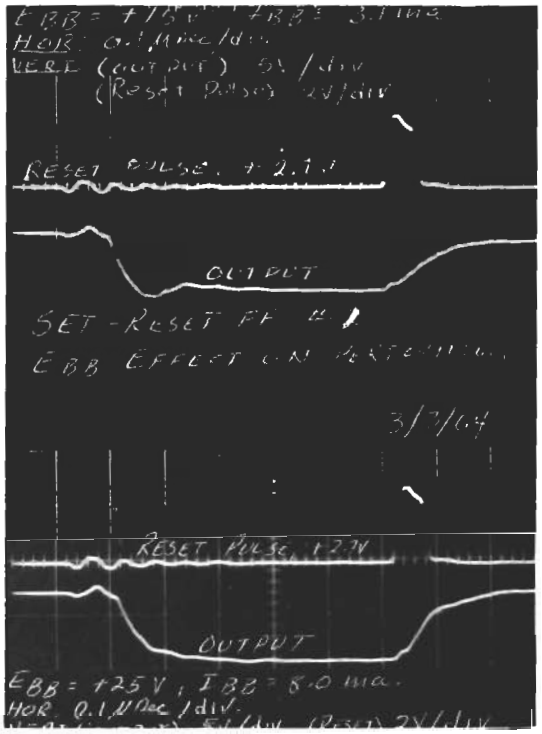
   $E_{T_1}$, tf = 0.06 μ sec., $E_{T_2}$, tf = 0.06 μ sec.

5. Grid voltage swing, unloaded:

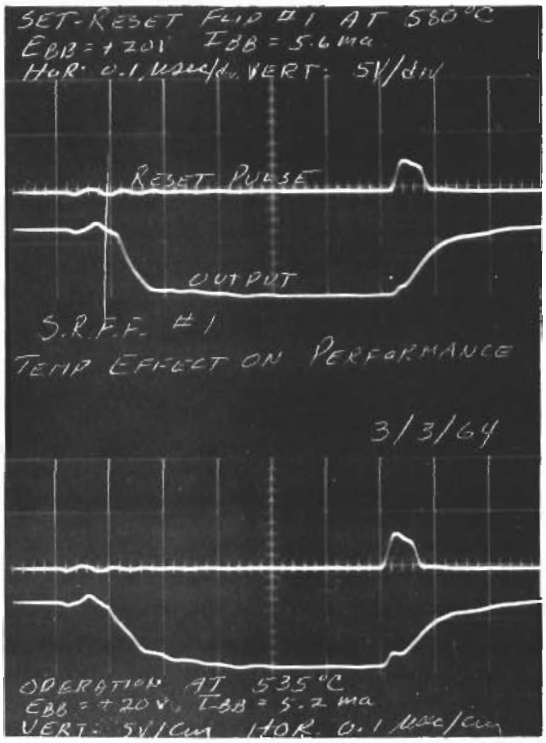
| | | |
|---|---|---|
| $E_{g_1}$ (max.) = +2.6v | $E_{g_1}$ (min.) = 0 | $\Delta E_{g_1}$ = 2.6v |
| $E_{g_2}$ (max.) = +2.5v | $E_{g_2}$ (min.) = 0 | $\Delta E_{g_2}$ = 2.5v |




Photograph #1

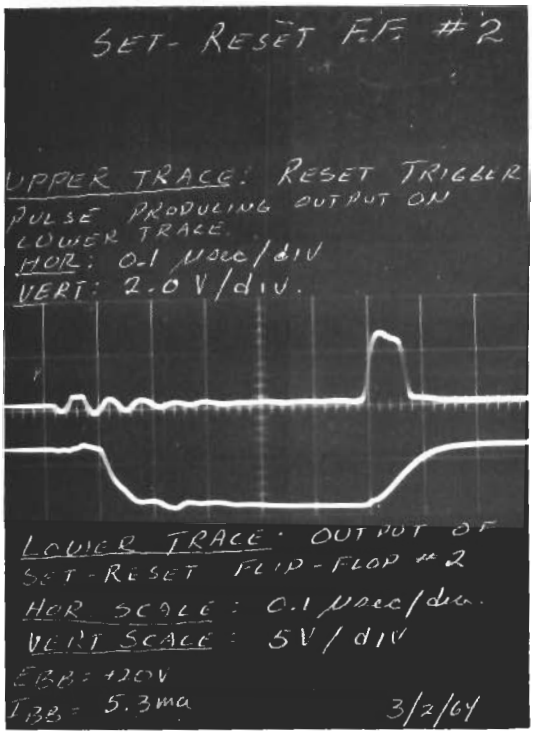



Photograph #2

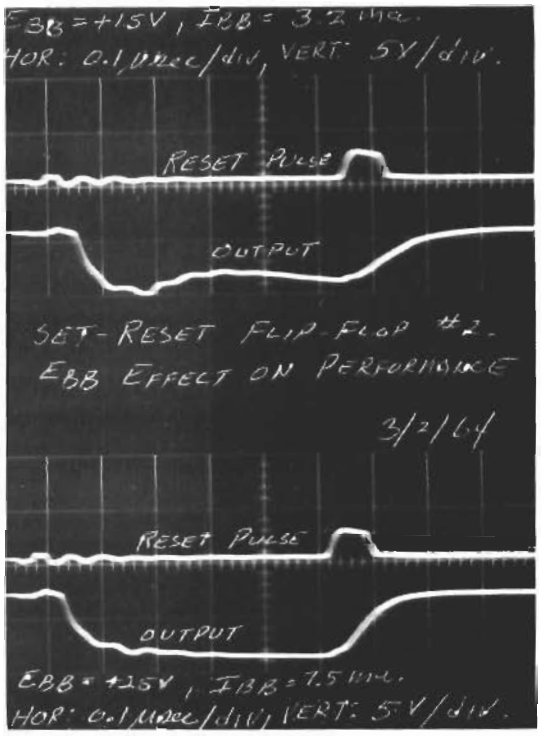



Photograph #3

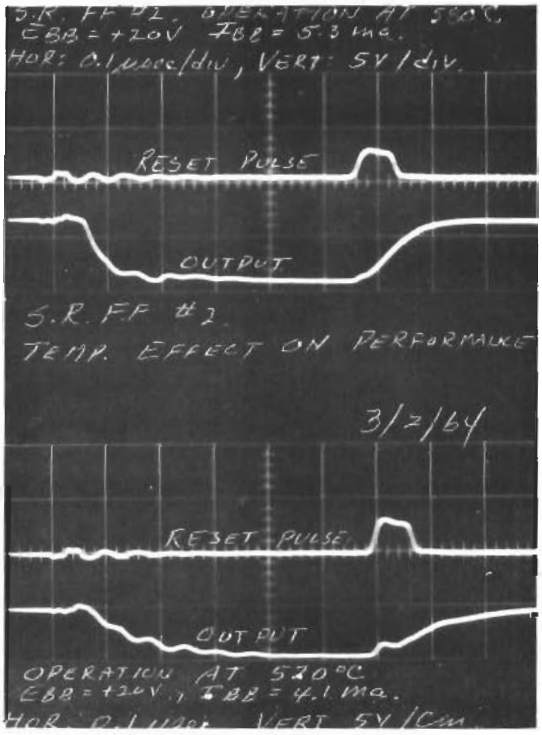
Fig. 80 Performance Oscillographs, TIMM Set-Reset Flip-Flop #1




Photograph #1




Photograph #2




Photograph #3

Fig. 81 Performance Oscillographs, TIMM Set-Reset Flip-Flop #2

## PULSED RADIATION TESTS OF TIMM CAPACITORS

TIMM capacitors were exposed at two different radiation facilities during the period of this contract. These were: (a) The 300 kv flash X-ray environment produced by the Flexitron X-ray machine at General Electric's Radiation Effects Operation in Syracuse, New York; and (b) The pure gamma and mixed neutron-gamma environment of the Linear Electron Accelerator of General Atomic, located at San Diego, California.

The same test packages were used in both tests. Each test package contained two capacitors constructed of the same material and possessing nominally the same electrical characteristics. These capacitors were wired so that the effects on each capacitor could be measured separately.

The capacitors were mounted in one end of a quartz tube with the electrical connections brought out the opposite end of the device. These devices were outgassed and evacuated to at least $10^{-6}$ torr before sealing off. An ion pump was attached to the device in order to maintain this low pressure during operation at high temperature. An ion gauge was also included in the device in order to measure the pressure at any temperature. External connections to the test device were made through RG-58 coaxial cables. The external connections between the cable and the test device were potted in paraffin to eliminate the effects of air ionization between the leads. Two balancing cables were connected to unterminated leads in the test device and served as part of a differential amplifier system designed to reduce the effects of coaxial cable transients along with the effects of radiation induced leakage in the support structure of the test package. Use of such a system greatly reduced extraneous effects leaving only the transient currents actually due to the effects of radiation on the component being tested. A photograph of this test device is shown in Figure 82.

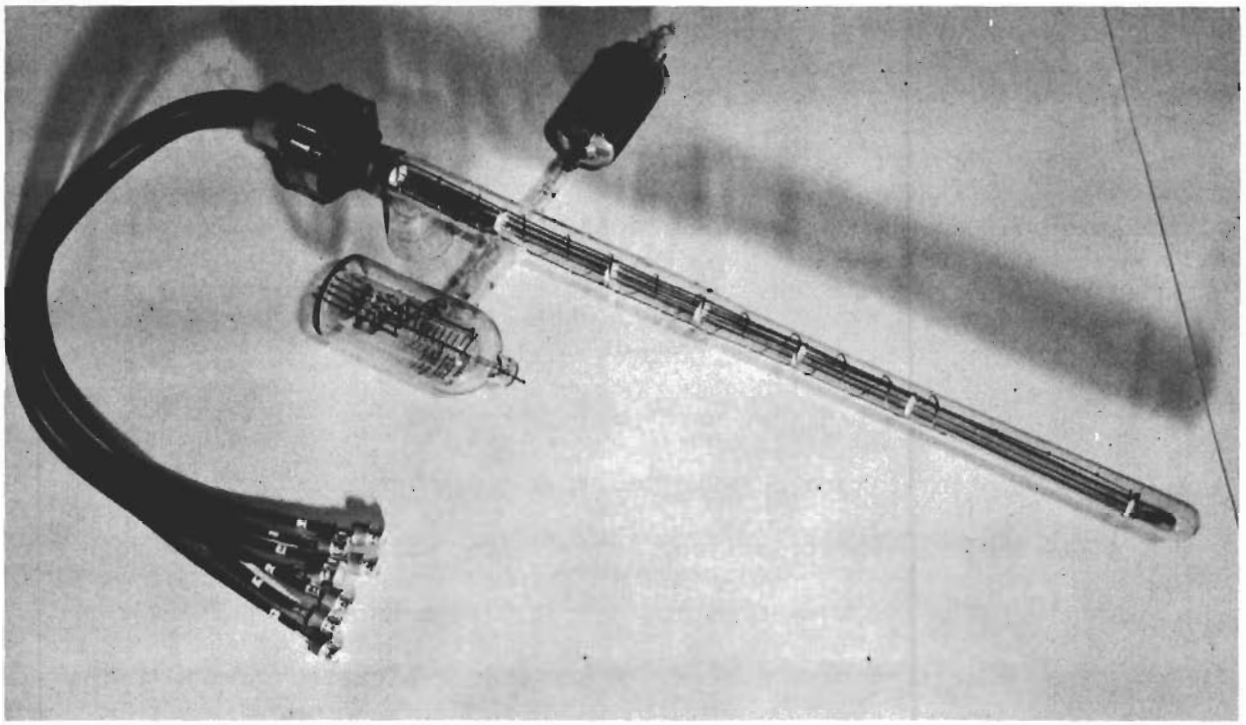


Fig. 82 Pulsed Radiation Test Device

TEST CIRCUITS

The test circuits were designed to take measurements on the capacitors under two conditions, A.C. and D.C. The purpose of the A.C. test was to detect a change in capacitance during the radiation pulse. The D.C. test was to detect a change in shunt or leakage resistance during the radiation pulse and to measure any loss of charge due to electron ejection.

The A.C. test circuit was designed to detect a change in capacitance and minimize the effect of transient conduction current. The circuit diagram is shown in Figure 83. A two-megacycle signal of 10 Vrms was impressed upon two series RC circuits. The capacitor in one RC circuit was the capacitor under test, $C_t$. The capacitor C in the second RC series circuit was a variable air

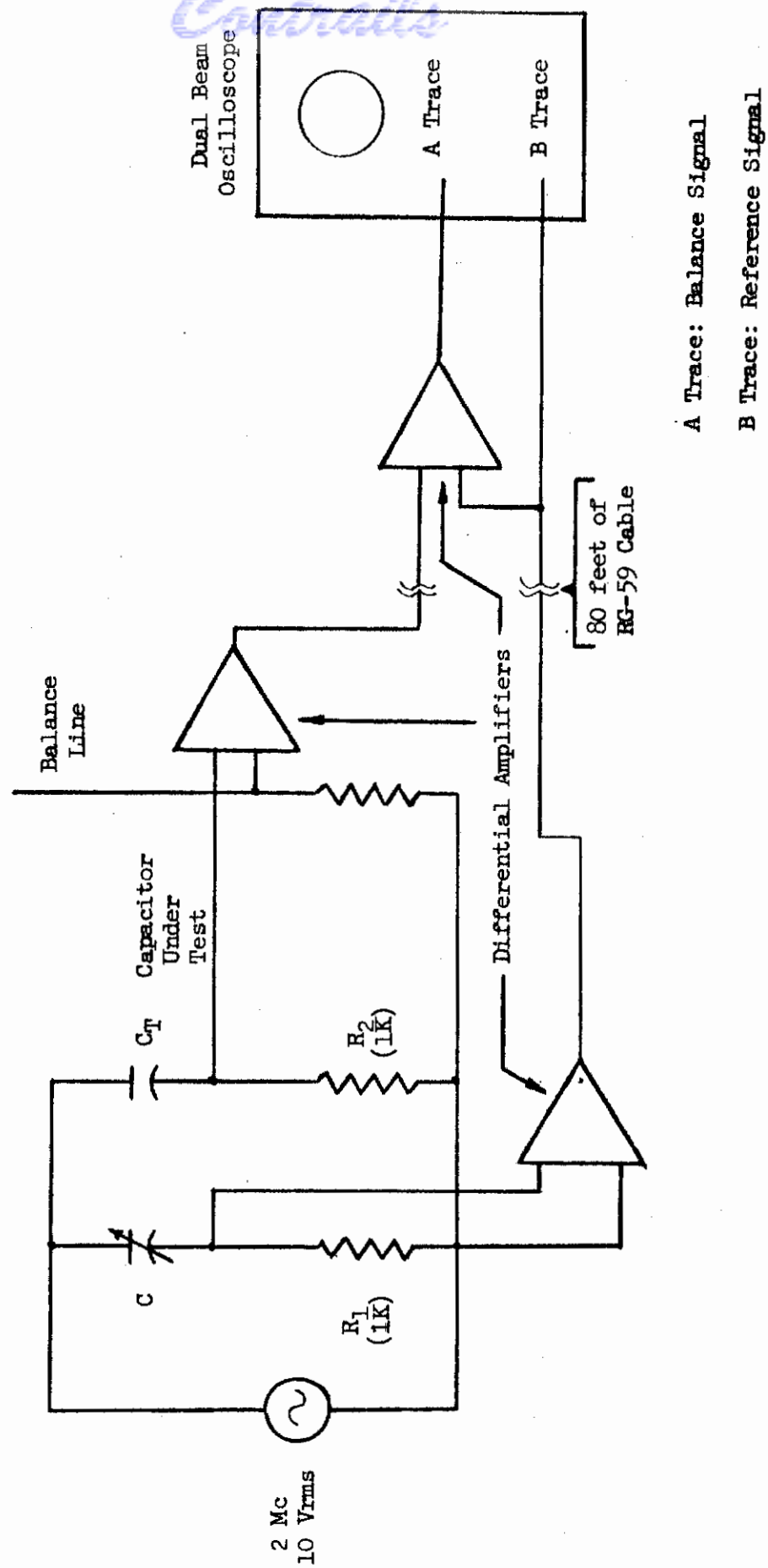



Fig. 83 A.C. Test Circuit

dielectric capacitor which was shielded from the radiation pulse. The capacitor C was varied until both the magnitude and phase of the signal across the resistor R equaled that developed across the resistor $R_2$. When the two signals were equal in magnitude and phase, the output of the differential amplifier as displayed on the oscilloscope indicated a minimum signal. If the capacitance would change due to the radiation pulse, a change in the balance signal would be seen. A comparison between the phase of the balance signal and the phase of the reference signal indicated whether an increase or decrease in capacitance occurred. The magnitude of the change in the balance signal indicated the magnitude of the change in capacitance. The circuit sensitivity was such that a change in capacitance of 0.4 picofarads could be detected. The D.C. test circuit is shown in Figure 84.

The transient current to each terminal of the capacitor was measured. The differential amplifiers subtract the stray leakage and noise currents on the balance lines from the capacitor leads thus eliminating lead effects. The two resulting signals are the currents due to the capacitor itself. An analysis of the two transient currents in the capacitor indicated the magnitude of the conduction current and also quantity of electrons ejected from or absorbed by the capacitor.

RESULTS OF FLASH X-RAY TEST

The purpose of this test was to determine the effect of the burst of radiation on certain D.C. characteristics of the capacitors. These include leakage resistance and charge ejection due to Compton scattering and photoelectric emission. The devices were exposed at both room temperature and at 580°C to determine the effect of temperature on the radiation tolerance of the capacitors. The circuit (Figure 84) designed to detect transient D.C. changes was used for this test. For the flash X-ray test, all termination resistors were 100 ohms.

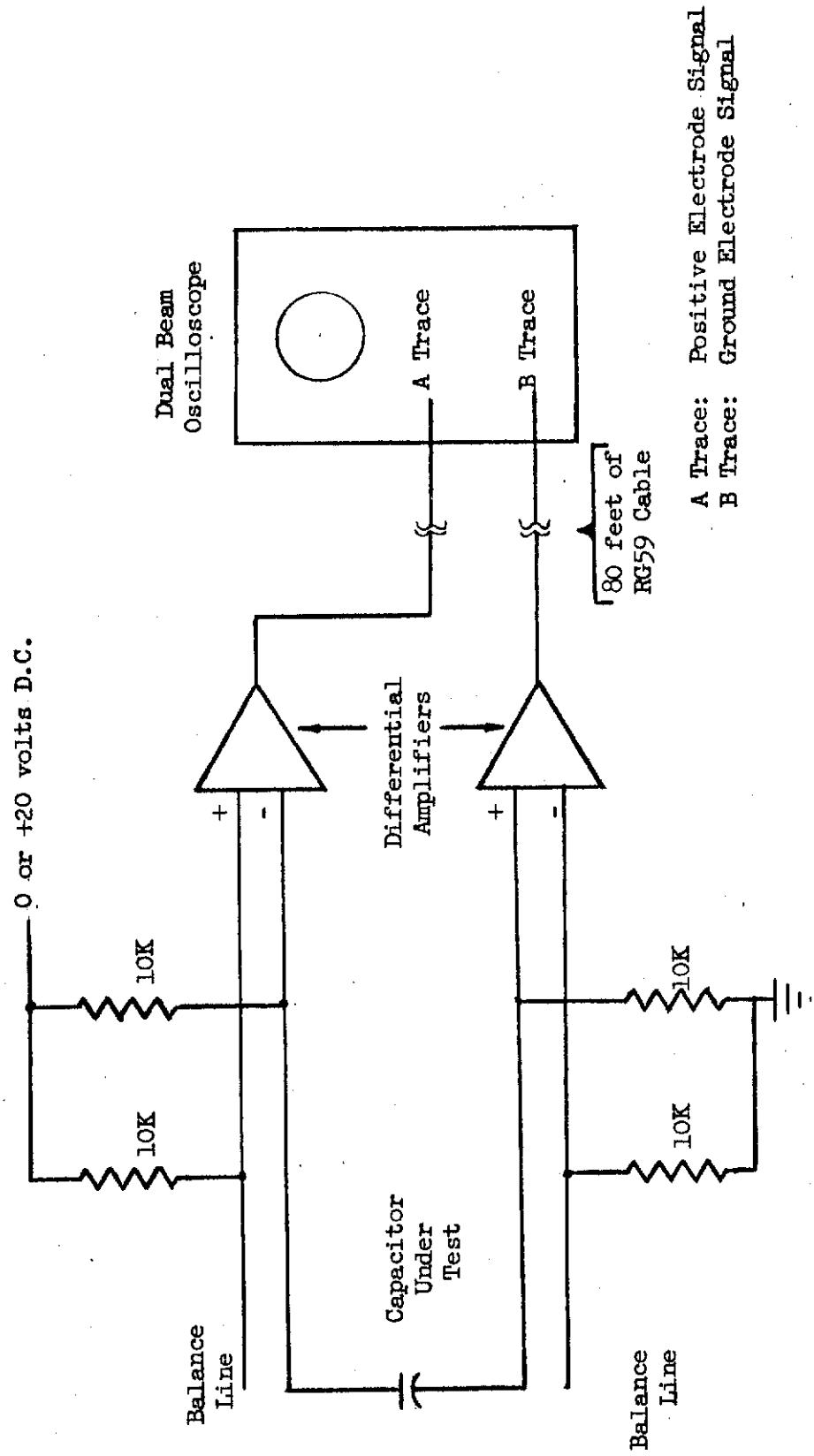



Fig. 84 D.C. Test Circuit

Two types of capacitors were exposed to the flash X-ray environment. One type, composed of OW-137 ceramic dielectric and titanium plates, had a nominal capacitance of 20 picofarads. The second type, composed of rolled mica dielectric enclosed in OW-102 ceramic with titanium electrodes, had a nominal capacitance of 400 picofarads.

No radiation-induced transient currents were observed above the electrical noise generated by the flash X-ray machine. At the time of the radiation burst, this noise level was such that no radiation-induced transient of less than 800 microamperes could be detected. A few tenths of a microsecond after the burst, the electrical noise level decreased to 80 microamperes. If a long-term radiation-induced transient occurred, it would have had to be greater than this 80 microamperes in order for it to be observed. Thus, it can be said that no prompt transient greater than 800 microamperes and no long-term transient greater than 80 microamperes could be observed.

The dose of radiation received during each burst was measured by an ion chamber placed directly in the X-ray beam but separated from the X-ray tube window by the test package and the oven assembly. The ion chamber recorded an average dose of 60 millirem. This dose was delivered in 0.1 microsecond pulses at a dose rate of $6 \times 10^5$ rad/sec. Correcting this dose rate to the position occupied by the capacitors yields a dose rate of $3 \times 10^6$ rad/sec.

RESULTS OF LINEAR ACCELERATOR TESTS

The purpose of this test was to determine the effect of the radiation on the D.C. characteristics that were studied in the flash X-ray test, viz., changes in leakage resistance and charge ejection. In addition, an effort was made to detect changes of capacitance during the burst of radiation.

Both D.C. and A.C. measurements were made at room temperature, 200°C, 400°C, and 580°C. The measuring circuits used are those shown in Figures 83 and 84.

Two different types of ceramic capacitors were tested. One type was composed of OW-133K ceramic dielectric with titanium electrodes. The second type was composed of Lucalox dielectric with niobium electrodes. As before, each test device contained two of the capacitors, which were electrically independent of each other.

At 580°C, the two OW-133K capacitors had very similar properties. The two Lucalox capacitors also had similar properties but they were not the same as the OW-133K properties. These properties are listed below:

| | $C_p$ μμf | $R_p$ Kohm | $I_c$ at 20 Vdc μamp |
|---|---|---|---|
| OW-133K #1 | 2.40 | 1300 | 0.95 |
| OW-133K #2 | 25.2 | 1100 | 1.1 |
| Lucalox #1 | 16.9 | 64 | 1.5 |
| Lucalox #2 | 16.8 | 705 | 0.2 |

The linear accelerator produced a 4.5 microsecond pulse of gamma radiation. The average photon energy is about 8 Mev. The capacitors were exposed to a gamma dose rate of approximately 4-5 x $10^7$ rads/sec.

With two inches of lead inserted between the gamma beam and the capacitors, a portion of the gamma beam is converted to neutrons. This results in a neutron dose of approximately $10^{12}$ n/cm$^2$/sec. with an energy distribution similar to that of a fission spectrum. At the same time, the gamma dose rate is reduced to 2-3 x $10^6$ rads/sec by the lead converter.

In summarizing, at the linear accelerator, the capacitors were exposed to two environments. One was a relatively pure gamma environment of 4-5 x $10^7$ rads/sec. The other was a mixed neutron-gamma environment of $10^6$ rads/sec. gamma and $10^{12}$ n/cm$^2$/sec.

There was no transient observed in the mixed neutron-gamma environment. The electrical noise level was about three microamperes during these tests. Any radiation signal above this level would have been detected. From this test, it can be concluded that the OW-133K ceramic capacitor was not affected by the mixed neutron-gamma environment. The Lucalox ceramic capacitor was not tested in this environment.

In the pure gamma environment, no change of capacitance could be detected. However, both capacitor types exhibited D.C. transient response to this environment.

At each temperature the capacitors were tested with both electrodes connected through measuring resistors to ground and then with 20 volts applied to one of the electrodes. With no voltage applied, the results are a measure of the net exchange of high energy electrons between the capacitor and the surrounding structure of the test device. With voltage applied to one electrode of the capacitor, the observed transient is due in part to the above mentioned exchange of electrons but is primarily due to radiation induced leakage currents across the capacitor.

The results of these tests are shown plotted in Figures 85, 86, 87, and 88. Figures 85 and 86 show the peak transient currents as a function of temperature for the OW-133K capacitors for applied voltage of zero and 20 volts, respectively. Figures 87 and 88 show the same information for the Lucalox capacitors.

With no voltages applied, the OW-133K ceramic capacitor showed a general decrease in transient current as temperature was increased. This is shown in Figure 85. This decrease was not apparent with the Lucalox ceramic as shown in Figure 87. Note that the magnitude of the transients plotted in Figure 87 is greater than the magnitude of the transients in

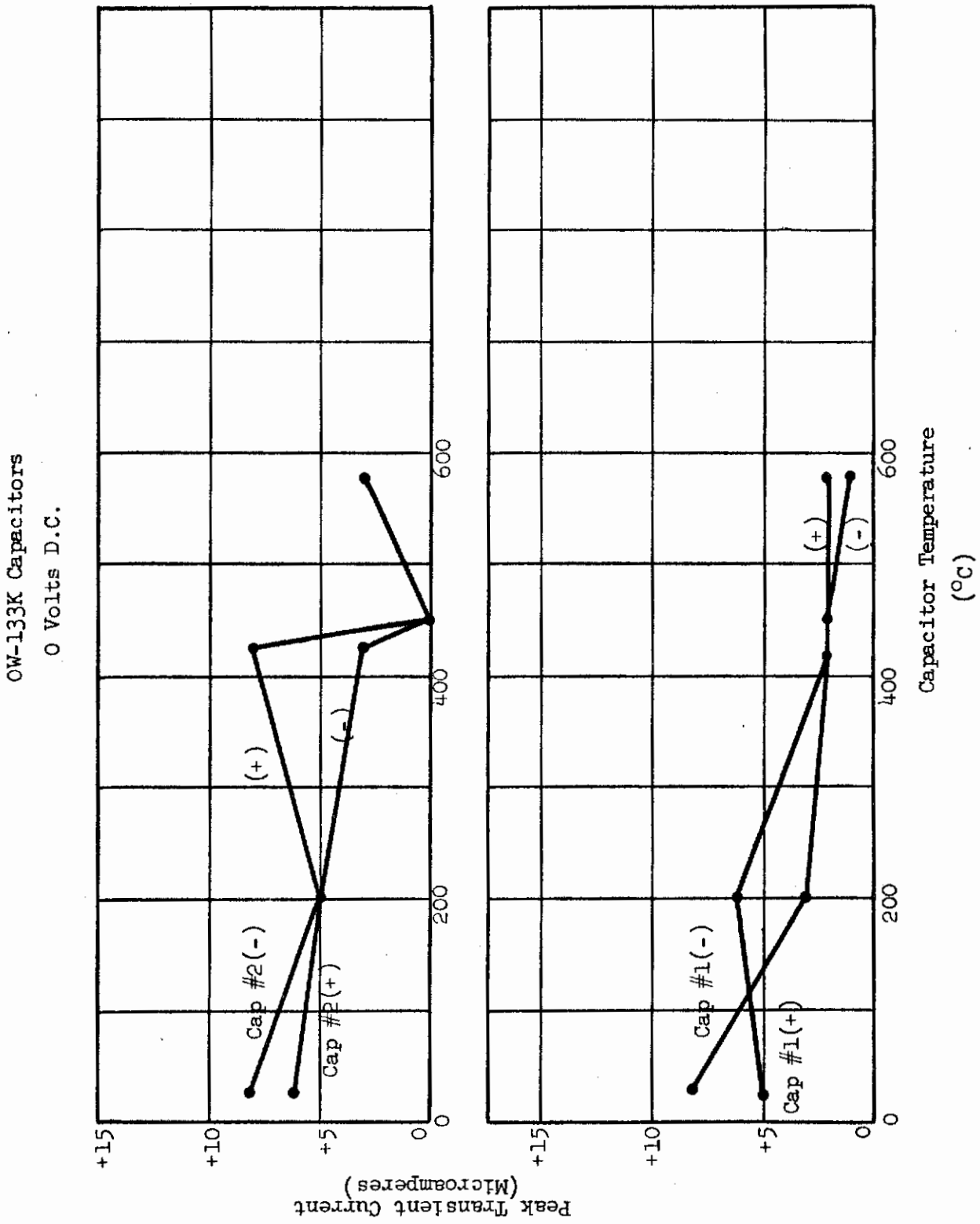



Fig. 85 Peak Transient Current Vs Temperature

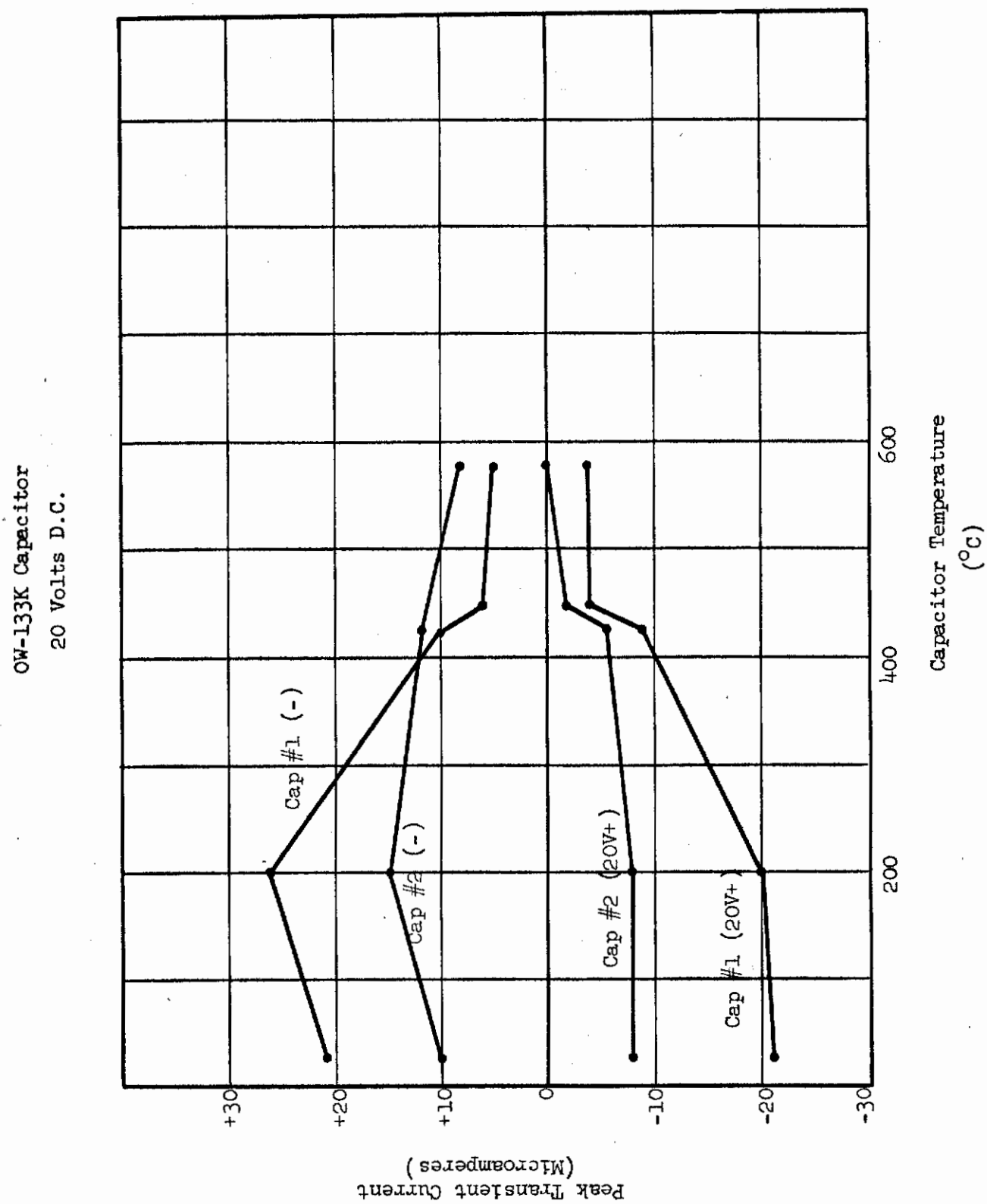



Fig. 86 Peak Transient Current Vs Temperature

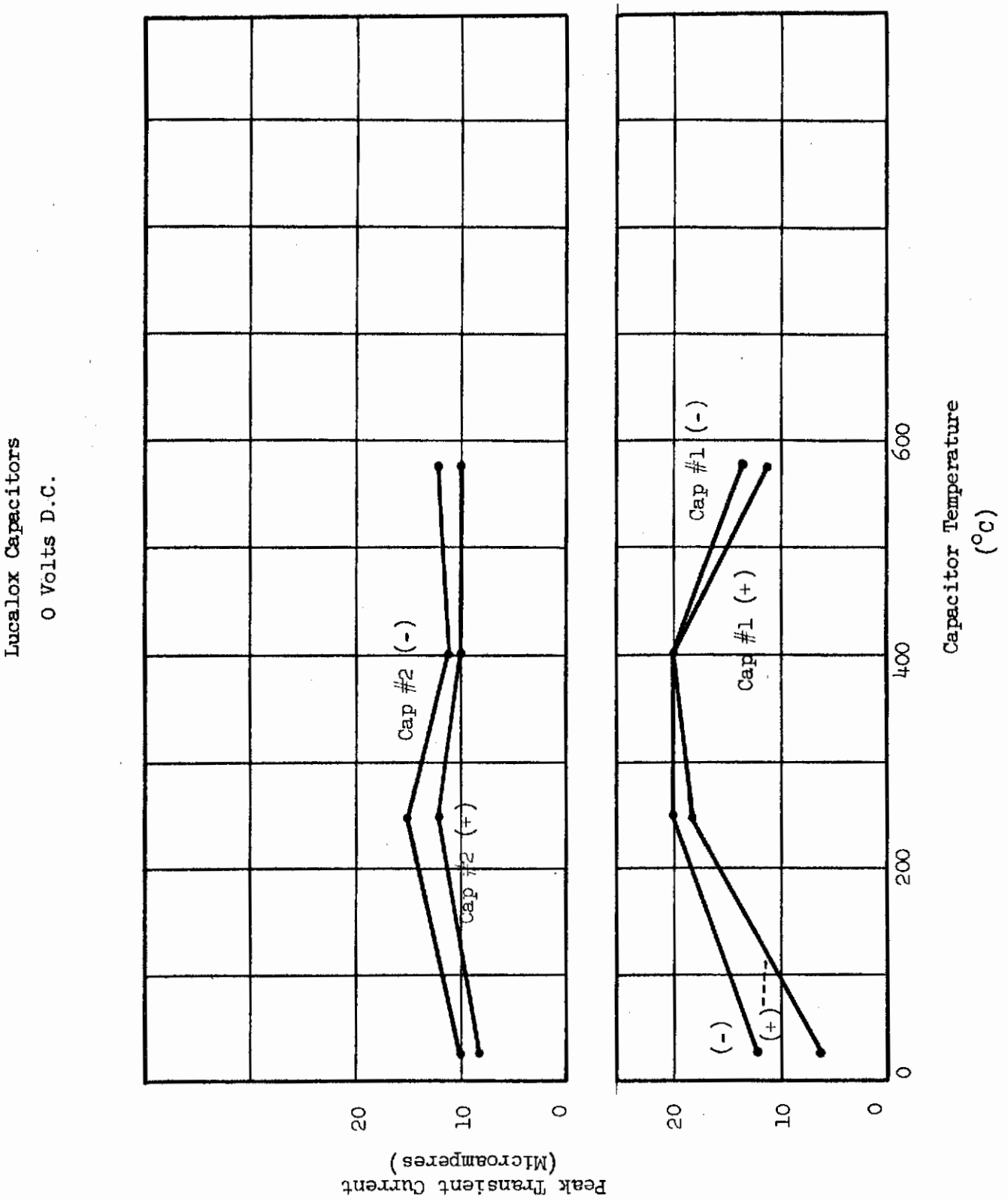



Fig. 87 Peak Transient Current Vs Temperature

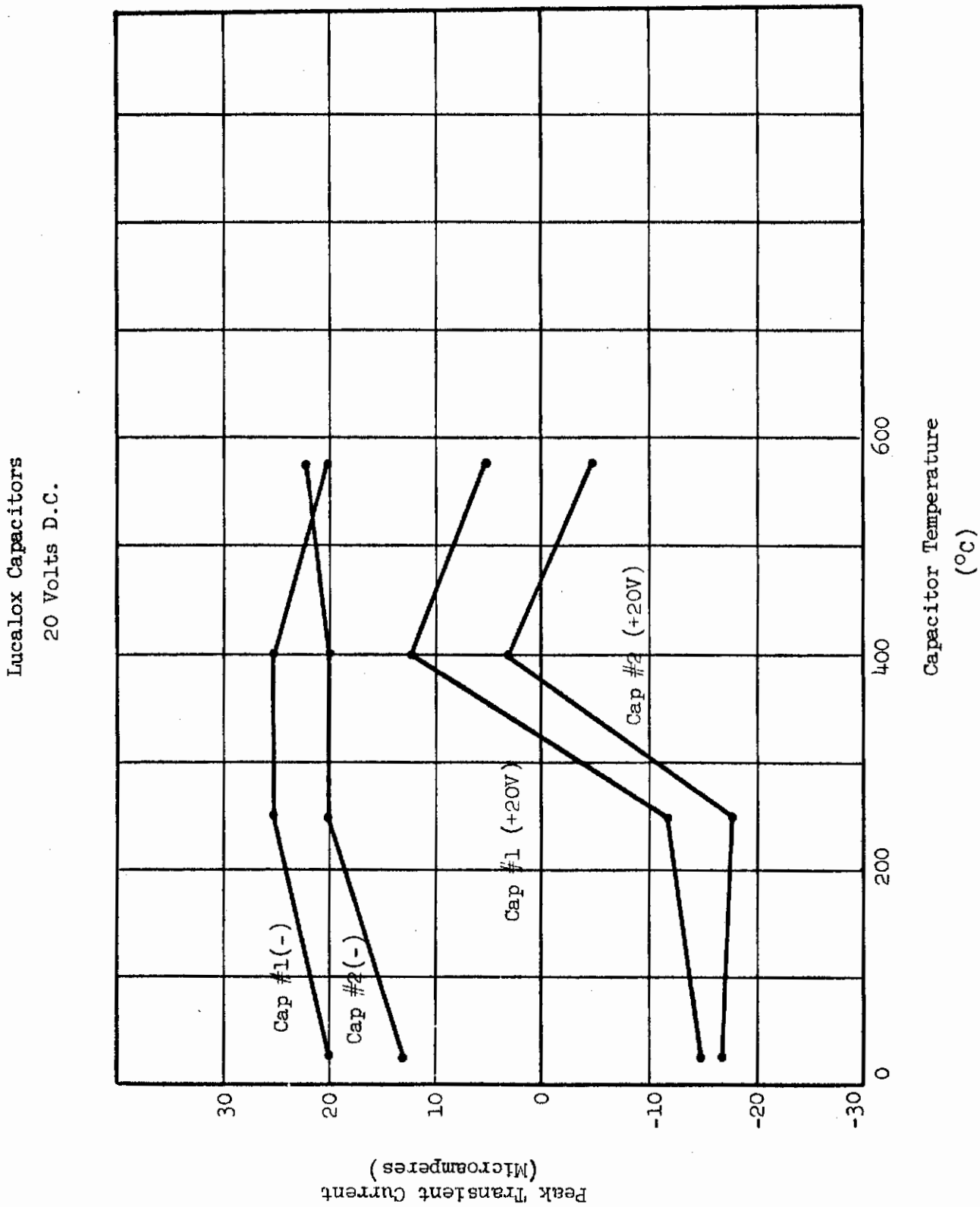



Fig. 88 Peak Transient Current Vs Temperature

Figure 85. This is thought to be due primarily to the differences in gamma attenuation coefficients of the two electrode materials. Niobium has a larger coefficient and therefore should suffer a greater loss of electrons through photoemission, Compton scattering and pair production. With 20 volts applied to the capacitors, the behavior was quite different. Both OW-133K capacitors exhibited an increase in leakage current. As the temperature was increased this leakage current decreased to a minimum at 580°C. This is shown in Figure 86. A pure leakage current would be indicated by transients on the (+) electrode (electrode to which voltage is applied) and the (-) electrode (electrode connected to ground) which are equal in magnitude but opposite in direction. The actual displacement of these transients in the positive direction is caused by the ejection of electrons from the capacitors as shown in Figures 85 and 87.

The behavior of the Lucalox ceramic capacitors at high temperature was quite different from that of the OW-133K. The variation of the peak transient current with temperature and with 20 volts applied is shown in Figure 88. These curves do not show any clear reduction in the amount of leakage current at higher temperatures. In fact, there was no clear indication of any increase in leakage current during the burst. However, the magnitude of the transient current was greater in the Lucalox ceramic capacitor than in the OW-133K ceramic capacitor. The cause of the Lucalox transient is not understood.

## CONCLUSIONS

TIMM triodes capable of low voltage operation in several types of circuits were built and proven feasible. Present state-of-the-art dictates the use of a photoetched titanium grid for optimum characteristics, in conjunction with a center support for mechanical rigidity. Cathode coating thickness was shown to be critical but more refined coating methods appear to be feasible with further efforts. Zero contact potential devices were built and proven to be satisfactory for low voltage operation.

Capacitor performance and reliability were improved through further development of the "glass-free" circuit which minimizes polarization, and through development of processing techniques which eliminates capacitor leakage effects.

The development of a technique for making an advanced stacked capacitor was begun and exhibited promise of making possible a substantial size reduction.

Module assembly, interconnection and mounting techniques were improved through further development. A resistance braze technique was developed which eliminated the apparent shelf life problem with earlier modules. Techniques for depositing metallized interconnects on module boards and welding module lugs to shield anchor pins on the boards show promise of reducing module board processing time by as much as 50%. Module seal reliability was improved through the development of a dry-pressed shim technique for making titanium-to-titanium seals.

Two each of five different TIMM circuit modules were designed, constructed and tested. All of the circuits are useful functions for computer use as well as many other systems. The test data showed the circuits to be

good solid electronic units. The circuits are compatible with each other in operating conditions and driving capability.

The diode matrix is a versatile unit which has many uses. The TIMM NAND gate is capable of a good fanout ratio of about 8:1. Its rise and fall times are fast enough to allow its use in a medium speed computer system and its output "one" to "zero" differential is completely non-ambiguous. The phase shift oscillator is a voltage tunable signal generator which may be used as a clock generator or as a signal source which may be frequency modulated. It may also be used as a two or four phase signal source by taking outputs from appropriate points in the circuit.

The TIMM set-reset flip-flop exhibits exceptionally fast rise and fall times and is capable of driving other flip-flops, gates or a circuit such as the TIMM diode matrix. The cathode follower has such uses as circuit isolation and impedance matching.

In general, then, it has been demonstrated that the TIMM concept is adaptable to the electronic needs of a system such as a digital computer. The versatility in addition to the inherent radiation tolerance of the components of TIMM makes the TIMM approach ideally suited for military electronics applications.

TIMM capacitors composed of OW-137 ceramic and of rolled mica were exposed to a flash X-ray environment of $3 \times 10^6$ rads/sec. No transient effects were observed above the noise level of the machine.

TIMM capacitors composed of OW-133K and of Lucalox exhibited slight transient effects when exposed to a pure gamma environment of a linear accelerator of $4\text{-}5 \times 10^7$ rads/sec. In the OW-133K ceramic, the magnitude of the leakage current transient decreased as the temperature of the capacitor was increased. The Lucalox ceramic transient showed very little temperature dependence.

## 1.0 Follow-on Research and Technology Program

Progress, particularly under the U. S. Air Force sponsored TIMM Research and Technology Programs, has been rapid, and the basic TIMM concept has been proven feasible. This Research and Technology Program, however, has been defined problems where continued exploratory studies are needed to further develop existing basic functional circuit components and to extend the TIMM system into other areas where application of this unusual high temperature radiation tolerant approach has not been fully explored.

Individual active and passive circuit elements have been successfully constructed, assembled into modules and operated as integrated digital type electronic circuitry. There still remains the necessity to extend the performance capability of these active and passive elements and to extend the over-all concept of high temperature components into the areas of functional multistructure devices; pentode type construction; digital memory applications; power devices; and circuitry applications, such as radio frequency circuitry, analog-to-digital conversion and power output. Specific follow-on Research and Technology Programs necessary to accomplish these objectives are detailed below:

1.1 Extend performance characteristics of TIMM active circuit elements.

1.1.1 Complete development of zero contact potential devices needed to improve efficiency of digital circuitry.

1.1.2 Determine basic deterioration mechanisms of emission and contact potential. Relate effect of life conditions on emission level deterioration and improve process control and device reliability.

1.2 Develop active circuit elements required for high speed computer applications.

1.2.1 TIMM power diode.

1.2.2 TIMM pentodes - small signal and power.

1.2.3 High temperature tubes for hybrid circuits.

1.3 Develop advanced TIMM active circuit elements to increase performance without a proportionate volume increase and/or decrease volume without sacrificing performance.

1.3.1 Develop structural electrode assemblies, i.e., titanium coated, composite and thin film.

1.3.2 Determine feasibility of advanced active circuit element configurations, such as cylindrical structures.

1.3.3 Determine feasibility of multifunctional devices to reduce cost and component volume.

1.4 TIMM Resistors

1.4.1 Develop power resistors required for high power circuitry, such as the inverter.

1.4.2 Evaluate power dissipation of the 0.3" design in a modular structure and establish dissipation ratings related to circuit parameters. Determine factors leading to performance improvements permitting dissipation of 0.5 watts. These programs are necessary for more effective circuit design.

1.4.3 Extend and improve high frequency performance of resistors. This work is needed for high speed digital circuitry applications.

1.4.4 Develop variable resistors required for circuit adjustment.

1.5 TIMM Capacitors

1.5.1 Develop capacitors using high resistance material (OW-133 ceramic) for improved dielectric constant and elimination of polarization. Determine the frequency-temperature response.

1.5.2 Develop metallized electrode system eliminating the external lug arrangement to improve both space factor and component reliability.

1.6 Inductors

1.6.1 Conduct exploratory work to extend the capabilities of inductors for circuit applications.

1.7 Component and Module Research

1.7.1 Study and improve electrode and module interconnection designs to increase the usefulness of standardized components to improve efficiency of utilization.

1.7.2 Develop techniques for assembly of modules, module board construction and interconnections, and establish shock and vibration tolerances of both modules and module board assemblies.

1.7.3 Evaluate new materials, such as the Nb-Lucalox system, to provide higher temperature tolerances and possibly higher radiation tolerance.

1.8 New Circuit Applications

1.8.1 Develop analog-to-digital conversion circuit so that application base of the TIMM system may be extended.

1.8.2 Establish requirements and investigate designs for RF high power circuitry typical of airborne system power supply. This type of circuitry could also be used for driving indexing selenoids and for reactor controls.

1.8.3 Establish design parameters for radiation tolerant hybrid systems for high frequency (RF) circuitry utilizing heated cathode ceramic tubes, TIMM components, inductors and variable components for operation for -65 to 300-400°C.

1.8.4 Develop variable capacitor and inductor circuit elements for operation in the TIMM environment.

1.9 Environmental Testing

1.9.1 It will be necessary to conduct both radiation and life tests on all components developed in the programs above which utilize materials and/or configurations other than those which have been evaluated.

1.9.2 Conduct radiation tests on modules and circuit subassemblies.

1.9.3 Life test modules and circuit subassemblies under temperature and vacuum conditions which simulate ultimate computer package conditions.

1.9.4 Evaluate new components and modular assemblies for shock and vibration resistance under typical operating conditions (See 1.7.2 above).

1.10 Interface Studies

The TIMM concept foresees a system package in which a number of circuits and subassemblies are hermetically sealed in a vacuum enclosure. Several such packaged subsystems might be involved in a radiation hardened system. To interconnect between such packages in the system, it will be necessary to consider temperature gradients and radiation tolerance for the interface region between one hermetically sealed package and another. Within the sealed packages, additional interface problems exist involving thermal insulation, lead-through density and associated thermal losses.

1.11 Memory

Consider various computer memory components for possible application to the TIMM concept. Recognizing that high density high speed computer component systems require compatible memory components, we propose to research this area to determine the potential of:

1.11.1 Magnetic core and drum.

1.11.2 Sonic delay line.

1.11.3 Saturable core at intermediate temperature operation and with EM pulse shielding.

1.11.4 Thin film memory techniques.

Recommendations will be made based upon these studies.

1.12 Switches

Develop functional switches required for application to the TIMM concept and for application in hardened hybrid circuits.

1.13 Temperature sensing and Control Devices

Develop temperature sensing and control devices for the TIMM computer equipment packages.

1.14 Module and Computer Package Heaters

Develop heater for TIMM modules and computer equipment packages.

2.0 Manufacturing Methods for Thermionic Integrated Micromodules

A Manufacturing Methods Program is needed to provide for development of manufacturing knowledge, equipment and methods for timely and economical production of a family of radiation resistant high temperature electronic devices (diodes, triodes, resistors, capacitors for digital computer service). To transition TIMM devices from their present stage of development to production status, equipment and methods for a number of processes must be considered with the objective of determining equipment and methods of processing which are adaptable to efficient and reproducible operations.

In addition to the Circuit Element Manufacturability Program, a TIMM Equipment Applications Technology Program should be carried out in parallel so that the Circuit Element Program may benefit from the interplay of problems and solution of the Applications Technology Program. The parallel tasks would result in more nearly optimum tradeoffs between system and component design parameters, thus enhancing the economy (of both time and money) of the manufacturing methods program.

## APPENDIX I

This report covers a compilation of the data collected to March 1, 1964, on three capacitor life tests which were started during the contract reporting period of December, 1963, and January, 1964. The tests are listed below:

(1) 20 Volts squarewave at 15 KC and 0 volts bias, OW-133K, temperature 580°C.

(2) 20 Volts squarewave at 15 KC and 0 volts bias, OW-137, temperature 580°C.

(3) 200 Volts D.C., OW-137, temperature 580°C.

### 20 VOLTS SQUAREWAVE AT 15 KC AND 0 VOLTS BIAS, OW-133K

Ten OW-133K single plate units (nominally 17 picofarads) were originally put on test. One unit proved inoperative at start-up due to a broken lead. At the end of 500 hours, the none units were operating satisfactorily. The average D.C. resistance was 3400 megohms, dissipation factor was .005, and there was no change in capacitance at the end of 500 hours.

Ten OW-133K stacked plate units (nominally 36 picofarads) were originally put on test. One unit was inoperative at start-up due to a broken lead. At the end of 500 hours, these nine units were still operating satisfactorily. The average D.C. resistance was 1400 megohms, dissipation factor was .002, and there was no change in capacitance at the end of 500 hours.

Capacitance and dissipation factor are plotted versus time in Figure 89. D.C. resistance is plotted versus time in Figure 91.

### 20 VOLTS SQUAREWAVE AT 15 KC AND 0 VOLTS BIAS, OW-137

Ten OW-137 single plate units (nominally 20 picofarads) had an average D.C. resistance of 417 megohms, a dissipation factor of .019, and exhibited an increase in capacitance of 2.38% at the end of 1,500 hours.

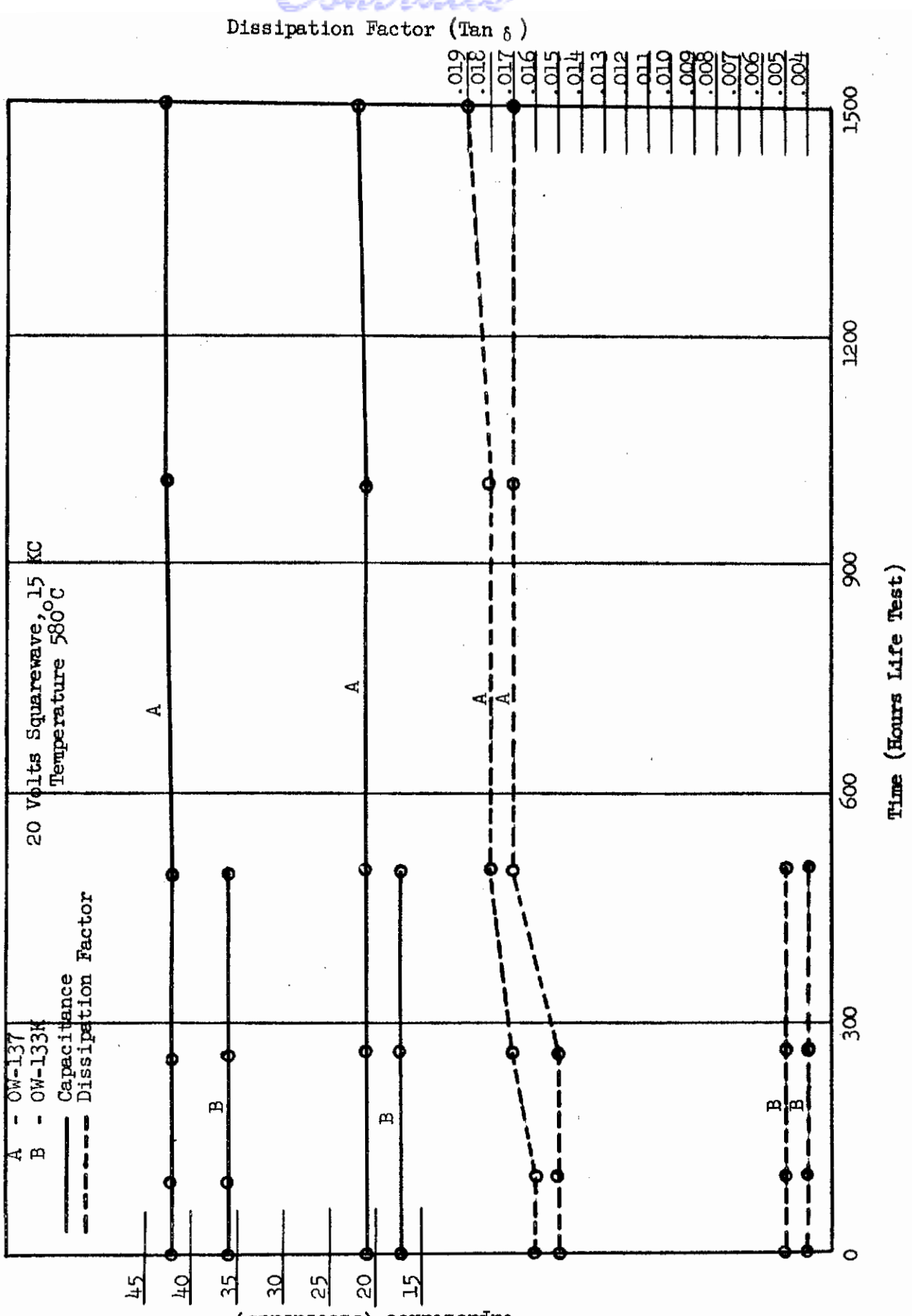



Fig. 89 Capacitor Life Test Data

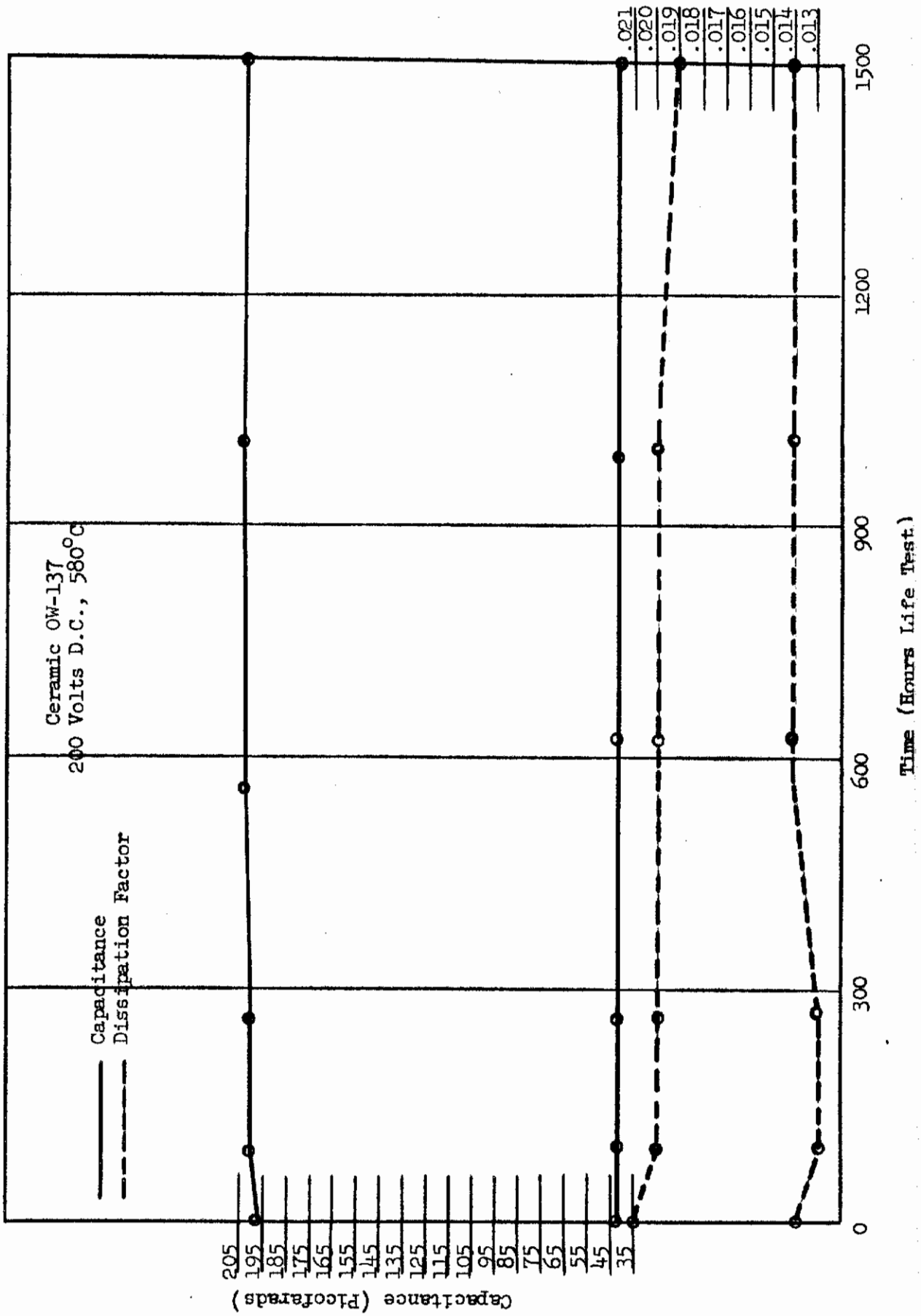



Fig. 90 Capacitor Life Test Data

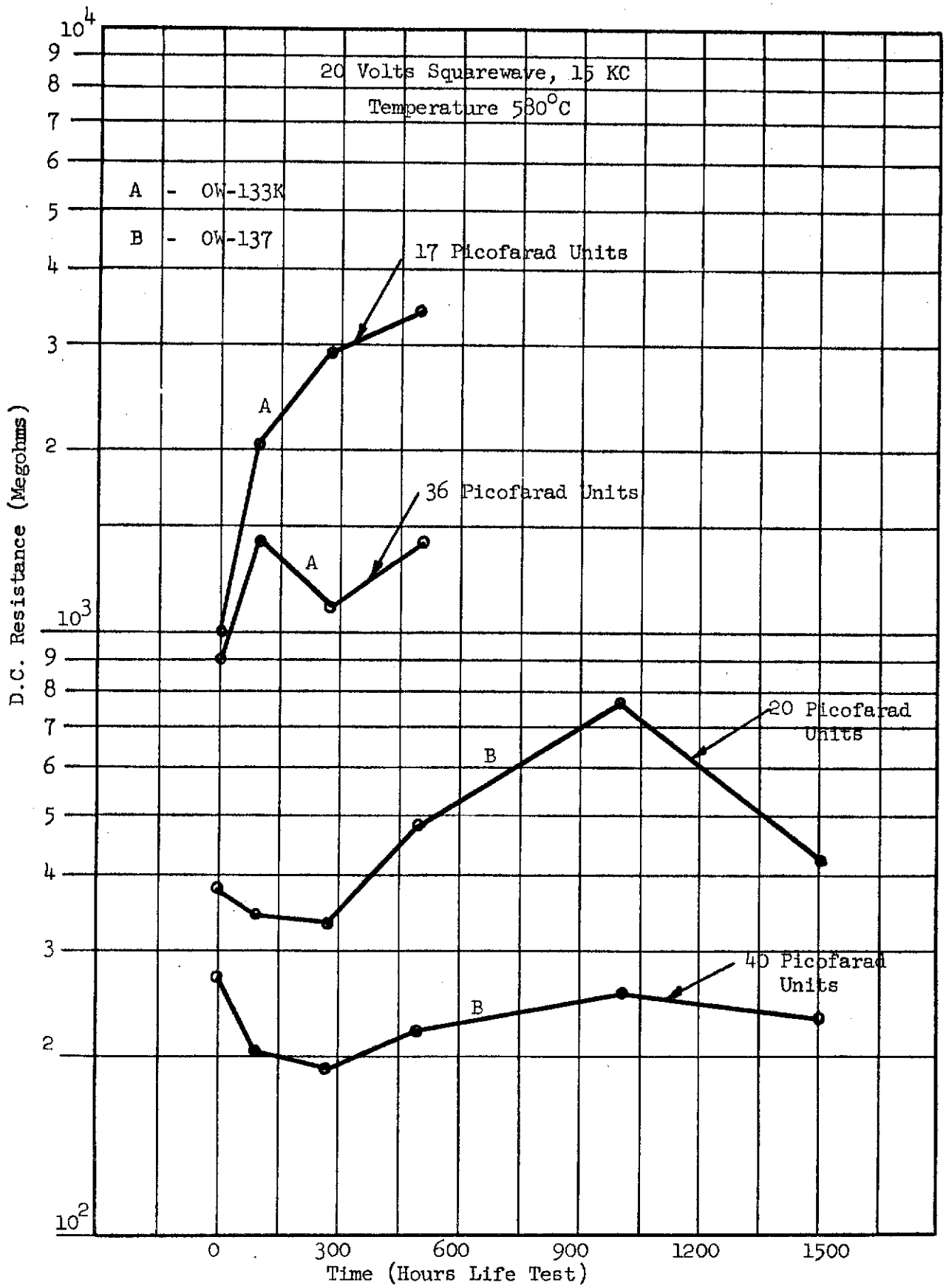



Fig. 91 Capacitor Life Test Data

Ten stacked plate units (nominally 40 picofarads) had an average D.C. resistance of 226 megohms, a dissipation factor of .017, and exhibited an increase in capacitance of 2.38% at the end of 1,500 hours.

Capacitance and dissipation factor are plotted versus time (hours life test) in Figure 89. D.C. resistance is plotted versus time in Figure 91.

200 VOLTS D.C., OW-137

Ten stacked plate units (nominally 40 picofarads - 2 five mil plates) on test had an average D.C. resistance of 4,700 megohms, a dissipation factor of .014, and exhibited an increase of 2.38% in capacitance at the end of 1,500 hours.

Nine 200 picofarad units (10 five mil plates) on test had an average D.C. resistance of 6,700 megohms, a dissipation factor of .019, and exhibited an increase in capacitance of 2.52% at the end of 1,500 hours. There was one failure at 96 hours which was due to a low D.C. resistance (less than 1 megohm).

Capacitance and dissipation factor are plotted versus time (hours life test) in Figure 90. D.C. resistance is plotted versus time in Figure 92.

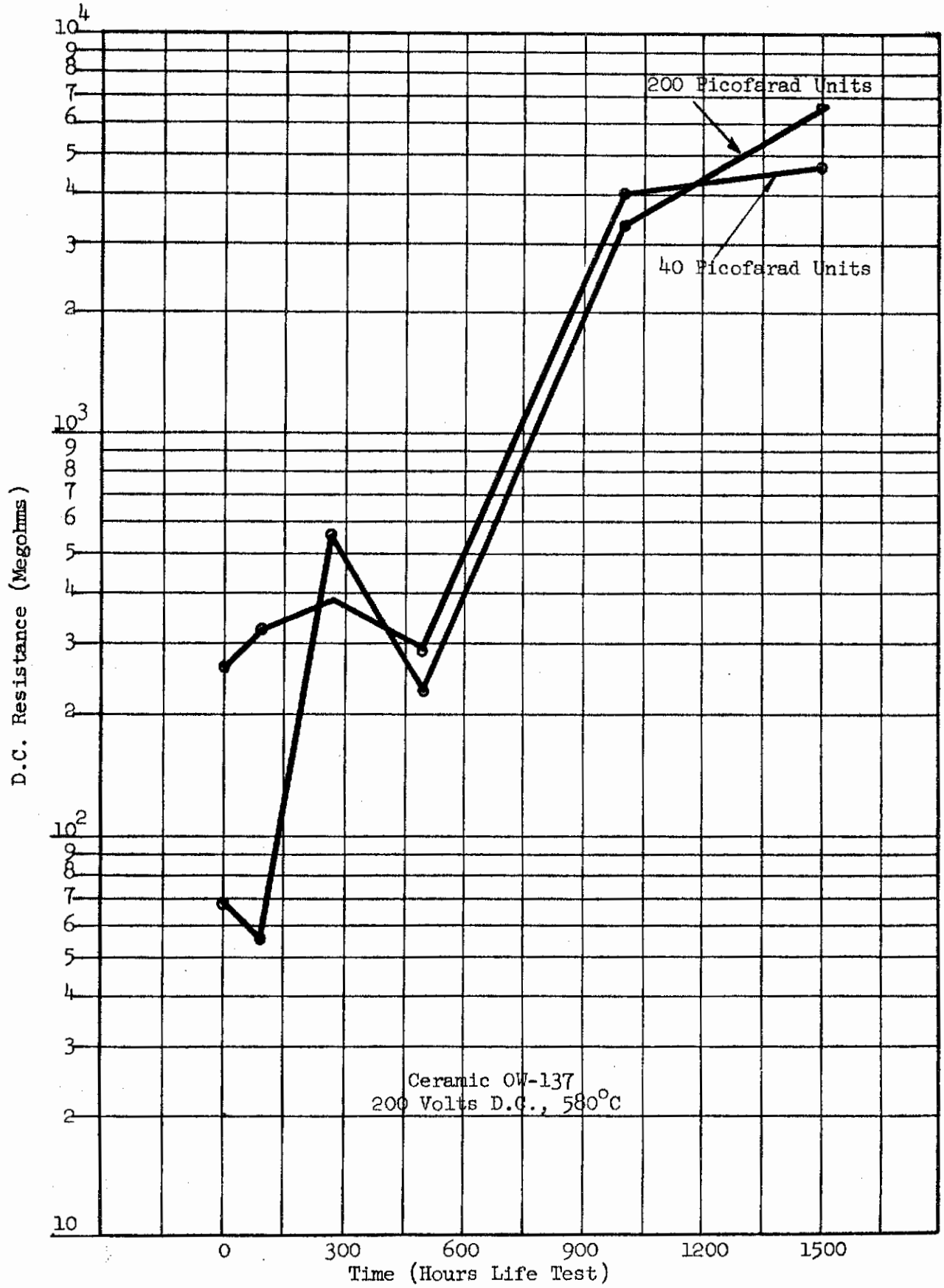



Fig. 92 Capacitor Life Test Data

# APPENDIX II

This report covers a compilation of the data collected to January 6, 1964, on the three capacitor life tests which were started under contract AF 33(616)-8096, during the contract reporting period of January 1, 1962 - October 31, 1962. The tests are as follows:

(1) 20 Volts squarewave at 15 KC and 0 volts bias, OW-102, temperature 580°C.

(2) 20 Volts squarewave at 10 KC and 25 volts D.C. bias, OW-102, temperature 580°C.

(3) 200 Volts D.C., temperature 580°C.

## 20 VOLTS SQUAREWAVE AT 15 KC AND 0 VOLTS BIAS, OW-102

Twenty OW-102 stacked plate units (nominally 60 picofarads) on test have completed 10,500 hours and all units are still operating satisfactorily. The D.C. resistance was greater than 84 megohms, the dissipation factor was less than .016, and the capacitance increased only 5.88% during 10,500 hours.

During this test the range of insulation resistance for all units was 84 to 156 megohms with a peak of 156 megohms at 6,500 hours. This range of insulation resistance closely approximates the intrinsic resistance of OW-102 dielectric with no apparent indication of polarization.

The ohm-farad product and dissipation factor (Tan $\delta$ ) are plotted versus time (hours life test) in Figure 93. The capacitance and D.C. resistance are plotted versus time in Figures 94 and 95, respectively.

## 20 VOLTS SQUAREWAVE AT 10 KC AND 25 VOLTS D.C. BIAS, OW-102

Eight OW-102 single plate units (nominally 20 picofarads) on this test had a D.C. resistance of 1,311 megohms, a dissipation factor of less than .018, and exhibited an increase in capacitance of 6.11% during the 10,000 hour test.

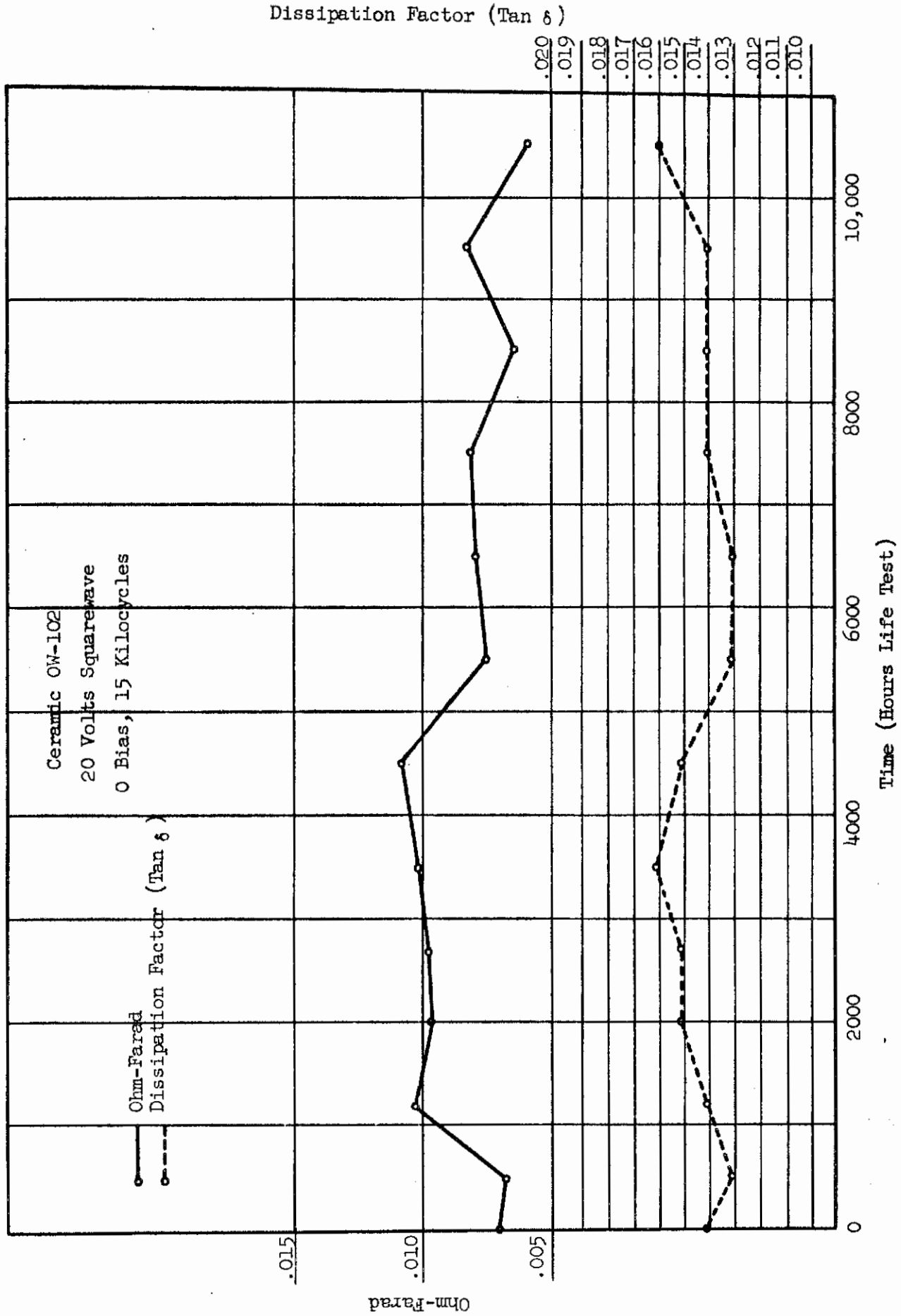



Fig. 93 Capacitor Life Test Data

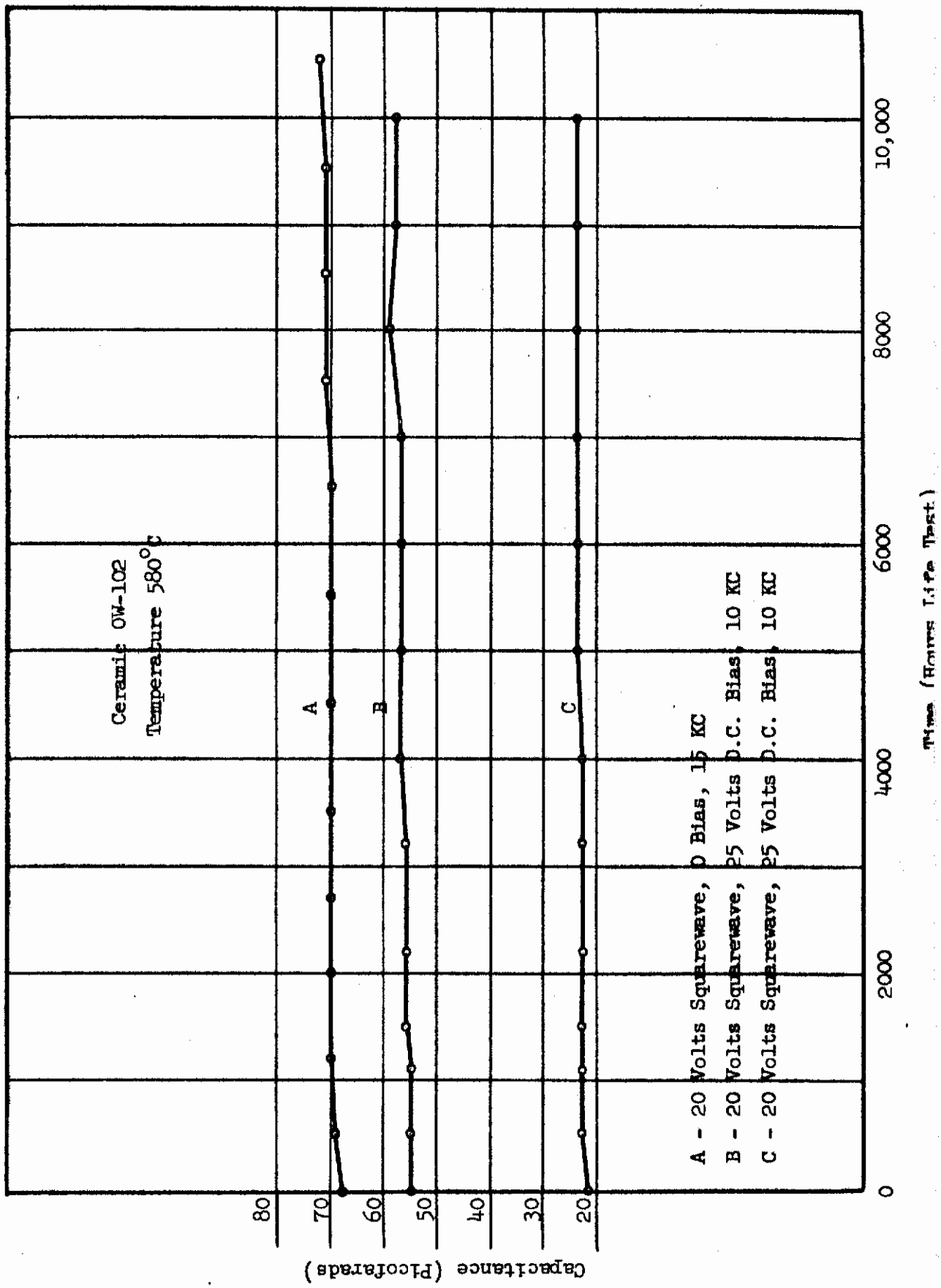



Fig. 94 Capacitor Life Test Data

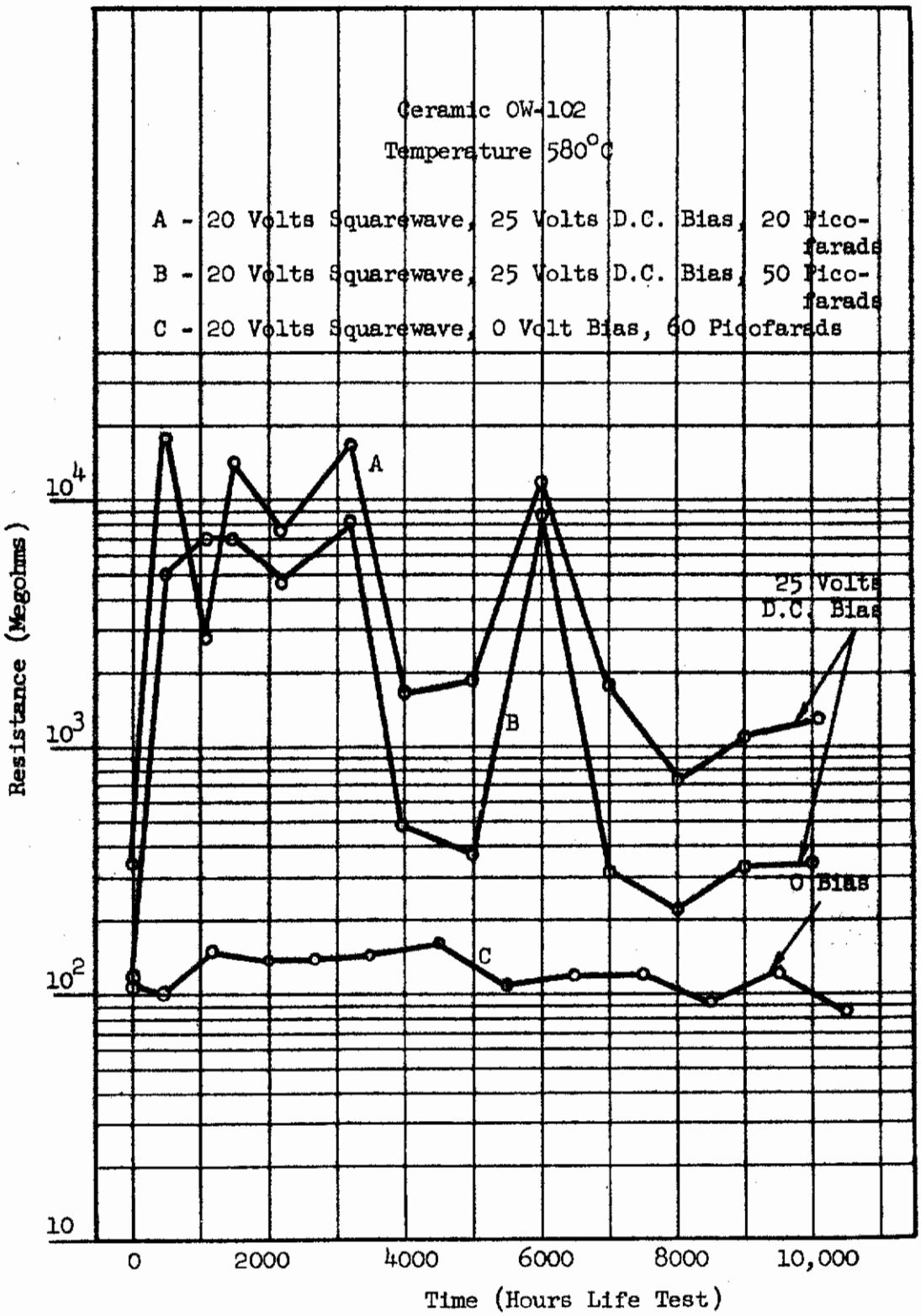



Fig. 95 Capacitor Life Test Data

Two units failed due to a low D.C. resistance (less than 10 megohms) at 5,000 hours. There was no indication of failure at the last reading (4,000 hours) and since readings are made every thousand hours after the 2,000 hour reading, it is not possible to determine how suddenly the two units failed.

Nine good OW-102 stacked plate units (nominally 50 picofarads) on test had a D.C. resistance greater than 345 megohms, a dissipation factor of less than .018, and exhibited an increase in capacitance of 5.18% at the end of 10,000 hours. One unit failed at the beginning of the test and failure was probably due to a poor furnace connection (i.e., broken lead). The high D.C. resistance of the units on this test is indicative of polarization due to the 25 volt D.C. bias.

The ohm-farad product and dissipation factor (Tan $\delta$ ) are plotted versus time (hours life test) in Figure 96. The capacitance and D.C. resistance are plotted versus time in Figures 94 and 95, respectively.

200 VOLTS D.C. TEST

Twenty synthetic mica roll units (nominal value: 300 - 800 picofarads) were initially put on 200 volts D.C. test. At the end of 10,500 hours, eight were still operating satisfactorily. These eight units had an average D.C. resistance of 230 megohms, a dissipation factor of less than .022, and exhibited an increase in capacitance of 17.8% during the 10,500 hours test. The eleven units that failed had an average D.C. resistance of 1.5 megohms, a dissipation factor of .023, and exhibited an increase in capacitance of 4.82% at 10,500 hours.

The ohm-farad and dissipation factor (Tan $\delta$ ) are plotted versus time (hours life test) in Figure 97. The capacitance is plotted versus time in Figure 98.

MICA ROLL CAPACITORS

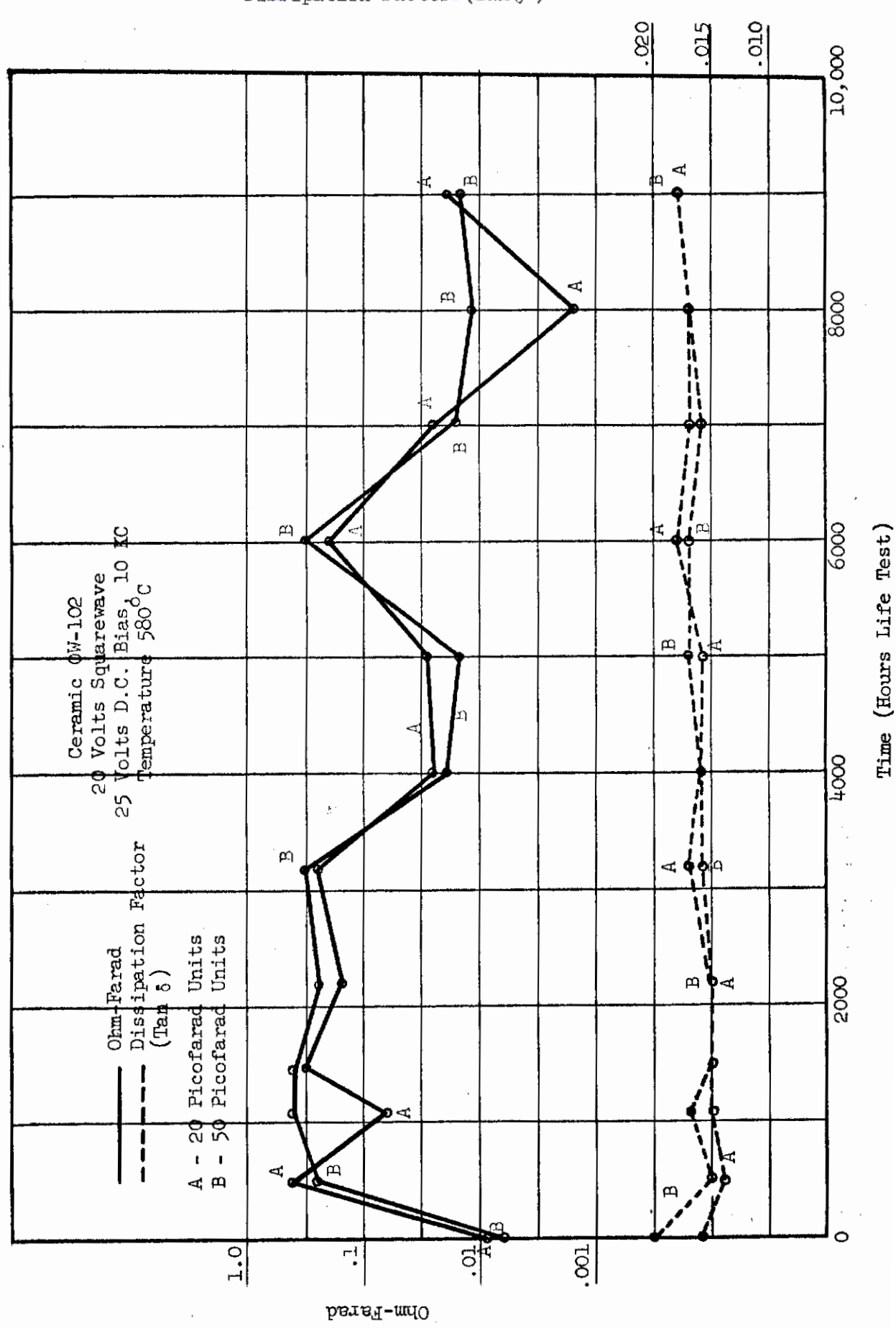



Fig. 96 Capacitor Life Test Data

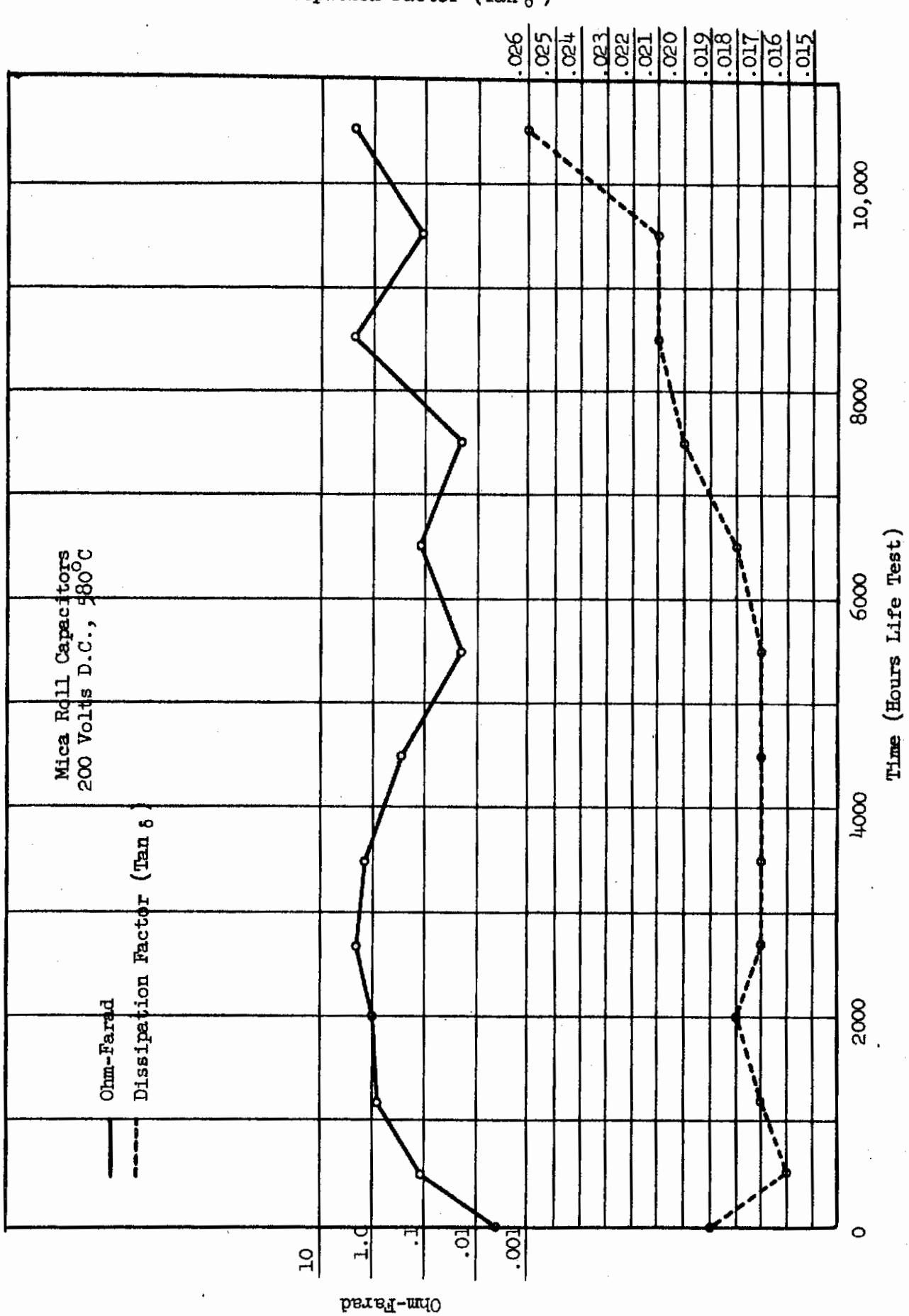



Fig. 97 Capacitor Life Test Data

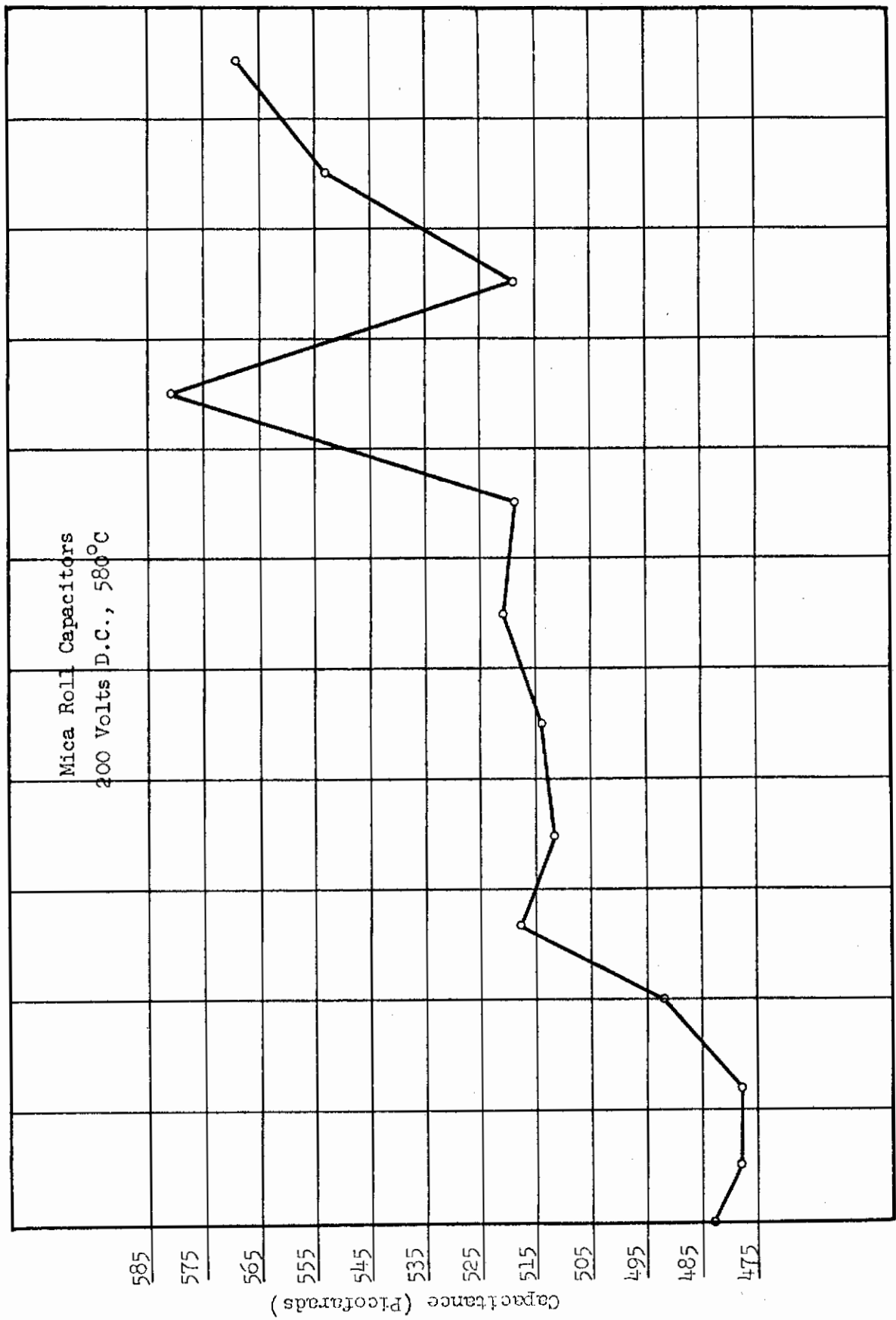



Fig. 98 Capacitor Life Test Data

On the 200 volt D.C. test there was no indication of deterioration due to increase in dissipation factor; however, the cause of failure for eleven of the twelve units that failed was a low D.C. resistance (less than 10 megohms). The twelfth unit failed due to a poor furnace connection (possibly a broken weld). The time (hours life test) at which the units failed and the D.C. resistance readings are listed below:

| Hours Life Test | Failures | Average D.C. Resistance |
|---|---|---|
| 24 | 4 | 5 megohms |
| 2,000 | 2 | 8 " |
| 5,500 | 2 | 5 " |
| 7,500 | 2 | 4 " |
| 8,500 | 1 | 1 " |

Since the voltage level in the resistance measurement is approximately 100 volts and the bridge voltage measurement is less than 3 volts, dielectric breakdown must be occurring at some intermediate level. A capacitance measure with the same voltage as the working voltage is indicated if the results are to be correlated.

NORMAL OPERATING CONDITIONS

The 20 volts squarewave, 0 bias 15 KC test and the 20 volts squarewave, 25 volts D.C. bias 10 KC tests are comparable to actual circuit conditions for this type capacitor.

Throughout the duration of these tests, the effect of polarization, as shown by the D.C. resistance of the units on 20 volts squarewave, 25 volts D.C. bias test, was very evident. At the end of 10,000 hours, the units on 20 volts squarewave, 25 volts D.C. bias test had an average D.C. resistance of 828 megohms as compared to an average D.C. resistance of 84 megohms for the units on 20 volts squarewave, 0 bias D.C. test.

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