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DESIGN, DEVELOPMENT, AND FLIGHT TEST OF MULTIPLEXING HARDWARE FOR USE IN A FLY-BY-WIRE FLIGHT CONTROL SYSTEM

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Approved for public release; distribution unlimited.

FOREWORD

This report was prepared by Convair Aerospace Division of General Dynamics under Air Force Contract F33615-71-C-1147, Design, Development, and Flight Test of Multiplexing Hardware for use in a Fly-by-Wire Flight Control System. The contract was initiated under Project 8225. The work was administered under the direction of Mr. Thomas D. Lewis of the Control Systems Development Branch, Flight Control Division, Air Force Flight Dynamics Laboratory.

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Mr. J. H. Watson, Supervisor of the Flight Dynamics - Advanced Programs Group, was the Program Manager. Dr. J. G. Mrazek was the principal investigator in this research; Messrs. R. O. Roberts and R. S. Goree were key contributors. The contribution of the Flight Research Department of Calspan Corporation in the installation and flight test phase of the program is acknowledged.

This technical report has been reviewed and is approved.

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ABSTRACT

This report contains a description of the design, development, airworthiness testing and flight test of multiplexing hardware for use in a fly-by-wire flight control system.

The multiplexing concept employed makes use of bi-phase Manchester baseband modulation of pulse coded digital data. Each analog value to be transmitted is converted to a digital format serially and transmitted over a twisted-shielded-pair cable. The bi-phase modulation combines the clock signal with the digital data and permits the clock and data to be reconstructed at the receiver. A partyline transmission concept was employed to permit two transmitters to share the same transmission line.

The completed hardware was tested for airworthiness through both environmental and electromagnetic interference tests before it was taken to the Calspan facility for installation in the flight test airplane. The airplane selected for the flight tests was the NC-131H Total Inflight Simulator airplane.

A total of 23.2 flight hours were accrued during this flight test. The multiplexing equipment was operating during approximately 19 hours of this period. The equipment functioned well during the flight test and provided a demonstration of the use of multiplexing in a fly-by-wire flight control system. None of the Calspan test pilots could detect the presence of multiplexing at any of the four data update rates (400, 200, 100 and 50 per second). The concept of multiplexing critical flight control signals has been demonstrated by this program but there are several design details that require additional research before a standard design specification can be derived. Among the areas requiring additional consideration are (1) failure tolerant transmission line coupling techniques, (2) data rate requirements expressed in terms of significant system dynamic characteristics, and (3) methods of detecting failures in redundant systems. This program has provided experience that will be valuable in future considerations of digital flight control systems.

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SECTION 1

PROGRAM SUMMARY

The Fly-by-Wire Multiplexing program is made up of two contracted segments. The first contract, F33615-690C-1574, was aimed at identifying a preferred multiplexing concept through trade studies and laboratory demonstration hardware. The results of that study are reported in AFFDL-TR-70-80, dated June 1970. The second contract, F33615-71-C-1147, has involved the development of airworthy multiplexing hardware that was flight tested aboard the Total Inflight Simulator (TIFS) aircraft. This report covers the events and results of the second program.

1.1 FLIGHTWORTHY MULTIPLEXING FLIGHT TEST PROGRAM

1.1.1 Flightworthy Hardware Development

In order to demonstrate the capabilities of a multiplexing system to function satisfactorily in a real flight environment, it was necessary to design, fabricate and test flightworthy hardware to be used in subsequent flight tests. The design of the flightworthy hardware was similar in many respects to that of the laboratory demonstrator that was developed during the first multiplexing program. The major difference was in the area of the data bus control which will be discussed in detail in a later section. After the hardware was fabricated it was tested for flightworthiness. These test included electromagnetic interference tests, vibration and shock test and temperature and electric power tolerance tests. At the completion of these tests the equipment was delivered to the flight test site for installation in the test airplane.

1.1.2 Flight Test Demonstration

The multiplexing equipment was installed in the Total Inflight Simulator airplane, an NC-131H, (see Figure 1-1), operated by the Calspan Corporation. After ground checkout, approximately 24 flight hours were accrued on the equipment in actual flight conditions. Primary control signals in all three axes of control were included in the multiplexed data. Of particular interest is the fact that the relatively high bandpass sideforce and direct lift flap servo loops were included in the multiplexed data also. The equipment functioned well during the flight tests, with the only abnormal behavior being traced to an apparent malfunction of one sample and hold channel. Four data update rates were provided in the flight demonstration equipment to permit evaluation of the effect of lower sample rates on the dynamic performance of the TIFS system. The dynamic range of the TIFS airplane is such that no degradation in dynamic performance was noted at any of the four update rates. Earlier analog computer simulations of a fighter type airplane however, did result in degradation at the lower rates. This test program pointed out that additional development of multiplexed flight control systems is necessary to arrive at what might be termed an optimum configuration. The particular areas requiring additional consideration include (1) the minimum allowable ratio of sample rate to significant corner frequency, (2) the optimum method of coupling remote multiplexing units to the data bus, and (3) methods of reducing noise levels in the reconstructed analog data.

Fig. 1-1 FLIGHT TEST AIRPLANE (TIFS)

SECTION 2

MULTIPLEX SYSTEM DESCRIPTION

2.1 FUNCTIONAL CONFIGURATION

The design of the flight test multiplexing hardware was influenced by the selection of the airplane in which the flight tests were to be performed. This influence was related to the signal paths selected to be multiplexed and the number of signals chosen for each path. The number of multiplexing units and their arrangement in the data transmission network were selected in order to demonstrate the data bus concept and yet retain a relatively simple design.

2.1.1 Aircraft Selection

At the time the RFP statement of work was written the test airplane had not yet been selected. In the interim period between the submission date of the proposal and the start date of the contract, the Air Force decided to use the Total Inflight Simulator (TIFS) airplane for the multiplexing flight test. This was an excellent selection in that the interfaces between the control system signals and the multiplexing equipment were much simpler in this airplane than would be the case in any other airplane that could have been selected. In addition, the TIFS airplane had built-in failure protection which eliminated the need for special provisions to be included in the multiplexing equipment. A photograph of the TIFS airplane is shown in Figure 1-1. This airplane contains an evaluation cockpit which has been added to the forward end of the original fuselage. This cockpit makes use of fly-by-wire controls and includes a variable feel system which controls the force gradients and gains of the pilot inputs. The pilot inputs are electrically connected to a 10-volt analog computer located in the aft fuselage area. This computer is normally employed in variable stability and other dynamic simulations in which this airplane is use.

Immediately behind the evaluation cockpit is the original C-131 cockpit where the safety pilot is stationed. There are numerous system out-of-tolerance conditions that will automatically trip the TIFS system off line at which time the safety pilot assumes control through the normal mechanical control system of the original airplane. The safety pilot can also disengage the TIFS system at his discretion. These safety features simplified the safety provisions required in the multiplexing equipment.

The analog computer, located in the aft portion of the fuselage, contains all the signals used in the TIFS control system. This computer permitted convenient access to any signal of interest.

2.1.2 Multiplex Signal Selection

In selecting the signals to be multiplexed in the flight test demonstration, several decision policies were observed: (1) It was desired to multiplex primary control commands and feedback signals in all three axes of control, (2) it was desired to include signals that would tax the capabilities of the multiplexing system, and (3) the signals to be multiplexed should be grouped so that various multiplexed data paths could be selected in a logical manner.

The signals selected for multiplexing are indicated in Figure 2-1. Three information source/user stations were assumed in the development of the flight test multiplexing data network; (1) the flight control computer (not to be confused with the TIFS analog computer), (2) the feel system (forward cockpit area), and (3) the actuators. In actuality, all of these signals were available at the analog computer but this division was made so that the decision could be made to either multiplex or not multiplex the pilot inputs and feel system signals or the actuator commands and position feedback signals. It was possible to leave some blank data slots for future growth. Equipment was included to accommodate all of the signals and blank slots shown in Figure 2-1. Unit 1 was designed to accommodate ten continuously variable input and output signals, two input test signals and two output test signals, and two input and three output discrete words. The continuously variable signals are sampled serially and converted to a digital format before transmission. The test signals are a fixed five volt level which is converted to a digital format, transmitted, reconstructed to an analog format at the receiver and compared to a standard five volt source in the receivers to check the converters. The discrete words contain ten bits of discrete information. Only three of the ten bits available were used in the two discrete words received from Units 2 and 3. Five bits were used in the discrete word transmitted from Unit 1 to Unit 4, the failure annunciator unit.

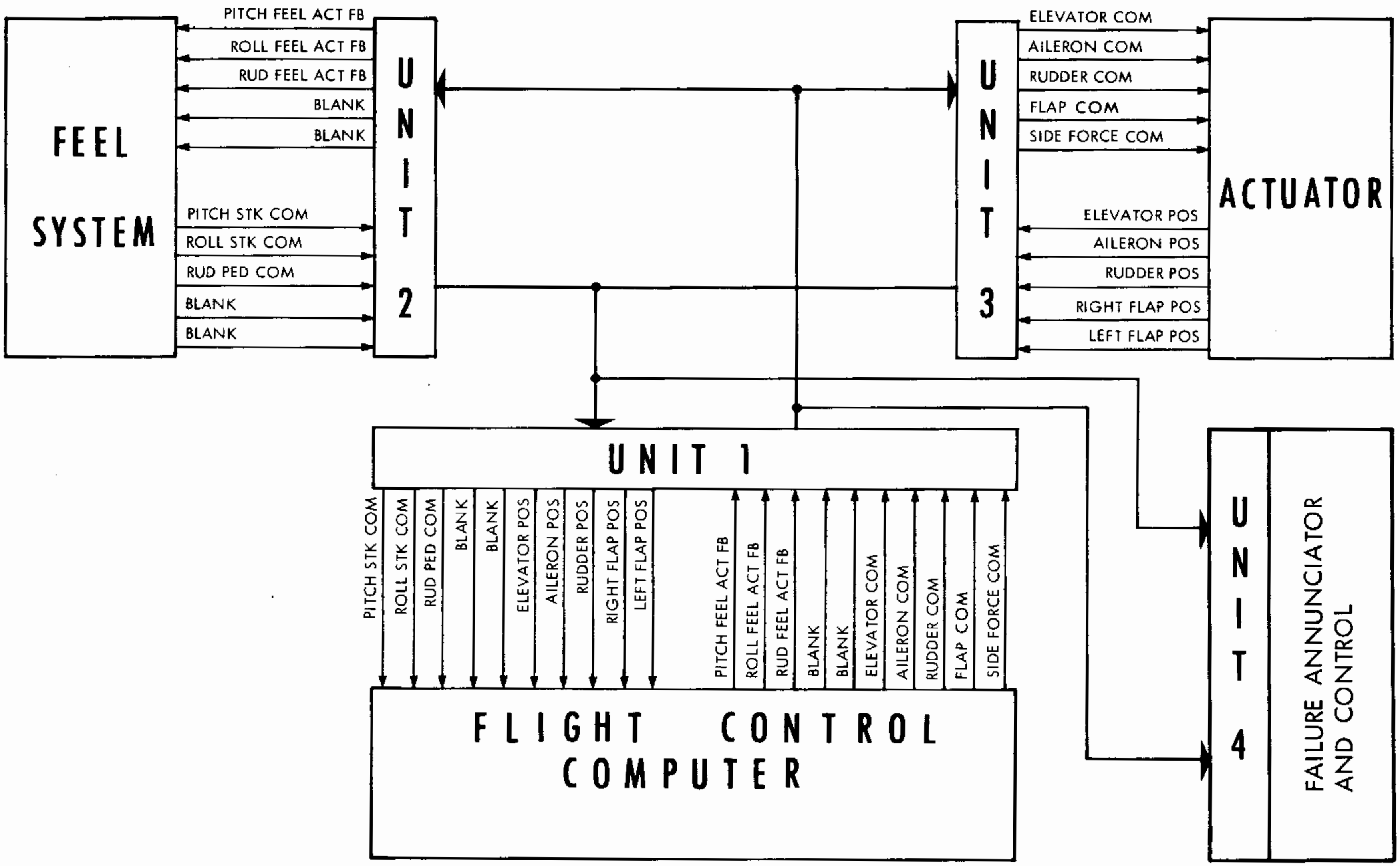
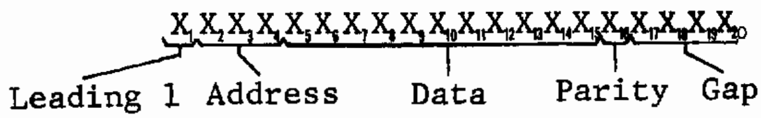


Fig. 2-1 SIGNAL FLOW DIAGRAM

Units 2 and 3 are identical to each other in configuration and data handling capability. Each will accommodate five continuously variable input and output signals, one input and output test signal and one input and output discrete word.

2.1.3 Data Transmission Concept

The data transmission concept includes the following characteristics; (1) digital format, (2) baseband modulation (0 and 5 volt pulse train), and (3) serial time division multiplexing. Each digital word is made up of 16 bits of information followed by a gap which is four bit periods in length. Each word has the following general character:



The digital words are in non-return-to-zero (NRZ) form, i.e., combinations of 1's and 0's, as they come from the analog to digital converter. Before transmission, the NRZ data is converted to Bi-phase Manchester code (discussed in later paragraphs) which combines the clock with the NRZ data.

The data transmission is over a twisted-shielded pair transmission line (22 gauge, stranded copper conductor, copper braid shield, polyalkene insulated). A separate line is used to transmit data from Unit 1 to Units 2 and 3 from that used to transmit in the oposite direction. Units 2 and 3 share the same transmission lines through the use of tri-state logic line drivers. Both units receive all data transmitted by Unit 1 but only the data with the appropriate series of addresses are processed and stored in each unit. Units 2 and 3 transmit alternately, controlled by the most significant bit of the addresses being received by each corresponding receiver. For example, Unit 2 transmits when its receiver senses that Unit 1 is transmitting a series of addresses whose most significant bit is 1. When the most significant bit of the addresses received is 0, Unit 2 stops transmitting and Unit 3 begins transmitting. In order to allow for differences in transmitting frequencies between the three units, a guard time of one word period was provided in the transmitter of Units 2 and 3. As a result of this built-in guard time, Unit 1 is capable of transmitting 16 digital words but Units 2 and 3 can only transmit 7 words each.

Units 2 and 3 are permitted to share the same transmission line through the use of tri-state logic line drivers. The specific tri-state components employed in the subject flight test hardware were National Semiconductor part DM7831D. These devices can be driven to a high impedance state which for practical purposes removes the element from the system. Using this feature, it was possible to allow Unit 2 to transmit then Unit 3 on the same transmission line.

The transmitted data was modulated in a Bi-phase Manchester format. This format is achieved through the use of a coincidence circuit as shown in Figure 2-2. The Boolean expression describing the combination of non-return to zero (NRZ) data and the clock to achieve the Bi-phase Manchester (Bi-ϕ) format is given as follows:

$$\text{Bi-}\phi = (\text{Clock} \cdot \text{NRZ}) + (\overline{\text{Clock}} \cdot \overline{\text{NRZ}})$$

$$= \text{Clock} \odot \text{NRZ}$$

It will be noticed in the timing diagram of Figure 2-2 that a state transition in the Bi-ϕ data occurs during each clock period. This characteristic permits a clock signal to be reconstructed from the Bi-ϕ data at the receiver.

2.1.4 Clock Reconstruction Approach

The Bi-ϕ data is received as shown in Figure 2-3. The positive and the negative going transitions in the Bi-ϕ data are converted to pulses by the logic shown. These pulses are introduced as inputs to a monostable multivibrator which is the key element in reconstructing the clock from the Bi-ϕ data. The natural period of the multivibrator was set at 3/4 of the clock period. The reconstructed clock signal is used to enable the Bi-ϕ data into the input shift register. Because of the finite time required to generate the reconstructed clock signal, the Bi-ϕ data has completed its transition before the leading (positive going) edge of the clock signal occurs. The data which is clocked into the shift register becomes NRZ data because each bit is defined by the state of the Bi-ϕ data at the time of the positive going edge of the reconstructed clock. Figure 2-3 contains a timing diagram which shows the original clock and Bi-ϕ data generated in the transmitter as well as the signals generated in the receiver. It will be noticed that the reconstructed NRZ data is shifted in time by 1/2 clock period relative to NRZ data that was transmitted.

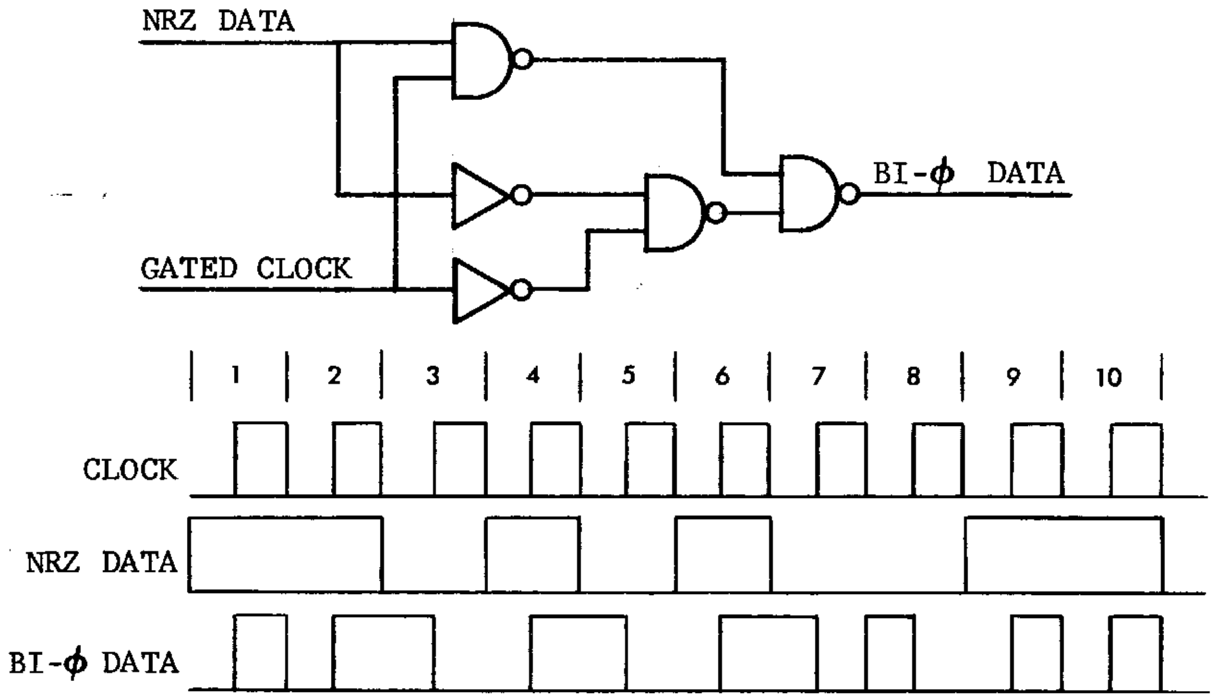


Figure 2-2 BI-PHASE MANCHESTER ENCODER

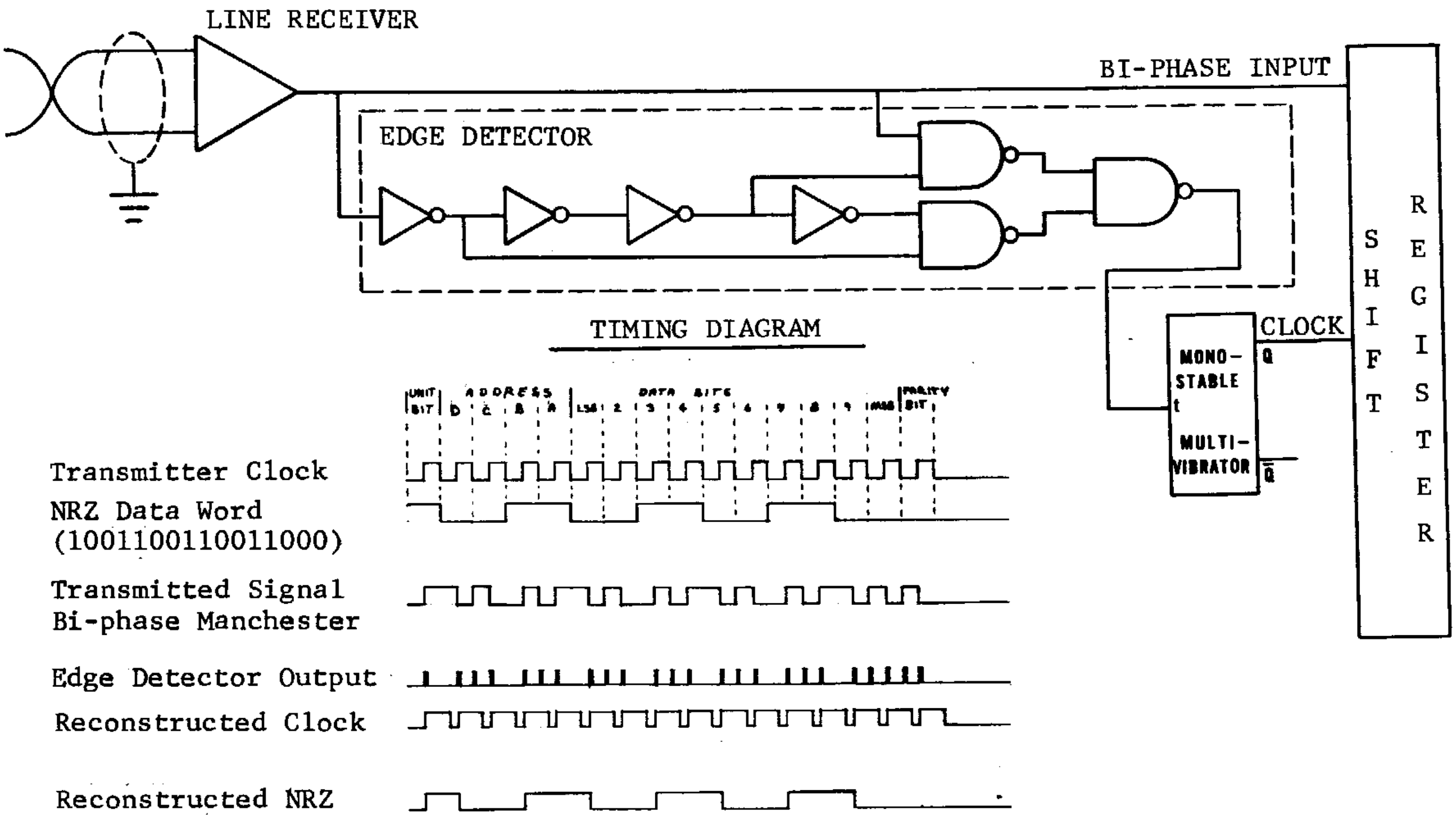


Figure 2-3 CLOCK AND DATA RECONSTRUCTION APPROACH

2.1.5 Failure Detection Provisions

Each receiver in the system was equipped with a means of detecting failures. A retriggerable monostable multivibrator was employed in each receiver to detect a dead transmission line condition. This condition is characterized by an absence of pulses at the output of the line-receiver. The analog to digital and digital to analog converters were checked in the following manner. In each of the three transmitters that included converters, one test word was generated by using the five volt reference source as a pseudo analog input. This voltage was converted to digital format, transmitted serially with the other converted analog signals, and reconstructed to analog form in the appropriate receiver. The reconstructed five volt signal was then compared with a five-volt signal reference source in the receiver. The comparator was strobed by a "data good" discrete signal that is generated with each word received. The "data good" signal is made up of a combination of good parity, register full and no overflow conditions at the input shift register. The output of the comparator is a series of pulses in normal operation. These pulses, indicating a satisfactory comparison, are then applied as inputs to a retriggerable monostable multivibrator which remains in a high state as long as the input pulses continue to come from the comparator. Should the pulses cease coming, the multivibrator state will fall to a low value indicating a failure. The state of this multivibrator is used as a discrete signal which is transmitted to the failure annunciator unit, Unit 4. Tolerance of transient failure indications can be built in by stretching the period of the multivibrator to span several normal pulse periods.

2.2 SYSTEM DESCRIPTION

2.2.1 General

The five unit Fly-By-Wire Multiplexing System is shown in Figure 2-4. The system consists of three transmitter/receiver units, a failure annunciation unit, and a signal transfer relay unit. Units 1, 2 and 3 are identical in external configuration and are very similar functionally. Units 2 and 3 are identical internally as well. Unit 1 is capable of accommodating 16 digital words whereas Unit 2 and 3 handle only seven each. Unit 1 was assigned the task of processing the input and output signals associated with the flight control computer. Unit 2 processes the signals

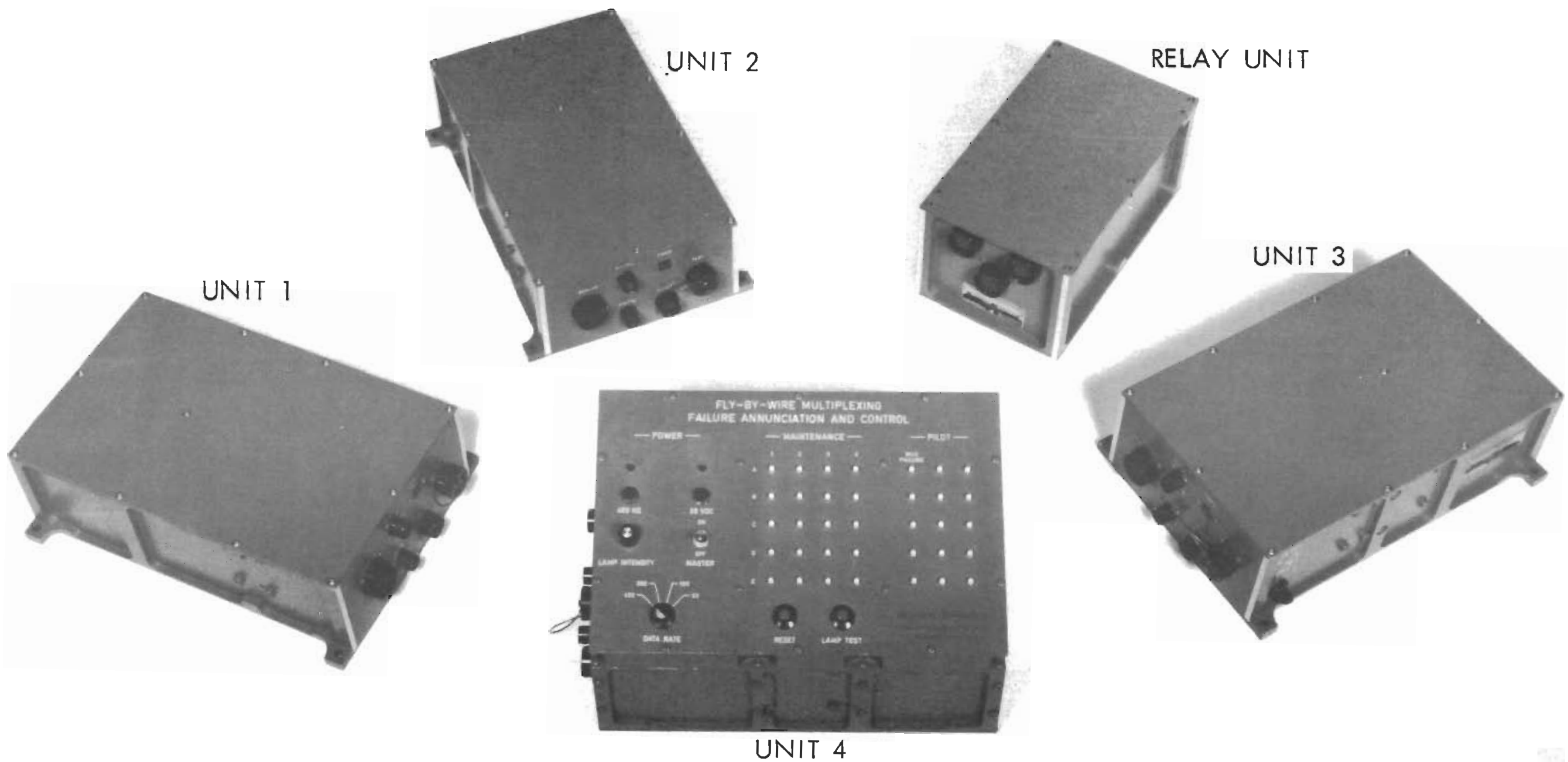


Fig. 2-4 AIRWORTHY MULTIPLEXING EQUIPMENT

associated with the feel system and Unit 3 processes the actuator signals.

Unit 4 contains the Failure annunciation and control panel shown in Figure 2-5 which (1) controls the distribution of power to the other units, and (2) annunciates failures within the multiplexing system. Failure lights were provided on the Maintenance Panel as an aid in isolating a failure down to a faulty LRU.

Data Rate switches on each unit allow selection of data update rates of either 400, 200, 100, or 50 times per second for each parameter.

The Relay Unit is used for inflight transfer from the multiplexing system to the normal TIFS system. The relay unit, which is controlled from the TIFS computer rack, allows inflight comparison of the TIFS system and the multiplexing system. This unit contained "make before break" relays so that the analog output, whether reconstructed multiplexed signals or TIFS signals would never be interrupted.

The cabling that connected the units during operation involved three major segments, i.e., analog and digital transmission cables and power cables. The analog signals were routed over single wires in the analog cable. A signal ground wire was also included for ground reference. The entire bundle was shielded for protection against electromagnetic interference effects. The digital transmission lines were a twisted-shielded pair configuration. There were two of these cables, one for data transmitted from Unit 1 and Units 2 and 3 and one for transmission in the opposite direction. Unit 4 was connected to both of these transmission lines for failure annunciation purposes. Both 28-volt dc and 400 Hz 115-volt ac were also routed to each of the four transmitter receiver units. Each unit contained its own local power supply, using only this raw aircraft power as a source.

The following paragraphs contain discussions of a typical transmitter and receiver. All of the transmitters and receivers were very similar. The primary difference between Unit 1 and Units 2 or 3 was in the number of signals processed. The purpose of explaining the operation is therefore served by discussing the transmitter and receiver operation of Unit 2 or 3.

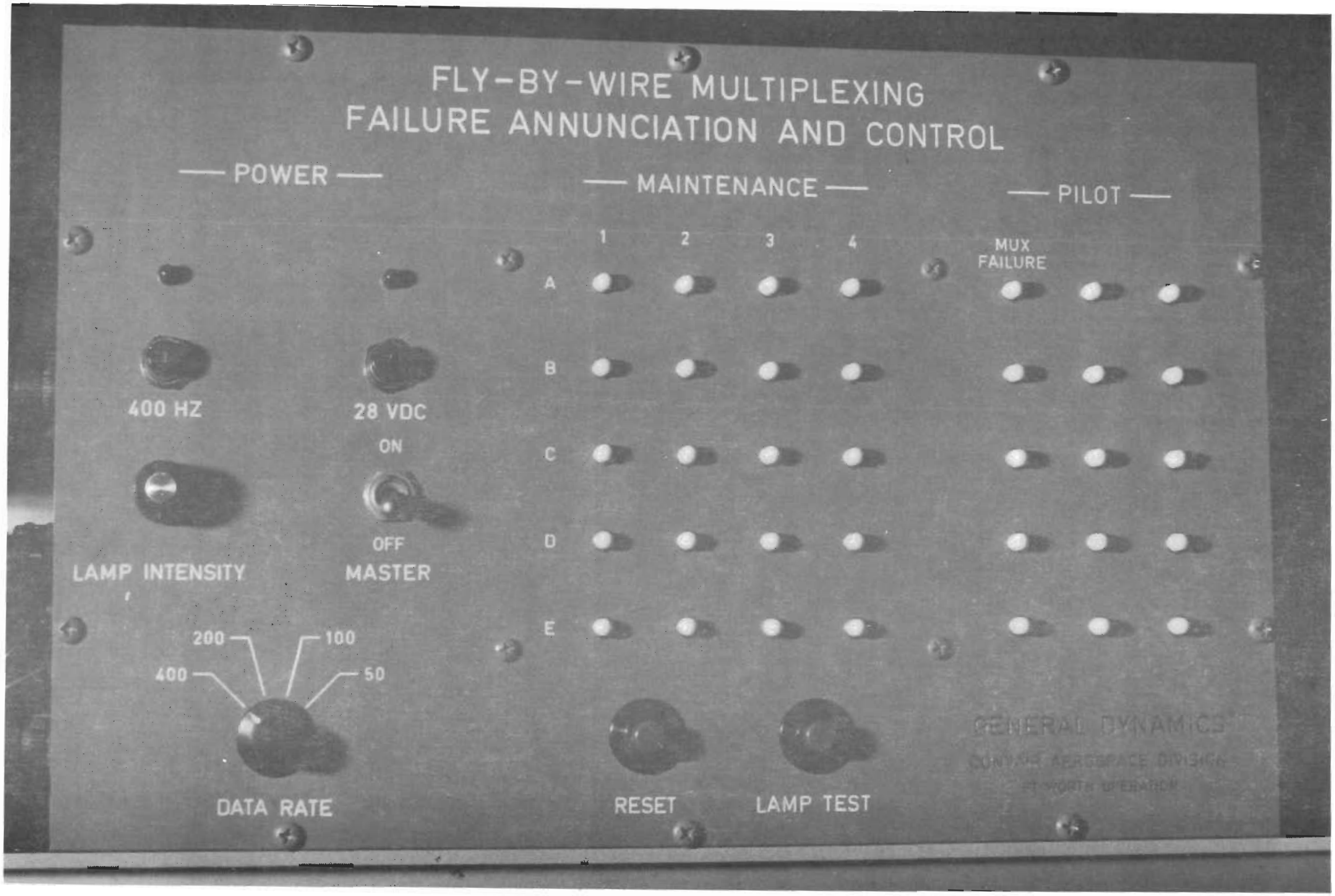


Fig. 2-5 FAILURE ANNUNCIATION AND CONTROL PANEL

2.2.2 Typical Transmitter Configuration

Although there are three transmitters included in the test hardware, they are all similar in concept and the transmitter in Units 2 and 3 are identical. Figure 2-6 contains a schematic diagram of a transmitter of the level of complexity found in Units 2 and 3.

The analog inputs are applied to input buffer amplifiers as shown in the upper left corner of the diagram. Each of these amplifiers is set up as a low pass filter whose corner frequency is approximately 200 Hz. This feature band limits the analog inputs to attenuate high frequency noise that may be present on the signals. The outputs of the amplifiers are routed directly to six FET switches which are controlled by an address decoder that will be discussed later. The FET switches are normally open and are sequentially closed by the decoder. Each analog voltage is admitted to the Analog to Digital (A/D) converter in turn. The analog voltages are converted to 10-bit digital words and these 10-bit states are clocked (in parallel) into a shift register on an appropriate signal from the transmitter control logic, which will be discussed more fully later. It will be noticed that the shift register contains 16 bits in its output word. As mentioned earlier, this word is made up of the following:

1. a leading 1
2. four bit address
3. ten data bits
4. one parity bit

The sixteenth or last bit in the shift register is set at a zero state before the word is shifted out. After the shift register has been loaded, the gated clock shifts the data from the shift register through the odd parity generator (OPG). The OPG is essentially a toggle flip-flop that changes state with each five-volt bit that is shifted out of the register. A zero-volt bit has no effect on the toggle state. Since the toggle is reset to the $\bar{Q}$ state before the shifting of data begins, an even number of 1's in the data will result in the toggles being in the $\bar{Q}$ state at the sixteenth clock pulse. The sixteenth bit was grounded in the shift register so taking the inverter into account it presents a high state of one side of the output NAND gate of the OPG. The $\bar{Q}$ state of the toggle in combination with the parity enable signal (taking into account its inverter)

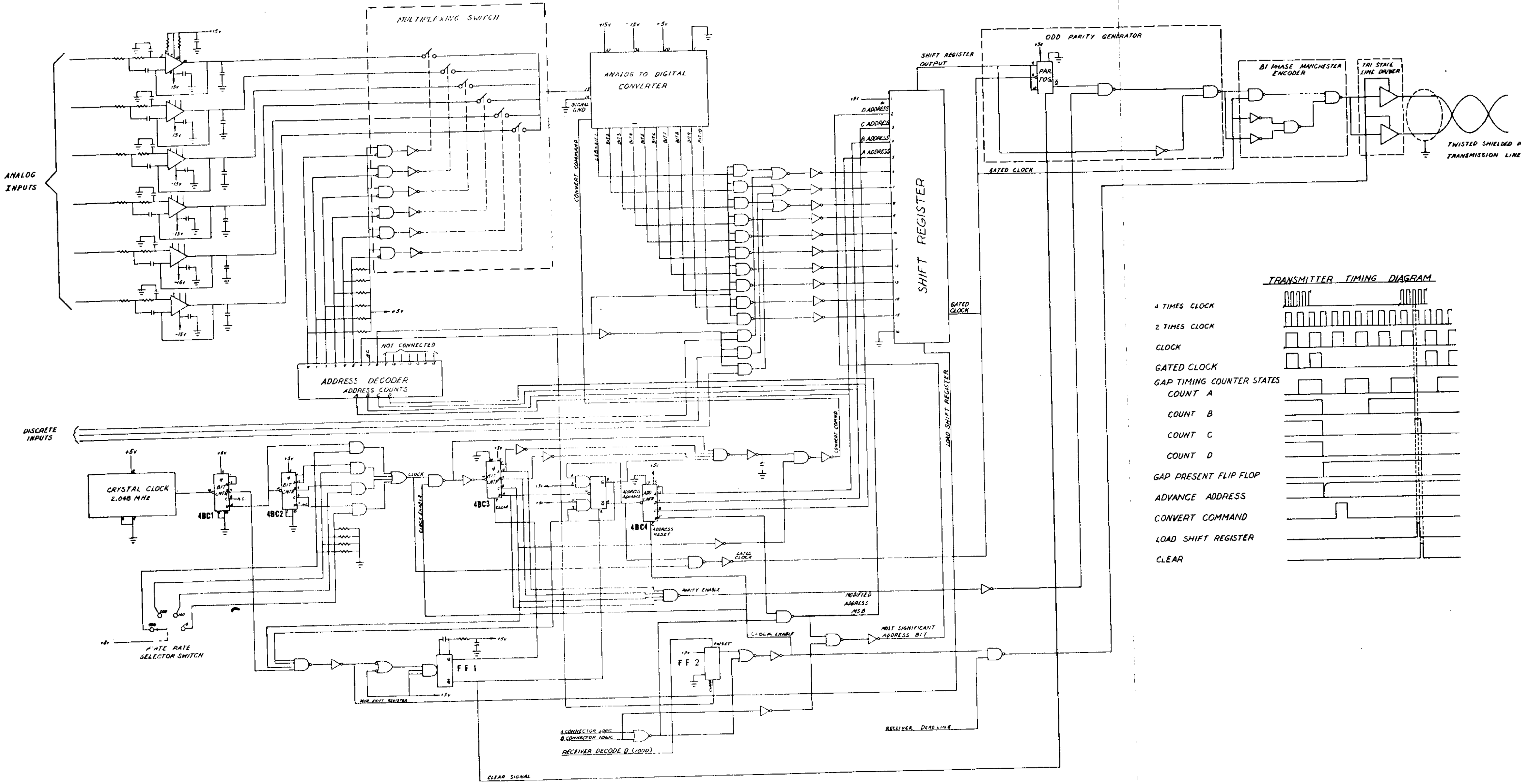


Figure 2-6 TYPICAL TRANSMITTER SCHEMATIC DIAGRAM

results in a low signal to the other side of the output NAND gate. This combination of a low and high signal result in a high state at the output NAND gate. This high state becomes the sixteenth bit of the word which now exhibits odd parity. If the number of 1's in the shift register is odd, then the last bit of the word becomes zero.

The data from the output gate of the OPG, termed non-return to zero (NRZ), is combined with the gated clock in the Bi-phase Manchester encoder. This encoder is essentially a coincidence circuit which produces a 1 when the clock and the NRZ data are in the same state and a 0 when their states differ. The output of the encoder is applied to the input of a differential line driver. The line driver provides the power to drive the signal over the twisted-shielded pair transmission line.

The functions accomplished in the transmitter, e.g., FET switch selection, A/D conversion, load shift register, etc., are controlled by a logic network. This network occupies the lower portion of Figure 2-6. The heart of the control logic is the clock. In order to achieve a stable clock frequency, the transmitter clock is derived from a crystal oscillator whose natural frequency is 2.048 MHz. The output from the crystal oscillator is counted down by a factor of 16 through a four bit counter. The resulting frequency is 128 KHz. This frequency permits sixteen 20 bit words to be transmitted 400 times per second, the highest update rate provided. Three other data rates are provided through the use of a four bit counter that uses the 128 KHz signal as an input. The "A" stage of this counter provides the necessary clock frequency for a data update rate of 200 per second and the "B" and "C" stages provide the clock frequencies for rates of 100 per second and 50 per second, respectively. The selection of the desired clock frequency is made by properly positioning a selector switch to supply a five volt enable signal to the appropriate gate. As stated earlier each word contains only sixteen bits of information. A gap is provided between words which is four bit periods in length making the total word frame 20 bit periods long. During this gap, a number of information management operations take place. The selected clock signal is gated into a four bit counter by a clock enable signal that will be discussed later. The result of this gating operation is a gated clock which consists of 16 clock pulses followed by a dead time whose length is four bit periods. The clock pulses are used to trigger the four-bit counter. After a count of

16 has been reached and the D stage of the counter falls from a 1 to an 0 state, a bistable multivibrator is triggered to a Q state. This flip-flop, in conjunction with the four bit counter, controls all of the functions that occur during the gap. The timing diagram in Figure 2-6 illustrates the timing of the operations that take place during the gap. The first action is a pulse that advances the address in the address counter. This pulse is the result of a flip-flop going from a $\bar{Q}$ state to a Q state. The address from the address counter is applied to the address decoder which selects the appropriate FET switch and admits an analog voltage to the A/D converter. The second action is a command pulse to the A/D converter to start the conversion of the analog voltage which is present at the input to the converter. The third action is that of loading the shift register with the converted digital word. This action takes place near the end of the gap. The last action is that of clearing all of the flip-flops in this control logic circuitry. The clearing signal is generated by a monostable multivibrator which is triggered by a combination of signal states. The three signals required to obtain a "clear" pulse are the Q state of FF1, the C stage high in 4BC3, and the B state of 4BC1 falls from 1 to 0.

Four-bit counter, 4BC3, also provides the signals required to enable the addition of the proper parity bit to the digital output words. When all four stages of 4BC3 are high, i.e. , a count of 16, the parity is enabled.

Although units 2 and 3 are identical within the enclosures, they function in response to different series of addresses received from Unit 1. The difference between Units 2 and 3 lies in the connectors on the transmission lines to the LRU's. Four pins are used in the connector to identify which location the particular box is in. Two of these pins are wired to +5 volts and ground respectively and the other two are the identification pins for the connector logic. The following truth table illustrates the identification algorithm. A logical 1 was obtained by wiring

TABLE 2-1 PIN LOGIC TRUTH TABLE

PIN A B	LRU
0 0	Unit 1
0 1	Unit 2
1 0	Unit 3

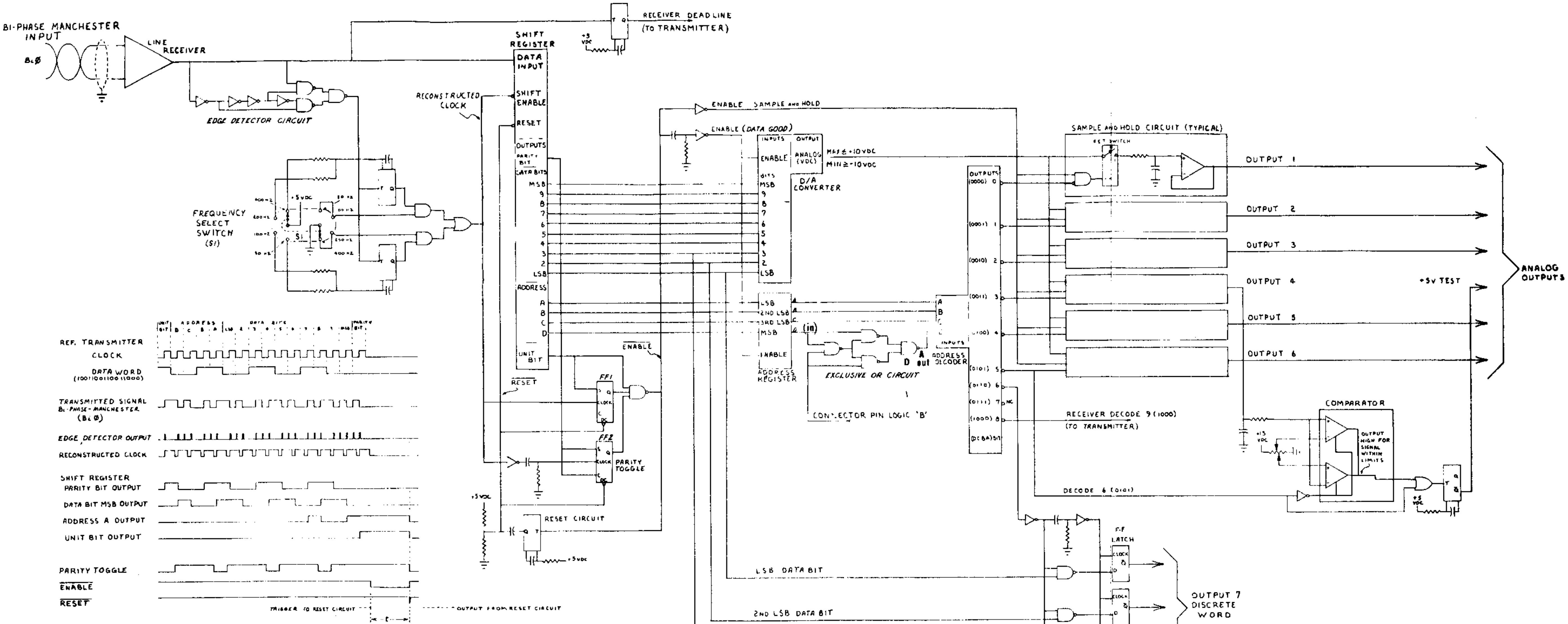
5 volts to the appropriate logic pin in the harness side connector. Similarly a logical zero is obtained by wiring a ground signal to the appropriate logic pin. This connector logic is used to control the transmitter and to modify the most significant bit of the address so that the proper series of addresses is transmitted corresponding to the location of the LRU in the system.

In the case of Unit 1, pins A and B are both at ground or zero level. The transmitter is enabled continuously and the address placed in the shift register is the same as that produced by the address counter, 4BC4. Unit 2, however, only transmits while it is receiving a series of addresses whose MSB is 1. The transmitter must therefore be inhibited during the alternate periods during which the address MSB is 0. This inhibiting action is obtained through the use of the receiver address decoder. The ninth decoder output (address 1000) presets FF2 and creates an enabling signal for the gated clock and also enables the transmitter. The Unit 3 transmitter works in exactly the same manner, the only difference being in the fact that the connector logic is used to modify the MSB of the received address before it is input to the address decoder. The circuitry required to modify the MSB of the received address will be discussed in the pages covering the receiver operation.

2.2.3 Typical Receiver Configuration

The logic circuitry required to perform the functions of the receiver in Units 2 and 3 is shown in Figure 2-7. The transmission line (twisted shielded pair) is shown connected to the differential line receiver in the upper left portion of the figure. The line receiver output is in Bi-ϕ data format and is monitored by a dead line detector (retriggerable monostable multivibrator). This multivibrator remains in a set state as long as pulses are present at the output of the receiver. The natural period of the multivibrator was set so that it exceeds the normal gap between words at the lowest data rate. Sufficient margin was provided in this natural period to allow for the effects of temperature variations and manufacturing tolerances.

The output of the line receiver is also fed to an edge detector circuit which generates a pulse at each positive going or negative going edge of the Bi-ϕ data. The timing diagram included in Figure 2-7 illustrates the pulse pattern obtained as a result of sensing the edges of the Bi-ϕ data.



DURING TIME t ; ADDRESS DATA FROM SHIFT REGISTER, STORED IN ADDRESS REGISTER, IS DECODED UNDER CONTROL OF PIN LOGIC.

SIGNAL DATA FROM SHIFT REGISTER IS CONVERTED TO ANALOG DATA AND IS APPLIED TO FET SWITCH CONTROLLED INPUTS OF SAMPLE AND HOLD CIRCUITS.

DECODED ADDRESS OUTPUT OF DECODER CLOSES THE FET SWITCH OF A SINGLE SAMPLE AND HOLD CIRCUIT AND SELECTED OUT RESPONDS TO ANALOG (VDC) INPUT.

AFTER TIME t ; FET INPUT SWITCHES OPEN AND INPUT OF SAMPLE AND HOLD CIRCUIT IS ISOLATED FROM D/A CONVERTER. OUTPUT OF SAMPLE AND HOLD CIRCUIT LOCKS AT LAST INPUT VALUE.

ALL OUTPUTS OF SHIFT REGISTER GO TO LOGIC "0".

PARITY TOGGLE OUTPUT GOES TO LOGIC "0".

UNIT BIT FLIP-FLOP OUTPUT GOES TO LOGIC "0".

RECEIVER CYCLE: A COMPLETE RECEIVER CYCLE CONSISTS OF SEVEN (7) DATA WORDS.

THE FIRST SIX DATA WORDS CAUSE RESPONSE OF ANALOG OUTPUTS 1 THRU 6. ANALOG OUTPUT 4 IS THE ANALOG TEST OUTPUT AND IS STROBED BY DATA WORD 6.

DATA WORD 7 CONTROLS OUTPUT 7. OUTPUT 7 CONSISTS OF THE THREE LEAST SIGNIFICANT DATA BITS OF DATA WORD 7.

DATA WORD 8 IS NOT TRANSMITTED.
DATA WORD 9 CONFIRMS THAT UNIT IS IN TRANSMITTER CYCLE.

Figure 2-7 TYPICAL RECEIVER SCHEMATIC DIAGRAM

For the sake of illustration, a transmitter clock and an arbitrarily selected NRZ data word are shown above the corresponding Bi-ϕ data. The pulses from the edge detector circuit are used to reconstruct a clock signal. This reconstruction is accomplished by applying the pulses to the input of a monostable multivibrator whose natural period is approximately 3/4 the period of the transmitter clock. The timing diagram illustrates that when a pulse from the edge detector triggers the multivibrator to a set state, it stays in that state for its natural period (3/4 clock period). Any pulses that occur while the multivibrator is set are ignored. The result is a reconstructed clock signal. The reconstructed clock signal is used to enable the shifting of data through the shift register. Because of the fact that a finite time is required to reconstruct the clock from the Bi-ϕ data, the positive going edge of the clock occurs slightly later than the beginning of the bit period of the Bi-ϕ data. A characteristic of Bi-ϕ data is that an NRZ zero state is represented by Bi-ϕ data bit that is at a "zero" state for the second half of the period. The phasing is reversed for an NRZ "one" state. The state of the Bi-ϕ data at the beginning of the clock period is the state of the desired NRZ bit. By applying the Bi-ϕ data to the shift register input and enabling the shift by the positive going edge of the reconstructed clock, the original NRZ data is recovered. Since in the reconstruction of the clock, the period of the multivibrator must be coordinated with the transmitter clock frequency, it is necessary to change the multivibrator natural period to suit each data update rate. This is accomplished by switching the timing resistors. It is practical to use a given timing capacitor with only a limited range of resistors so the four data update rates required were obtained through the use of two multivibrator circuits, one for the upper two frequencies and one for the lower two frequencies.

The shift register is cleared after each word has been shifted into the D/A converter permitting a full register to be detected by sensing the presence of the leading 1 in the first bit position (the bottom position shown in Figure 2-7) of the register. This condition is combined with two other conditions, i.e., overflow and parity, to form a "data good" discrete signal that is used to enable data into the D/A converter and into the sample and hold circuits. The overflow condition is sensed through the use of the bi-stable multivibrator FF1 in Figure 2-7. The output from the last bit position of the shift register is applied to FF1. If a clock pulse occurs while a "one" is in the last bit of the shift register, FF1 will be set to a Q state and will remain in that state until it is cleared.

When the "data good" discrete occurs, the ten data bits are transferred in parallel to the D/A converter and the conversion process begins. The address bits are also shifted from the register to a temporary storage address register. The shift register is then cleared in preparation for the next digital word to be clocked in. It was necessary to store the address of the previous word to permit sufficient time for the sample and hold circuits to settle out to a final value. The alternative was to make the sample and hold circuits rapid enough to be settled out during the four-bit gap period, about 30 μsec at the fastest update rate. A sample and hold circuit designed to respond this rapidly will in general, bleed off more rapidly also. The stored address permits a whole word period, about 156 μsec, to allow the sample and hold to settle out. This longer period permits a more stable sample and hold circuit to be employed at a cost of only four bi-stable multivibrators to store the address.

The MSB of the stored address is modified by the connector logic and an exclusive OR circuit to yield the following truth table. This table indicates that when B_{pin} is "0",

TABLE 2-2 ADDRESS CHANGE TRUTH TABLE

B_{pin}	D_{in}	D_{out}
0	0	0
0	1	1
1	0	1
1	1	0

D_{out} is the same as D_{in} but when B_{pin} is "1", D_{out} is the complement of D_{in}. This logic permits the LRU's representing Units 2 and 3 to be interchangeable.

The modified stored address is applied to the address decoder. The discrete outputs from the decoder are used to enable a sample and hold circuit that corresponds to the address applied to the decoder. The analog information from the D/A converter is placed on a common bus to all of the sample and holds (S&H) but the input to each S&H is controlled by a combination of the "data good" condition discussed earlier and a discrete output from the address decoder. The analog information is stored in the appropriate S&H and is updated each 1/400, 1/200, 1/100 or 1/50 second depending on the position of the update rate selector switches. Since the discrete words received are also identified by an address, the corresponding decoder output is used to enable the discrete word bits into solid state latches for storage.

The five-volt test signal, shown in Figure 2-7 as output 4, is compared to an internal five-volt source in a comparator circuit. The comparator is strobed (sampled) by the sixth decoder output. Between strobe signals the comparator output is high. If the comparison between five volts and output 4 is within a prescribed tolerance when the strobe signal arrives, the output of the comparator goes to a low state. This low pulse is combined with the decoder output (low also when selected) through a NOR gate to produce a high pulse. This high pulse is used to trigger a retriggerable monostable multivibrator. A pulse is produced once each frame of words if the comparison between the test voltage and five volts remains satisfactory. The period of the multivibrator is set to permit the loss of several pulses before a failure is indicated. This provision was made to avoid the difficulty of transient out-of-tolerance conditions.

SECTION 3

EQUIPMENT TESTING

3.1 GENERAL

In addition to the normal bench tests that were performed as the multiplexing equipment was assembled, the statement of work for the program required that certain other test be performed. These additional tests included a demonstration of the equipment operation in conjunction with an analog computer simulation of an airplane. This simulation was designed so that the dynamic characteristics of the airplane could be adjusted, thereby permitting a preliminary evaluation of the effects of multiplexing on the dynamic performance of the airplane.

When the proper operation of the equipment had been verified and the analog computer simulation work was complete, the equipment was moved to the EMI screen room for electro-magnetic interference tests. These tests and the environmental tests that followed were aimed at verifying the airworthiness of the equipment.

3.2 BENCH TESTING

Bench testing of the multiplexing equipment was initiated as soon as the fabrication of significant subassemblies was completed. The early bench testing consisted primarily of checking each assembled circuit board for proper operation. Although this was a routine task it occupied much of the time expended in the bench testing process.

After the circuit boards were completed and each of the TR units housings was completed, the components were assembled and operated as a data transmission system. At this time input/output tests were made to compare the reconstructed analog voltages at a receiver to the original analog voltage input at a corresponding transmitter. The results of these tests are presented in Table 3-1. Input voltages of +10V, +5V, 0V, -5V and -10V were input to the transmitters of units 1, 2 and 3. The outputs of the receivers in each of these units was then recorded. It was found that the data was very linear throughout the voltage range except within 0.1V of the -10V extreme. The slight nonlinearity in this narrow region can be attributed to the

Table 3-1

BENCH TEST GAIN DATA

CHANNEL OUTPUT	INPUT (VOLTS)				
	+10	+5	0	-5	-10
R1-1	10.01	5.01	0.00	-5.00	-9.95
R1-2	10.01	5.02	0.01	-5.00	-9.95
R1-3	10.01	5.02	0.01	-5.00	-9.95
R1-4	10.01	5.02	0.00	-5.00	-9.95
R1-5	10.01	5.02	0.01	-5.00	-9.95
R1-6	9.90	4.95	-0.01	-4.98	-9.94
R1-7	9.90	4.95	-0.01	-4.98	-9.95
R1-8	9.90	4.95	-0.01	-4.98	-9.94
R1-9	9.90	4.95	-0.01	-4.97	-9.95
R1-10	9.90	4.95	-0.01	-4.97	-9.93
R2-1	9.95	4.98	0.00	-4.99	-9.95
R2-2	9.96	4.99	0.02	-4.98	-9.94
R2-3	9.96	4.98	0.00	-5.00	-9.95
R2-4	9.96	4.98	0.00	-4.99	-9.94
R2-5	9.96	4.98	0.01	-4.99	-9.96
R3-1	9.96	4.99	0.00	-5.01	-9.77
R3-2	9.96	5.00	0.00	-5.00	-9.92
R3-3	9.94	4.99	0.00	-5.01	-9.94
R3-4	9.93	4.98	0.00	-5.02	-10.28
R3-5	9.95	4.99	0.00	-5.00	-9.93

characteristics of the FET multiplexing switches that were employed. Although the nonlinearity could have been eliminated by a power supply design change, it was not considered to be of significance to the operation of the system.

3.3 ANALOG COMPUTER TESTING

3.3.1 Description Of Computer Setup

A five degree of freedom (constant velocity, u) analog simulation was set up for the purpose of demonstrating the performance of the multiplexing equipment in a representative dynamic loop. The contract statement of work indicated that the simulation should be based on the test aircraft dynamics. Since the NC131H aircraft is capable of representing a range of dynamic characteristics, it was agreed between the General Dynamics project leader and the Flight Dynamics Laboratory program manager that the computer simulation would be capable of permitting adjustments to the airframe natural frequencies.

3.3.2 Description Of Simulation Aircraft Dynamics

The aircraft simulation was based on two flight conditions, one at M = 0.9 at 30,000 feet, representing a highly responsive airplane, and one at M = 0.45 at 30,000 feet to demonstrate flight at a low dynamic pressure.

This range of flight conditions yields closed loop natural frequencies that vary by a factor of 2.28. It was assumed, for the purpose of this simulation, that variations in the stability derivatives due to Mach number were unimportant. A listing of pertinent simulation parameters is presented in Table 3-2. The primary purpose of this simulation was to demonstrate that the airplane dynamics were not adversely affected by the presence of multiplexing in the flight control system data paths.

The equations of motion that were mechanized in this simulation are shown in Figure 3-1. The flight control system was simulated as shown in Figure 3-2, wherein the time constants were selected to yield good handling qualities.

3.3.3 Description Of Tests

The aircraft closed-loop dynamics were set up first without multiplexing in the loop. Rudder, aileron and

TABLE 3-2
ANALOG SIMULATION PARAMETERS

Parameter Name	Value	Parameter Name	Value
Weight	34,200 Lbs.	C_{y_r}	.3003/rad
Reference Area, S	608 ft^2	C_{y_p}	.0442/rad
Long. Ref. Length, $\bar{c}$	16 ft	C_{n_β}	.00263/deg
Lat.-Dir. Ref. Length, b	42.7 ft	$C_{n_{\delta r}}$	-.00123/deg
I_{xx}	25,150 slug-ft^2	$C_{n_{\delta a}}$	-.00012/deg
I_{yy}	155,600 slug-ft^2	C_{n_r}	-.3053/rad
I_{zz}	175,500 slug-ft^2	C_{n_p}	-.01668/rad
J_{xz}	800 slug-ft^2	C_{l_β}	-.00174/deg
$C_{L_{\delta_H}}$	.0091/deg	$C_{l_{\delta r}}$	.000077/deg
C_{L_α}	.0822/deg	$C_{l_{\delta a}}$	-.0008/deg
α_{L_o}	-.04 deg	C_{l_r}	.0614/rad
$C_{m_{\delta_H}}$	-.0101/deg	C_{l_p}	-.245/rad
C_{m_α}	-.0057/deg		
C_{m_o}	.0055	K_1	1.5 deg/g
$C_{N_q} - C_{N_{\dot\alpha}}$	5.61/rad	K_2	.325 deg/deg/sec
$C_{m_q} + C_{m_{\dot\alpha}}$	-5.31/rad	K_3	.125 deg/deg/sec
$C_{D_{min}}$	.0211	K_4	9.2 deg/g
$C_{D_i} / (C_L - C_{L_o})^2$	.159	K_5	1.0 deg/deg/sec
C_{L_o}	.060	τ_1	0 sec
C_{y_β}	-.01624/deg	τ_2	3.0 sec
$C_{y_{\delta r}}$	.00266/deg	τ_3	0 sec
$C_{y_{\delta a}}$	.000257/deg	τ_4	3.0 sec

$$u = \text{constant}$$

$$V = \sqrt{u^2+v^2+w^2}$$

$$\dot{v} - wp + ur - g\cos\theta\sin\phi = \frac{1}{m}\left[C_{y_\beta}\beta + C_{y_{\delta_a}}\delta_a + C_{y_{\delta_r}}\delta_r + C_{y_p}\frac{pb}{2V} + C_{y_r}\frac{rb}{2V}\right]\left[\frac{\rho S V^2}{2}\right]$$

$$\dot{w} - uq + vp - g\cos\theta\cos\phi = \frac{1}{m}\left[-C_L\cos\alpha - C_D\sin\alpha - (C_{N_q} + C_{N_\alpha})\frac{q\bar{c}}{2V}\right]\left[\frac{\rho S V^2}{2}\right]$$

$$\dot{p} - \frac{1}{I_{xx}}\left[(I_{yy} - I_{zz})qr - I_{xz}(\dot{r} + pq)\right] = \frac{1}{I_{xx}}\left[C_{\ell_\beta}\beta + C_{\ell_{\delta_a}}\delta_a + C_{\ell_{\delta_r}}\delta_r + (C_{\ell_p}p + C_{\ell_r}r)\frac{b}{2V}\right]\left[\frac{\rho S V^2 b}{2}\right]$$

$$\dot{q} - \frac{1}{I_{yy}}\left[(I_{zz} - I_{xx})pr - I_{xz}(r^2 - p^2)\right] = \frac{1}{I_{yy}}\left[C_{m_o} + C_{m_\alpha}(\alpha - \alpha_{Lo}) + C_{m_{\delta_H}}\delta_H + (C_{m_q} + C_{m_\alpha})\frac{q\bar{c}}{2V}\right]\left[\frac{\rho S V^2 b}{2}\right]$$

$$\dot{r} - \frac{1}{I_{zz}}\left[(I_{xx} - I_{yy})pq - I_{xz}(\dot{p} - qr)\right] = \frac{1}{I_{zz}}\left[C_{n_\beta}\beta + C_{n_{\delta_a}}\delta_a + C_{n_{\delta_r}}\delta_r + (C_{n_p}p + C_{n_r}r)\frac{b}{2V}\right]\left[\frac{\rho S V^2 b}{2}\right]$$

$$C_L = C_{L_\alpha}(\alpha - \alpha_{Lo}) + C_{L_{\delta_H}}\delta_H$$

$$C_D = C_{D_{MIN}} + \frac{C_{D_I}}{(C_L - C_{Lo})^2}(C_L - C_{Lo})^2 \quad ; \quad C_{Lo} = C_L \text{ at } C_{D_{MIN}}$$

Figure 3-1 ANALOG SIMULATION EQUATIONS OF MOTION

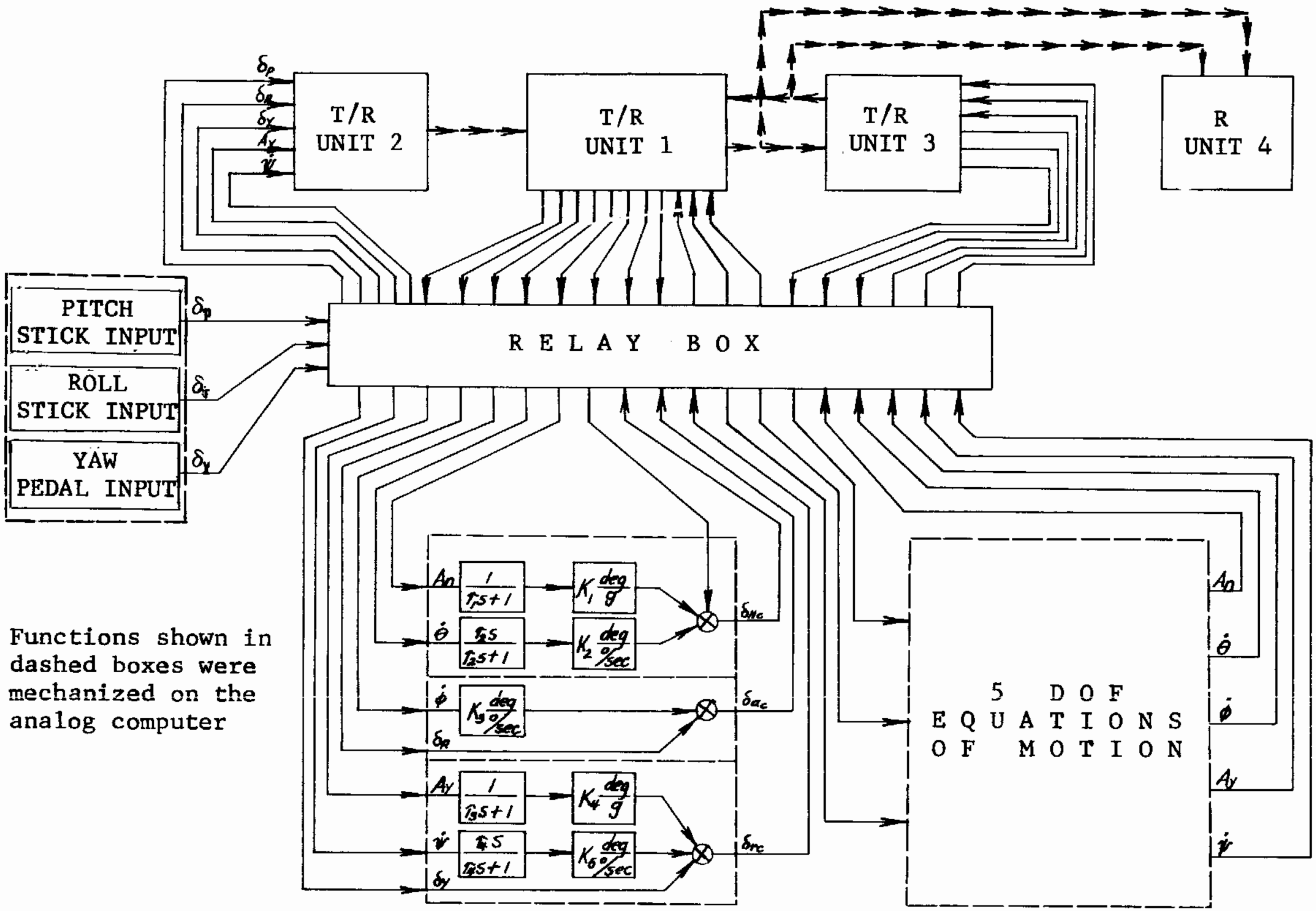


Figure 3-2 INTERFACE OF COMPUTER SIMULATION WITH MULTIPLEXING EOUIPMENT

elevator pulses, initial conditions on angle-of-attack and sideslip angle, and 1-cos shaped gust inputs were applied and responses recorded. The multiplexing equipment was then inserted in the flight control system as shown in Figure 3-2 and the input signals were repeated. Comparisons were made with and without the multiplexing equipment in the loop for 400, 200, 100 and 50 per second update rates. Test data in the form of analog strip chart recordings for the initial conditions of angle-of-attack and sideslip angle are shown in Figures 3-3 through 3-6. Additionally, qualitative pilot evaluations of the multiplexing equipment performance were made with the use of the cockpit simulator.

3.3.4 Analog Test Results

The performance of the multiplexing equipment in conjunction with the analog computer simulation was excellent. As evidenced from the data in Figures 3-3 through 3-6, the only significant effect of the multiplexing equipment was to cause a reduction in the short-period damping ratio for the high speed flight condition at the lower data rates. This result was anticipated due to the relatively low ratio of the airplane natural frequency to the sample rate. Pilot in the loop evaluations indicated an inability on the part of the pilot to detect when the multiplexing equipment was in the loop. All tests conducted with analog computer aircraft simulation indicated that the equipment would operate satisfactorily in the TIFS aircraft.

3.4 ELECTROMAGNETIC INTERFERENCE TEST DATA

3.4.1 Description Of Test Apparatus

EMI testing on the Flight Test Multiplexing equipment was conducted in an eleven-foot by twenty-two foot shielded enclosure provided with filtered 115 volt AC power. Hewlett-Packard spectrum analyzers were used in the measurement and determination of all electromagnetic interference characteristics. To verify EMI compliance with MIL-STD 461A specifications, the test equipment was calibrated prior to testing by use of laboratory standards which are transferable to the National Bureau of Standards. Individual items of test equipment and assessories used in conjunction with each MIL-STD-462 test method are listed in Appendix A in Table A-1. The tabulated bandwidth for the spectrum analyzers is presented in Table A-2.

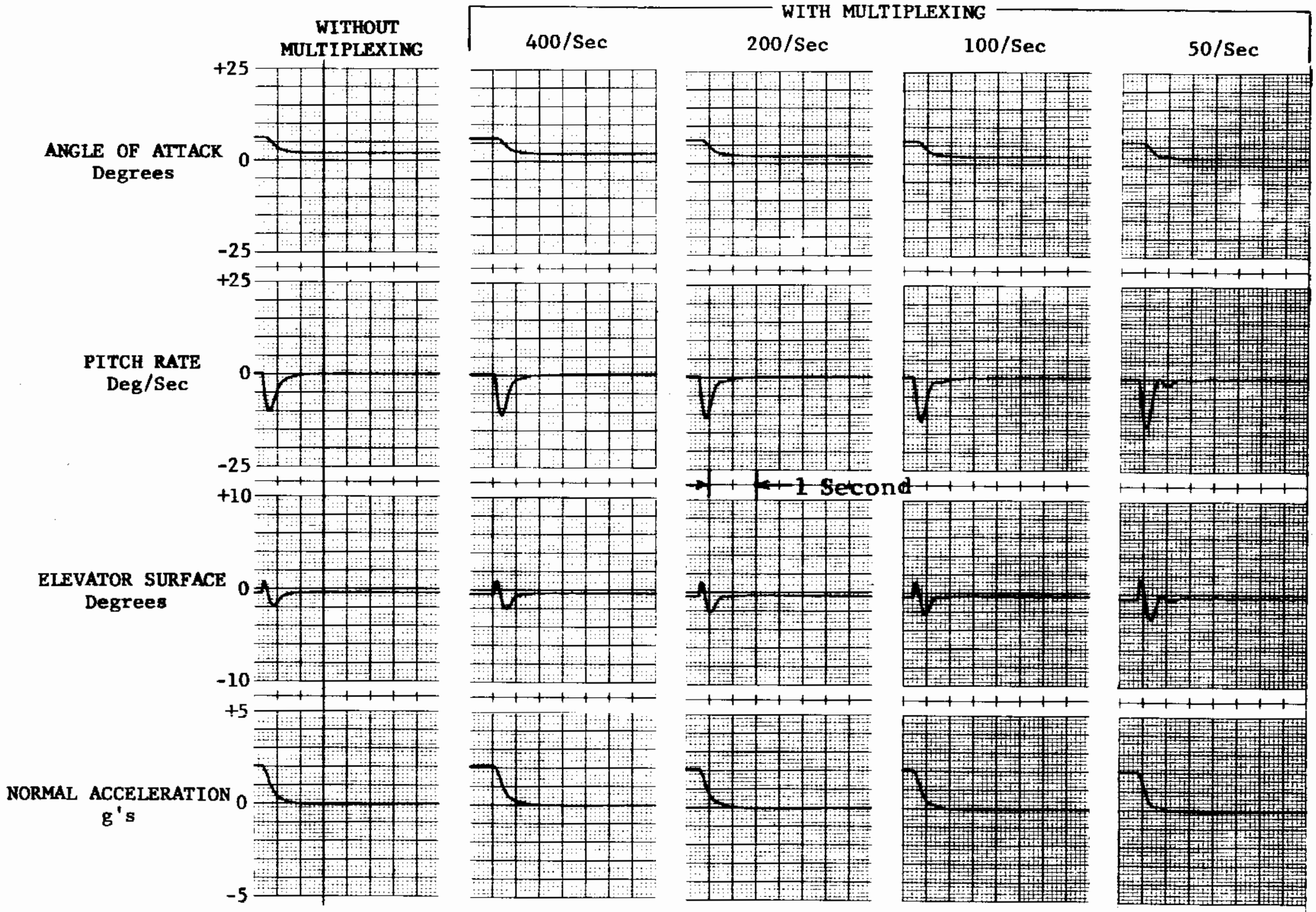


Figure 3-3 DAMPED AIRFRAME RESPONSE TO INITIAL CONDITION ON ANGLE OF ATTACK - HIGH SPEED FLIGHT CONDITION

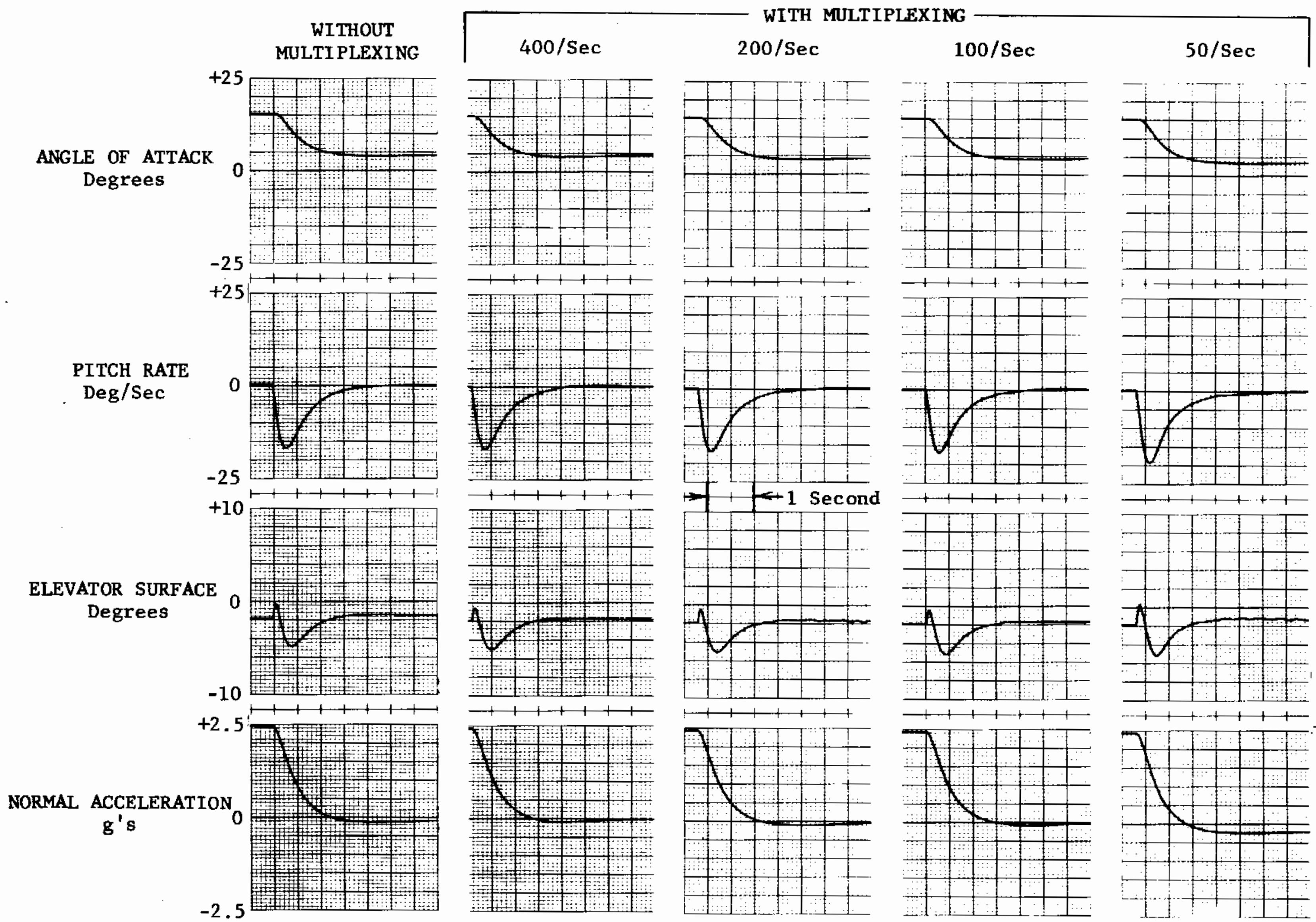


Figure 3-4 DAMPED AIRFRAME RESPONSE TO INITIAL CONDITION ON ANGLE OF ATTACK - LOW SPEED FLIGHT CONDITION

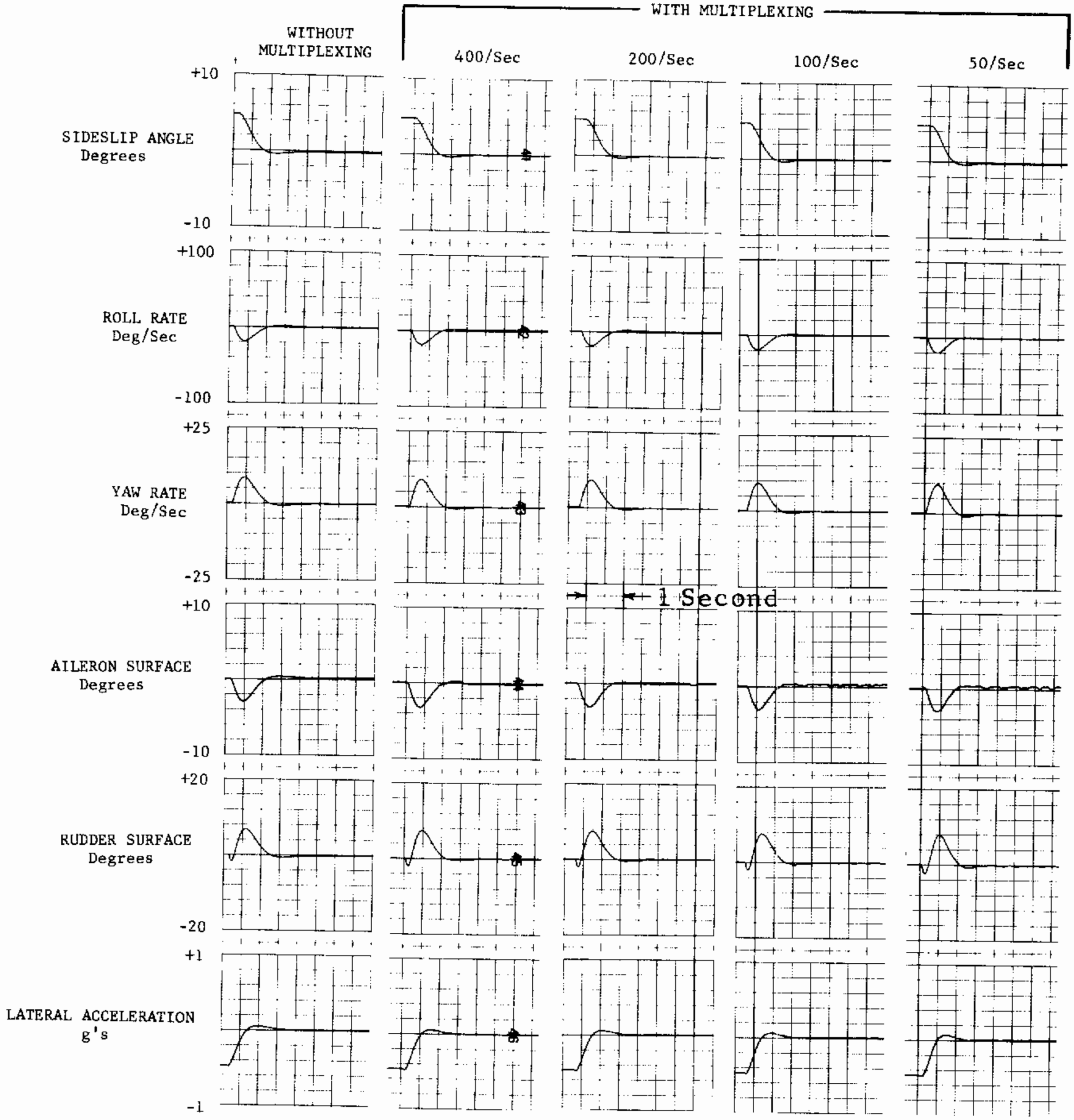


Figure 3-5 DAMPED AIRFRAME RESPONSE TO INITIAL CONDITION ON SIDESLIP ANGLE - HIGH SPEED FLIGHT CONDITION

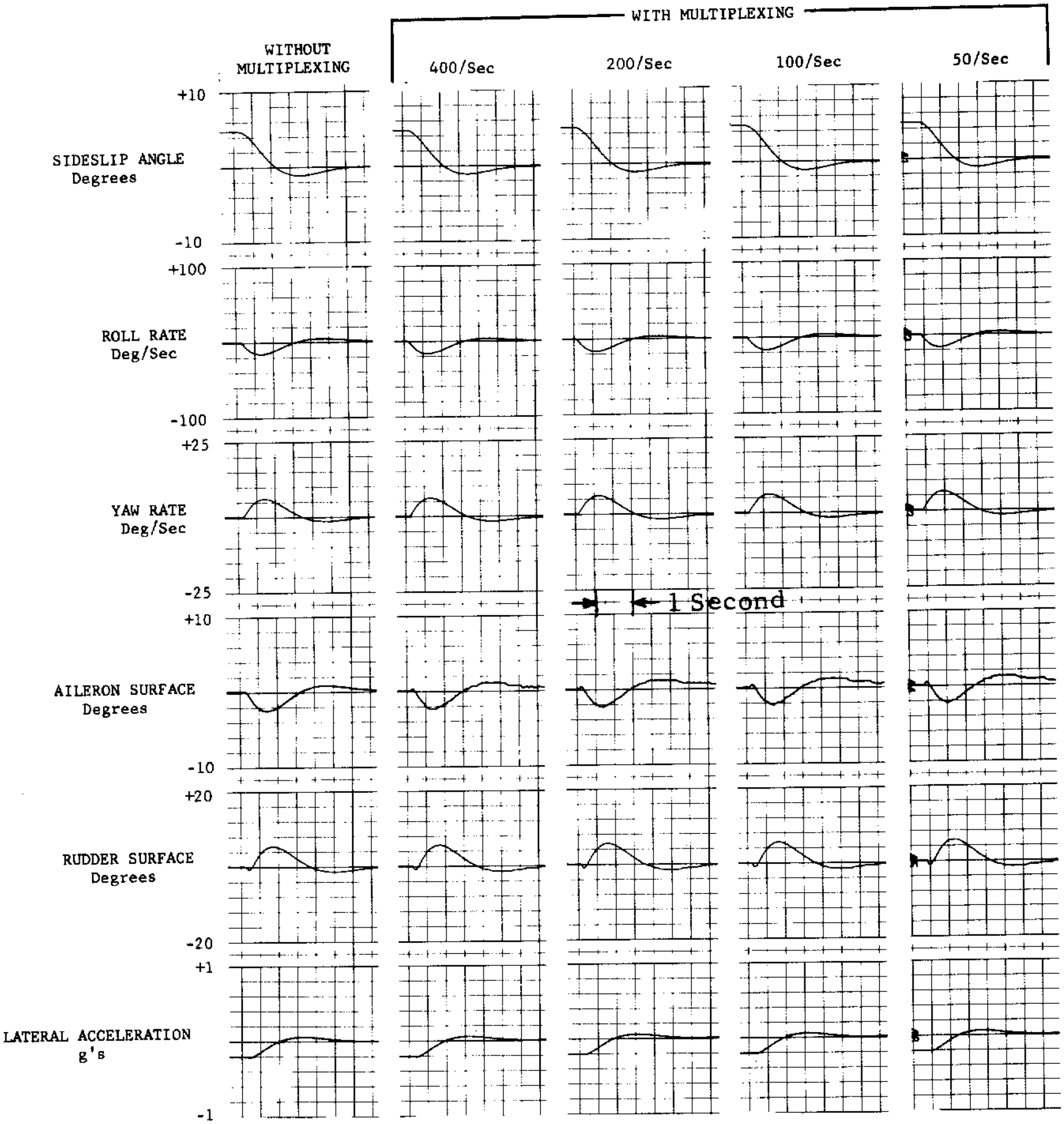


Figure 3-6 DAMPED AIRFRAME RESPONSE TO INITIAL CONDITION ON SIDESLIP ANGLE - LOW SPEED FLIGHT CONDITION

3.4.2 Test Configuration

The Multiplexing equipment was installed in the shielded enclosure and bonded to the ground plane in such a manner as to simulate installation conditions (see Figure 3-7). A ground plane of 0.020-inch copper was installed as illustrated in Figure 3-8 and extended 10 centimeters beyond the front of the equipment. All cables were supported 5 centimeters above the ground plane.

3.4.3 Test Procedures

The Multiplexing equipment was tested during the period of June 15 through June 19, 1972. The detailed procedures followed during the EMI Test program can be found in the test plan document, FZE-1159, dated 4 February 1972. The Multiplexing equipment was operated as described in the above document.

3.4.4 Test Data

The data presented in this document are of two types. First, the results of testing for the narrowband and broadband emissions are presented in the form of CRT photographs of spectrum analyzer displays. Narrowband and broadband limits are displayed on overlays which are attached to the CRT. The methods used to derive overlays are detailed in the test plan. Second, tables of tabulated data used in the performance of radiated susceptibility test are presented.

3.4.5 Test Results

The results of the test program are summarized in Table 3-3. These results are discussed in the following paragraphs.

3.4.5.1 Test Method CE03, Conducted Emissions

When conducted interference tests were performed on the DC and AC power leads, the measured levels of broadband and narrowband signals did not exceed the specification limit. Four separate measurements were made in this test to cover the frequency range. The data are presented in Appendix A in Figures A-1 through A-8.

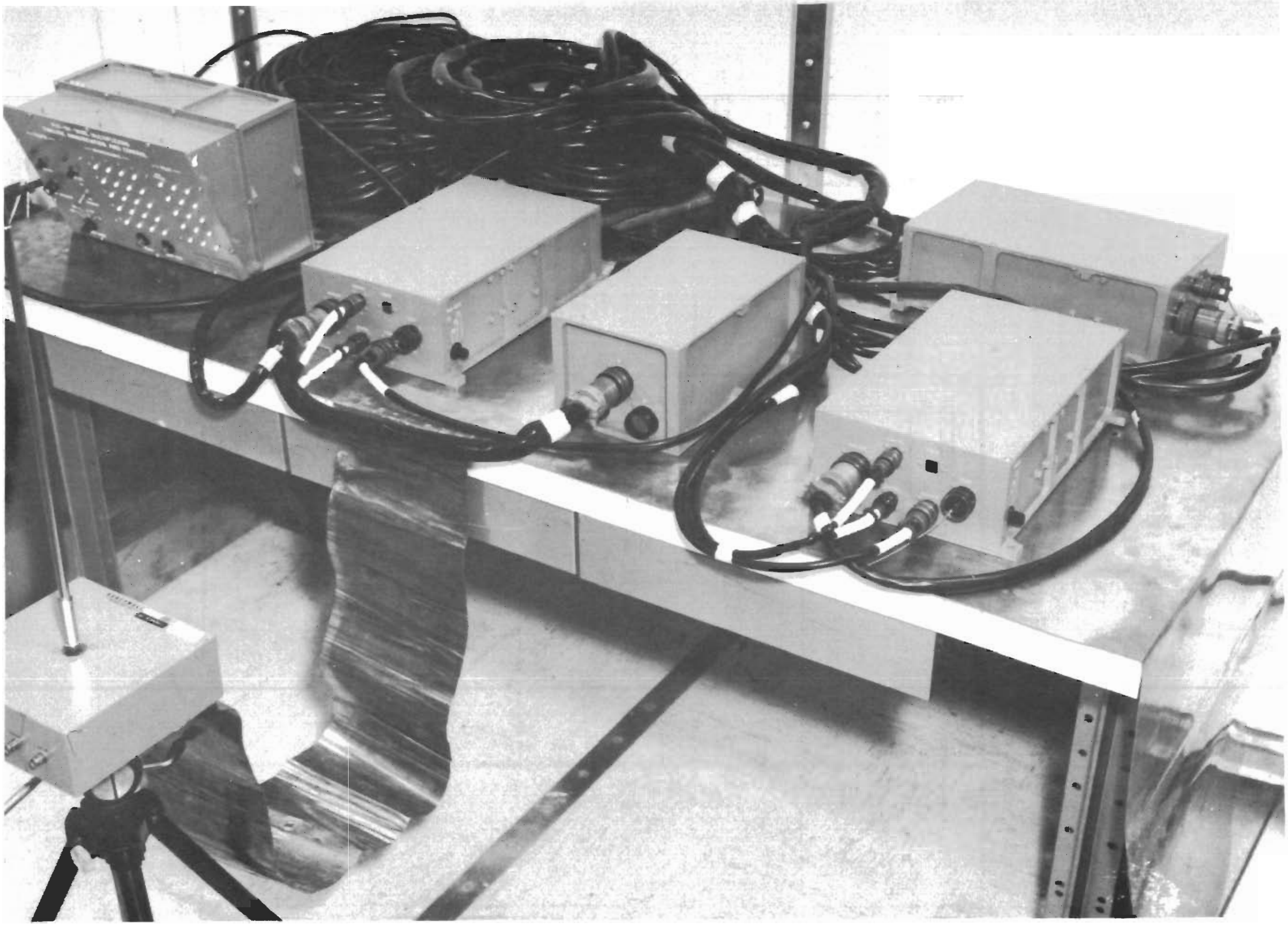


Figure 3-7 EMI TEST EQUIPMENT ARRANGEMENT

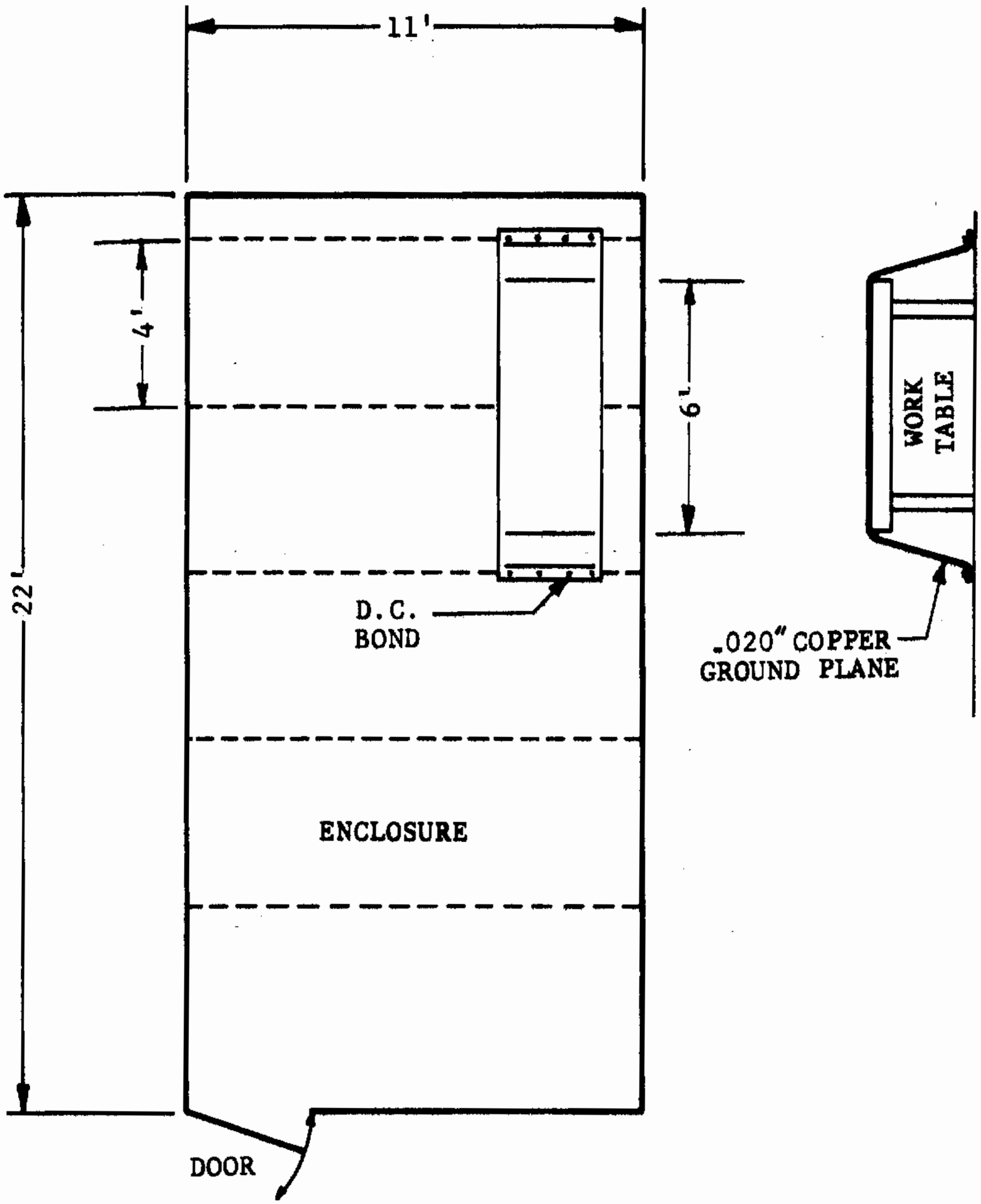


Figure 3-8 SCREEN ROOM AND GROUND PLANE PROVISIONS

3.4.5.2 Test Method CS01, Conducted Susceptibility

When conducted susceptibility tests were performed on DC and AC power leads, the equipment under test did not exhibit evidence of malfunction or degradation of performance.

3.4.5.3 Test Method CS02, Conducted Susceptibility

The performance of the multiplexing equipment was not degraded when conducted susceptibility tests were performed on the DC and AC power leads.

3.4.5.4 Test Method CS06, Conducted Susceptibility

The multiplexing equipment did not exhibit evidence of malfunction or degradation of performance when the specified transient was applied to its AC and DC power leads.

3.4.5.5 Test Method RE02, Radiated Emissions

The test data for the radiated emission tests are presented in Appendix A in Figures A-9 through A-11. As seen in Figure A-11 interference signals between 32 MHz and 150 MHz were noted which were above the specified limits. These signals were identified as narrowband emissions. The worst case was 14 dB above the limit at 64 MHz. It was determined that the interference signals were being radiated from the cable harnesses and cable connectors and could be satisfactorily reduced only by replacing all connectors with RFI types. Due to cost and program delay associated with the modification, the Air Force project manager was notified and was sent the data for review. He indicated that, although the level was outside the overlay boundries, it was adequate for this program.

3.4.5.6 Test Method RS03, Radiated Susceptibility

The multiplexing equipment did not exhibit evidence of malfunction or degradation of performance when exposed to the specified electric fields. The tabulated data used in the performance of the radiated susceptibility test are presented in Table A-3.

3.4.5.7 Test Method RS02, Magnetic Induction Field

No malfunction or degradation in performance was detected when the multiplexing equipment, and all associated

Table 3-3 EMI Test Summary

Test Sample Flight Test Multiplexing System
Contractor General Dynamics
Specification MIL-STD-461A and Notice 3

Test Method No.	Initial Test Dates		Initial Test Results		Overlimit Conditions	Remarks
	Start	End	Under	Over		
CE03	6-15-72	6-15-72	X			
CS01	6-16-72	6-16-72	X			
CS02	6-16-72	6-16-72	X			
CS06	6-16-72	6-16-72	X			
RE02	6-15-72	6-15-72		X	Narrowband signals between 32 and 150 MHz	Interference signals radiating from interconnecting cables and cable connectors
RS02	6-19-72	6-19-72	X			
RS03	6-15-72	6-15-72	X			

interconnecting cables were exposed to the specified magnetic induction fields.

3.5 ENVIRONMENTAL TESTS

3.5.1 General

The purpose of this portion of the test program was to demonstrate the ability of the equipment developed under this contract to comply with the operational and safety requirements of the equipment specification when subjected to the environmental test conditions as stated in later paragraphs. One each of the multiplexing equipments was subjected to the test environments.

3.5.2 Test Criteria

The equipment that was subjected to this test program had previously met the operational requirements of the equipment performance specification.

Deterioration or material failure of any part which could prevent the equipment from meeting the operational or safety requirements for this program was considered to be a test failure. A resolution of each problem encountered was determined and incorporated into the equipment before testing was resumed. A discussion of equipment malfunctions and their dispositions is contained at the end of each test section.

All test equipment utilized during this test program compiled with the applicable requirements of paragraph 3.1.3 of MIL-STD-810B.

3.5.3 Test Sequence And Schedule

Testing was conducted in the following sequence:

1. Vibration
2. Mechanical Shock
3. High Temperature
4. Low Temperature
5. Voltage and Frequency Variation.

Testing was conducted between the periods of 30 June 1972 and 28 August 1972.

3.5.4 Standard Test Conditions

Unless otherwise specified, all testing was conducted under the following standard test conditions:

Temperature - 23 $\pm$ 10°C

Relative Humidity - 50 percent $\pm$ 30 percent

Atmospheric Pressure - 28.5 $^{+3.0}_{-4.5}$ inches of mercury.

3.5.5 Test Procedures

3.5.5.1 Visual Inspection

The equipment tested was visually examined to determine conformance to the engineering specification requirements, outline drawings, and any requirement not covered by a test. No discrepancies were noted.

3.5.5.2 System Operation

While the multiplexing equipment was undergoing the environmental tests, the operation of the equipment was monitored for satisfactory performance. Satisfactory performance was verified during the tests by continuously monitoring reconstructed sine wave signals at the output of randomly selected analog channels. In addition, the multiplexing system failure annunciation lights were monitored during all tests. Illumination of any of these lights was defined as an equipment failure and the cause was corrected. It should be noted that all failures that were encountered during the environmental testing resulted in illumination of a failure light.

3.5.5.3 Vibration Test

3.5.5.3.1 Test Equipment. The following test Equipment was utilized for this test:

1. Vibration Controller System - Ling Electric - R-1007-C, PP-20/20
2. Vibration Exciter - MB Manufacturing Company - C25H
3. Vibration Recording System
    a. Accelerometers - Endevco Model 2222A & MB Model 124

b. Amplitude Servomonitor - Spectral Dynamics Model 5D105A
c. Electronic Tracking Filters - Spectral Dynamics Model SD1012
d. Galvanometer Amplifiers - Endevco Model 2710Z
e. Logarithmic Converters - F. L. Mosely Model 60B
f. X-YY' Recorder - Honeywell Model 580
g. Counter - Hewlett Packard Model 521A
h. Oscilloscope - Tektronix Model 549
i. Audio Oscillator - Spectral Dynamics Model SD104A-5
j. Timer - Standard Electric - Model SM60.

3.5.5.3.2 Test Procedure. The equipment tested was attached to a rigid vibration test fixture capable of providing the vibrational inputs over the frequency range specified in Figure 514-1, Curve C of Specification MIL-STD-810B. The equipment is shown in Figure 3-9 with the signal transfer unit mounted on the vibration table. The method of attachment to the test fixture was the same as the intended attachment in the test aircraft. Accelerometers were mounted on and within the test articles in the following locations:

A.	Failure annunciator Unit:	1. Card No. 1
		2. Diode Mounting Plate
		3. Center of Front Panel
		4. Upper Rear Panel
B.	Transmitter - Receiver:	1. Card No. 8
		2. Card No. 15
		3. Card No. 9
		4. Diode Mounting Plate
C.	Signal Transfer Unit:	1. Relay K7
		2. Center of Tray.

The equipment was operating during the test and it was monitored for any evidence of adverse performance throughout the test.

A resonance survey was conducted in each of the three mutually perpendicular axis by slowly varying the vibration inputs over the range specified in Figure 514-1, Curve C of MIL-STD-180B. The responses of the equipment under test were recorded on a X-YY' recorder. The resonance survey in each axis was of 15 minutes duration.

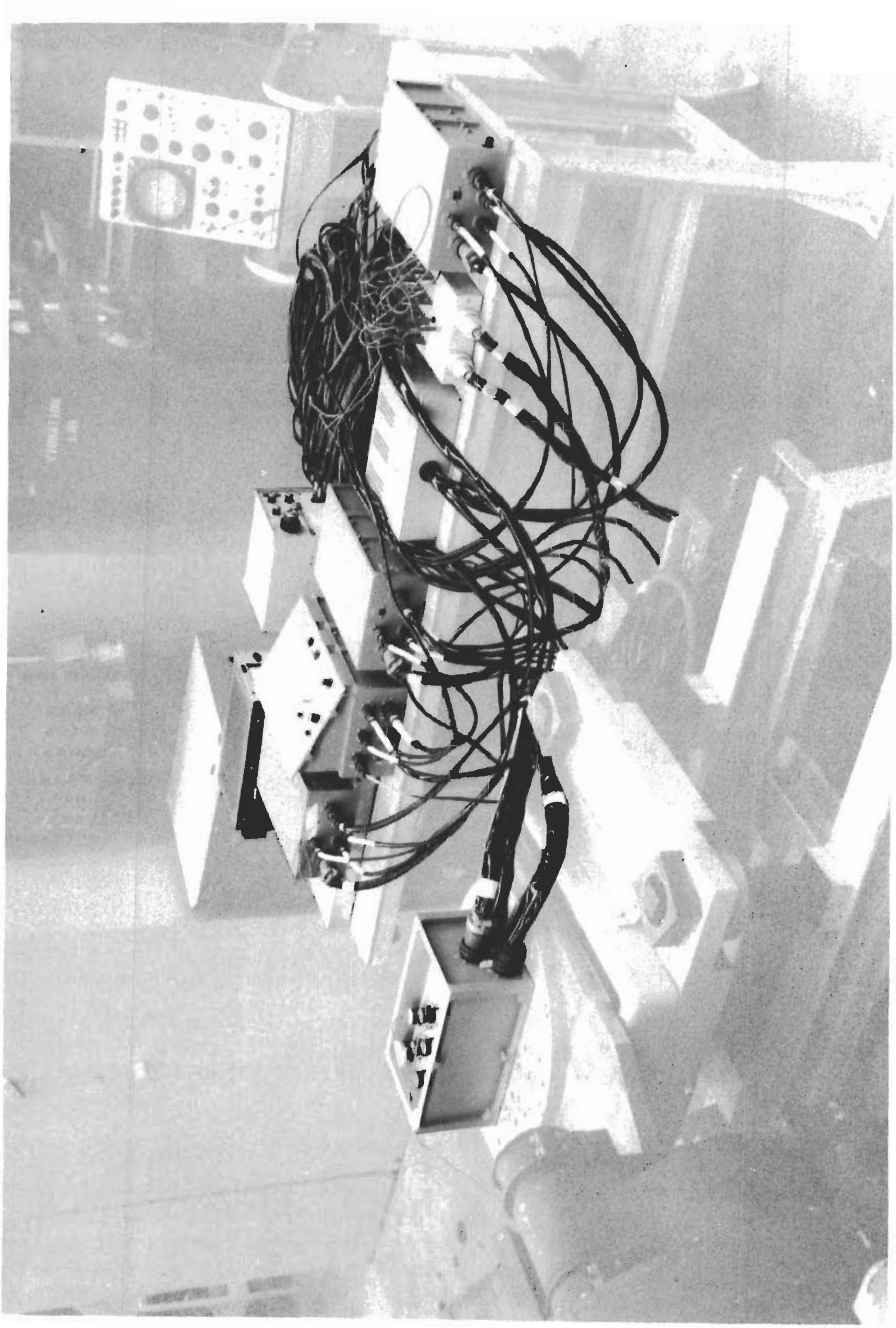


Figure 3-9 MULTIPLEXING EQUIPMENT PREPARED FOR VIBRATION TESTING.

Following the resonance survey, the equipment was vibrated for a period of 5 minutes at each of the points determined in the above resonance survey.

A complete visual examination and operational check was made following completion of the vibration test.

If the same resonance occurred in more than one axis of vibration, the resonance dwell was not repeated on these resonance points.

3.5.5.3.3 Discussion and Results. The equipment under test was subjected to the vibration test in accordance with the above test procedure. The results of the resonance survey are shown in Appendix B (Figures B-1 through B-9).

Resonance dwell was conducted for a period of 5 minutes at each of the resonance points shown below.

A. Failure Annunciator Unit:
   1. Lateral Axis
      122 "g" response at 202 Hz on front panel, center
   2. Longitudinal Axis
      14 "g" response at 500 Hz - Card No. 1
   3. Vertical Axis
      46 "g" response at 125 Hz - Card No. 1

B. Transmitter-Receiver Unit
   1. Lateral Axis
      64 "g" at 350 Hz - Card No. 9
   2. Longitudinal Axis
      55 "g" at 495 Hz - Card No. 9
   3. Vertical Axis
      23 "g" at 350 Hz - Card No. 8
      40 "g" at 393 Hz - Card No. 15

C. Signal Transfer Unit
   1. Lateral Axis
      32 "g" response at 469 Hz - center of tray
   2. Longitudinal Axis
      24 "g" response at 317 Hz - center of tray
   3. Vertical Axis
      120 "g" response at 152 Hz on center of tray
      70 "g" response at 152 Hz on relay K5.

Four discrepancies occurred as a result of this test and they were repaired and corrections implemented to preclude their reoccurrence. Two wires in Unit 4 were not properly supported and broke during the test, and a capacitor on a printed circuit card in Unit 1 broke. The broken wires were reattached and retied in such a manner as to provide additional support. The capacitor leads were reshaped and the capacitor was glued to the circuit board. The capacitor fix was also incorporated on similar boards in each of the other units. One maintenance light, C2, failed during the vibration test.

3.5.5.4 <u>High Temperature</u>

3.5.5.4.1 <u>Test Equipment</u>. The following test equipment was utilized during this test:

1. Temperature Chamber - Tenney
2. Temperature Recorder - Brown, Model 153 x 62 P16-x-13, -100°F to +500°F

3.5.5.4.2 <u>Test Procedure</u>. The equipment to be tested was mounted in the test chamber in a manner similar to that of its installation in the test aircraft. Thermocouples were installed to monitor temperature stabilization.

Power was applied to the equipment and an operational check was conducted. The chamber controls were then adjusted to obtain and maintain a temperature of +71°C, $\pm$ 2°C for a period of four hours. At the conclusion of this four-hour period, and while still maintaining these test conditions, the equipment performance was checked.

Following completion of the functional check, the equipment was returned to room ambient conditions were another performance check was made and the equipment was examined for any deterioration resulting from this exposure.

3.5.5.4.3 <u>Discussion and Results</u>. During the high temperature (71°C) test, two failures and one operational problem were encountered. The two failures were concerned with a 0.5 amp fuse and a 5 amp circuit breaker. It was determined that the trip point on both the fuse and the circuit breaker were reduced by approximately 30 percent at this elevated temperature. Both the fuse and the circuit breaker were replaced by slightly higher rated components. These higher rated parts still provide adequate protection.

An additional problem encountered at the elevated temperature concerned the occurrence of a false failure indication on the annunciation panel. This problem was traced to an intermittent oscillation that would occur in an enable gate to the particular lamp driver. The cause of the oscillation was found to be a resistor of too large a value on the input gate. The resistor on the faulty gate, as well as all the other similar gates, were changed to a lower value to eliminate the oscillation.

3.5.5.5 Low Temperature

3.5.5.5.1 Test Equipment. The test equipment is the same as that used in paragraph 3.5.5.4.

3.5.5.5.2 Test Procedure. With no power applied to the equipment under test, the test chamber controls were adjusted to obtain and maintain a temperature of -54°C, ±2°C. This temperature was maintained for a period of four hours, after which power was applied to the system and it was checked for proper functional operation after a five-minute warm-up period.

Following completion of this test, the environment was returned to room ambient conditions and functionally checked and visually examined for evidence of any detrimental effects resulting from the exposure.

3.5.5.5.3 Disucssion and Results. The low temperature test was conducted in accordance with the above procedure and the loss of several channels of analog output signals was encountered while the equipment was stabilized at -54°C. This problem was traced to a -15 volt regulator circuit on the input to the analog to digital and digital to analog converters. Earlier tests had indicated that the converters were performing satisfactorily without the regulator, so this circuit was by-passed in all units. One additional occurrence that was noted at the low temperature condition was the failure of the -15 volt power supply in Unit 1 to operate upon initial turn-on of the equipment. The power supply would operate within approximately 2 minutes after power was turned on and this warm-up time is well withing the specified requirement of five minutes maximum, and therefore, is not a test failure, but is mentioned here for information purposes only.

3.5.5.6 Mechanical Shock

3.5.5.6.1 Test Equipment. The following equipment was utilized during this test:

1. Memory Scope, Tektronix - Model 549
2. Accelerometer, Endevco Dodel 2252
3. Bandpass Filter, Kron-Hite, Model 330M
4. Charge Amplifier, Endeco Model 2718
5. Barry Impact Shock Machine, Model 150-400V0

3.5.5.6.2 Test Procedure. This crash safety test was conducted to verify the structural integrity of the equipment mounting means. An Equipment chassis with no internal components but with dummy loads which simulated the mass distribution of the system components, was mounted to the shock machine first in the manner of Units 1, 2, and 3 and then in the manner of Unit 4.

Two shocks were applied to each test configuration in a direction along each of the three mutually perpendicular axes for a total of 12 shocks for each mounting configuration. The shock impulse shape was a half sine in accordance with Figure 516-2 of MIL-STD-810B at an amplitude of 30 peak g's and 11 millisecond duration.

Following completion of the shock test, the test specimen was visually examined for evidence of any structural damage as a result of this test.

3.5.5.6.3 Discussion and Results There was no detrimental effect to the test specimen when tested to the above procedure in the two different mounting configurations. No test was conducted on the signal transfer unit since it weighs only 7 pounds and is mounted with four number 10 screws. This would have given a loading on these mounting screws under test of a magnitude less than those of the failure annunciator unit which is mounted with eight number 10 screws and weighs 17 pounds. Therefore, there was no need to test the signal transfer unit; verification of compliance is by similarity to the failure annunciator unit.

3.5.5.7 Voltage and Frequency Variation Test

3.5.5.7.1 Test Equipment. The following test equipment was utilized during this test:

1. Variable Voltage and Frequency Power Supply - Leach
2. Transient Voltage Generator - General Dynamics
3. Memoryscope - Tektronix, Model 549
4. Counter, Hewlett-Packard, Model 521
5. Digital Voltmeter, Cimron, Model P9300

3.5.5.7.2 Test Procedure. All components of the system were interconnected under standard conditions and operated to verify proper equipment performance. Following this operational check, the input power to the system was changed to the limits of MIL-STD-704A and as delineated in Table 3-4. The equipment performance characteristics were again checked under these emergency power conditions. When tested under these power conditions, it was required that the equipment meet all performance requirements, remain safe and not suffer any permanent physical or operational damage. During the power transient test, the system was monitored to detect any adverse effect on the system performance. AC and DC transients were initiated independently.

3.5.5.7.3 Discussion and Results. There were no detrimental effects on the system performance when subjected to the power variation tests as described above.

TABLE 3-4

EMERGENCY POWER CONDITIONS AND
TRANSIENT VOLTAGE VARIATIONS

EMERGENCY POWER CONDITIONS			
TEST CONDITION	AC VOLTAGE	DC VOLTAGE	FREQUENCY
a	104	16	360
b	104	16	440
c	122	24	360
d	122	24	440

TRANSIENT VOLTAGE VARIATIONS			
TIME	AC VOLTAGE	TIME	DC VOLTAGE
0.1 Sec.	180	0.1 Sec.	78
0.5 Sec.	162	0.5 Sec.	62
1.0 Sec.	145	1.0 Sec.	49
5.0 Sec.	124	5.0 Sec.	30

SECTION 4

TIFS AIRCRAFT INSTALLATION

4.1 GENERAL

The multiplexing equipment was installed by Calspan personnel during the 100-hour inspection of the TIFS aircraft. The three transmitter/receiver units were mounted on a shelf that was attached to the ballast box in the aft section of the fuselage (see Figure 4-1). The failure annunciation and control unit was mounted on the upper portion of the Test Engineer #2 console. The multiplex data transmission lines were routed along the handrails that run the entire length of the fuselage (see Figure 4-2). The transmission lines were doubled back on themselves several times in order to accommodate the 200-foot cable lengths.

Four switches were mounted on the Test Engineer #1 console to control the portions of the system where the multiplexed signals were used (see Figure 4-3). These four data paths, selectable in any combination, include: (1) the pilot command signals, (2) the feel system feedback signals, (3) the surface actuator command signals, and (4) the surface actuator feedback signals. A diagram of the TIFS fly-by-wire flight control system showing the location of the multiplexing units is shown in Figure 4-4.

4.2 GROUND CHECKOUT

After installation of the multiplexing equipment, ground checkout proceeded in several steps. The first step was to check continuity of the cables that were assembled by Calspan to interface the multiplexing relay box with the analog patch panel. The input power cable (also assembled by Calspan) was checked prior to being mated with the multiplexing equipment. During this phase of the checkout, the 28-volt DC input wire was found to have been connected to the wrong terminal on the TIFS power terminal strip. This error was corrected prior to the continuation of the ground checkout.

The patch panel of the analog computer that had been wired for the multiplexing program was put in place at this time and sine-wave signals were supplied to each multiplexing input. The proper TIFS outputs were monitored

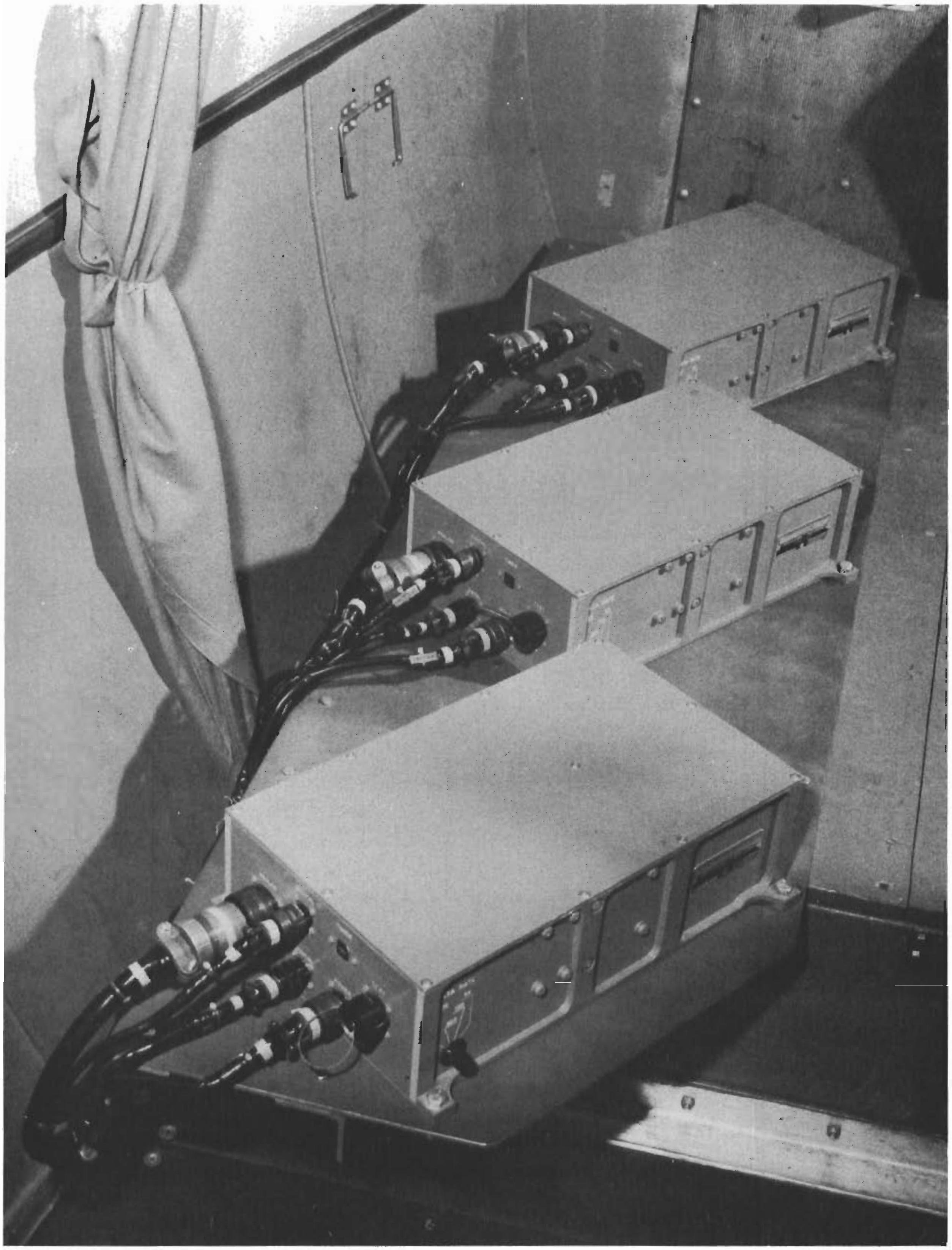


Fig. 4-1 INSTALLATION OF TRANSMITTER/RECEIVER UNITS

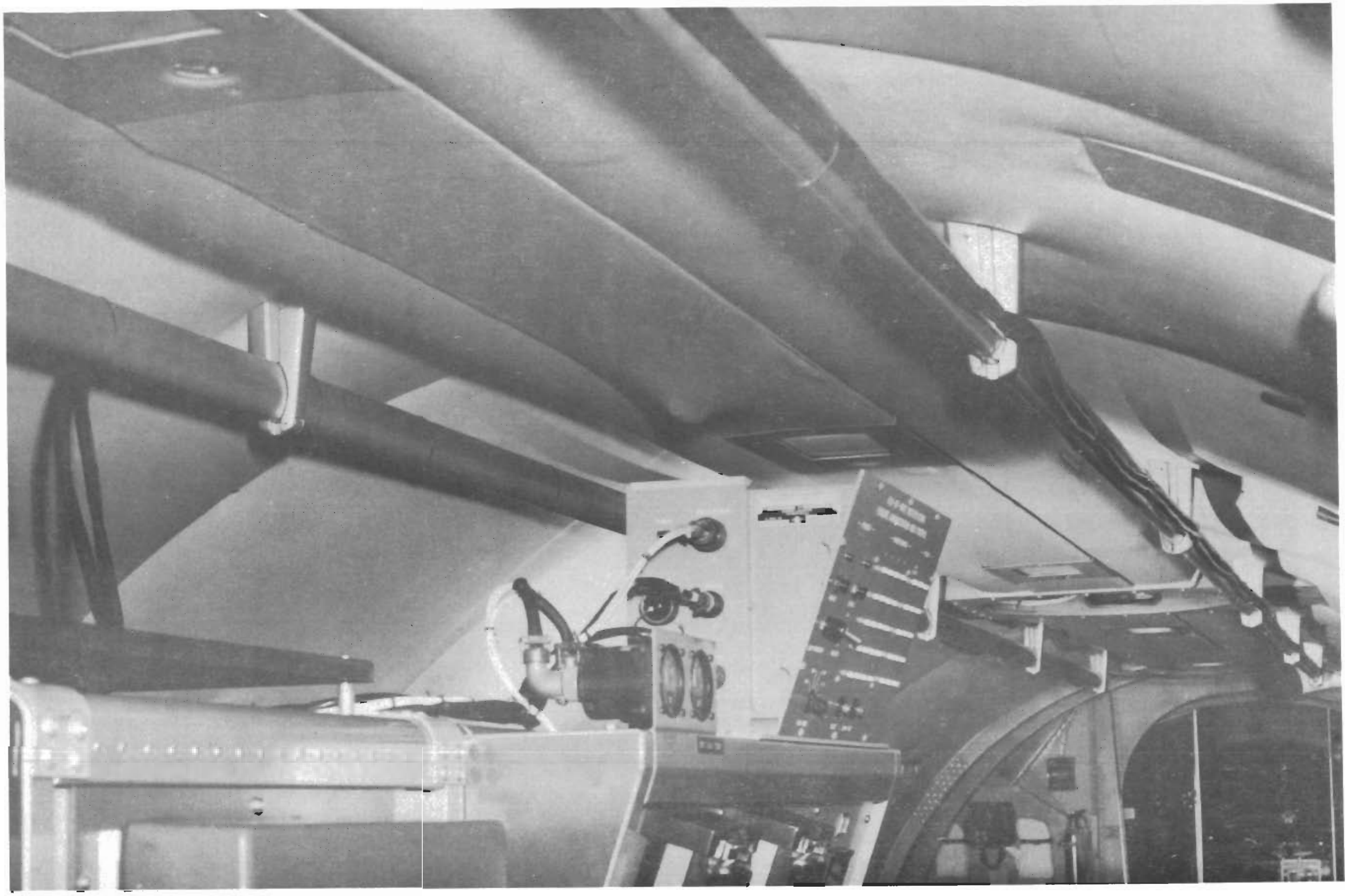


Fig. 4-2 INSTALLATION OF UNIT 4 AND TRANSMISSION LINES

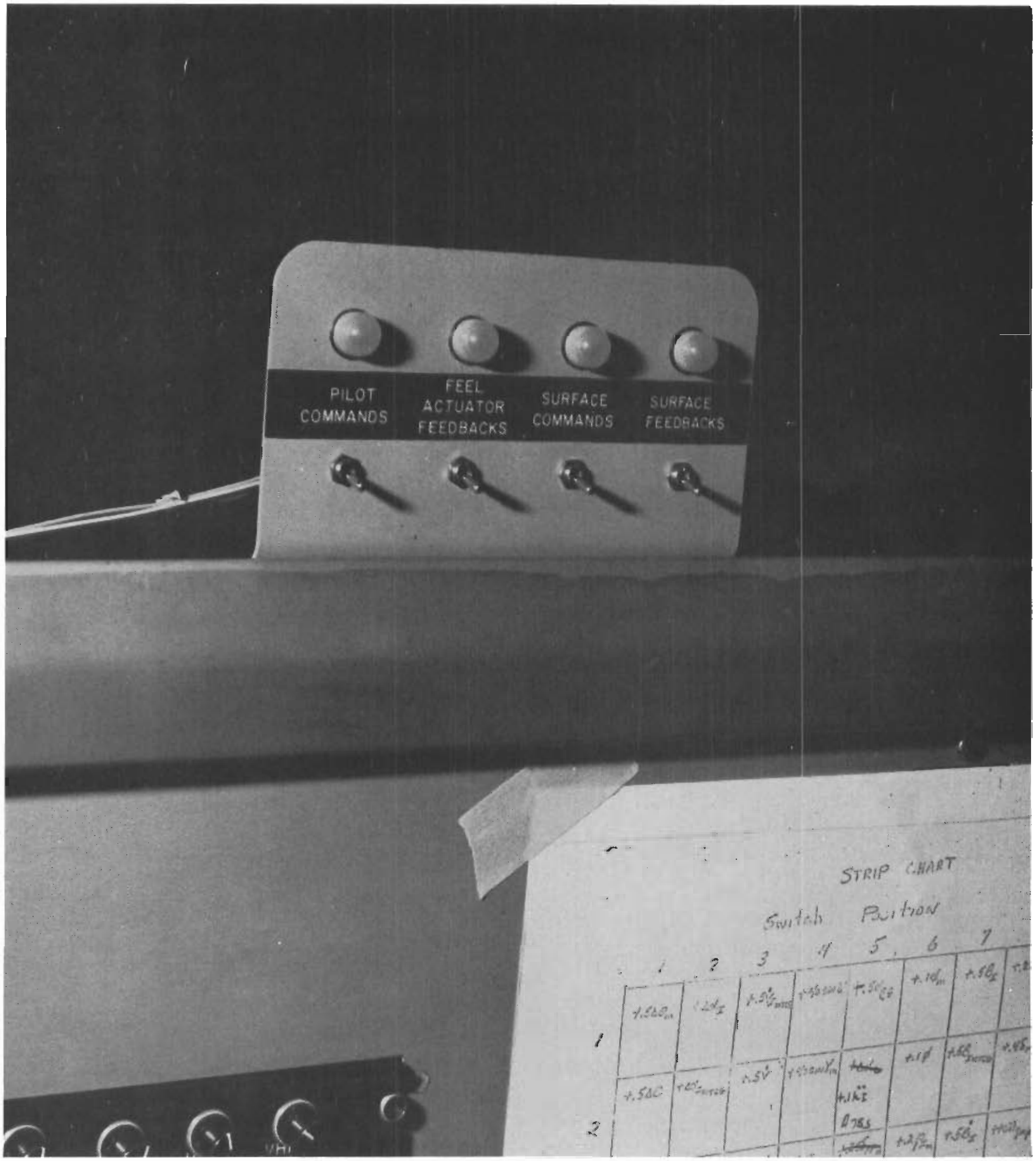


Fig. 4-3 PROVISION TO SWITCH MULTIPLEX DATA PATHS

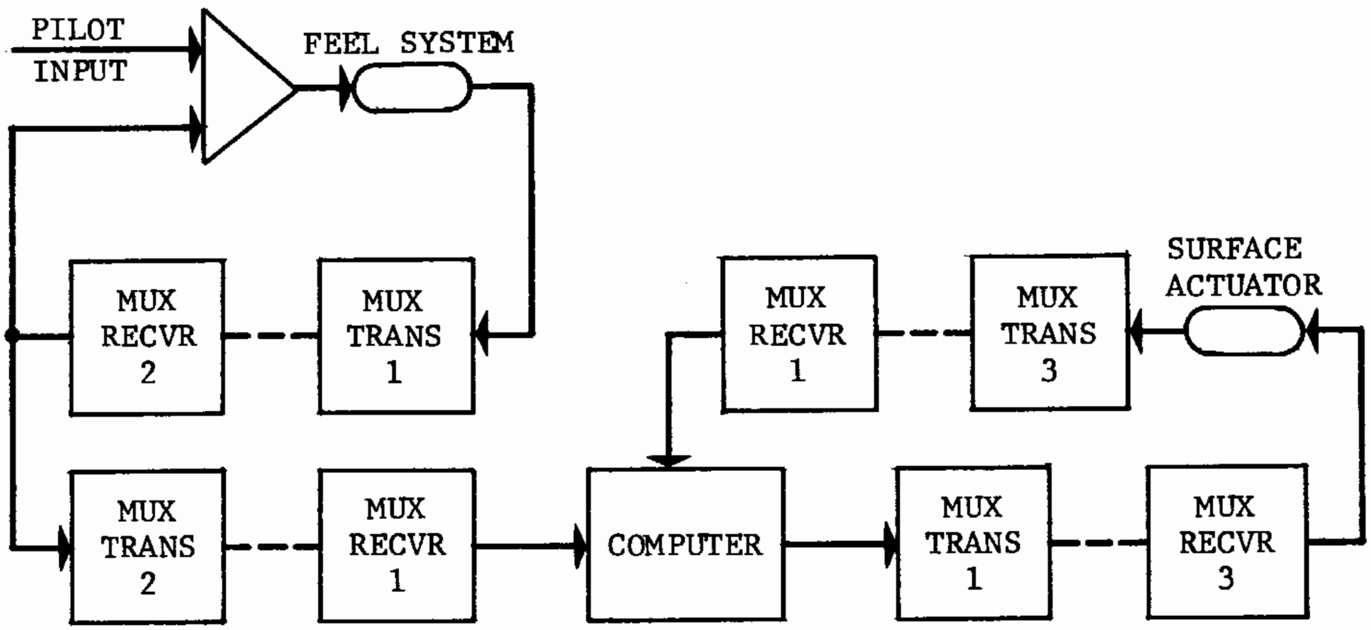


Fig. 4-4 TIFS MULTIPLEXING ARRANGEMENT

to verify both the patch panel wiring and the TIFS printed circuit card modifications. No problems were encountered during this phase of the checkout. These initial open-loop ground tests were conducted using electrical power supplied by ground carts and without hydraulic power to the feel system and surface actuators. As soon as it had been verified that the proper signals were appearing at the outputs of the surface servo power amplifiers, the sine-wave inputs were repeated with hydraulic power on the aircraft.

At this time it was possible to evaluate the actual amount of noise and random motion that appeared on the control surfaces. A small amount of noise could be detected on the direct-lift flaps and side force surfaces. Various methods of grounding the cable shielding were evaluated in order to achieve the minimum noise level. The grounding method that had been selected initially (all shields grounded on one end only) was determined to be preferred. In an effort to determine the noise source, the digital words in both the transmitters and receivers were monitored. It was determined that only the least significant bit was changing in both the transmitted and received words indicating that the noise was not present in the digital words. However, it was found that a noise level of approximately 100 millivolts was superimposed on the analog signal out of the D/A converter. It was determined that this noise was coming in on the ±15 volt power supply lines to the converter card. The decoupling capacitors of the power supplies were changed from 0.1 μf to 68 μf and the noise level was decreased to within 20 mv (the resolution limit of the 10-bit data word). This change was made to all of the D/A cards and the noise on the surface was significantly reduced.

During the ground checkout with hydraulic power on, it was also determined that for the 50/sec data rate, the flap and side force surface valves were being saturated by the large amplitude step changes in the reconstructed analog commands that resulted from high rate inputs. This characteristic is illustrated in Figure 4-5. In order to preclude damage to the servo valves at the low data rate, various filters were evaluated on the surface servo command signals. Since the filters had an effect on the servo loop stability, it was necessary to select a filter characteristic that would eliminate the servo valve saturation without significantly affecting the actuator stability. It was

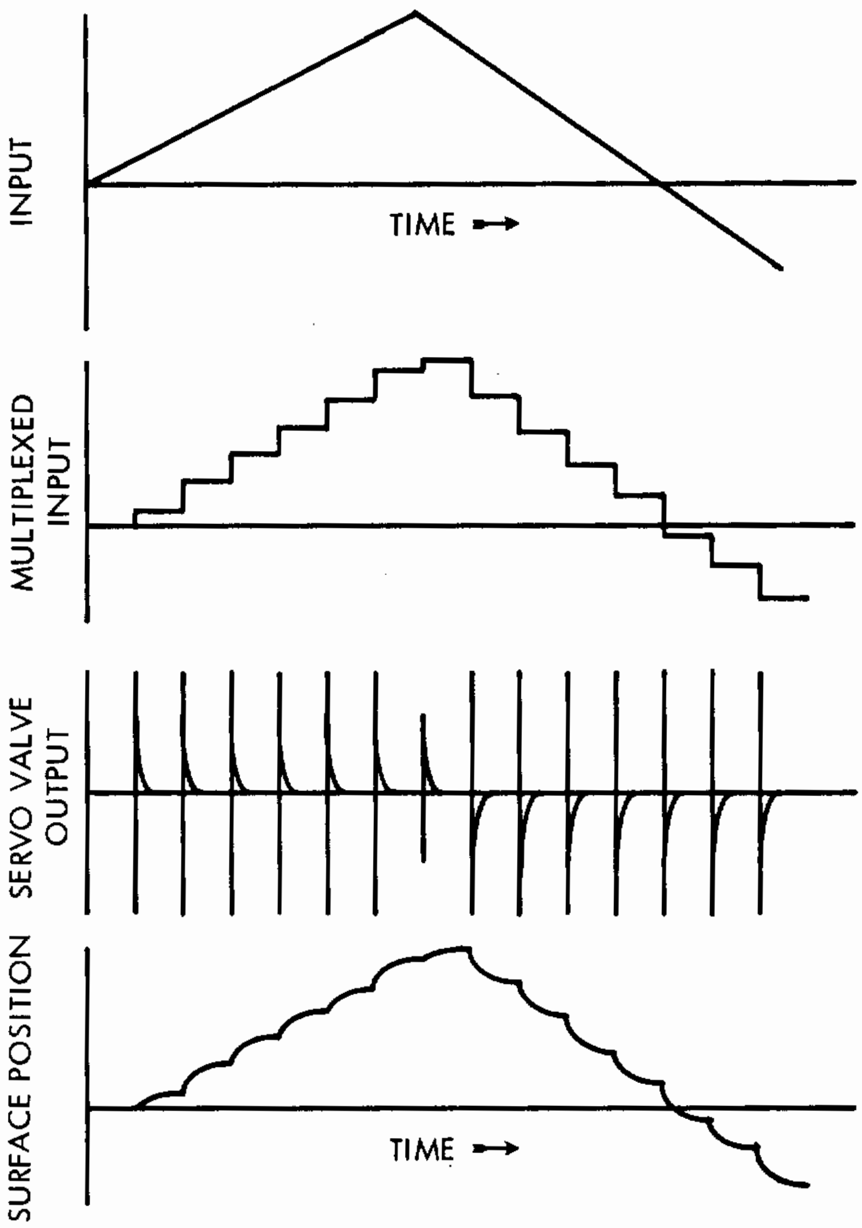


Fig. 4-5 SURFACE SERVO CHARACTERISTICS

determined that a single 50 Hz first-order lag in the servo position feedback signals and two 50 Hz lags in the input commands was best from the standpoint of eliminating the valve saturation for maximum rate signals while having very little effect on the servo stability. This configuration reduced the spikes on the valve output from full scale to about half-scale for the most rapid inputs and yielded a significantly smoother reconstructed analog signal. These filters were used on the flap and side-force servos throughout the flight testing of the multiplexing equipment.

The final ground checkout of the multiplex system consisted of taxi and ground engine run up with the multiplex system engaged and utilizing aircraft electrical and hydraulic power. These tests were uneventful and did not indicate any additional system problems.

SECTION 5

FLIGHT TEST PROGRAM

A separate and more detailed discussion of the flight test program is contained in Reference 2. Only the highlights of the flight tests, as they apply to the design and feasibility of the multiplexing concept, are discussed in this report.

The flight testing of the multiplexing system consisted of 12 flights during which 23.2 hours of total flight time was accrued. The flight tests were conducted during the two week period from October 6 through October 18. Flight test points were flown at airspeeds up to 240 knots and altitudes to 14,500 feet. The first two flights were used to obtain pilot qualitative evaluations of the multiplexing system at airspeeds of 160 and 240 knots. These two flights were made in the basic TIFS fly-by-wire configuration with no feedback loops closed. Pilot evaluations were made by switching the multiplexing in and out of the system at each of the data rates. Flights 3 and 4 were used to select the feedback gains that were to be used for the closed-loop multiplex evaluations. The multiplexing system was engaged during the time the gains were being selected.

The remaining flights were used to allow pilot evaluations of the multiplexing system with all of the selected feedback loops closed and to obtain aerodynamic data on the TIFS airplane. All of the aero data points were obtained using the multiplexing system at the 400/sec data rate. On the last flight, several simulated landings were made with the evaluation pilot flying the aircraft with the multiplexing system operating. Also, comparison response data for each of the multiplexing data rates were obtained using automatic step inputs into each of the control surfaces.

The only problem that was encountered with the multiplexing equipment occurred on the first flight. At two different times during the flight, the safety pilot reported feeling light glitches on his aileron control wheel. These were felt only by the safety pilot and did not result in any perceptible aircraft response. The first glitch occurred when the multiplex system was being operated at 400/sec. The second glitch occurred at a 50/sec update rate and caused the TIFS safety trip circuits to disengage the variable stability system. From an analysis of the inflight digital recorder data, it was determined that the extraneous signals had been generated in T2-R1 multiplexing path between the feel system and the computer. The aileron wheel command signal was being transmitted as the second word in that multiplex frame. This channel output was monitored for about 2 hours on the ground after the flight and in that time 2 output glitches were noted. At that time, the aileron signal was rewired from the second multiplex input to the fourth channel which was not being used. The remainder of the flight test program was flown using the fourth channel instead of the second. On Monday, October 16 weather conditions prohibited flying, so this time was used to further investigate the problem. The sample and hold card from which the glitch occurred was replaced and its output was monitored for about 2 hours. During this time no glitches were observed. Verification that the problem had been solved would have required a considerable period of ground operation. It appeared that the problem had been corrected by the installation of the new card, but the evidence was not considered to be conclusive. No further glitches were observed in the remainder of the flight test program.

The flight test program was completed successfully. The airplane was flown by seven different Calspan pilots and each expressed a complete inability to ascertain when the multiplexing system was engaged and when it was disengaged. Therefore, for the TIFS aircraft dynamics, the frequency and resolution capabilities of the multiplexing system at a 50/sec data rate were adequate.

SECTION 6

CONCLUSIONS

The feasibility of multiplexing fly-by-wire flight control signals has been verified through actual flight test. Although only 23.2 flight hours were accrued on the multiplexing equipment it was adequately demonstrated that multiplexing could be employed without adverse effects on the dynamic characteristics of the TIFS airplane. Although the lowest data update rate provided in the multiplexing system (50/sec) resulted in satisfactory dynamic performance, the simulation work, performed on an analog computer, indicated that higher rates may be required in more responsive airplanes such as an F-15 or YF-16. Some experimental evidence also exists which indicates that when lower sample rates begin to degrade the dynamic performance of a closed loop system it is sometimes possible to adjust the gains of the system to correct the degradation. More research is needed in this area to permit the lowest practical sample rate to be selected without degrading the dynamic performance of the system. The ability to select a low sample rate will be beneficial in reducing the computer cycle frequency requirement in a digital flight control system.

It was determined in the ground tests of the equipment in the TIFS airplane that in very responsive servo loops, such as the direct lift flaps and side force surfaces, care must be taken in designing the interface between the digital and analog equipment. It was found that rapid inputs can result in large vertical steps in the reconstructed analog signals at lower sample rate. It appears that by giving proper consideration to the processing of these signals, valve saturation problems such as those experienced in the ground tests can be avoided.

Although the feasibility of multiplexing fly-by-wire signals was demonstrated in this program, there are several design aspects that required additional consideration. One of these aspects is the manner in which the transmission lines are coupled to the transmitters and receivers. The equipment developed in this program employed direct coupling. This choice was made because past experience had indicated that it functioned well and the goals of this program did not include a requirement for research in coupling techniques.

Considerable interest has been generated in the industry in AC coupling methods to minimize the influence of dc type failures of a given LRU on the data bus. In particular, transformer coupling has come under study. This type of coupling provides immunity from loss of the entire transmission line as a result of a failure in one of the remote units. The limitations of various types of AC coupling should be investigated to determine their suitability for use in multiplexing of flight control signals.

The management of redundant multiplexing systems is another subject that should be studied. The detection of a failure among the signals of several redundant branches which are functioning asynchronously requires careful consideration.

REFERENCES

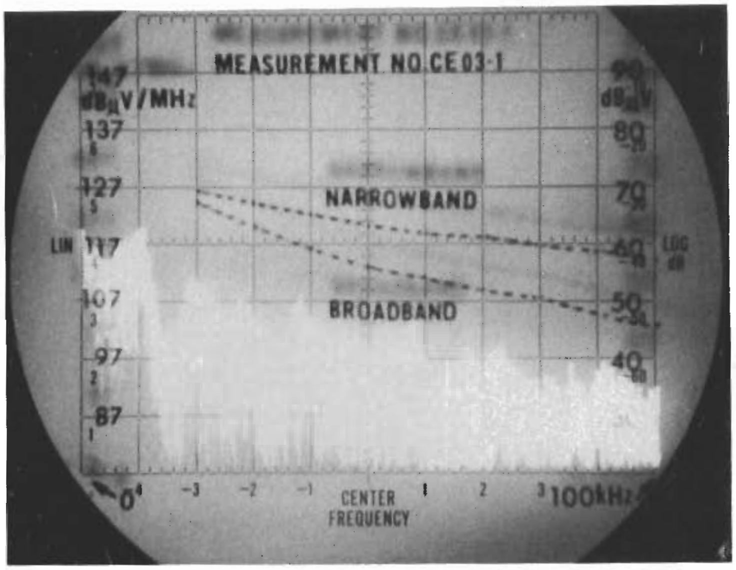
1. J. G. Mrazek, R. O. Roberts, and D. H. Daggett, Research into the Definition and Demonstration of an Optimum Solid State Switching and Multiplexing System for use in a Fly-by-Wire Flight Control System, Air Force Flight Dynamics Laboratory Report AFFDL-TR-70-80, June 1970

2. James N. Dittenhouser, C. J. Fabian and Arno E. Shelhorn, Inflight Testing of a Flight Control System Multiplex System in the NC-131H Total Inflight Simulator, Air Force Flight Dynamics Laboratory Report AFFDL-TR-73-11, March 1973

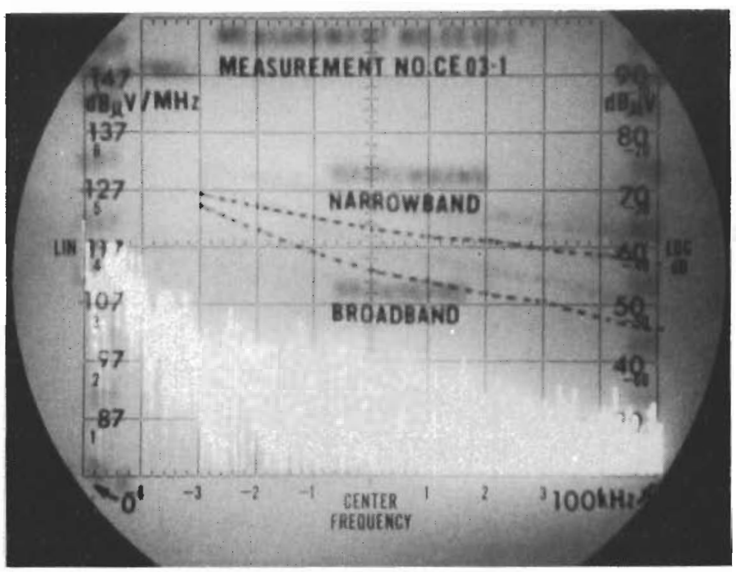
APPENDIX A

ELECTROMAGNETIC INTERFERENCE

TEST DOCUMENTATION

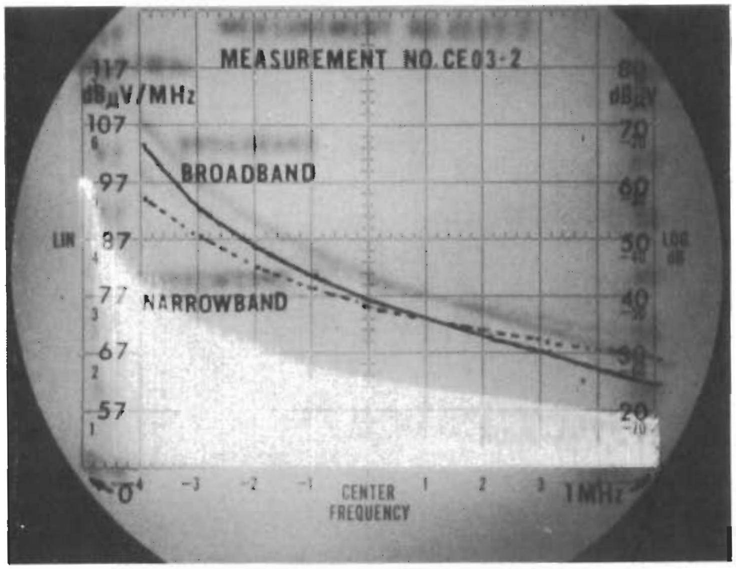


a. High, Measurement CE03-1

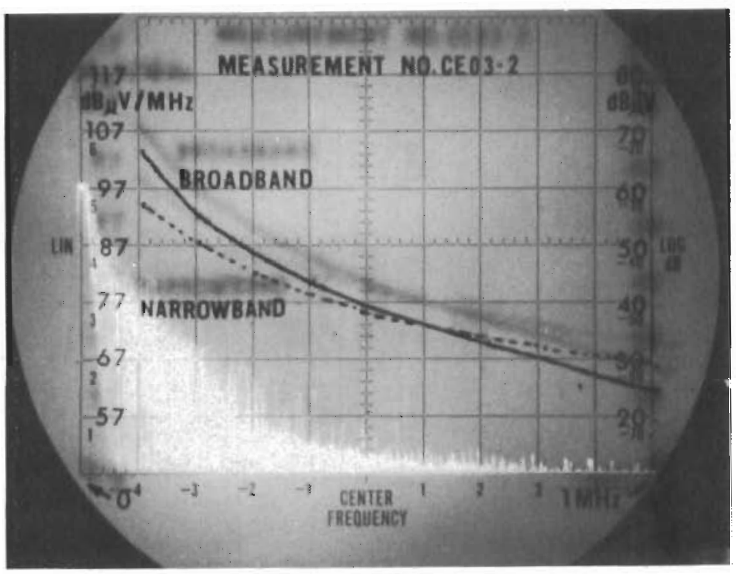


b. Neutral, Measurement CE03-1

Figure A-1 Test Method CE03, Measurement 1, AC Input to System

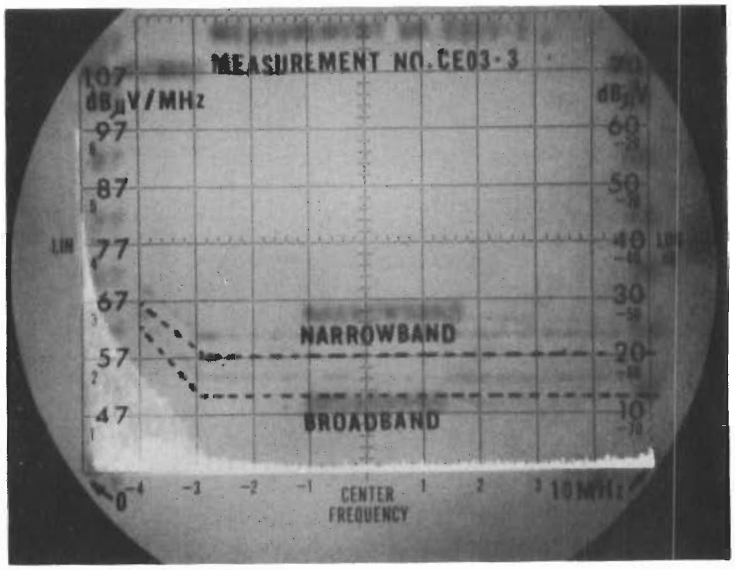


a. High, Measurement CE03-2

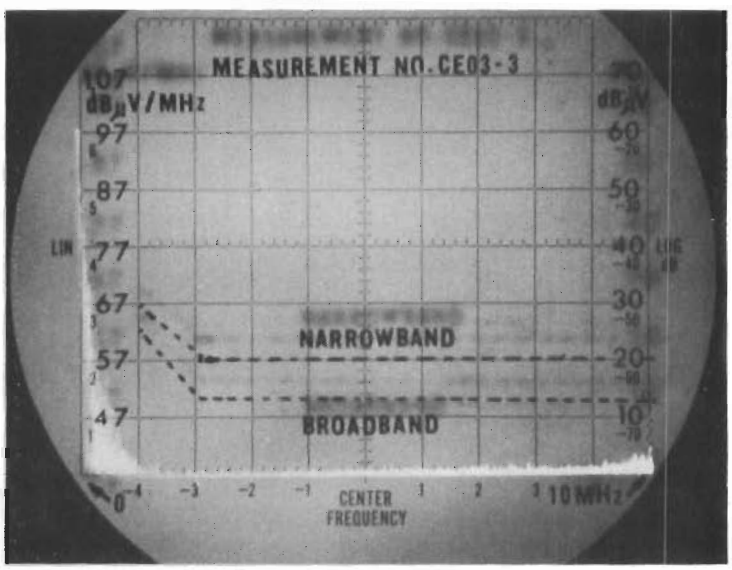


b. Neutral, Measurement CE03-2

Figure A-2 Test Method CE03, Measurement 2, AC Input to System

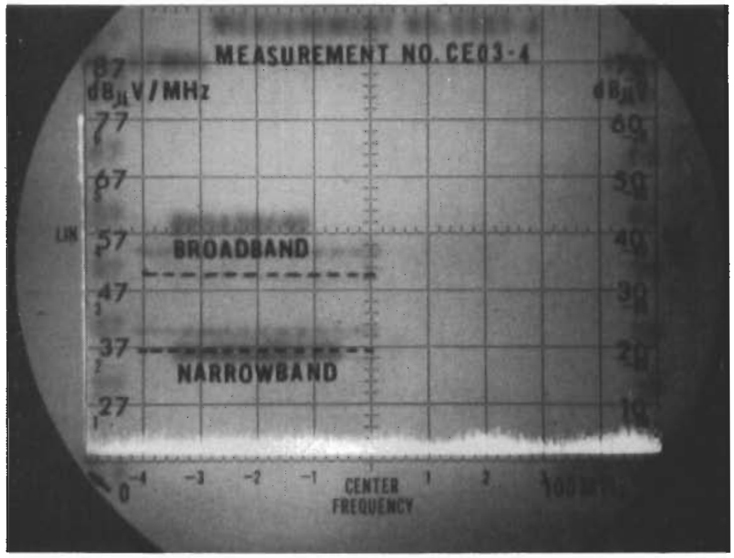


a. High, Measurement CE03-3

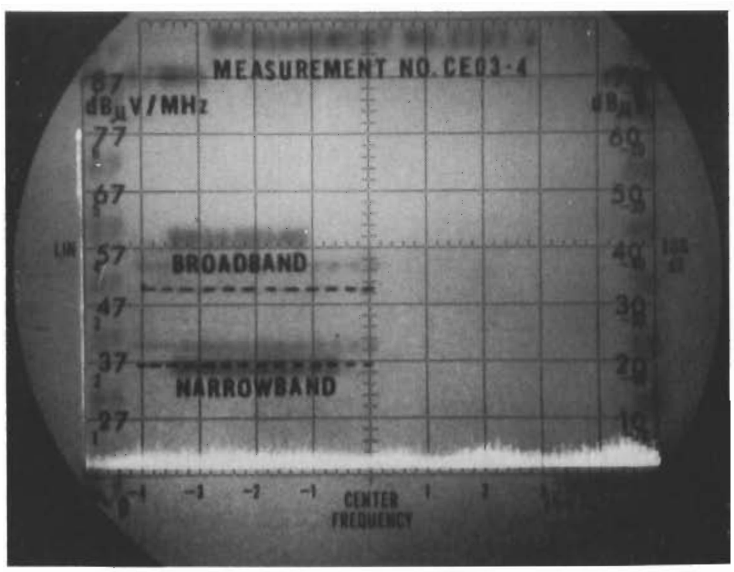


b. Neutral, Measurement, CE03-3

Figure A–3 Test Method CE03, Measurement 3, AC Input to System

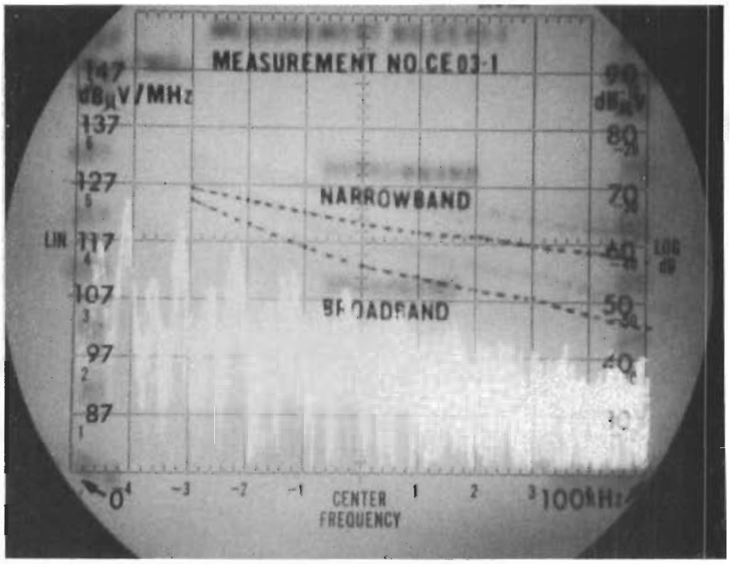


a. High, Measurement CE03-4

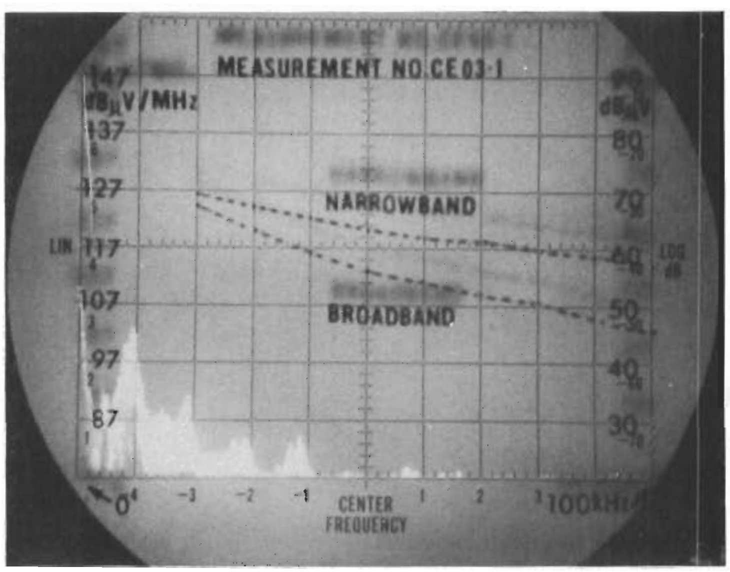


b. Neutral, Measurement CE03-4

Figure A-4 Test Method CE03, Measurement 4, AC Input to System

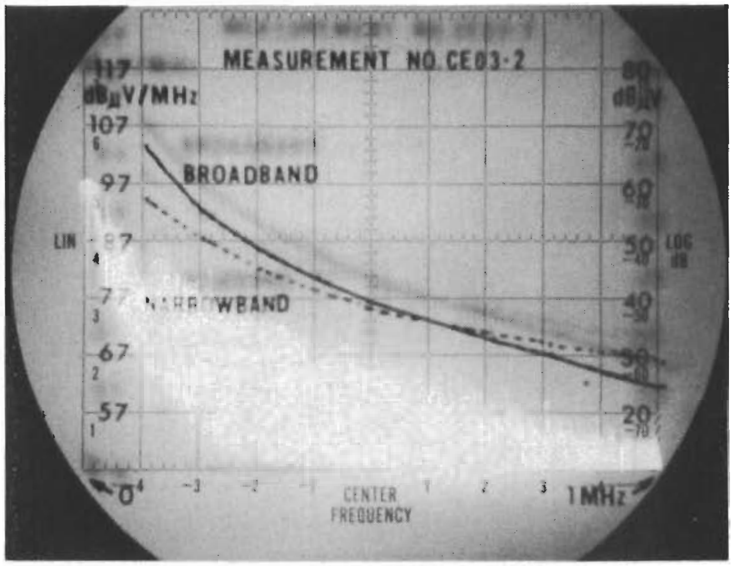


a. High, Measurement CE03-1

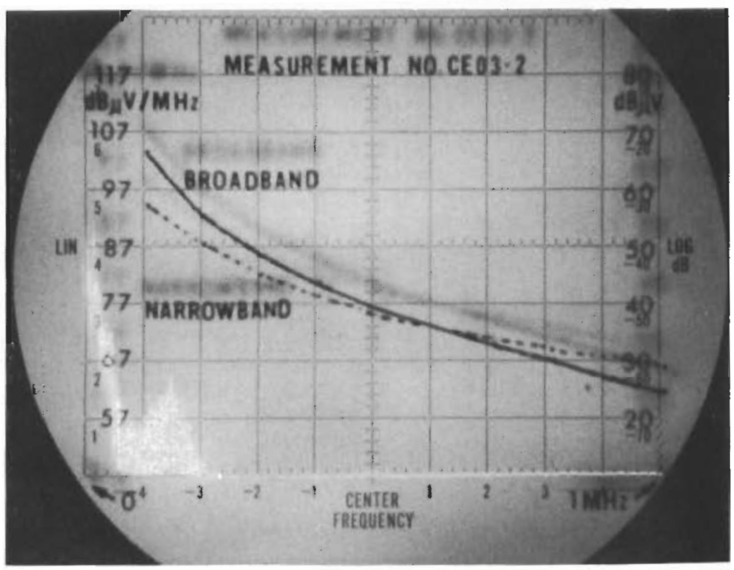


b. Neutral, Measurement CE03-1

Figure A-5 Test Method CE03, Measurement 1, DC Input to System

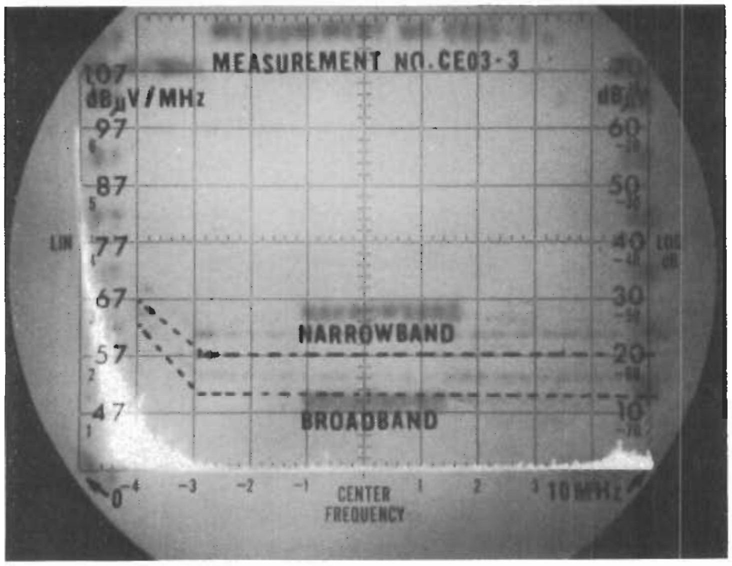


a. High, Measurement CE03-2

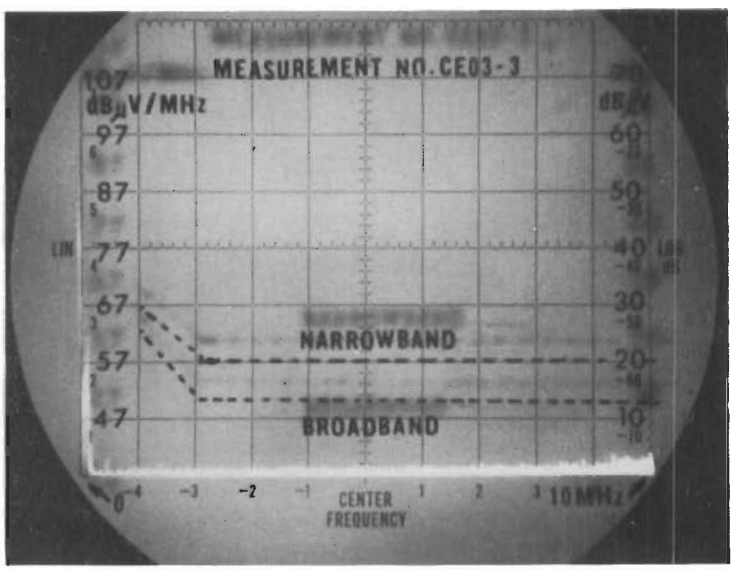


b. Neutral, Measurement CE03-2

Figure A—6 Test Method CE03, Measurement 2, DC Input to System

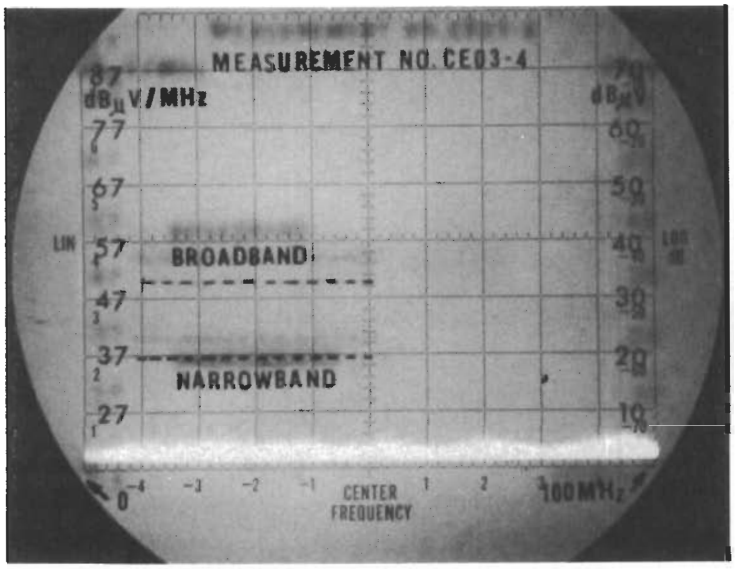


a. High, Measurement CE03-3

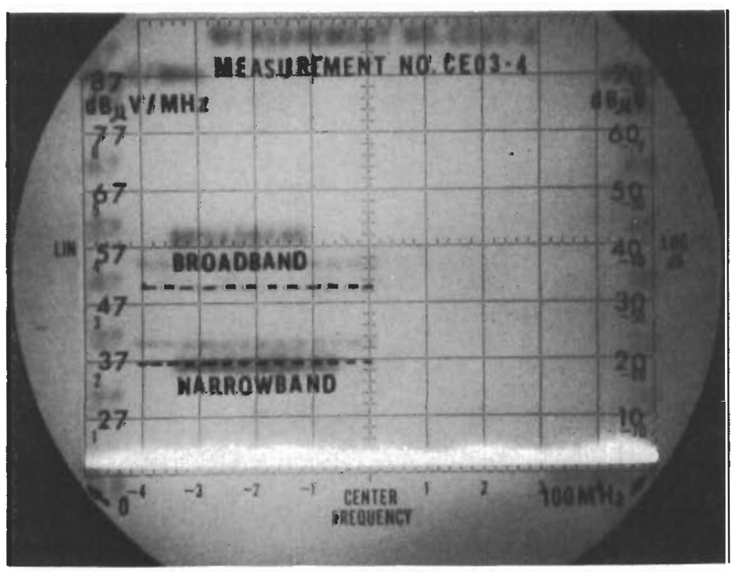


b. Neutral, Measurement CE03-3

Figure A–7 Test Method CE03, Measurement 3,
DC Input to System

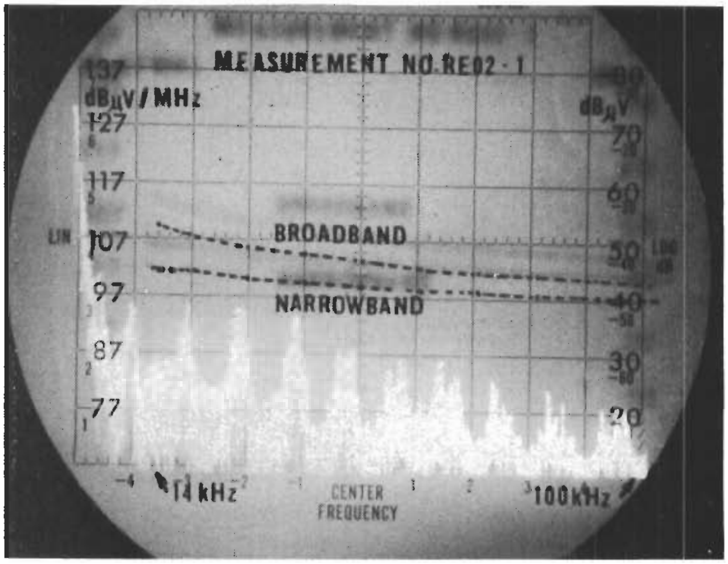


a. High, Measurement CE03-4

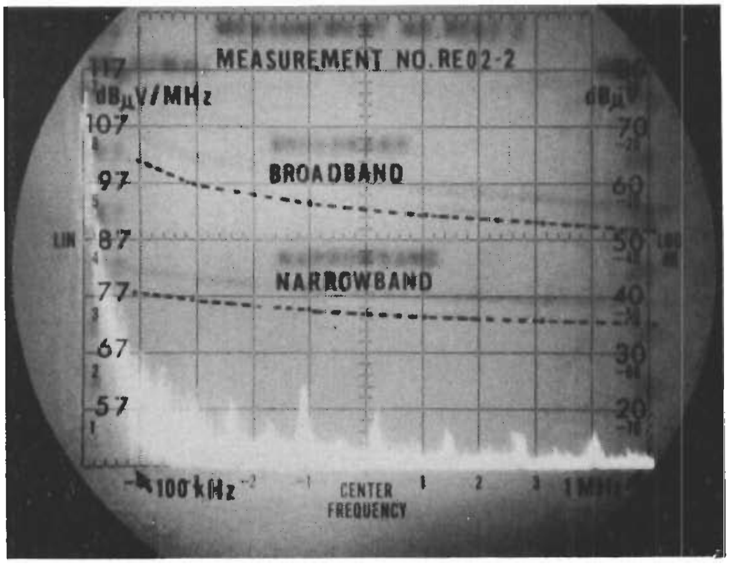


b. Neutral, Measurement CE03-4

Figure A-8 Test Method CE03, Measurement 4,
DC Input to System

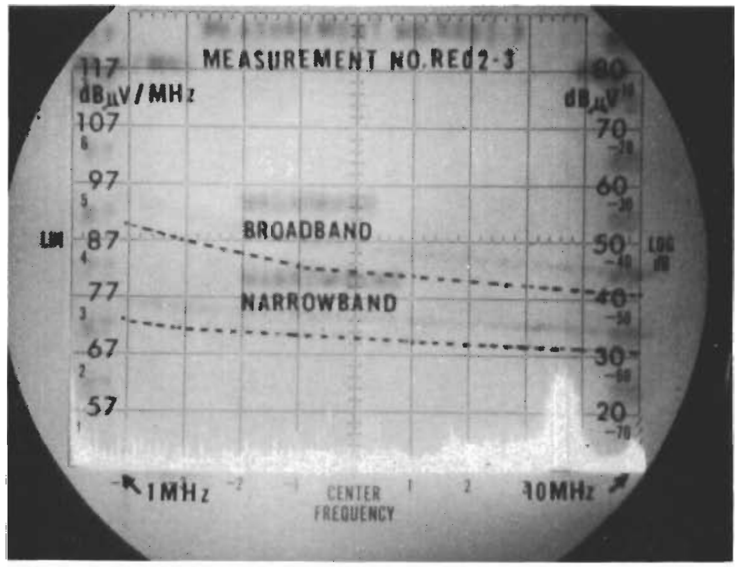


a. Measurement RE02-1

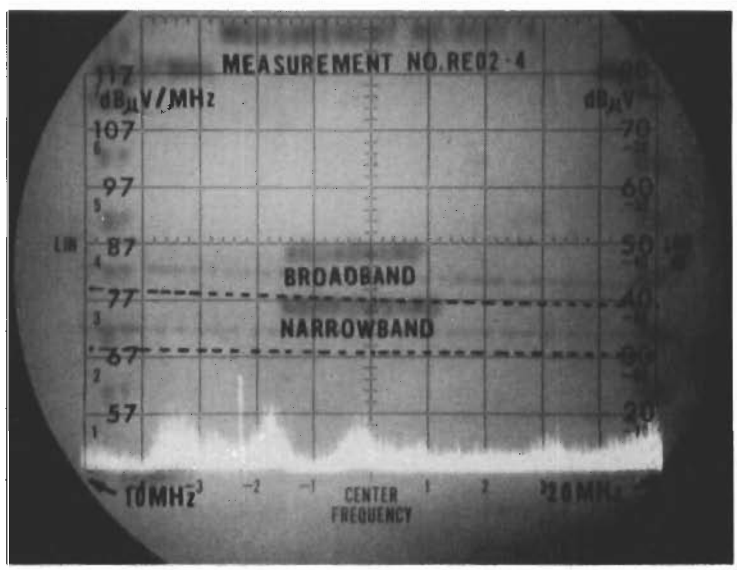


b. Measurement RE02-2

Figure A—9 Test Method RE02, Measurements 1 and 2, Radiated Emissions

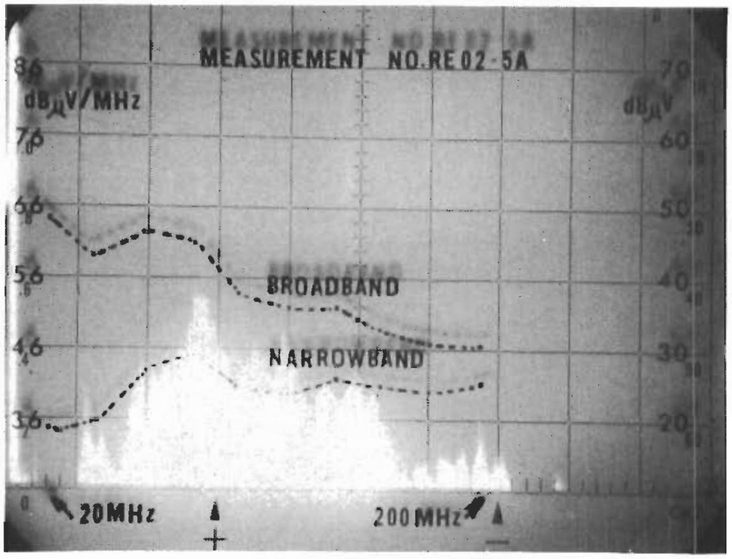


c. Measurement RE02-3

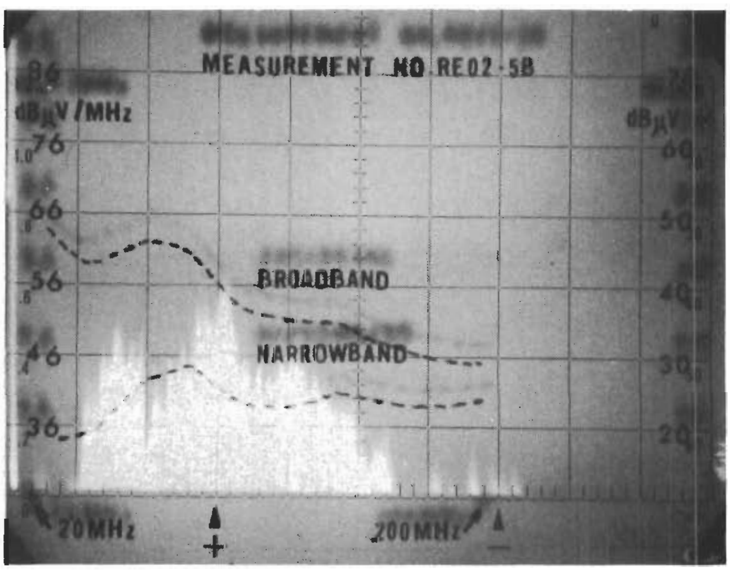


d. Measurement RE02-4

Figure A-10 Test Method RE02, Measurements 3 and 4, Radiated Emissions



e. Measurement RE02-5A



f. Measurement RE02-5B

Figure A-11 Test Method RE02, Measurements 5A and 5B, Radiated Emissions

Table A-1 TEST APPARATUS (Sheet 1 of 4)

MIL-STD-462 TEST METHOD NO.	NAME	MANUFACTURER	MODEL NUMBER	SERIAL NUMBER	LAST CALIBRATION DATE
CE03	Spectrum Analyzer Display Section	Hewlett Packard	141S	849-00457	6-1-72
	Spectrum Analyzer RF Section	Hewlett Packard	8553L	902-00527	6-1-72
	Spectrum Analyzer IF Section	Hewlett Packard	8552A	852-00507	6-1-72
	Oscilloscope Camera	Hewlett Packard	197A	805-02794	N/A
	Current Probe	Singer	CP105	N/A	N/A
	General Purpose Amplifier	Hewlett Packard	461A	606-03007	12-30-71
	10,uf Feedthrough Capacitors	Solar	6512-106	N/A	N/A
CS01	Oscilloscope	Tektronix	585	000651	5-1-72
	Audio Oscillator	Hewlett Packard	652A	632-00579	2-29-72
	Power Amplifier	Krohn Hite	101A	273	N/A
	Isolation Transformer	Solar	6220-2	N/A	N/A
	VTVM	Hewlett Packard	3400A	806-07959	4-25-72
CS02	Signal Generator	Hewlett Packard	606A	139-00729	12-30-71
	RF-Millivoltmeter	Hewlett Packard	411A	131-03712	5-2-72
	Signal Generator	Hewlett Packard	608C	1921	5-2-72
	Termination	Hewlett Packard	11048B	N/A	N/A
	VHF Oscillator	Hewlett Packard	3200B	735-02057	6-1-72

Table A-1 TEST APPARATUS (Sheet 2 of 4)

MIL-STD-462 TEST METHOD NO.	NAME	MANUFACTURER	MODEL NUMBER	SERIAL NUMBER	LAST CALIBRATION DATE
CS06	Spike Generator	Solar	6254-5	8-50-20	6-1-72
	10,uf feedthrough capacitors	Solar	6512-106	N/A	N/A
	Oscilloscope	Tektronix	585	012992	5-1-72
RE02	Spectrum Analyzer Display Section	Hewlett Packard	141S	849-00457	6-1-72
	Spectrum Analyzer IF Section	Hewlett Packard	8552A	852-00507	6-1-72
	Spectrum Analyzer RF Section	Hewlett Packard	8553L	902-00527	6-1-72
	Spectrum Analyzer Display Section	Hewlett Packard	851B	728-01539	2-29-72
	Spectrum Analyzer RF Section	Hewlett Packard	8551B	727-01458	2-29-72
	Antenna Amplifier	Honeywell	AW204/2805	197	5-2-72
	Unit Amplifier	Avantek	UA401-402	100	N/A
	Low Pass Filter	Telonic	TLP-1800-8FE1	H-194-2	N/A
	Bi-Conical Antenna	General Dynamics	N/A	1	N/A
	Antenna Coupler	Singer	DM-105-T1	N/A	N/A
	Log Conical Antenna	EMCO	3101	2405	N/A
	Oscilloscope Camera	Hewlett Packard	197A	805-02794	N/A

Table A-1 TEST APPARATUS (Sheet 3 of 4)

MIL-STD-462 TEST METHOD NO.	NAME	MANUFACTURER	MODEL NUMBER	SERIAL NUMBER	LAST CALIBRATION DATE
RS02	Spike Generator	Solar	6254-5	8-50-20	6-1-72
	Ammeter	Weston	749	N/A	6-1-72
	Transformer	Chicago Standard	N/A	N/A	N/A
	Variac	Superior	VC1MB	983	N/A
	Oscilloscope	Tektronix	585	012992	5-1-72
RS03	Spectrum Analyzer Display Section	Hewlett Packard	141S	849-00457	6-1-72
	Spectrum Analyzer RF Section	Hewlett Packard	8553L	902-00527	6-1-72
	Spectrum Analyzer IF Section	Hewlett Packard	8552A	852-00507	6-1-72
	Spectrum Analyzer Display Section	Hewlett Packard	851B	728-01539	2-29-72
	Spectrum Analyzer RF Section	Hewlett Packard	8551B	727-01458	2-29-72
	Resistive Divider Probe	Hewlett Packard	10201D	N/A	N/A
	Directional Coupler	Hewlett Packard	778D	826-00434	N/A
	Directional Coupler	Hewlett Packard	779D	922-00397	N/A
	Termination	Hewlett Packard	908A	N/A	N/A
	Signal Generator	Hewlett Packard	652A	632-00579	2-29-72
	Signal Generator	Hewlett Packard	606A	139-00729	12-30-71
	Signal Generator	Hewlett Packard	608C	1921	5-2-72
	Sweep Oscillator	Hewlett Packard	8690A	747-01776	5-2-72
	RF Unit	Hewlett Packard	8694B	724-00505	4-3-72

Table A-1 TEST APPARATUS (Sheet 4 of 4)

MIL-STD-462 TEST METHOD NO.	NAME	MANUFACTURER	MODEL NUMBER	SERIAL NUMBER	LAST CALIBRATION DATE
RS03 (Cont'd)	TWT Amplifier	ALFRED	560	167	N/A
	TWT Amplifier	ALFRED	561	220	N/A
	TWT Amplifier	Hewlett Packard	493A	842-01360	N/A
	TWT Amplifier	ALFRED	527	190	N/A
	Susceptibility Antenna	Singer	VR-1-105	N/A	N/A
	Calibration Antenna	Singer	VR-10105	H-815	N/A
	Susceptibility Antenna	Singer	VA-105	E-505	N/A
	Power Amplifier	Solar	6552-1A	9-10-15	12-30-71
	Power Amplifier	Instruments For Industry	5000L	119-535	12-30-71
	Calibration Antenna	Singer	VA-105	H-591	N/A
	Susceptibility Antenna	General Dynamics	N/A	1	N/A
	Antenna Coupler	Singer	DM-105-T1	N/A	N/A
	Calibration Antenna	General Dynamics	N/A	2	N/A
	Antenna Coupler	Singer	MD-105-T1	H-653	N/A
	Susceptibility Antenna	EMCO	3101	7405	N/A
	Calibration Antenna	Singer	DM-105-T2	N/A	N/A
	Calibration Antenna	Singer	DM-105T3	N/A	N/A
	Calibration Antenna	EMCO	3102	2349	N/A
	Power Signal Source	Air Borne Inst.	125	256	2-29-72
	Susceptibility Antenna	Singer	AT-112	N/A	N/A
	Signal Generator	Hewlett Packard	616A	3040	2-1-72
	Signal Generator	Hewlett Packard	618	Syl 26	6-2-72

Table A-2 (Sheet 1 of 3)
BANDWIDTH FIGURE B (10 kHz) FOR HP 8551B, S/N 727-01458

Attenuator Setting (dB)	$f_1 - f_2$ (kHz)	a_1 (dBm)	a_p (dBm)	Calculated BW_i (kHz)
0	200	-4.0	-20.8	14.5
10	200	-16.6	-31.4	18.2
20	200	-25.9	-40.5	18.6
30	200	-36.1	-50.2	19.7
40	200	-46.4	-60.2	20.4
Average BW_i = 18.3 kHz				

$$B = 20 \log \frac{18.3 \times 10^3}{1 \times 10^6}$$

$$B = -34.8 \text{ dB MHz}$$

Table A-2 (Sheet 2 of 3)
BANDWIDTH FIGURE B (100kHz) FOR HP 8551B, S/N 727-01458

Attenuator Setting (dB)	$f_1 - f_2$ (kHz)	a_1 (dBm)	a_p (dBm)	Calculated BW_i (kHz)
0	1960.0	+9.0	-7.0	155.0
10	1970.0	-3.7	-18.5	179.0
20	1980.0	-12.2	-27.8	164.0
30	1980.0	-22.3	-37.8	166.0
40	1980.0	-32.4	-48.2	160.3
Average BW_i = 164.8 kHz				

$$B = 20 \log \frac{164.8 \times 10^3}{1 \times 10^6}$$

$$B = -15.65 \text{ dB MHz}$$

Table A-2 (Sheet 3 of 3)
BANDWIDTH FIGURE B FOR THE 8553L, S/N 902-00527

	B = 20 log (BW/1 MHz)
1 kHz	$B = 20 \log \frac{1.34 \times 10^3}{1 \times 10^6} = -57.46$ dB MHz
10 kHz	$B = 20 \log \frac{1.5 \times 10^4}{1 \times 10^6} = -36.48$ dB MHz
100 kHz	$B = 20 \log \frac{1.45 \times 10^5}{1 \times 10^6} = -16.78$ dB MHz

FREQ.	SCOPE IND. NEEDED	DIVIDER PROBE IND.	RECEIVE ANTENNA CONFIGURATION	TRANSMIT ANTENNA CONFIGURATION
14 kHz	88 dBμV	88 dBμV	VR-1-105 (AL3738)	41" Rod with audio Xfer as coupler
20 kHz	90 dBμV	87 dBμV	" "	" "
30 kHz	93 dBμV	90 dBμV	" "	" "
40 kHz	94 dBμV	99 dBμV	" "	" "
50 kHz	94 dBμV	102 dBμV	" "	" "
60 kHz	94 dBμV	94 dBμV	" "	" "
70 kHz	94 dBμV	94 dBμV	" "	" "
80 kHz	94 dBμV	99 dBμV	" "	" "
90 kHz	94 dBμV	103 dBμV	" "	" "
100 kHz	94 dBμV	106 dBμV	" "	41" Rod coupler #1 out2
110 kHz	94 dBμV	105 dBμV	" "	" "
120 kHz	94 dBμV	105 dBμV	" "	" "
130 kHz	94 dBμV	105 dBμV	" "	" "
140 kHz	94 dBμV	104 dBμV	" "	" "
150 kHz	94 dBμV	104 dBμV	" "	" "
150 kHz	93.5 dBμV	100 dBμV	VA-105 (S/N I505)	" "
230 kHz	102 dBμV	94 dBμV	" "	" "
260 kHz	100.5dBμV	92 dBμV	" "	" "
300 kHz	99.5 dBμV	87 dBμV	" "	" "
330 kHz	98 dBμV	85 dBμV	" "	" "
360 kHz	98 dBμV	88 dBμV	" "	" "
360 kHz	97 dBμV	90 dBμV	" "	" "
400 kHz	98 dBμV	93 dBμV	" "	" "
500 kHz	101 dBμV	101 dBμV	" "	" "
600 kHz	102 dBμV	116 dBμV	" "	Coupler #2 in 1 out 5
700 kHz	103.5dBμV	117 dBμV	" "	" "
800 kHz	103.5dBμV	114 dBμV	" "	" "
870 kHz	103.5dBμV	112 dBμV	" "	" "
870 kHz	104 dBμV	112 dBμV	" "	" "
1.0 MHz	106.5dBμV	104 dBμV	" "	" "
1.2 MHz	108 dBμV	111 dBμV	" "	" "
1.4 MHz	106.5dBμV	104 dBμV	" "	Coupler #2 GR1 in 2 out5
1.6 MHz	106 dBμV	104 dBμV	" "	" "
1.8 MHz	105 dBμV	103 dBμV	" "	" "
2.1 MHz	105 dBμV	103 dBμV	" "	" "
2.1 MHz	104.5dBμV	101 dBμV	VA-105 (S/N I505)	" "
2.7 MHz	110.5dBμV	91 dBμV	" "	" "
3.4 MHz	111 dBμV	101 dBμV	" "	" "
4.0 MHz	110 dBμV	107 dBμV	" "	" "
4.6 MHz	108.5dBμV	111 dBμV	" "	" "
5.2 MHz	108 dBμV	96 dBμV	" "	" "

Table A-3 RS03 Radiated Susceptibility Data (Sheet 1 of 3)

5-9-72

FREQ.	SCOPE IND. NEEDED	DIVIDER PROBE IND.	RECEIVE ANTENNA CONFIGURATION	TRANSMIT ANTENNA CONFIGURATION
5.2 MHz	110.5μdB V	96 dBμV	VA-105 (S/N I505)	Coupler #2 Grl in 3 out 5
6.0 MHz	112 dBμV	93 dBμV	" "	" "
7.0 MHz	113 dBμV	102 dBμV	" "	" "
8.0 MHz	114 dBμV	102 dBμV	" "	" "
9.0 MHz	114 dBμV	114 dBμV	" "	" "
10.0 MHz	114 dBμV	116 dBμV	" "	" "
11.0 MHz	113.5dBμV	111 dBμV	" "	" "
12.7 MHz	112 dBμV	97 dBμV	" "	" "
12.7 MHz	112 dBμV	104 dBμV	" "	Coupler #3 in 1 out 2 3 sections of copper tubing
14.0 MHz	113.5dBμV	109 dBμV	" "	" "
17.0 MHz	116 dBμV	108 dBμV	" "	" "
20.0 MHz	118 dBμV	104 dBμV	" "	" "
20 MHz	118 dBμV	104 dBμV	" "	" "
23 MHz	119.5 dBμV	106 dBμV	" "	" "
26 MHz	119 dBμV	109 dBμV	" "	" "
28 MHz	118 dBμV	108 dBμV	" "	" "
30 MHz	117 dBμV	95 dBμV	" "	" "
35 MHz	128 dBμV	90 dBμV	MD-105-T1 (74.5") 10 V/M - 140 dB v	" "
35 MHz	122 dBμV	90 dBμV	MD-105-T1 (74.5") 5 V/M = 134 dB v	" "
40 MHz	123 dBμV	100dBμV	" "	DM-105-T1 (5 sect)
50 MHz	125 dBμV	108 dBμV	" "	" "
60 MHz	127 dBμV	98 dBμV	" "	" "
70 MHz	127 dBμV	102 dBμV	" "	" "
80 MHz	126 dBμV	92 dBμV	" "	" "
90 MHz	125 dBμV	113 dBμV	" "	" "
100 MHz	124 dBμV	99 dBμV	" "	" "
100 MHz	124 dBμV	109 dBμV	MD-105-T1 (74.5")	DM-105-T1 (2 sect)
200 MHz	115.5dBμV	117 dBμV	Change to H/P 778 Coupler	" "
200 MHz	118 dBμV	120 dBμV	DM-105-T2	EMCO 3101
300 MHz	114 dBμV	114 dBμV	" "	" "
400 MHz	111 dBμV	114 dBμV	" "	" "
500 MHz	109 dBμV	112 dBμV	DM-105-T3	" "
600 MHz	106.5dBμV	107 dBμV	" "	" "
700 MHz	105 dBμV	109 dBμV	" "	" "
800 MHz	103.5dBμV	113 dBμV	" "	" "
900 MHz	102 dBμV	111 dBμV	" "	" "
1000 MHz	101 dBμV	118 dBμV	" "	" "

Table A-3 RS03 Radiated Susceptibility Data (Sheet 2)

5-9-72

FREQ.	SCOPE INDICATION NEEDED	DIVIDER PROBE IND.	RECEIVE ANTENNA CONFIGURATION	TRANSMIT ANTENNA CONFIGURATION
1.0 GHz	108 dBμV	109 dBμV	EMCO 3102, S/N 2332	Singer AT-112 S/N A606
2.0 GHz	100.7 dBμV	108 dBμV	" "	" "
2.0 GHz	100.7 dBμV	107 dBμV	" "	" "
3.0 GHz	97.9 dBμV	111 dBμV	" "	" "
4.0 GHz	94.7 dBμV	103 dBμV	" "	" "
5.0 GHz	93.3 dBμV	106 dBμV	" "	" "
6.0 GHz	91.2 dBμV	102 dBμV	" "	" "
7.0 GHz	89 dBμv	103 dBμV	" "	" "
8.0 GHz	87.7 dBμV	105 dBμV	" "	" "
9.0 GHz	84.7 dBμV	106 dBμV	" "	" "
10.0 GHz	84.7 dBμV	111 dBμV	" "	" "

Table A-3 RS03 Radiated Susceptibility Data (Sheet 3)

APPENDIX B

ENVIRONMENTAL TEST DOCUMENTATION

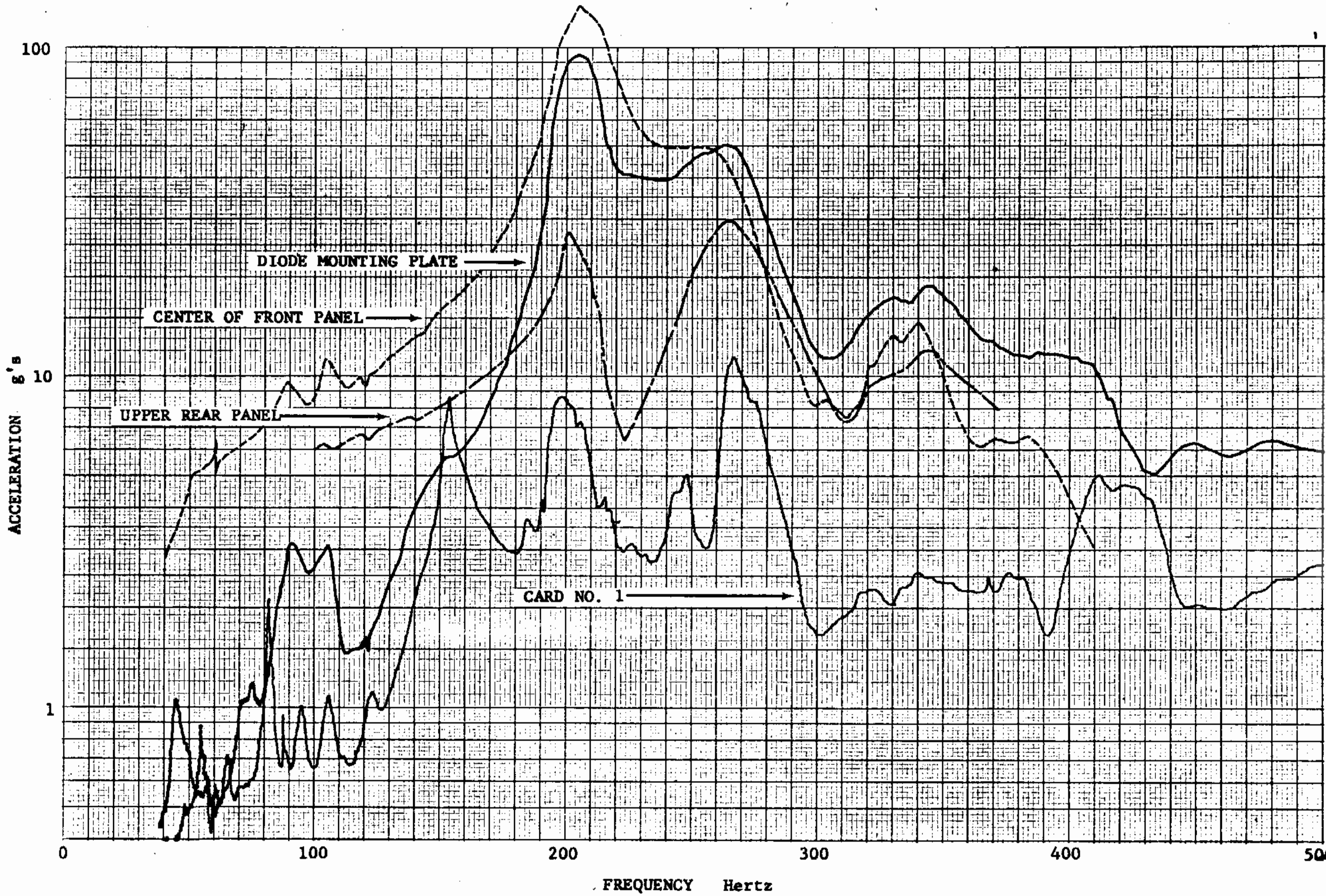


Figure B-1 **VIBRATION RESPONSE - UNIT 4, LATERAL**

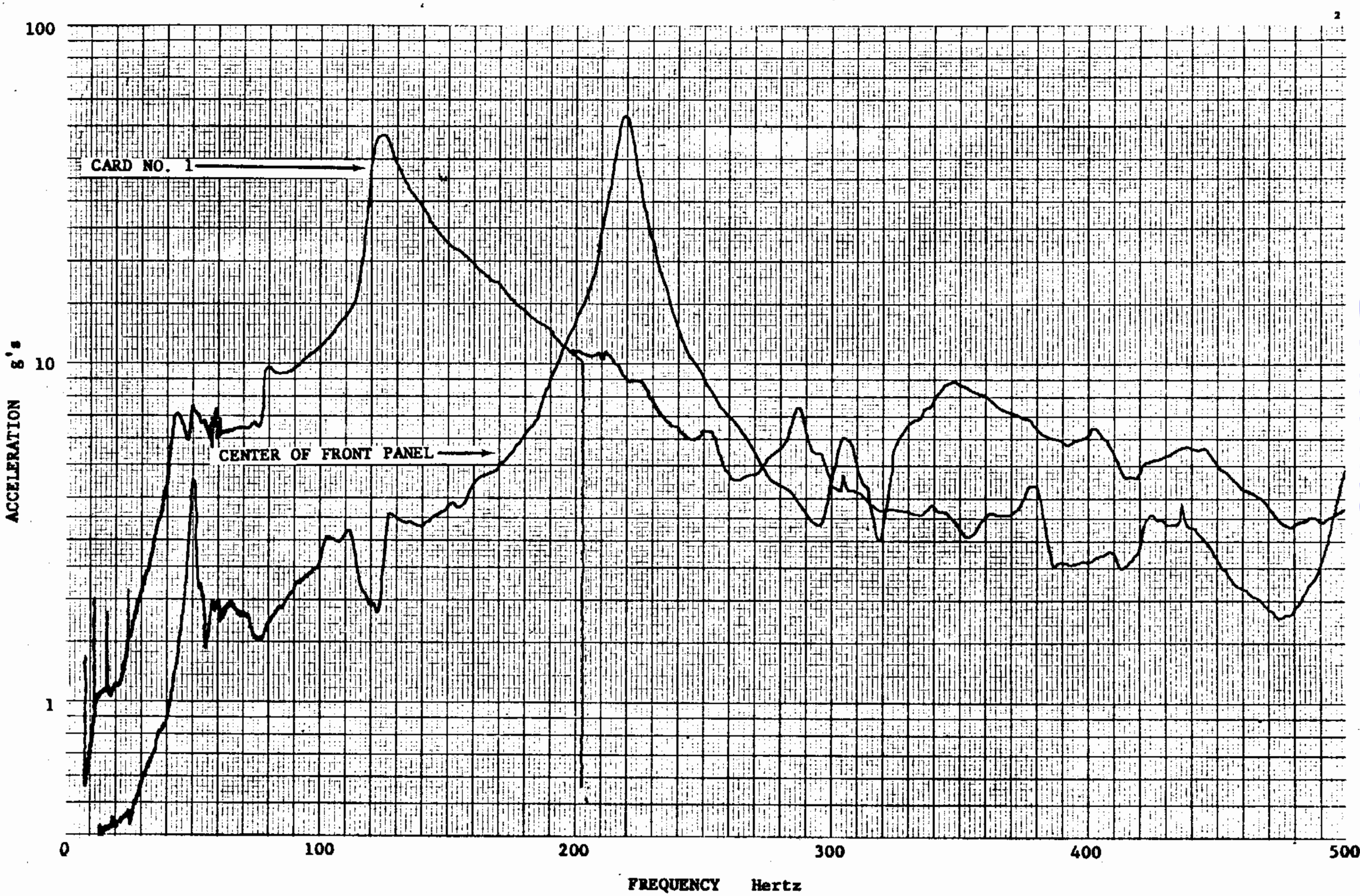


Figure B-2 VIBRATION RESPONSE - UNIT 4, VERTICAL

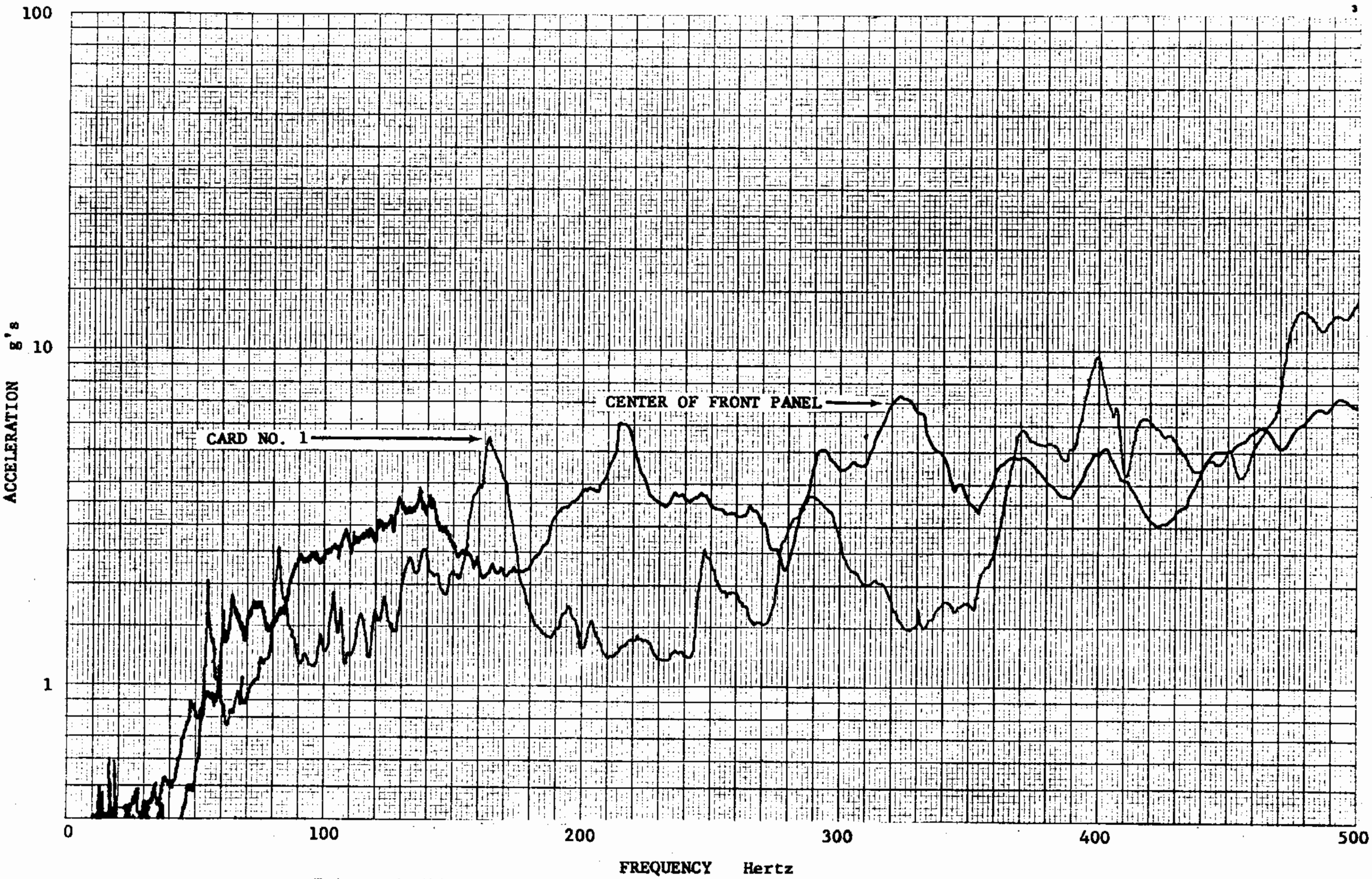


Figure B-3 VIBRATION RESPONSE - UNIT 4, LONGITUDINAL

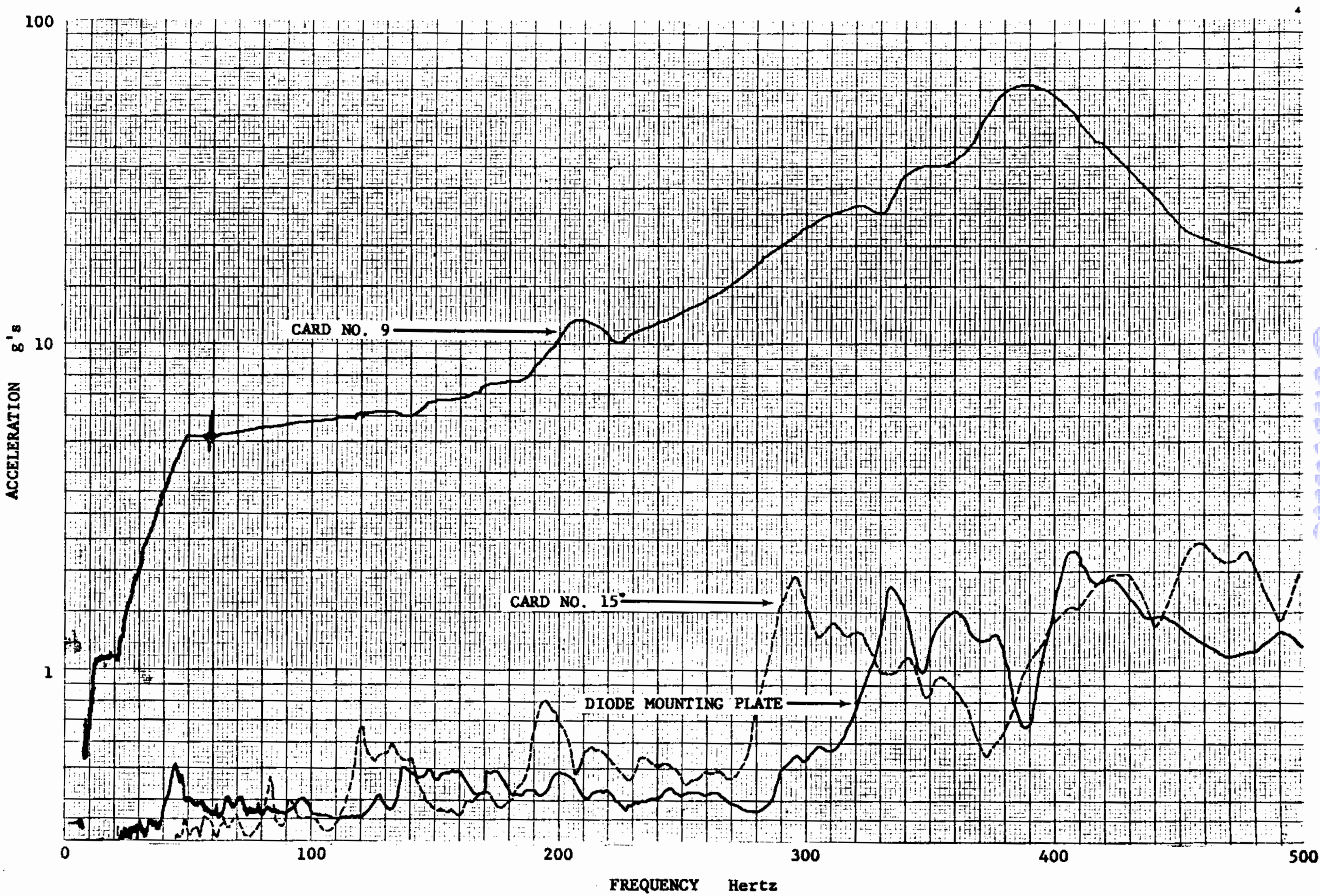


Figure B-4 VIBRATION RESPONSE - UNIT 1, LATERAL

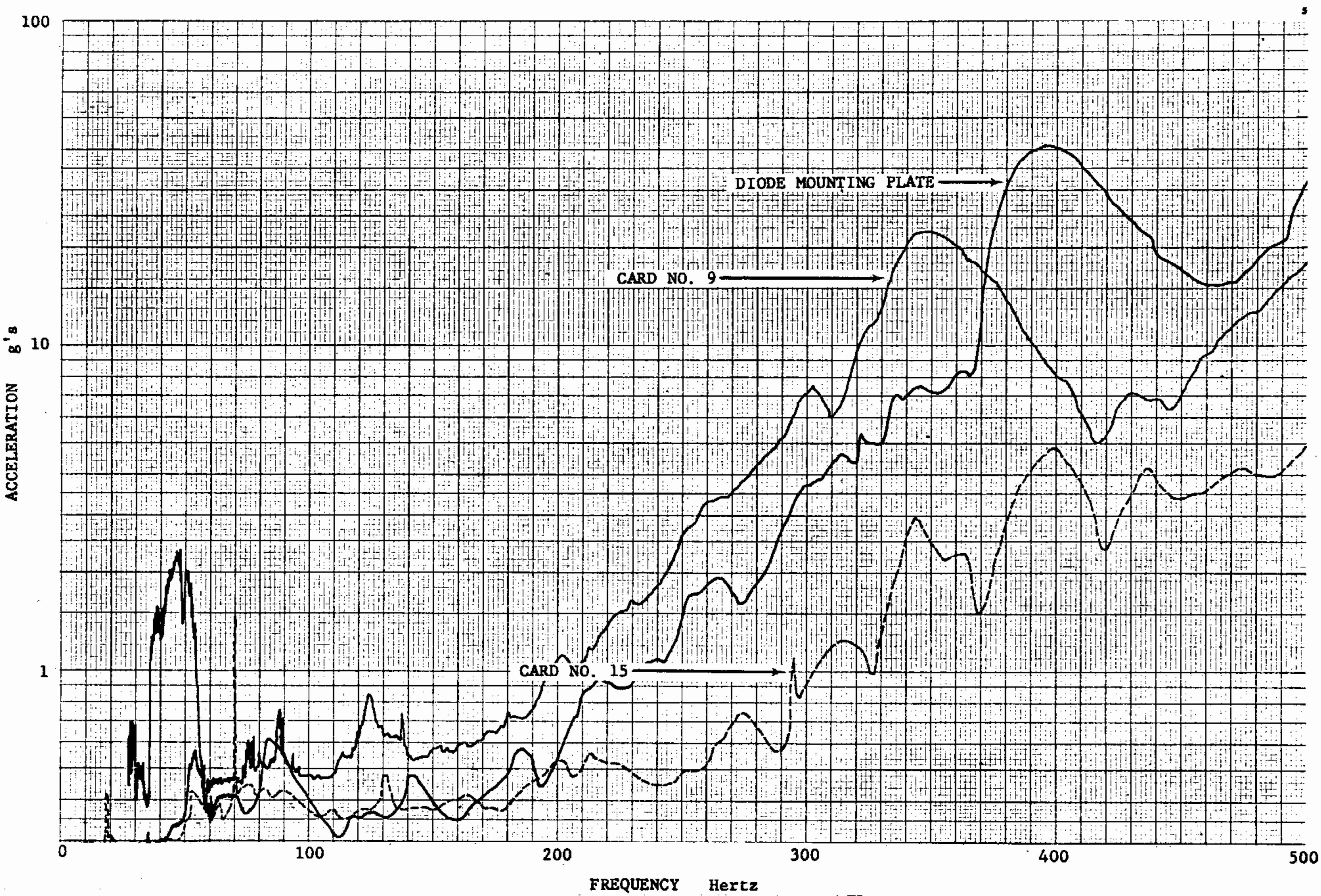


Figure B-5 VIBRATION RESPONSE - UNIT 1, VERTICAL

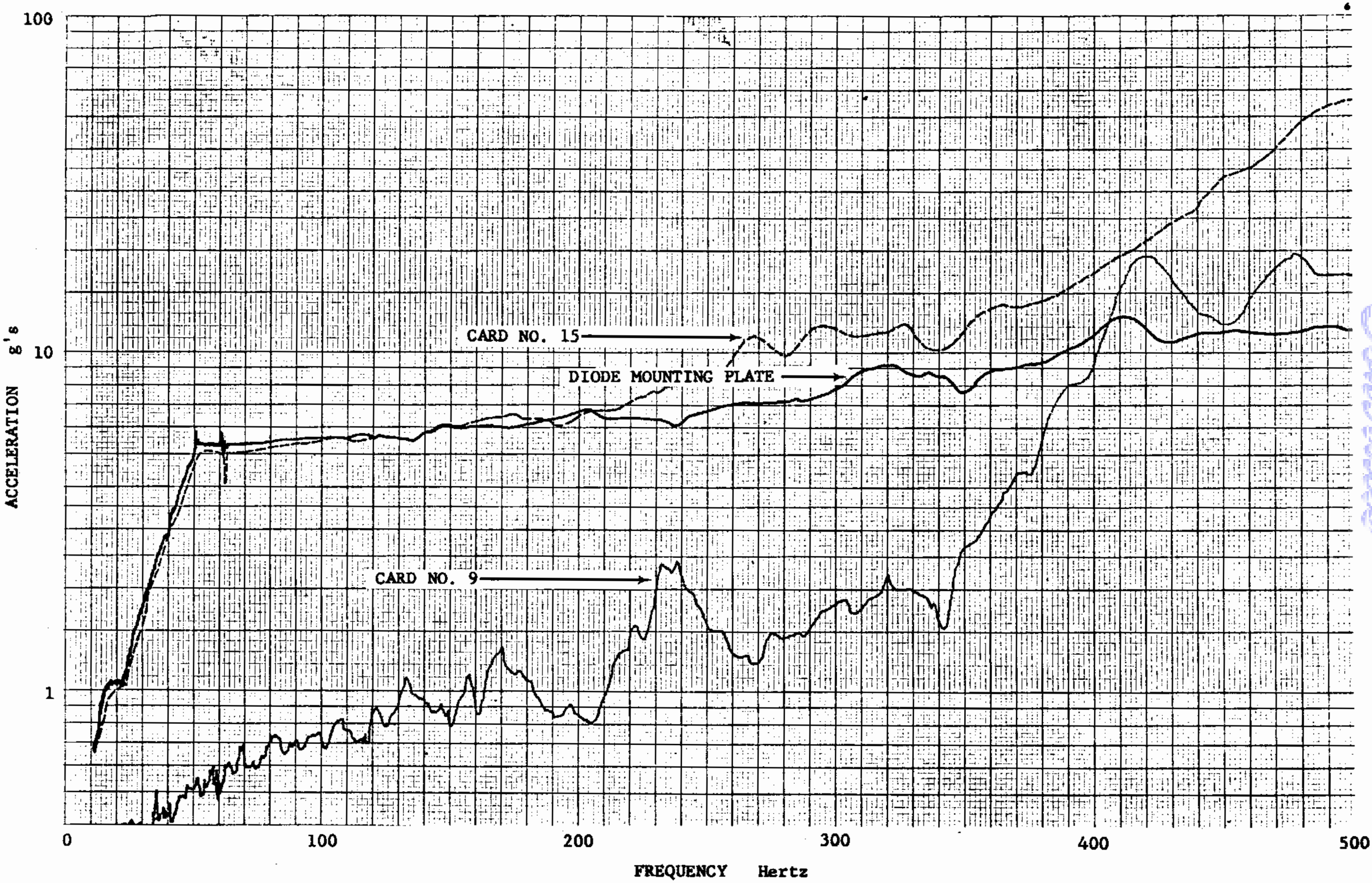


Figure B-6 VIBRATION RESPONSE - UNIT 1, LONGITUDINAL

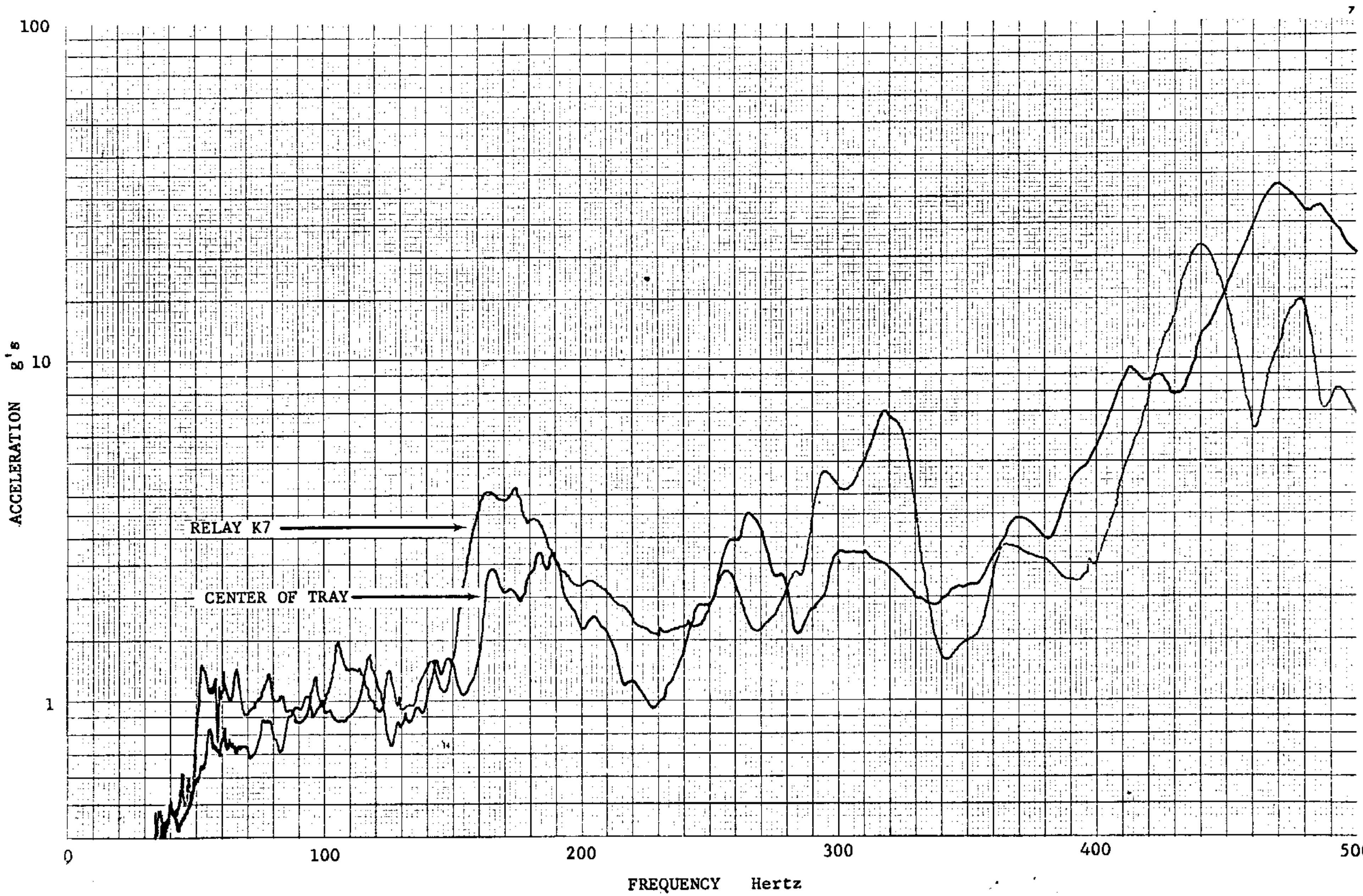


Figure B-7 VIBRATION RESPONSE - SIGNAL TRANSFER UNIT, LATERAL

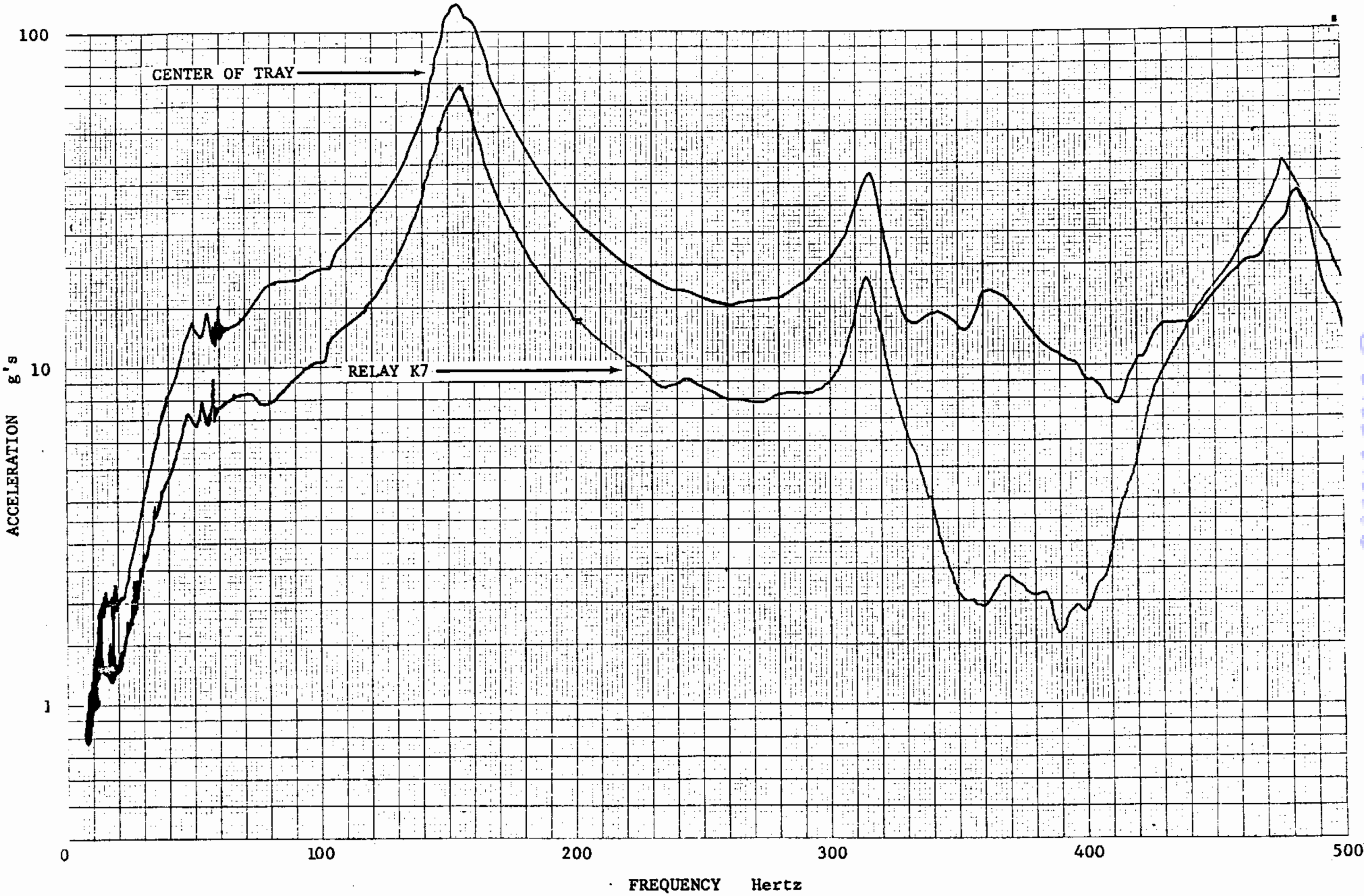


Figure B-8 VIBRATION RESPONSE - SIGNAL TRANSFER UNIT, VERTICAL

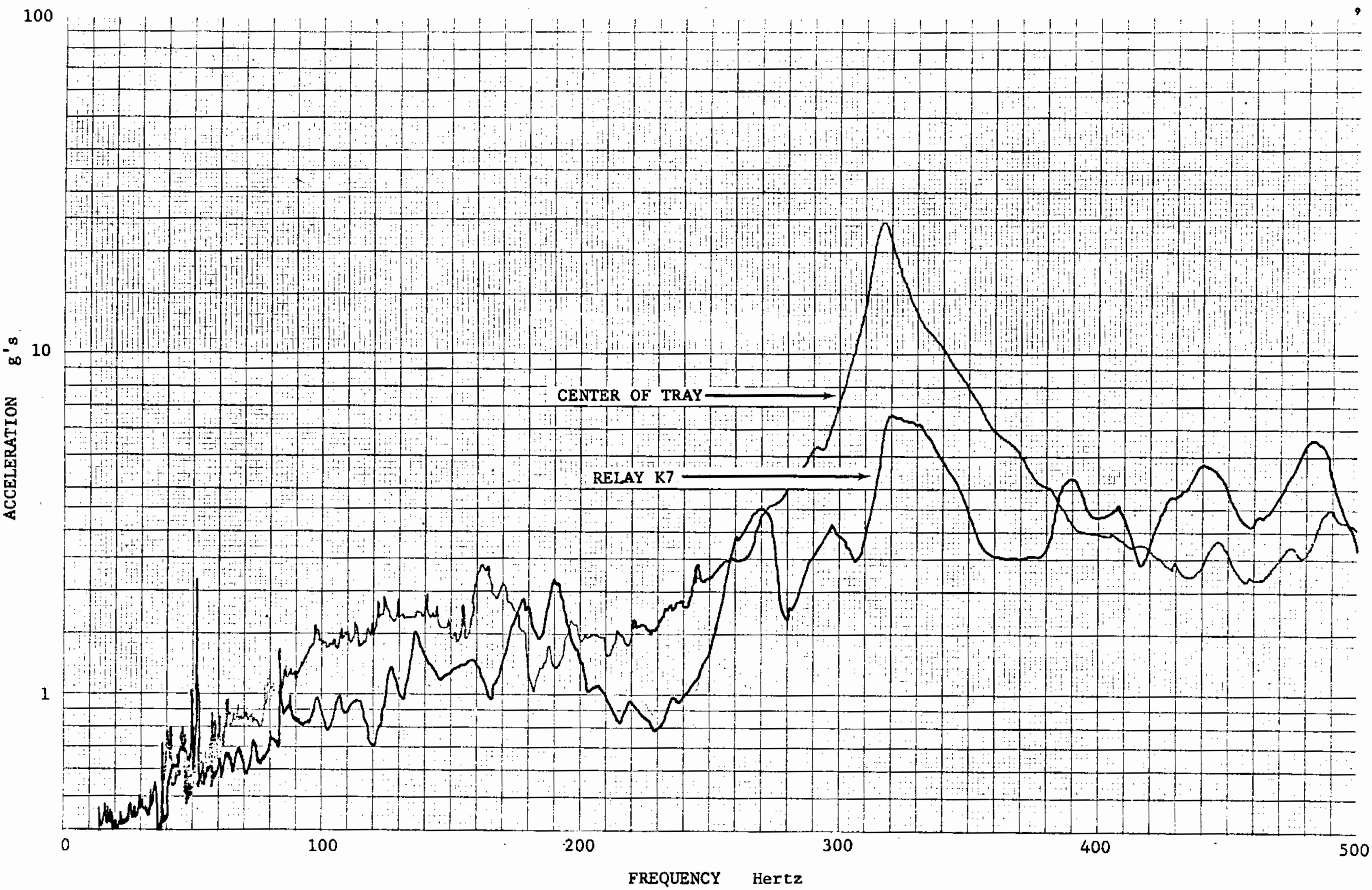


Figure B-9 VIBRATION RESPONSE - SIGNAL TRANSFER UNIT, LONGITUDINAL

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13. ABSTRACT This report contains a description of the design, development, airworthiness testing and flight test of multiplexing hardware for use in a fly-by-wire flight control system. The multiplexing concept employed makes use of By-phase Manchester baseband modulation of pulse coded digital data. Each analog value to be transmitted is converted to a digital format serially and transmitted over a twisted-shielded-pair cable. A party line transmission concept was employed to permit two transmitters to share the same transmission line. The air-worthy equipment was used to transmit signals in the fly-by-wire flight control system of the Total In-Flight Simulator (TIFS) aircraft. Installation and flight testing was accomplished by Calspan Corporation under contract F33615-72-C-1183. Multiplex system update rates of 400, 200, 100, and 50 samples per second were investigated. Although filters were required to smooth the signals to the servo valves at the lower sampling rates of 50 and 100/second, the evaluation pilots could not discern whether or not the control signals were being processed by the multiplexing equipment at any of the sampling rates. Twelve flights (23.2 hours) were accomplished. The results have shown the soundness of employing a multiplex scheme in fly-by-wire control systems and has provided experience that will be valuable in future considerations of digital flight control systems.

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Multiplexed Flight Controls						
Fly-By-Wire						
Digital Flight Control Systems						

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