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FOREWORD

This report was prepared by North American Aviation, Inc., Los Angeles Division, International Airport, Los Angeles 9, California, under Contract AF 33(616)-7859. Mr. R. N. Winner, Senior Research Engineer, served as project engineer for North American Aviation. The work was performed under the cognizance of the Training Research Division, Behavioral Sciences Laboratory, 6570th Aerospace Medical Research Laboratories, in support of Project No. 6114, "Simulation Techniques for Aerospace Crew Training," Task No. 611410, "Display Synthesis." Mr. R. G. Cameron, Simulation Techniques Branch, Training Research Division, served as contract monitor.

The design study sponsored by this contract was started in February 1961 and was completed in September 1962.

The personnel participating in the design study were A. Silgalvis, J. Pizzo, H. Shimabuku, and W. Kuykendall of North American Aviation, Los Angeles Division, Flight Simulation Group.

ABSTRACT

A design study was conducted leading to development of a flexible laboratory design tool for synthesizing and analyzing cockpit displays. The resulting cathode-ray tube instrument synthesis system (CRT-ISS) is compatible with standard analog computer systems and has a self-contained provision for generation of 50 alpha-numeric and geometric symbols, each of which can be displayed by any or all of the 64 time-shared display channels. In addition, the size, static vertical and horizontal positioning, and intensity of each symbol displayed can be independently controlled for each of the 64 channels. The preprogramming of the display is accomplished by patch cord plugging and adjustment of potentiometers. The output of the system consists of X-, Y-, and Z-axes signals which permit driving conventional cathode-ray tube oscilloscopes singly, in multiples, or in various combinations. An additional task of the design study was the development of a 21-inch solid-state display oscilloscope.

PUBLICATION REVIEW

This technical documentary report is approved.

Walter F. Grether

WALTER F. GRETHER
Technical Director
Behavioral Sciences Laboratory

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SECTION I

INTRODUCTION

In the course of simulating current aerospace vehicles and projecting toward the simulation of future aerospace vehicle configurations it has become apparent that an increasing number of pilot and operator displays will consist of cathode-ray tubes and electro-optical devices.

Creation of replicas of the above displays, for simulation purposes, usually requires some of the following techniques:

(1) Modification of meter faces or tapes
(2) Construction of servo driven gear trains
(3) Modification of film projectors
(4) Construction of special-purpose electronic image generating equipment via interconnection of standard pulse and wave circuits, electronic switches and closed-line television.

The purpose of this investigation has been to determine the feasibility of rapidly programming the electronic generation of all or part of the displays generally encountered in simulation and presenting them at the display interface via cathode-ray tube media.

A parallel purpose has been the development of an engineering model capable of demonstrating some generation techniques for cathode-ray tubes (CRT's).

SECTION II

DEFINITION OF THE PROBLEM

Most of the display techniques, used in the past, have proven costly from the standpoint of both hardware cost and the set-up time required for fabricating and integrating each display.

The CRT has several advantages as a display device.

1) Low-cost for most of the common CRT types
2) Wide variety of configurations
3) Brightness and spot size comparable to any display devices (under instrument lighting conditions)
4) Unrestricted format over the display face

Disadvantages of CRT displays may be summarized as follows:

1) Information must be introduced sequentially
2) For a constant acceptable flicker rate, writing time decreases directly with increasing information density
3) Observable flicker frequency varies with the contrast and separation between picture elements
4) Display contrast varies with ambient light and the color of the phosphor employed
5) Ratio of peak fluoresence to phosphoresence is generally high, for most phosphers, resulting in non-uniform brightness over the display interval
6) High-voltage requirements and deflection-sensitivity vary between tubes of different sizes.

Whether or not CRT's or actual aerospace vehicle displays are employed in a simulator some provision must be made for driving these displays dynamically in accordance with the flight equations as perturbed by the pilot.

Classically, flight simulator computation has been analog. More recently hybrid mechanizations or all digital mechanizations have been employed.

However digitized a simulator may be, it must ultimately drive aerospace vehicle hardware which to date has been largely analog. Due to these airborne instrument requirements a large number of signals will be available at the simulator computer interface in analog form.

SECTION III

SYSTEM APPROACH

A. SEQUENCER

From the previous discussion of the problem it may be readily seen that a display machine capable of accepting analog inputs should be more utilitarian than one operating strictly from a digital address.

Furthermore, if the usual array of instrument displays is considered from the standpoint of information content a large body of redundant alpha-numeric information may be found.

The distribution of this redundancy throughout a display panel area indicates that it would be desirable to keep a general machine configuration rather than a fixed format, useful for simulating only specific classes of instrument configurations.

"General purpose" in any system denotes a certain flexibility and within this connotation implies an expansible system which may readily adapt itself to functionally serve as many portions of the simulator display-interface as possible.

Selection of the number of display channels to be used was based on the following:

1. Tolerable display flicker frequency.
2. Typical simulator information.
3. Any multiple of 2, so that full advantage could be taken of binary switching circuits.

A flicker frequency of thirty cycles was decided to be the lowest tolerable, assuming P-1 or P-7 display screens.

Trace brightness was considered to be no greater than 35 ft.-Lamberts under ambient lighting not exceeding a highlight brightness of 40 ft.-Lamberts. Typical scope filter faces were assumed such as colored plexiglass and/or filter glass faceplates.

Thirty-two channel display capacity was chosen to demonstrate initial feasibility with the capability of expansion to 64 channels after evaluation.

A pre-prototype engineering model of a 32-channel sequencer was delivered to the 6570th Aerospace Medical Research Laboratories, Wright-Patterson AFB, Ohio, in July 1961 and after evaluation (in March 1962) a 64-channel unit was constructed.

A 32-channel unit utilized the same channel display time as the 64-channel unit but the frame time (display repetition rate) was 60 cps contrasted with the 30 cps employed in the 64-channel system. This difference was due to the two to one difference in the number of display channels between the two units.

Provision was made to divide the machine capacity between eight display devices, based on:

1. Amount of patch-panel space.
2. Complexity of the resulting switching circuitry.
3. Ability to run more than one simulator program at the same time while using only one display console.

Since many simulator studies are in support of programs not necessarily located within one laboratory, it seemed desirable to have a moderate degree of portability. Hence the system was housed in a table top cabinet capable of being moved about by two men.

B. CHARACTER GENERATOR

An ideal character generator would be capable of tracing every conceivable symbol within the limits of the imagination of the programmer. More practically, from the standpoint of simulating aerospace instruments, the capability was restricted to generating the entire alphabet in upper case letters, all numerals, and commonly used geometric symbols (rectangles, grids and circles).

The characters were permitted to be interchangeable with each other so that new symbols could be introduced in the machine at will. With regard to character format it became difficult to reduce circuit complexity without affecting legibility.

The difficulty was centered about the requirement that the character be written within the display time for one channel (520 microseconds) and that the legibility for characters approaching 1/4 screen diameter not be compromised.

Many character generation schemes were considered and they may be categorized as follows:

1. Scanned characters:
    a. Magnetic storage scan
    b. Flying spot scanned film
    c. Scanned monoscope
2. Waveform synthesized - employing passive network
3. Dot
4. Stroke matrix (all strokes deflected - unwanted strokes blanked)
5. Stroke character (only desired strokes deflected)

Scanned characters were ruled out from the standpoint of complexity, the excessive deflection bandwidths required for sharp points of discontinuity and the lack of legibility at small character size.

Waveform synthesized characters using passive and active networks required many precise inductors and capacitors to yield characters whose legibility suffered from a lack of uniqueness (waveform synthesized characters give the appearance of cursive writing).

Dot characters appeared very attractive from the standpoint of least circuit complexity but legibility suffered at large character size unless an impractical number of dots were used.

Larger numbers of dots were not considered practical since the flicker rate would decrease with increasing dot numbers unless display storage was used. Display storage was precluded due to the requirement for standard low cost CRT display devices.

Stroke matrix (with selective blanking) seemed to promise the best results for all character sizes, but was not used for the following reasons:

1. Moderately high deflection rates resulting in low display tract duty cycles with attendant loss in display brightness.
2. Complex blanking circuitry resulting in repetition rates comparable to the deflection rates.
3. The system requirement dictated compatibility with a wide variety of laboratory scopes, many of which employ low accelerating voltages.
4. A contemplated large screen display scope accessory development was intended to operate at high brightness and consequently high deflection powers.

"Off the shelf" large-screen scopes have historically operated with deflection bandwidths below 10 kc.

It was felt that components were becoming available which would permit an order of magnitude of improvement in large-screen scope electro-magnetic deflection-amplifier bandwidth, but nothing of the magnitude that would permit large-screen repetitive writing of complete stroke matrices.

As a result of the foregoing, a five-stroke character scheme was employed in which all five strokes were utilized, either in sequence or by restroking those characters where five unique strokes were not required for definition. This scheme permitted a character writing rate as low as 5 kc which could be sampled by the sequencer and presented on 32 channels at a 60 cps frame rate.

As mentioned earlier the sequencer was evolved as a general purpose sampling device. In line with this requirement the character generator system approach was to generate all characters in parallel time so that they might be used in any display channel without regard to programming restrictions, and also be available for use in other systems or sequencers simultaneously.

C. DISPLAY SCOPE

In applications such as energy management or navigation it is mandatory to present the system output in large-screen format. Here, due to the duty cycle and current density of the scanned phosphor area, one must consider the brightness to be achieved at the maximum display rate. Attendant with any brightness consideration is the spot size encountered with a given beam current. The apparent spot size is usually even greater due to optical spreading effects in the phosphor and in the glass.

For reasons of economy and versatility it was desirable to have a display scope chassis which would accommodate a large number of CRT screen sizes.

Thus the deflection angle, accelerating potential, focusing method and neck size should be chosen to encompass the widest variety of "off the shelf" cathode ray tubes. A 70 degree deflection angle was chosen along with a 1-7/16 inch neck size as covering the widest group of the electromagnetically deflected family.

Based on the requirements of the largest 70 degree CRT's commonly in use, 15 kv was selected for the 2nd anode voltage. Obviously, a reduction in anode voltage or deflection power angle would accommodate any CRT's in the family having lesser requirements.

Electrostatic focus was chosen based upon the increasing acceptance of this method among commercial consumers of CRT's and the fact that its use does not in any way interfere with the addition of electromagnetic focus when desired.

SECTION IV

SYSTEM DESIGN

A. TIMING & BLANKING CIRCUIT

Since the timing and blanking functions are inextricably involved with an understanding of the entire cathod-ray tube instrument synthesis system (CRT ISS) design, they will be discussed prior to presenting either the sequencer or character generator design approach.

The block diagram and schematics of the timing and blanking functions appear in figures 1, 2, and 3.

A master oscillator at 19.2 kc produces a negative pulse which is divided and reshaped by a binary. The binary triggers a scale of five counter which produces an output at the beginning of each of the 64 sequencer display intervals. This output is used to trigger the master blanking multivibrator whose output width is adjustable and insures that the CRT trace will not be visible while deflecting between channels.

Simultaneous to the foregoing action, the binary operates a delay multivibrator (master trigger delay) which in turn provides the system with a trigger via the character sequencer.

The delay is necessary to insure the start of trace blanking prior to the initiation of display switching in either the character generator or sequencer.

The output of the character generator is used to trigger the sequencer binary to move to a new display channel at the end of every fifth character stoke.

The binary is a counter which is scaled to generate the 64 pedestals required for sequencer operation.

The 32 to 1 output of the counter reoccurs at a 60 cps rate and is fed back to the master oscillator line lock section where it is compared with the 60 cps line. Any deviation in pulse width or phase creates a DC error which is applied degeneratively to the base of the master blocking oscillator for frequency control.

Thus, the entire display system remains in synchronism with the 60 cps line so as to freeze any ripple field effects that would otherwise cause random trace motion at the CRT.

Since the character generator operates at a rate which is five times the sequencer display rate some provision must be made for blanking between character strokes. The 9600 cps output of the 2 to 1 binary is also applied to the blanking trigger gate. This gate may be enabled on a channel by channel basis from the patch panel according to the discretion of the programmer. When enabled, the blanking trigger gate permits 9600 cps undelayed pulses to trigger the master blanking multivibrator and thus blank the trace between each character stroke.

B. SEQUENCER

The sequencer samples, in sequential fashion, each channel of information available at the patch panel until all 64 channels have been examined for equal periods of time. The process then continues repetitively at a 30 cps rate.

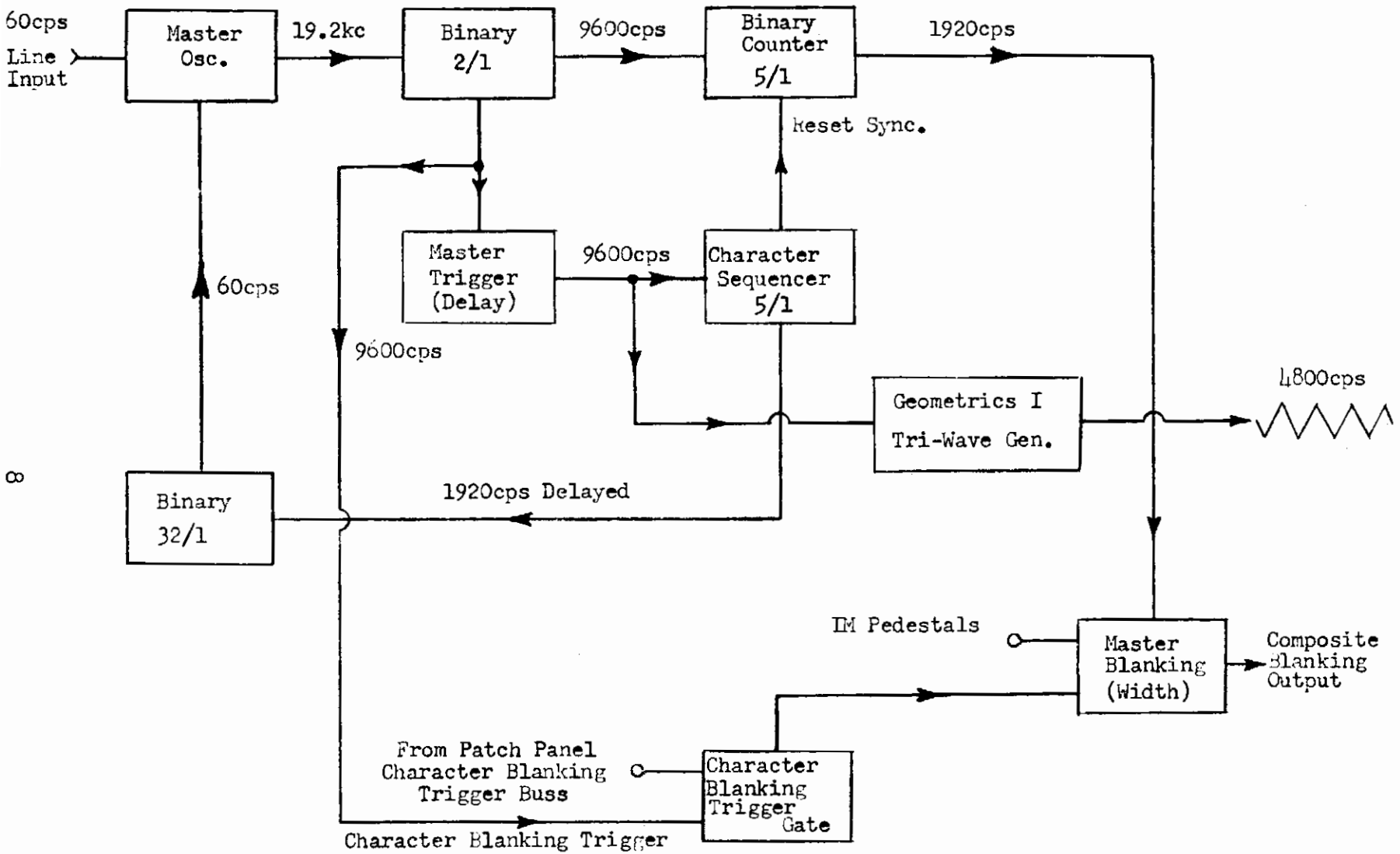


Figure 1. Timing Diagram

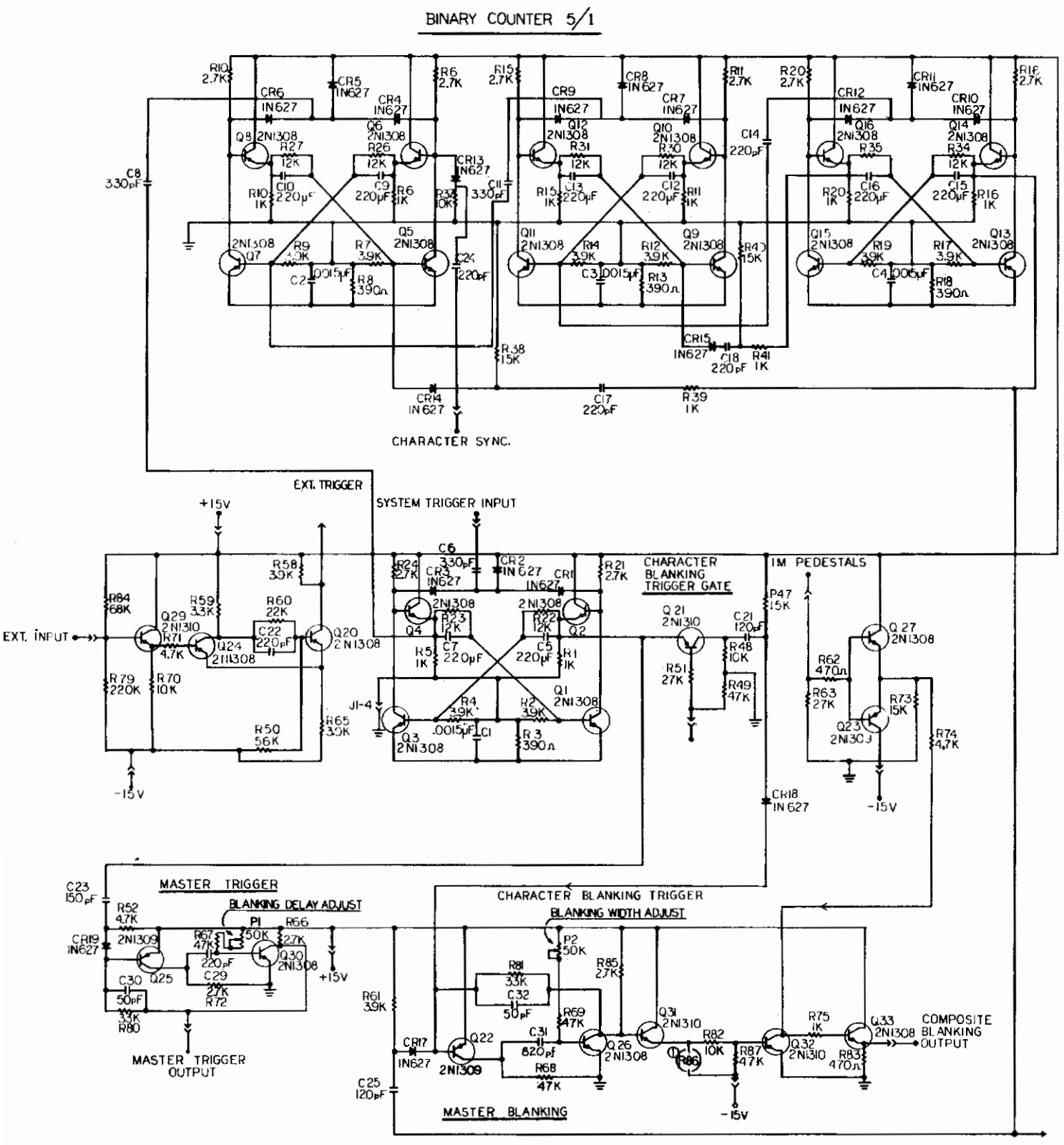


Figure 2. COMPOSITE BLANKING AND TRIGGER

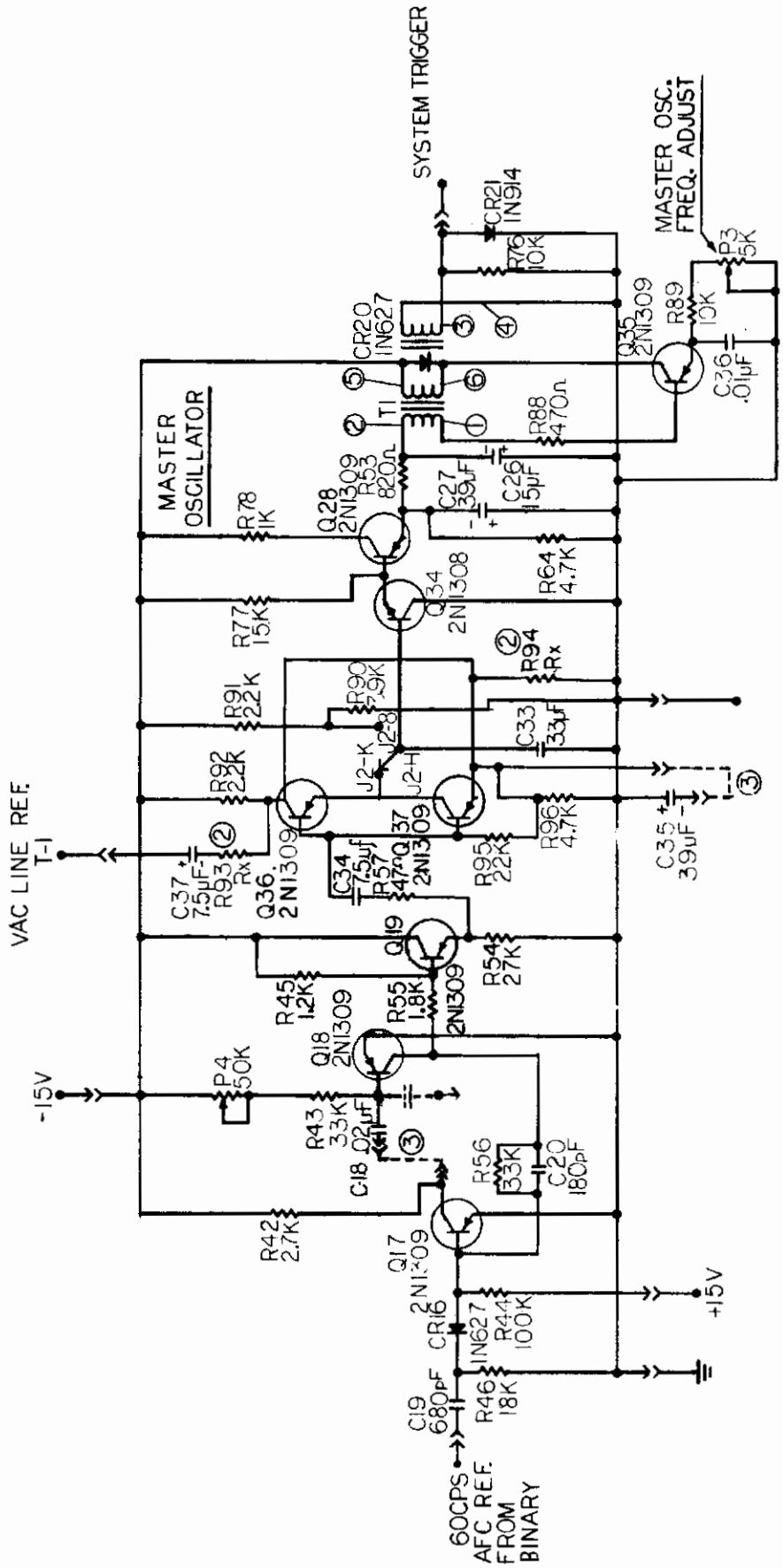


Figure 3. MASTER OSCILLATOR

Each channel consists of the algebraic sum of a coarse and fine positioning signal, an analog signal, and a character generator signal. A practical limit of DC to 20 kc between 20 and 200 V peak to peak was set for the f(t) optional inputs.

The block diagram of figure 4 illustrates sequencer operation on one of the 64 typical display channels.

The composite line lock and trigger, triggers the binary card once every 520 microseconds. The binary card is connected as a scale of 64 counter.

The 12 variable outputs (two from each of the six binaries in the counter) are converted to 64 minterms via the sectional matrix.

The first portion of the sectional matrix converts the 12 input variables into two sets of 8 minterms. One card of the second portion of the matrix yields the sum of the first 32 sequential minterms.

The other card of the second portion yields the sequential sum of minterms 33 through 64.

The matrix outputs are of low amplitude and have poor rise and fall times primarily due to diode capacitance and reverse recovery time. The inverter improves the pulse shape of the 64 matrix outputs and produces a pedestal having a rise and fall time of less than one microsecond, a zero signal level of -15V and a saturated output level of +25V.

The inverter output is buffered by the complimentary buffer and the 25V pedestal is applied as a turn-on pulse to three sets of two transmission gates each.

Character and analog signals f(t) are permitted to enter the system via the patch panel and pass through panel mounted attenuators, one for the component of the function along the Y-axis and one for the component along the X-axis. The attenuators permit continuous adjustment of the aspect ratio of the display elements on each channel. The third signal consists of the sum of a coarse and fine positioning signal also present in both the Y and X coordinates.

All of these functional display inputs are impedance transformed through signal emitter followers to isolate the effects of the attenuator setting versus gate loading and to provide a low impedance signal source to the gate so as to optimize switching time and high-frequency performance.

There is a total of 64 x 3 sets of two transmission gates each for the entire system (one set of 64 x 3 for Y and one set of 64 x 3 for X).

Each group of 64 gates has a common load resistor located on the deflection outputs module.

The deflection outputs module consists of summing amplifiers, inverting amplifiers and output switching to divide the sequencer output, according to the option of the programmer, among eight scopes.

The summing amplifiers, one for X and one for Y, sum positioning, character and analog computer inputs from the respective Y and X sets of transmission gates.

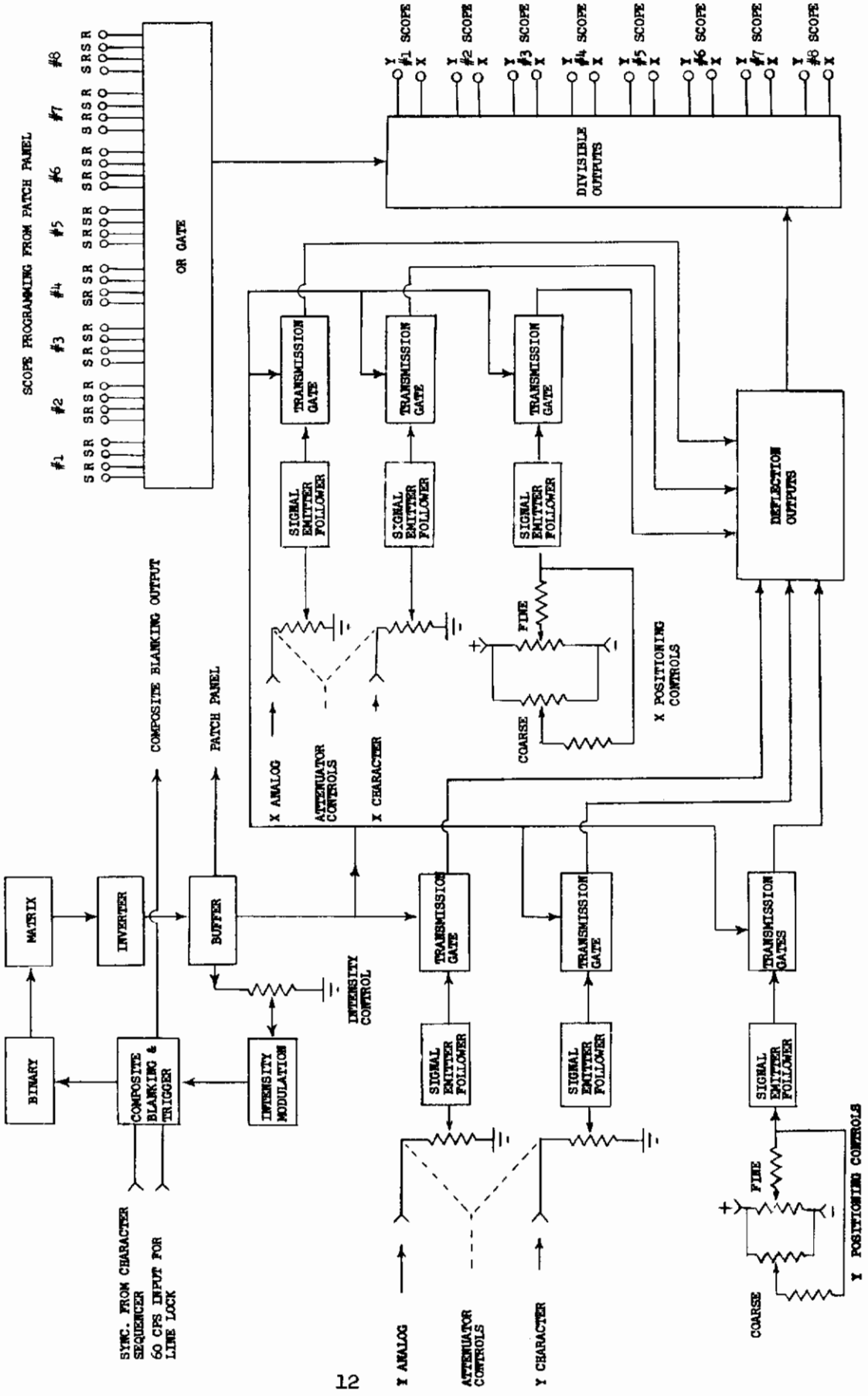


FIGURE 4. BLOCK DIAGRAM-TYPICAL DISPLAY CHANNEL

The second amplifier in cascade re-inverts the signal so that the console output has the same polarity as the externally originating computer signals introduced to the patch panel. Any transmission loss through the system is also negated here by rescaling.

Sixteen transmission gates for dividing the outputs (8 for X and 8 for Y) are bussed together and tied to their respective X and Y amplifiers.

Pedestals supplied from the divisible outputs card operate the deflection output gates.

The programmer may command the divisible outputs from the patch panel via the OR gate. The logic is arranged so that the main console output may be switched to a scope at the beginning of any channel period and may be switched off the screen edge at the end of any display interval. Two such choices of SET and RESET are permitted on each of the eight divisible output lines. The switching takes place on both the X and Y outputs simultaneously.

C. CHARACTER GENERATOR

The character sequencer is the heart of the character generation system. As the name implies it is very similar to the sequencer system used for sampling the 64 display channels.

Three binaries connected as a scale of five counter receive a delayed trigger signal from the composite blanking and trigger card. The six variables from the counter are converted by a square diode matrix into five sequentially occurring pedestals.

These five pedestals are inverted and re-inverted to produce a positive output for the first five character strokes.

Since a full 520 microseconds is allowed to display each character, an additional three outputs are provided which consist of combinations of the previous five pedestals for restroking on those characters having fewer than five strokes. For instance, stroke #6 repeats pedestals occurring during interval 2 and 3, stroke #7 repeats intervals 4 and 5 and stroke #8 repeats intervals 2, 3, 4 and 5 (see figure 5).

The character buffer is used to impedance transform the eight switching pedestal outputs from the character sequencer and to divide the pedestal load so as to relieve the component tolerances required for each pair of pedestal inverters. There are three sets of eight buffers each, assigned to the above task (see figure 6).

Symbol and character generation is accomplished within each of the 48 character cards. Although each card is printed to be identical with all others, individual option may be exercised in connecting components during construction, so that the advantages of restroking may accrue in the form of a reduction in the number of components required.

The schematic figure 7 shows a complete five stroke character card where the option of restroking has not been exercised.

The left side of the schematic illustrates the Y coordinates of the character and the right side illustrates the X coordinates.

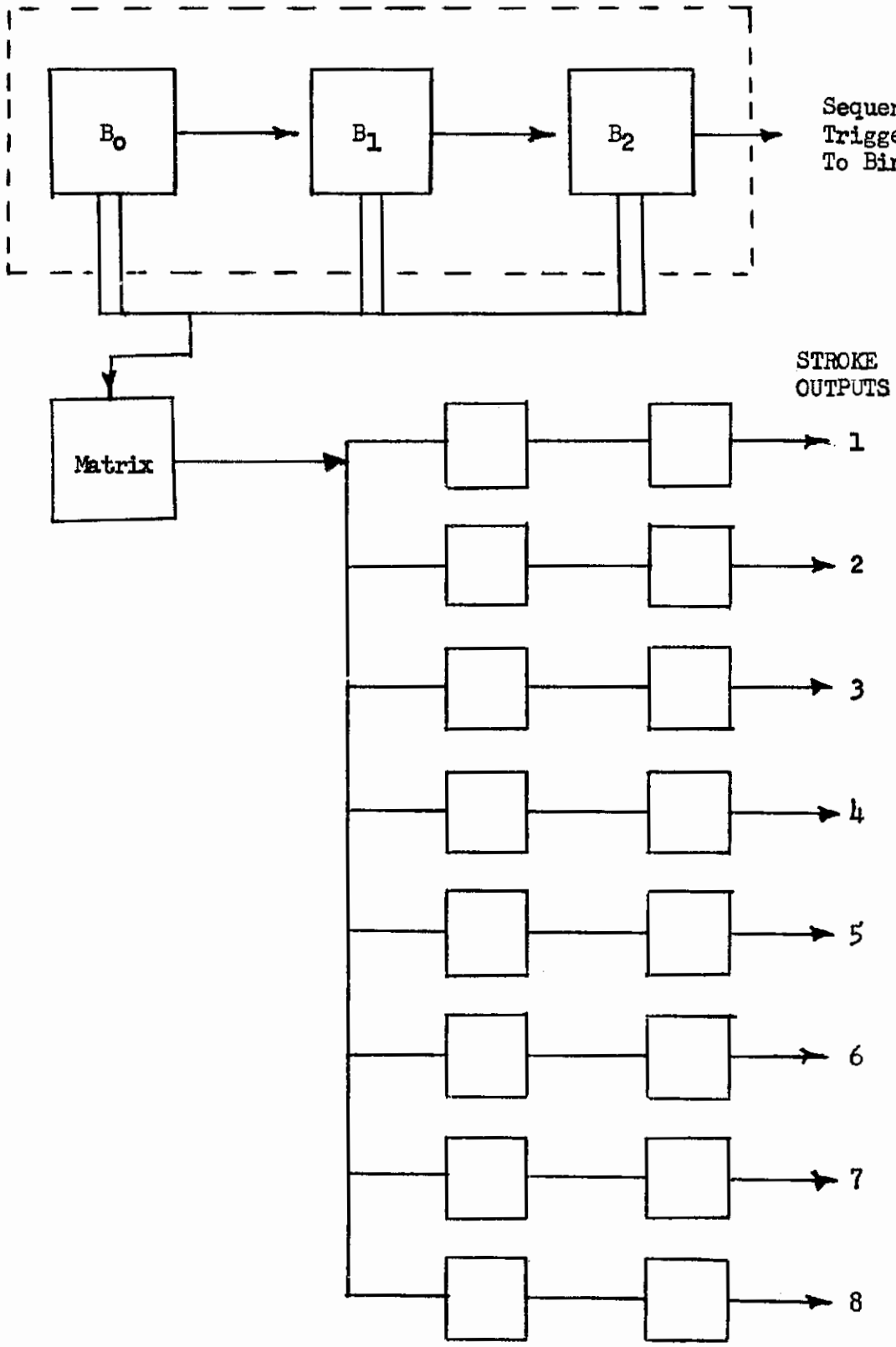
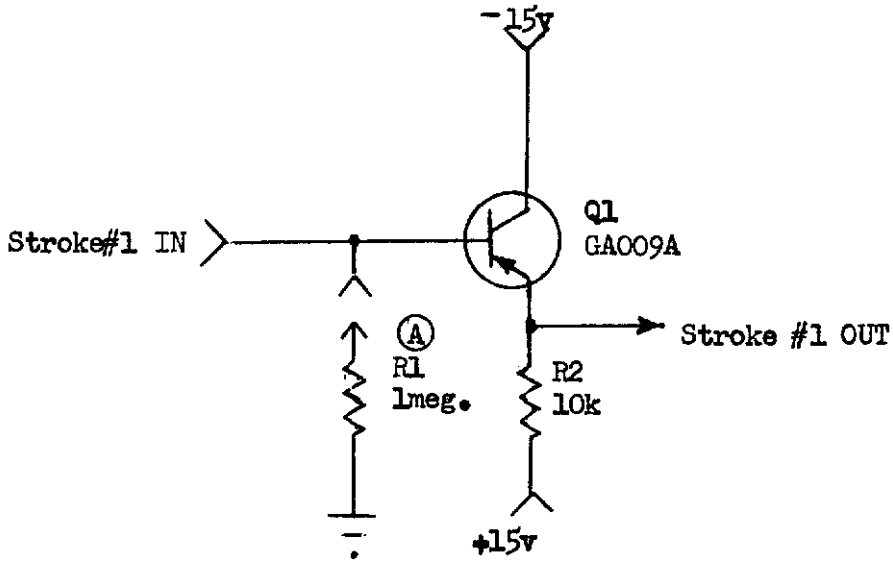


Figure 5. Block Diagram - Character Sequencer



NOTE: This is the circuit of the remaining stages.

Ⓐ This resistor is optional.

Figure 6 . CHARACTER BUFFER

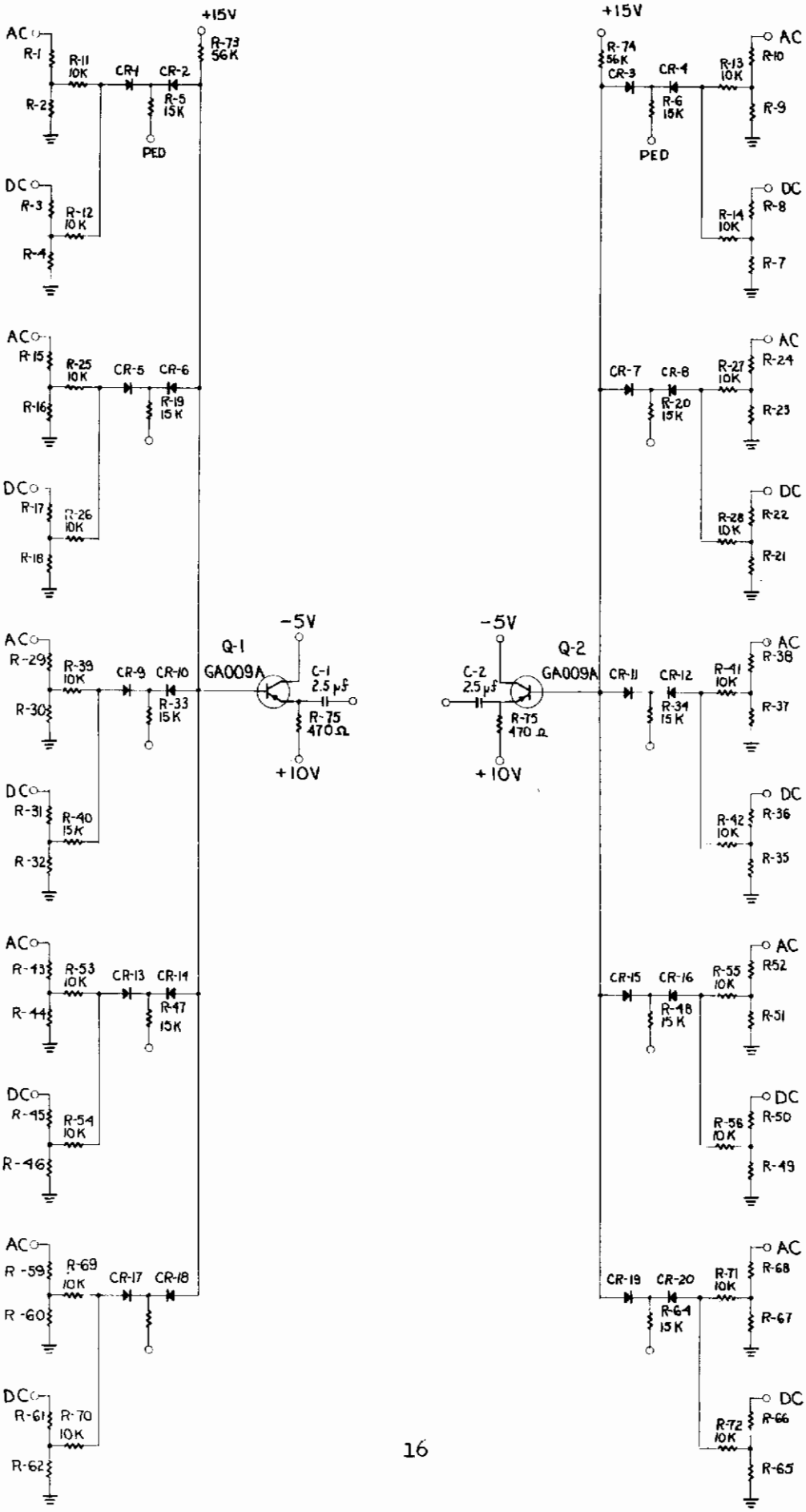


Figure 7. CHARACTER CARD

The inputs labeled AC are capable of accepting any f(t) up to 20 KC and are normally driven from the 0° and 180° outputs of the triangular wave generator located on the Geometrics I card.

The inputs labeled DC are attached to the +15V reference and the resistors R3, R4, R17, R18 and etc., are used to scale the DC voltage corresponding to the sub-coordinate positions of each of the character strokes.

The diode gates are turned on sequentially in Y and X pairs by the positive pedestal stroke from the character buffer.

For the schematic shown, strokes one through five would be required to activate all of the five pairs of gates shown. The Y gates are in shunt and their outputs appear across a common resistor R-73. The X gate outputs likewise appear at the junction of R-74 and CR-3. Both the Y and X outputs are impedance transformed via emitter followers Q-1 and Q-2. Capacitors C-1 and C-2 are present to protect Q-1 and Q-2 against continuous overload caused by accidental shorting at the patch panel and to isolate long-term DC offsets in the output due to IC_o.

The Geometrics I is the card that generates all of the f(t)'s necessary for character stroking and range circle generation.

The master trigger from the composite blanking and trigger card triggers a binary (see figures 8, 9 and 10) which is RC coupled to an operational integrator. The triangular wave output of the integrator is RC coupled to two inverting and isolating amplifiers in cascade yielding the 0° and 180° triangular wave outputs for the character cards.

Each 90° of the trapezoid constitutes a character stroke producing a constant velocity display scanning beam thus yielding uniform trace brightness over the face of each character.

The gating for the rotating pointer function, Geometrics II, is also contained with the Geometrics I card. These gates are used to modulate a DC analog voltage corresponding to the Sine and Cosine of the pointer angle.

Another gate comprised of Q-52 and Q-45 accepts a DC signal from the patch panel corresponding to the diameter of a circle.

The gate modulates the diameter signal (at the character stroking rate) and an operational bandpass filter. Amplifier "D" generates a Sine wave output the amplitude of which is directly proportional to the input diameter.

The output transformer (T-1) forms part of an adjustable phase shift network so that a precise circle diameter may be arrived at by adjustment of P-7. Amplifiers "F" and "E" impedance transform the phase-shifter output and compensate the attenuation through the phase shifting network.

The Geometrics II card (figures 11, 12 and 13) converts the display modulated voltages corresponding to the vector angle of the rotating pointer into resolved f(t)'s corresponding to the X and Y beam deflections necessary to sweep out the pointer.

Two operational bandpass amplifiers convert the modulated trig functions of the angle into sinewaves whose amplitude and phase correspond to the resolved sweep components of the vector. To insure rotation about the same pointer end throughout all four quadrants the two output gates are operated as clamps in synchronism with the input gates. The output becomes a sine wave whose point of inflection is always clamped to zero reference.

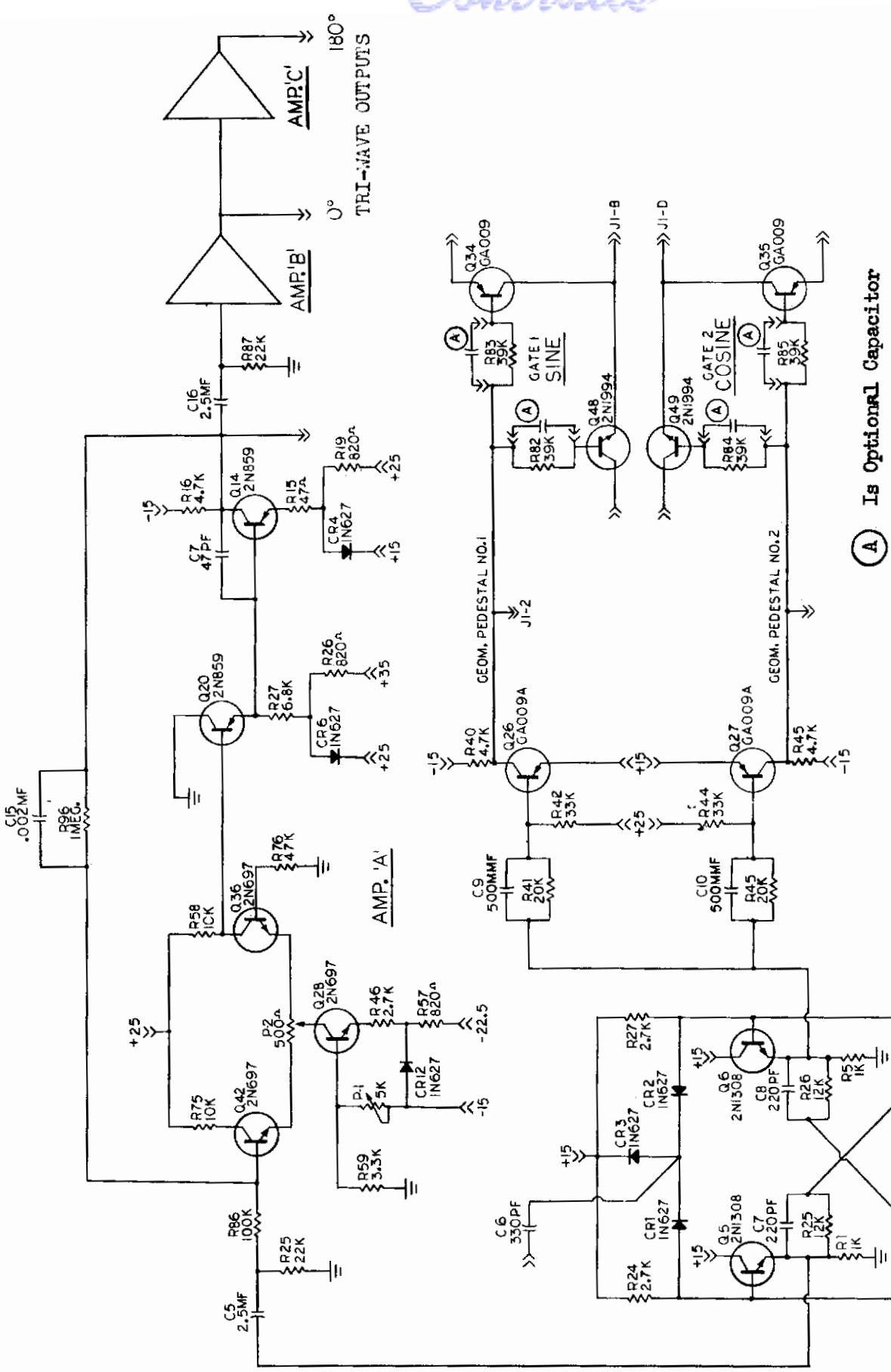
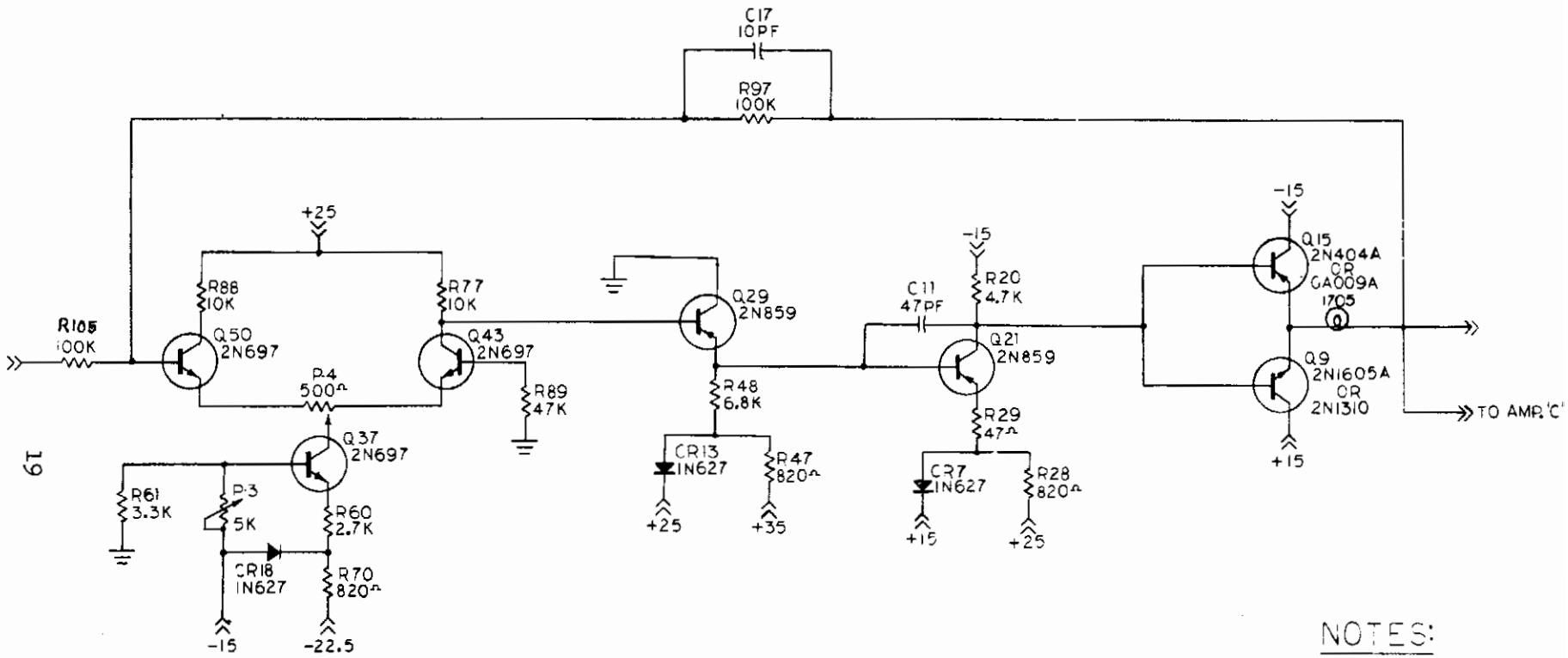


Figure 3. TRI-WAVE GENERATOR- SCHEMATICS



AMPLIFIER 'B'

AMPLIFIERS 'C' 'E' & 'F' ARE IDENTICAL

Figure 9. OPERATIONAL AMPLIFIER - GEOMETRICS I

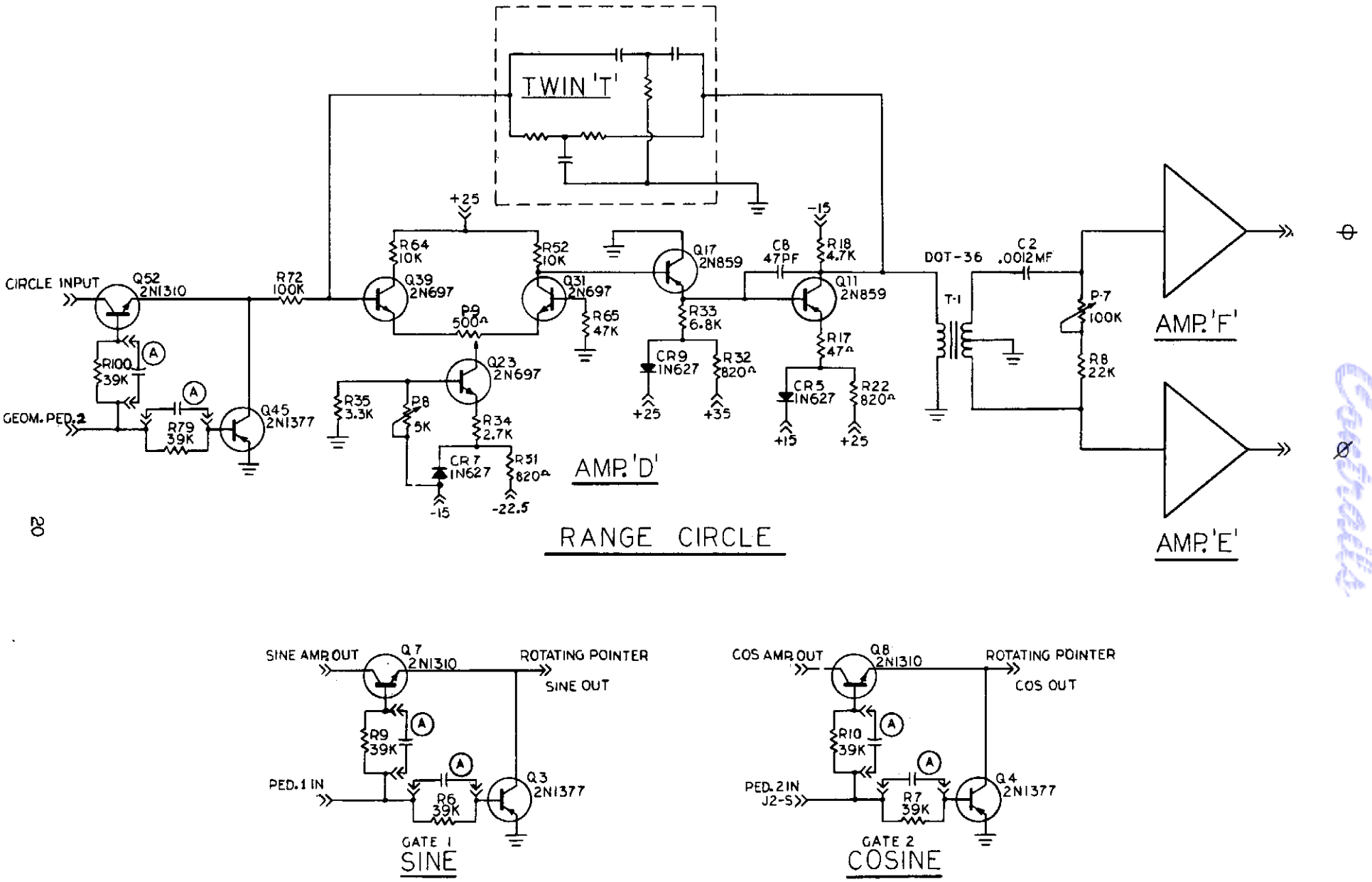


Figure 10. RANGE CIRCLE - GEOMETRICS I

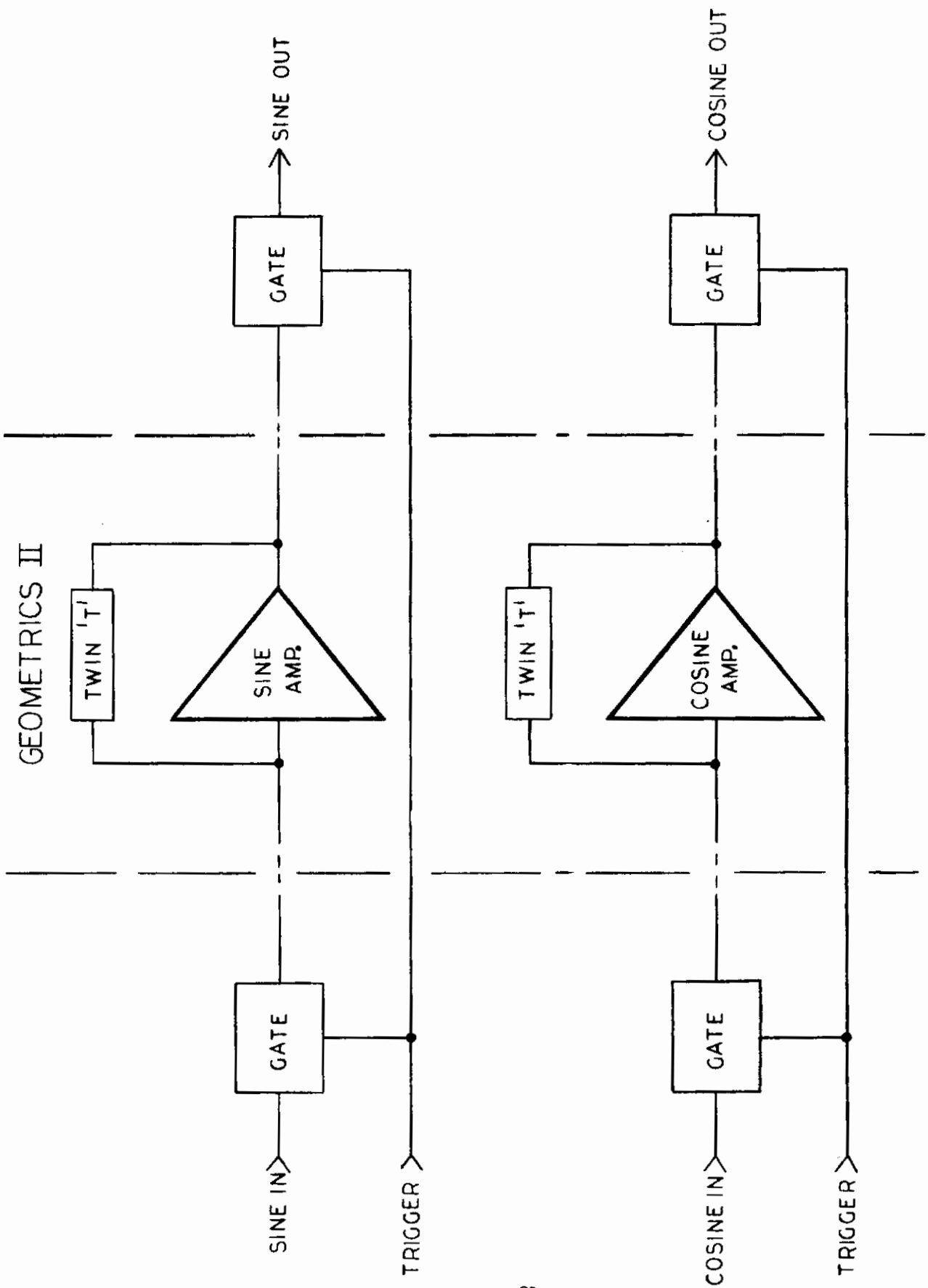


Figure 11. GEOMETRICS II - Rotating Pointer

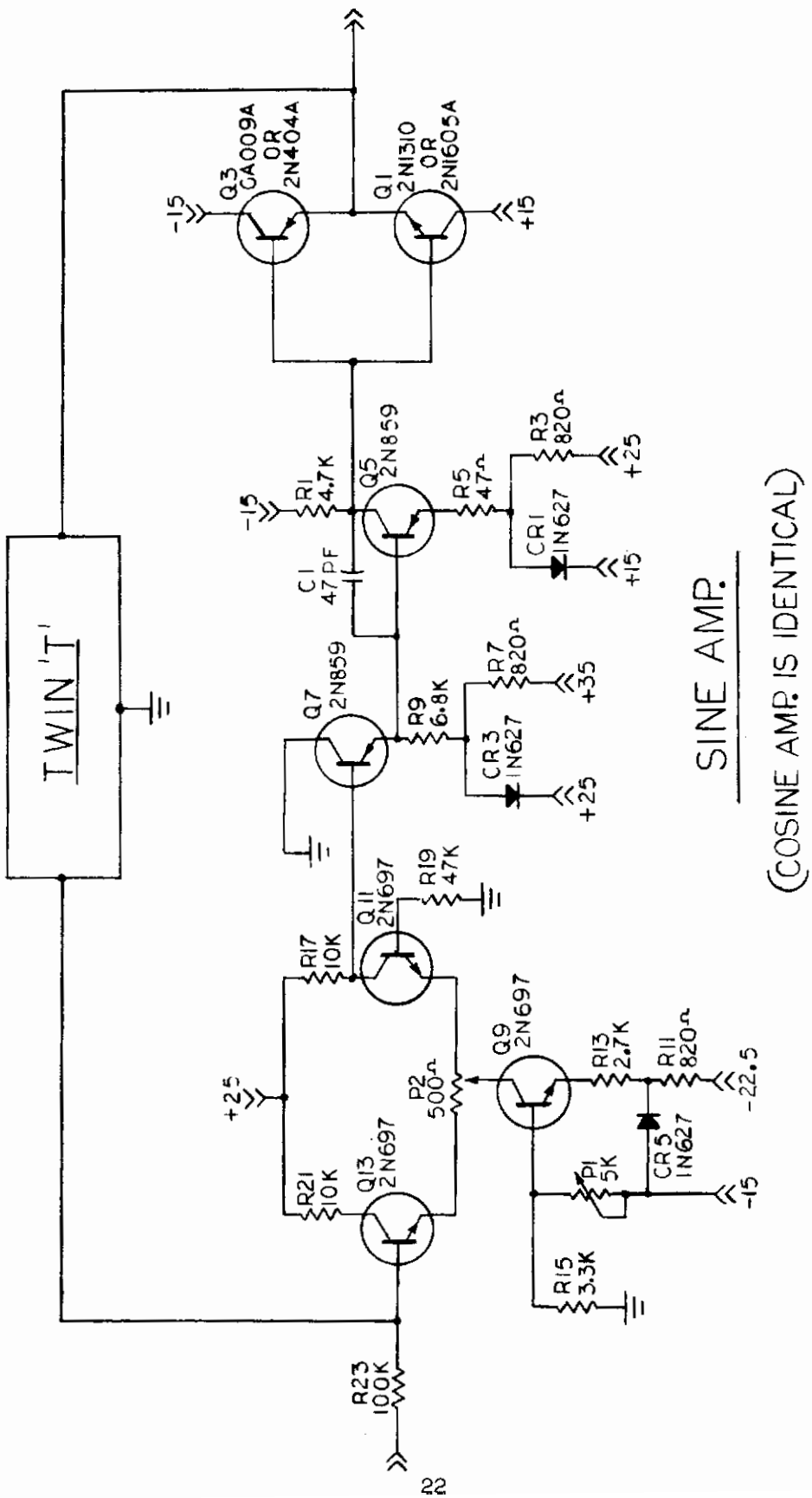


Figure 12. GEOMETRICS II - AMPLIFIER

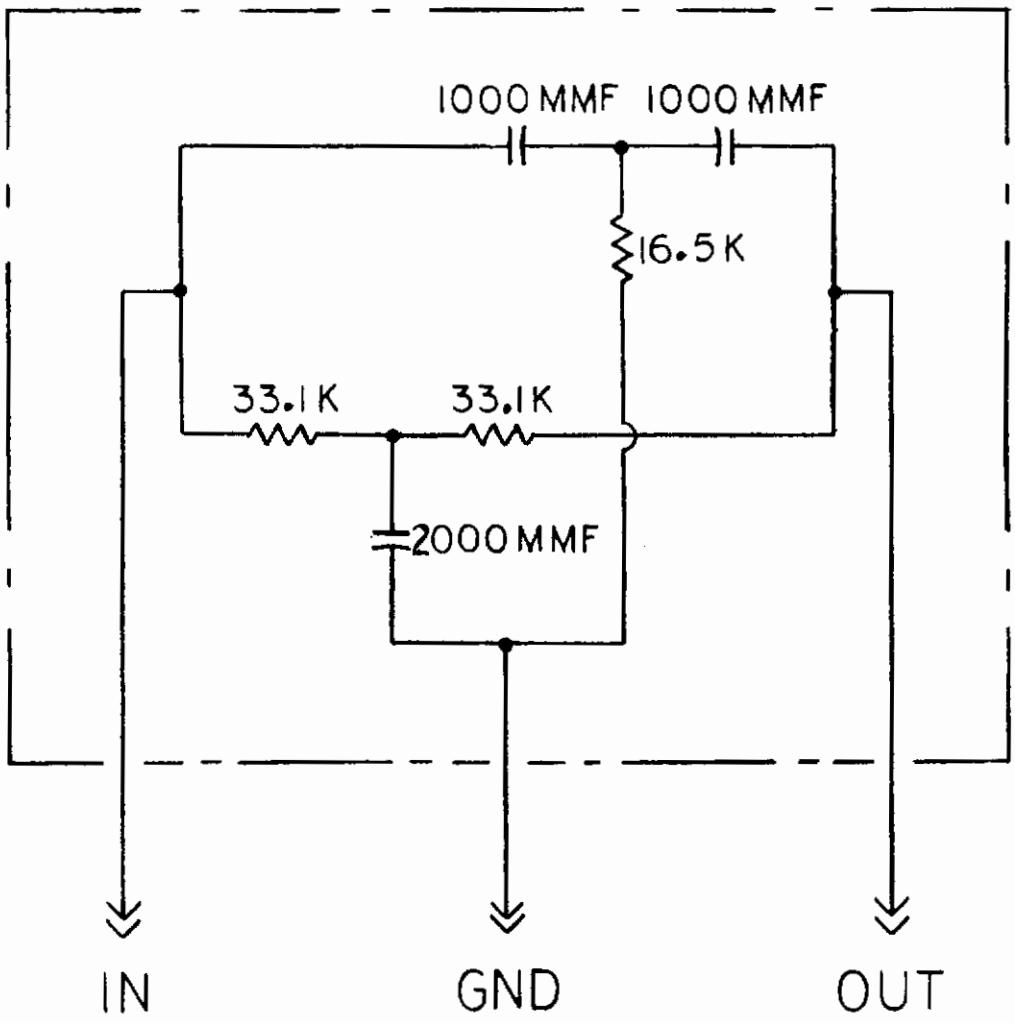


Figure 13. TWIN 'T'

D. VIDEO AMPLIFIER

The video amplifier permits laboratory scopes which have various or too short Z-axis RC time constants to be used as CRT ISS display scopes without recourse to modifying. Ten megacycles were chosen as the carrier frequency in order to preserve blanking pedestal rise and fall time.

The unit consists of three major sections (see figure 14):

1) Pulse amplifier V1 and V2.
2) Carrier generator V3 and V4.
3) Modulated amplifier V5.

V3 is a crystal controlled oscillator (9.72 megacycles) which is coupled to buffer amplifier V4. The RF signal from V4 is RC coupled to amplifier V5. In addition, the amplifier composite blanking signal from V2 is applied via R5 and C1 to the screen grid of V5. The resultant output at the plate of V5 is a 10 megacycles carrier modulated by the CRT ISS composite blanking signal. Panel adjustments L5 and C31 form a parallel resonant tank circuit with the output cable and load which is tuned to produce a current node at the display scope Z axis terminals.

The modulation depth is controlled by varying the gain control P1 which directly affects the peak to peak value of the carrier signal.

The output level may be reduced by detuning C31 and L5 to prevent overdriving scopes having small amplitude blanking requirements.

E. DISPLAY SCOPE

At the time of this requirement none of the electromagnetically deflected large screen scopes or amplifiers available could meet the requirement to deflect the electron beam from one side of the cathode ray tube to the other (21 inches, 70°) in 10 microseconds. Therefore, a state electromagnetic deflection amplifier was developed consisting of two identical deflection amplifiers for the X and Y axis which are required to display the sequenced deflection waveforms generated by the CRT ISS Main Console. The large screen display scope is presented as a means of satisfying the requirement for high-brightness and rapid refresh rates in the simulation of energy management, navigation or other displays where either large amounts of data or large map overlays must be presented to individual operators.

The first trials to design a direct coupled deflection amplifier were unsuccessful because of the voltage and power levels involved. After certain difficulties experienced with a direct coupled amplifier approach, it was decided to design an AC amplifier. The subsequent use of AC coupling between the driver stage and the single ended series-arranged transistor output stage minimized the coupling problems and improved the amplifier reliability.

The block diagram for the resulting deflection scheme using AC amplifiers is given in Figure 15. The AC coupled deflection amplifier for each axis consists of two main amplifiers each driving one coil of the deflection yoke. The block diagram for a main amplifier is given in Figure 16.

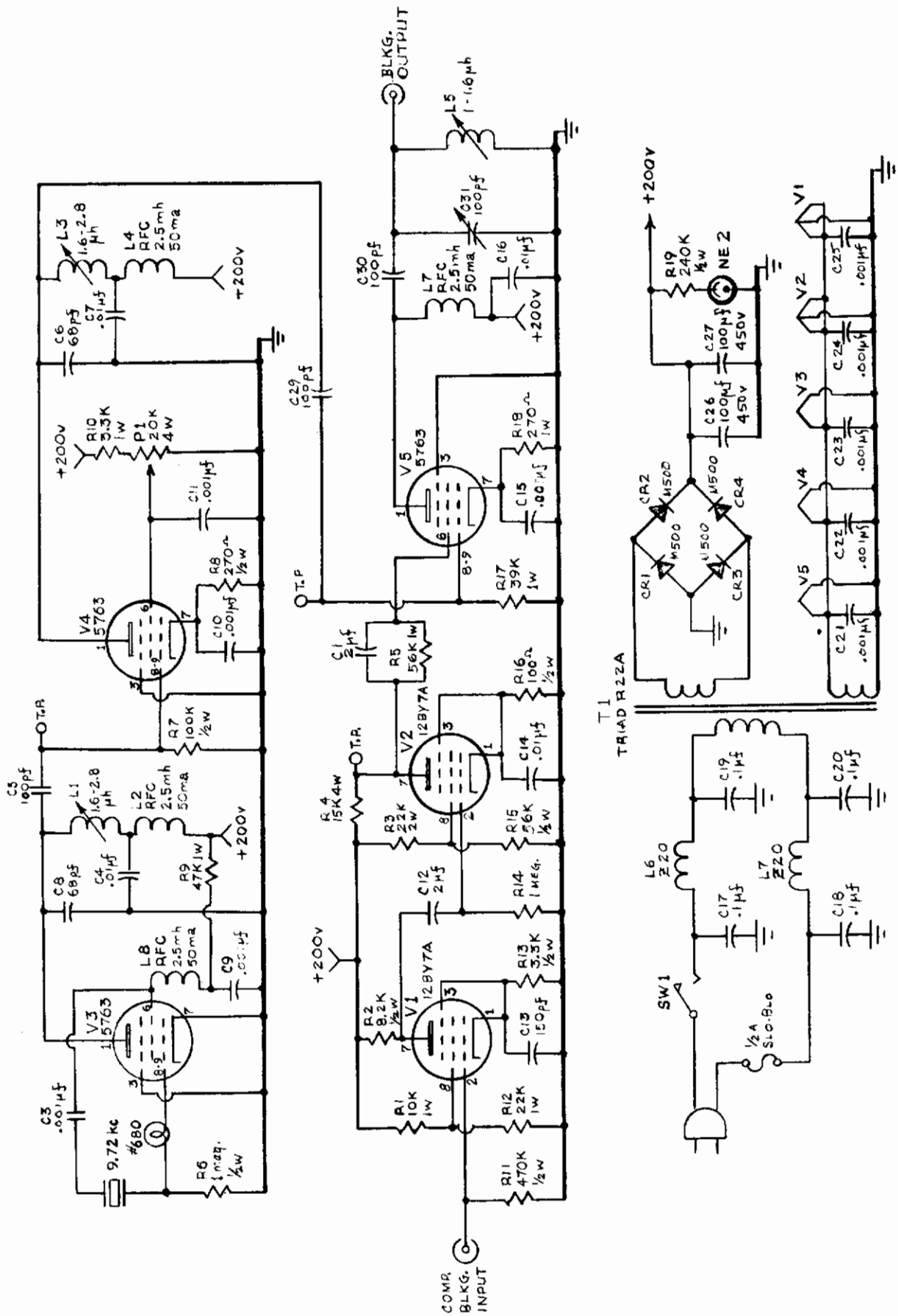


Figure 14. VIDEO AMPLIFIER

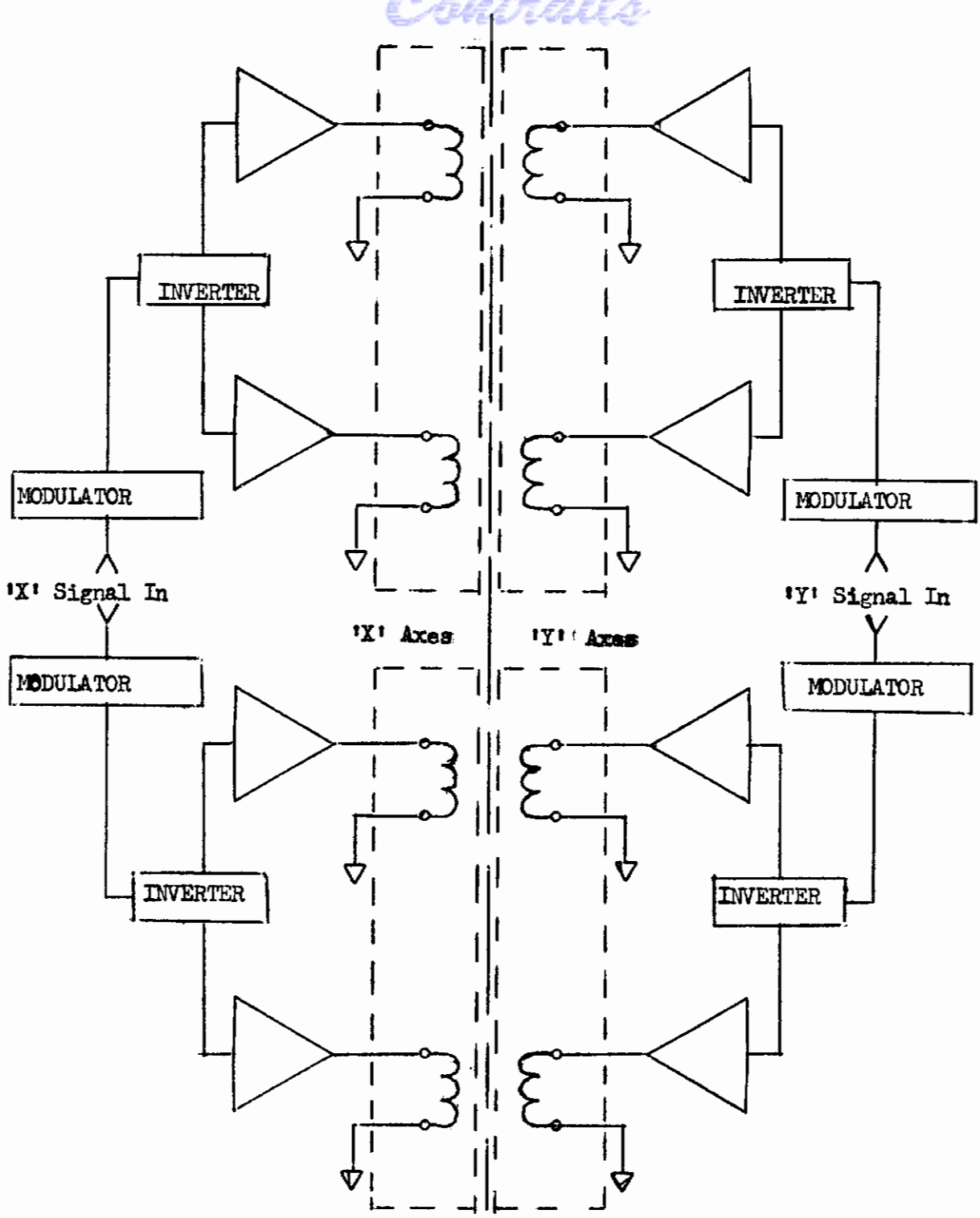


Figure 15. BLOCK DIAGRAM - DEFLECTION AMPLIFIERS

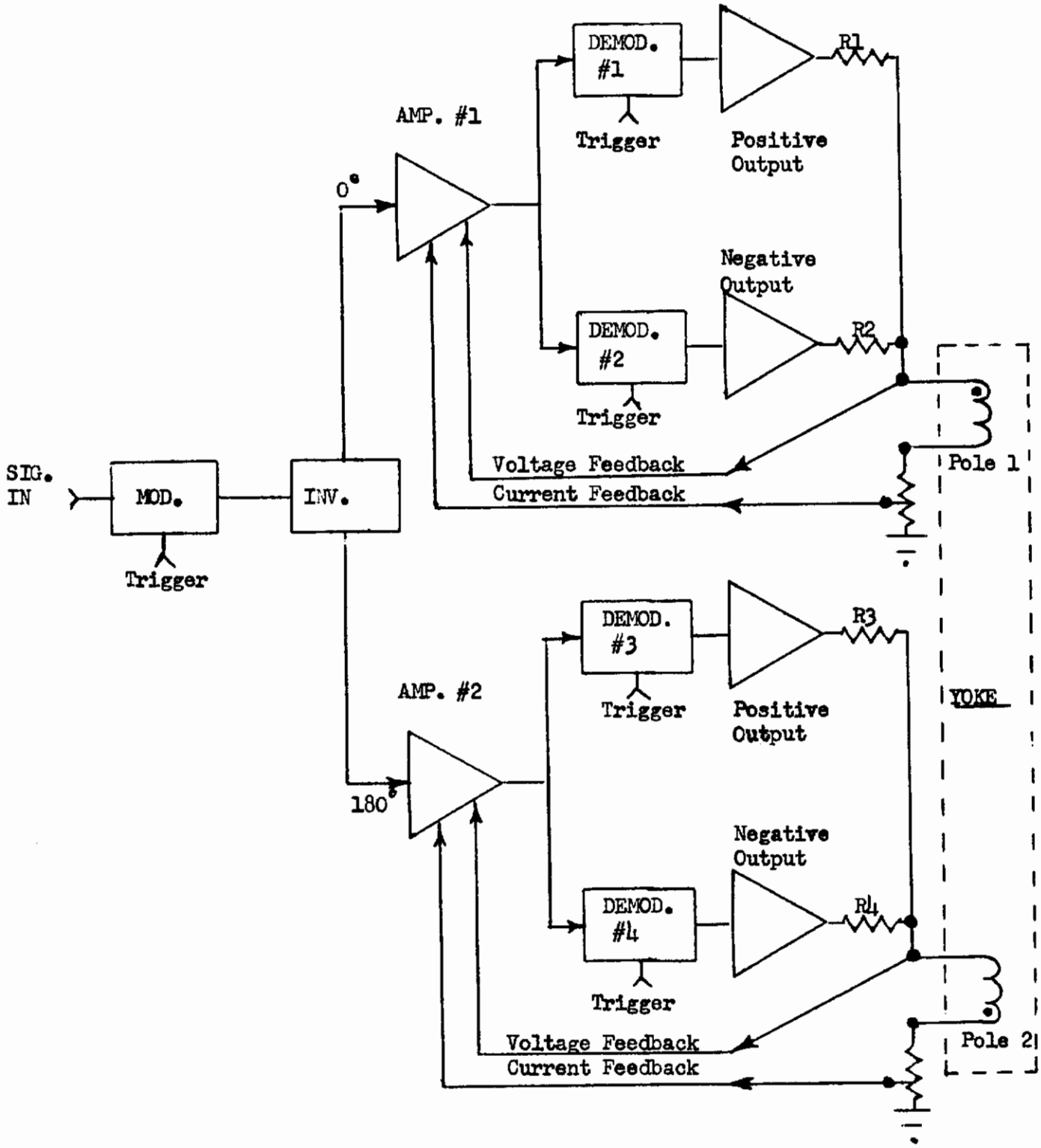


Figure 16. DEFLECTION AMPLIFIER FOR SINGLE COIL

During the time one amplifier is on the other amplifier is off. The on and off time of each amplifier is 520 microseconds. The 520 microseconds period is the display time of one channel of the alphanumeric information. Each main amplifier consists of two preamplifiers driving the two poles of each half-axis 180° out of phase. The poles are driven separately and out of phase, to minimize the voltage impulse needed to obtain the desired current switching time in the coil and also to reduce power supply current requirements.

The demodulation technique uses a synchronous clamp. The signal is clamped during the time the amplifier is off (input grounded). To obtain the desired maximum 10 microseconds rise and fall time, the amplifier should have a minimum upper 3 db frequency of:

$$f_2 = \frac{.35}{10 \times 10^{-6}} = 35 \text{ kc}$$

For the output stage of the deflection amplifier a Class B single-ended series-arranged transistor configuration was chosen (figure 17). The three transistors in each half of the output stage are in series to permit high power, large signal operation. Transistors Q1, Q2 and Q5, Q6 are connected in the common base configuration and are driven in series by the common emitter transistors. The common base transistors give the desired high output impedance for the amplifier to operate as a constant current generator. The reliability of the output stage is increased by the connection of two 20 ohm resistors in series with each half of the output stage thus limiting overload currents to values within the device ratings.

The driver stage is connected to the demodulators through a wide band transformer. A "pentafilar" winding technique was used to obtain the desired wide band frequency characteristics. A variable voltage and current feedback from the output stage to the driver stage permits adjustment of the amplifier transient response for optimum conditions.

Modulators at the amplifier inputs modulate signals up to $\pm$10 volts in amplitude. Next the inverter stage provides an output of phase signal for driving the preamplifiers. The input impedance seen by the signal is approximately 5000 ohms.

During the final stages of checkout of the A-C coupled deflection amplifier, a transient cross-talk problem was experienced. One of the causes of this difficulty was the complexity of the circuits used. At this time the possibility of using the existing circuits as a building block for a direct coupled push-pull amplifier was considered. The circuits were tested and satisfactory results were obtained.

Two deflection amplifiers are used for each of the X and Y axes (figures 18 and 19). Each deflection amplifier consists of two preamplifiers (figure 20), two driver stages and an output stage. The 180° out of phase input signals to the preamplifiers are supplied by the CRT ISS. There are two potentiometer controls in each preamplifier. The 500 ohm potentiometer adjusts the input stage balance. The 5K ohm potentiometer is used to adjust the forward bias of the output stage (figure 21). The two preamplifiers

apply signals to the driver stages which drive the output stage. The driver stage is an emitter follower (figure 22). There is no overall feedback in this deflection amplifier; therefore, the gain stability and linearity depend on local feedback.

The deflection yoke is made up of four coils. Each coil has two poles; the approximate inductance of a pole is 125 microhenries. A pole of the coil is driven by one side of the output stage (figure 21). Both poles of a coil are connected to the amplifiers so that they are energized at the same time. The polarity of the input signal determines which coil is energized, and the direction of electron beam deflection. The amplifier bandwidth is sufficient to permit deflection of the electron beam over the total width of the 21" cathode ray tube in 10 microseconds.

A blanking amplifier blanks the CRT during the retrace time (figure 23). The CRT biasing voltages are shown in figure 24.

The 21" oscilloscope illustrated in figure 25 reflects the circuit redesign.

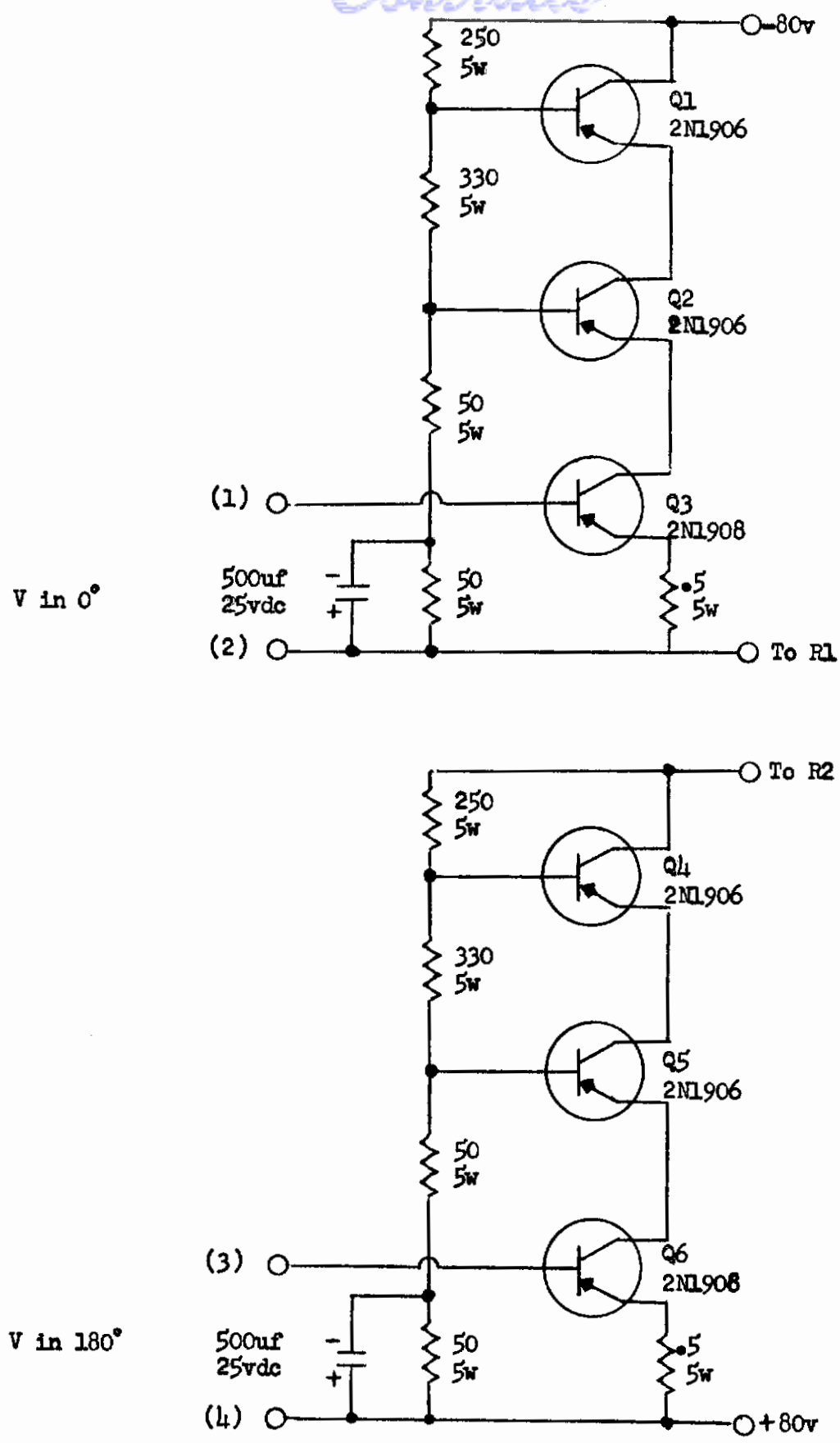
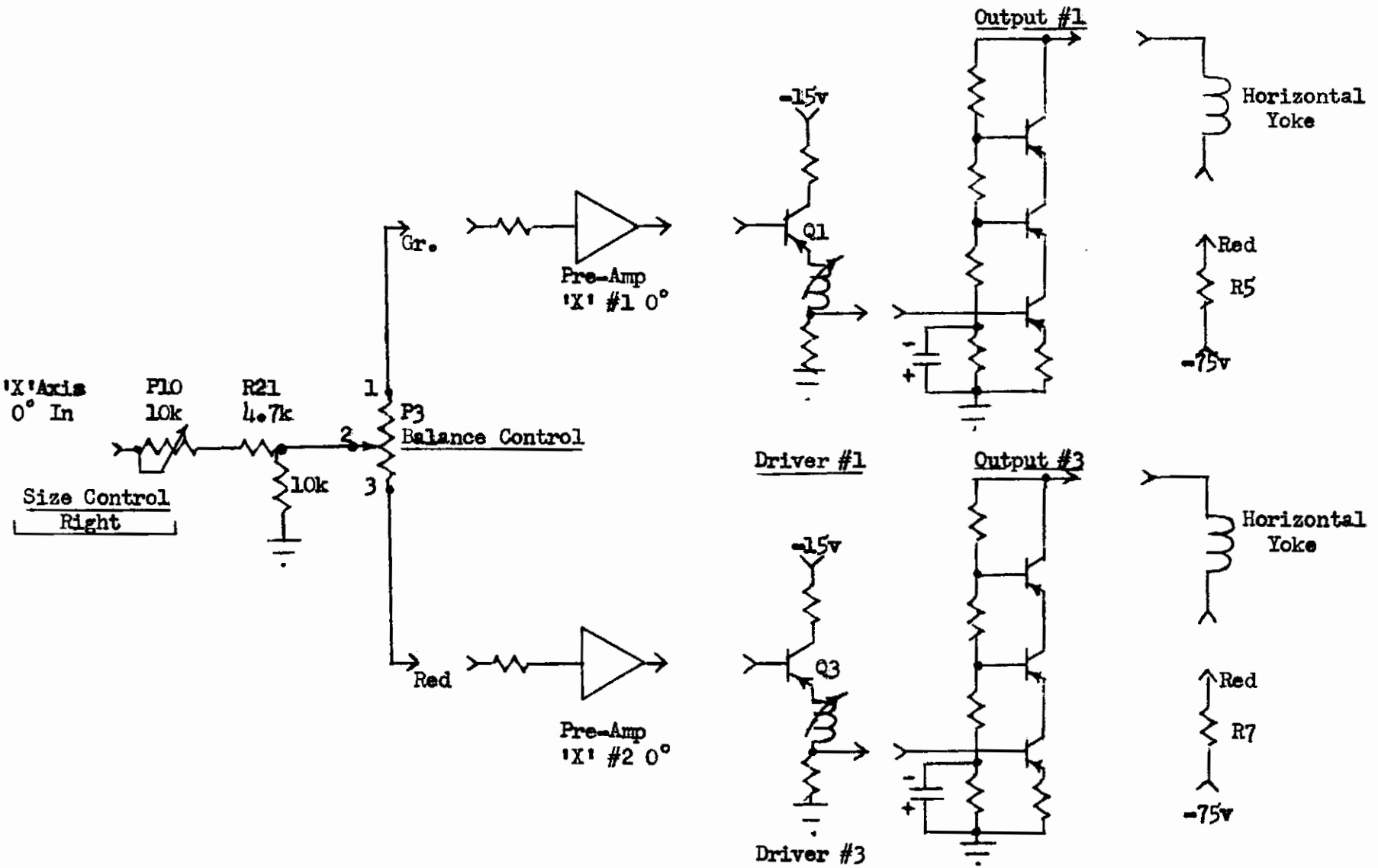


Figure 17. OUTPUT STAGE



DEFLECTION SIGNAL - 'X' 0°

Figure 18. DEFLECTION SIGNAL "X"

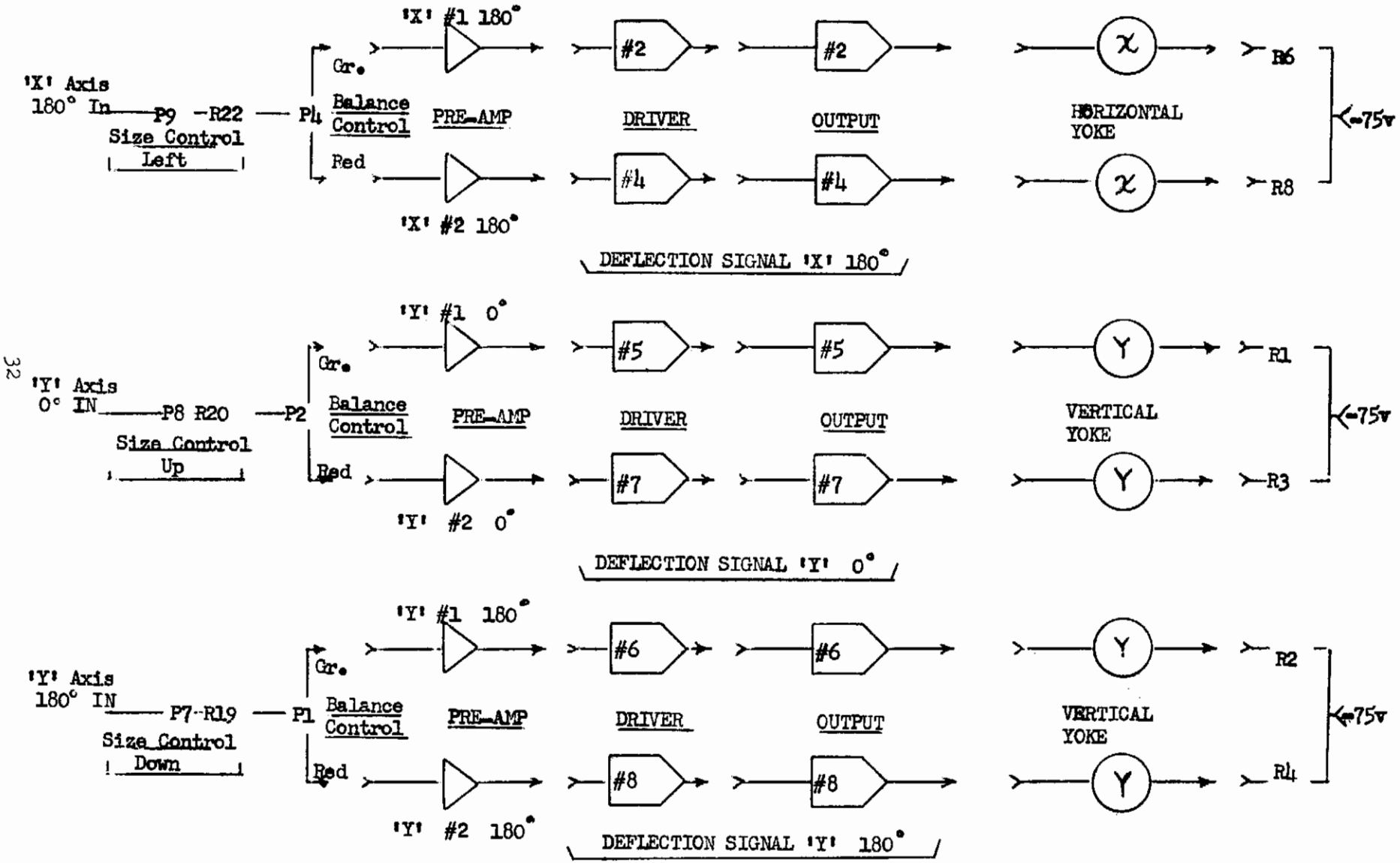
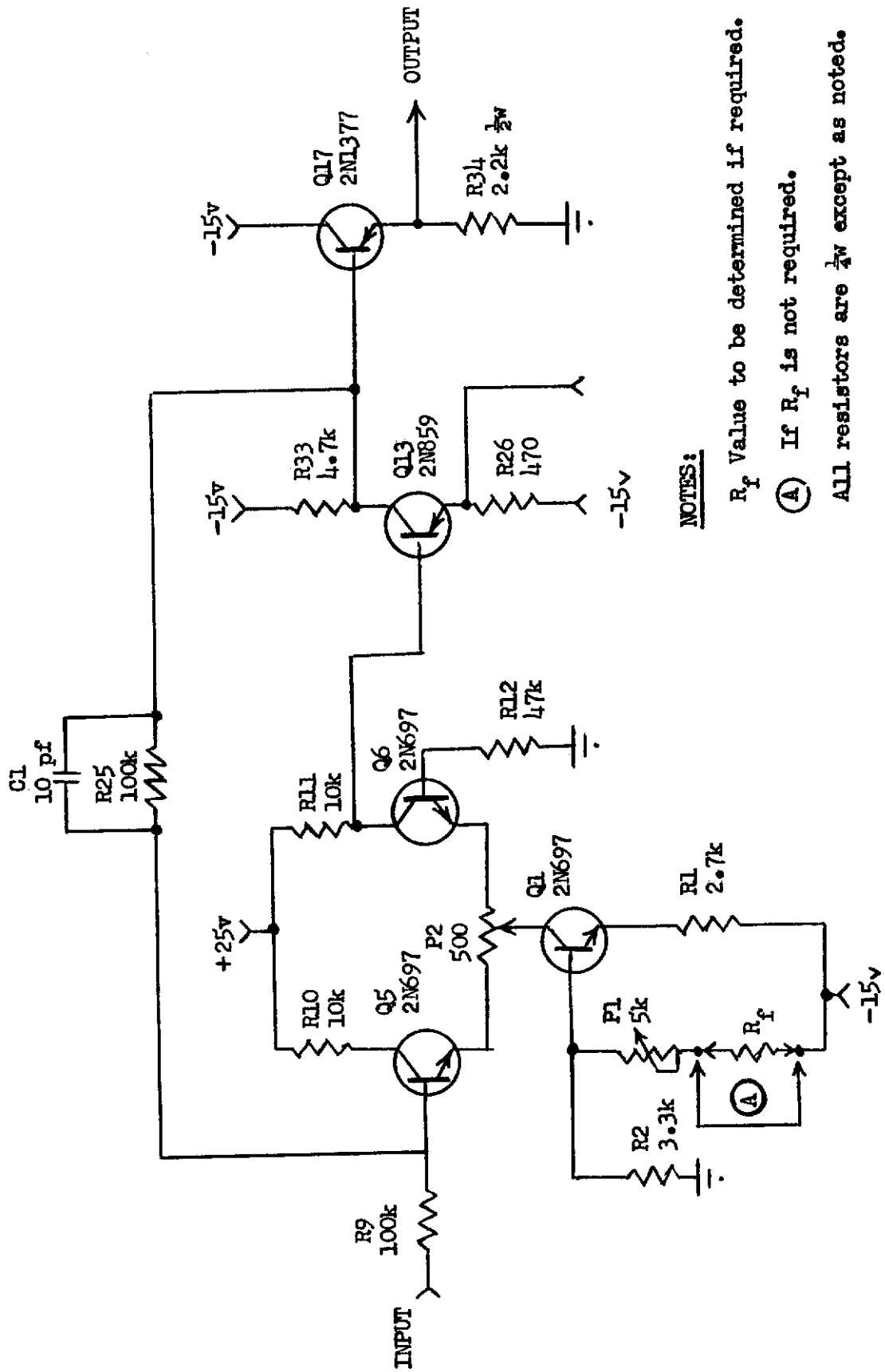


Figure 19. DEFLECTION SIGNAL "X" AND "Y"



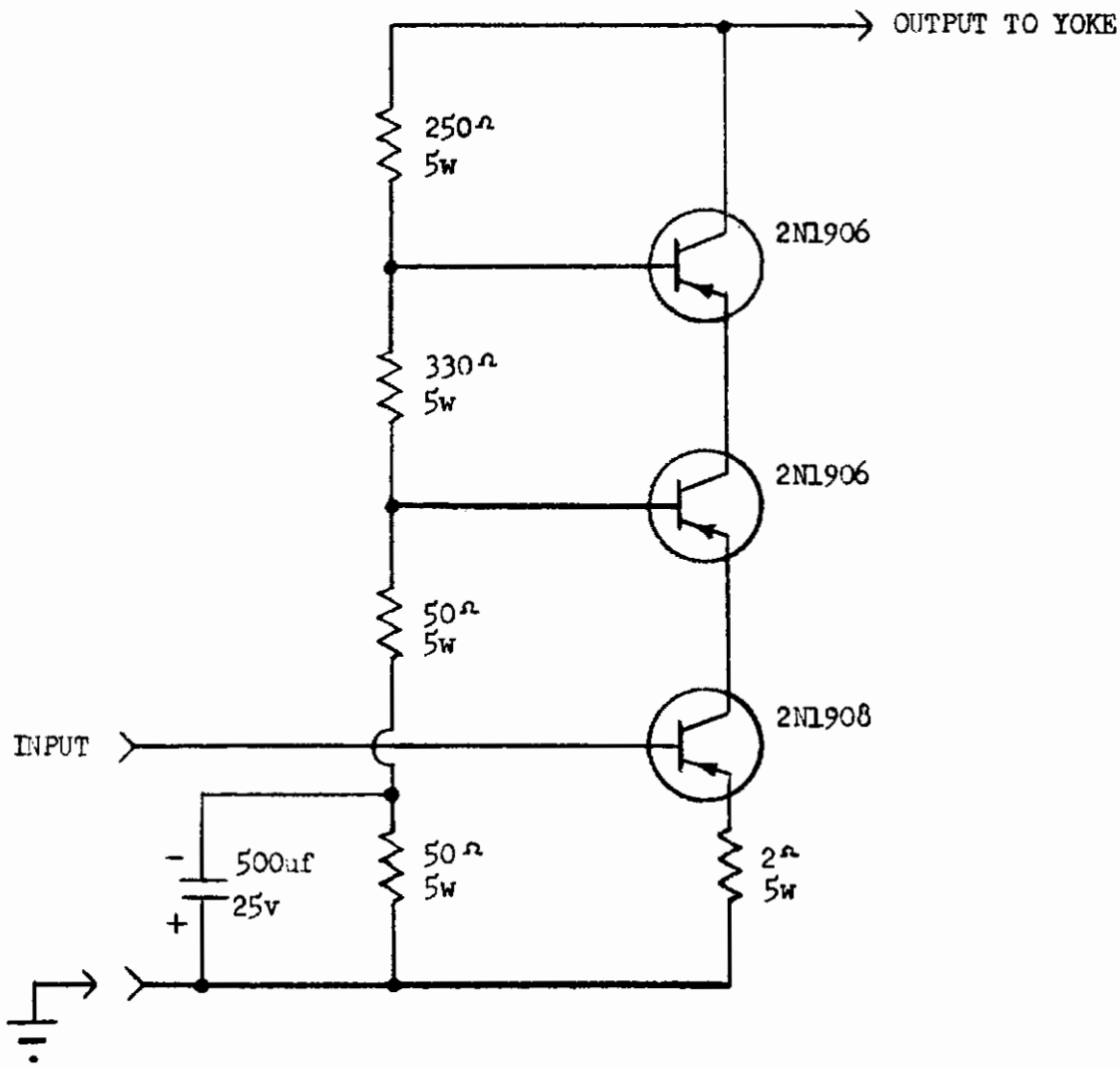
NOTES:

R_f Value to be determined if required.

(A) If R_f is not required.

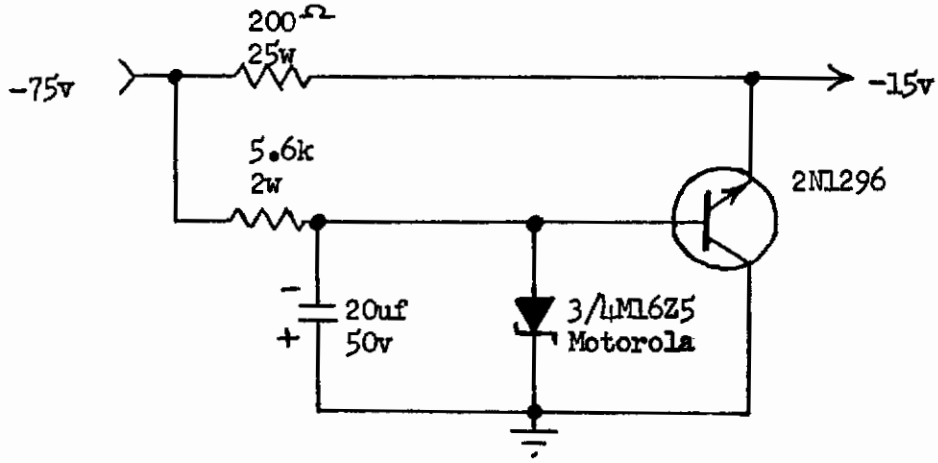
All resistors are ¼w except as noted.

Figure 20. DISPLAY SCOPE PRE-AMPLIFIER



Note: This is typical of the 8 stages found in the Display System.

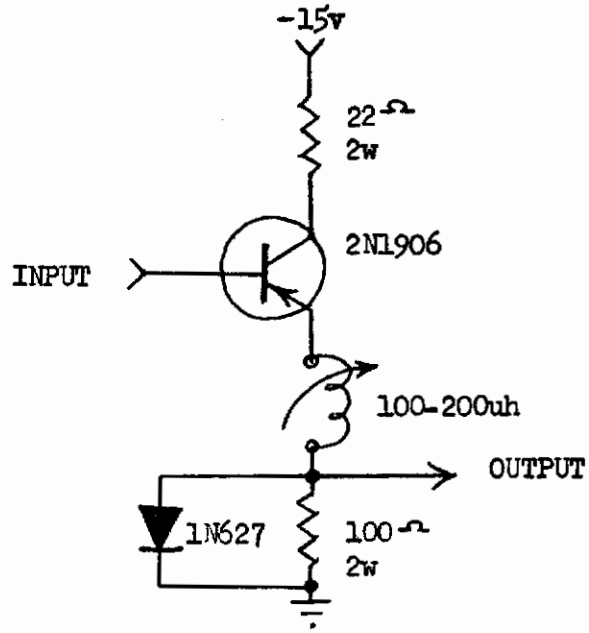
Figure 21. OUTPUT STAGE



Note: The -75v is taken from the Lambda Regulated Power Supply.

The 3/4M16Z5 Zener Diode Reference Voltage is as follows:
Eb_1 min. 15.2v
Eb_2 max. 16.8v

NEGATIVE 15 VOLTS SUPPLY FOR DRIVER STAGE



Note: This is typical of the 8 stages found in the Display System.

Figure 22. DRIVER STAGE

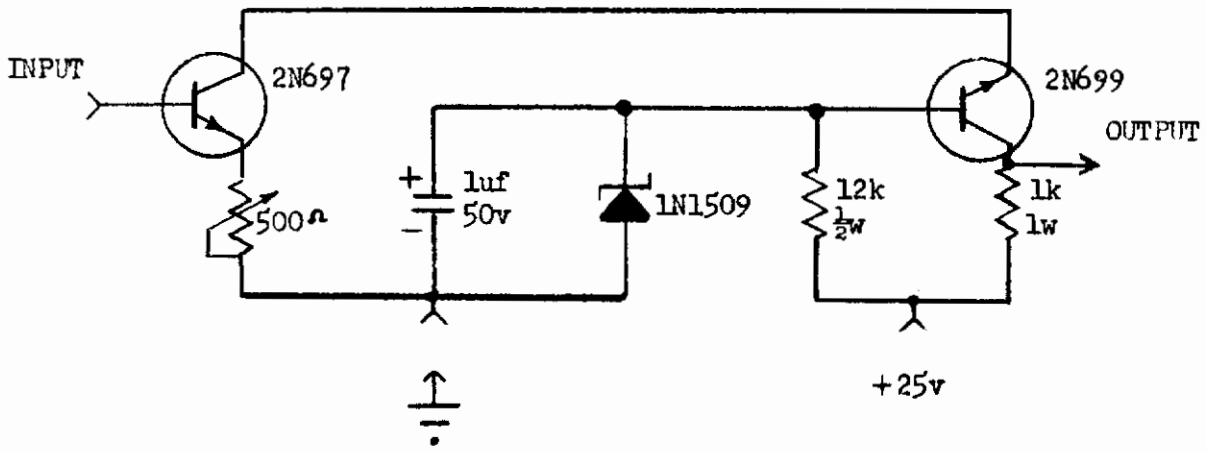
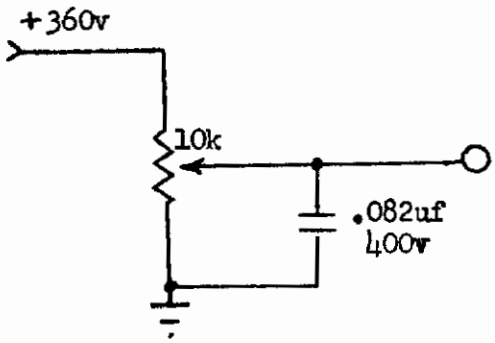
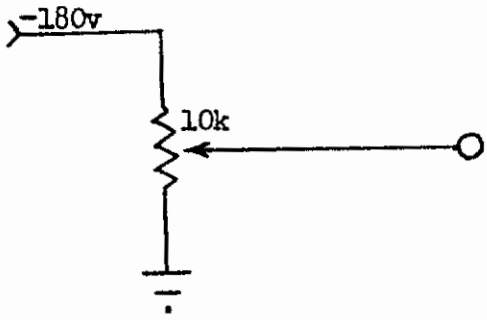


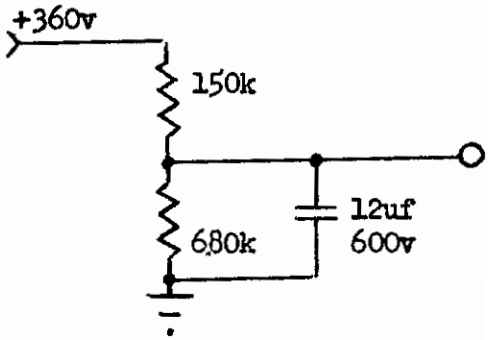
Figure 23. BLANKING AMPLIFIER FOR SCOPE DISPLAY



FOCUS



BRIGHTNESS



SCREEN GRID

Figure 24. CONTROL VOLTAGES FOR SCOPE DISPLAY

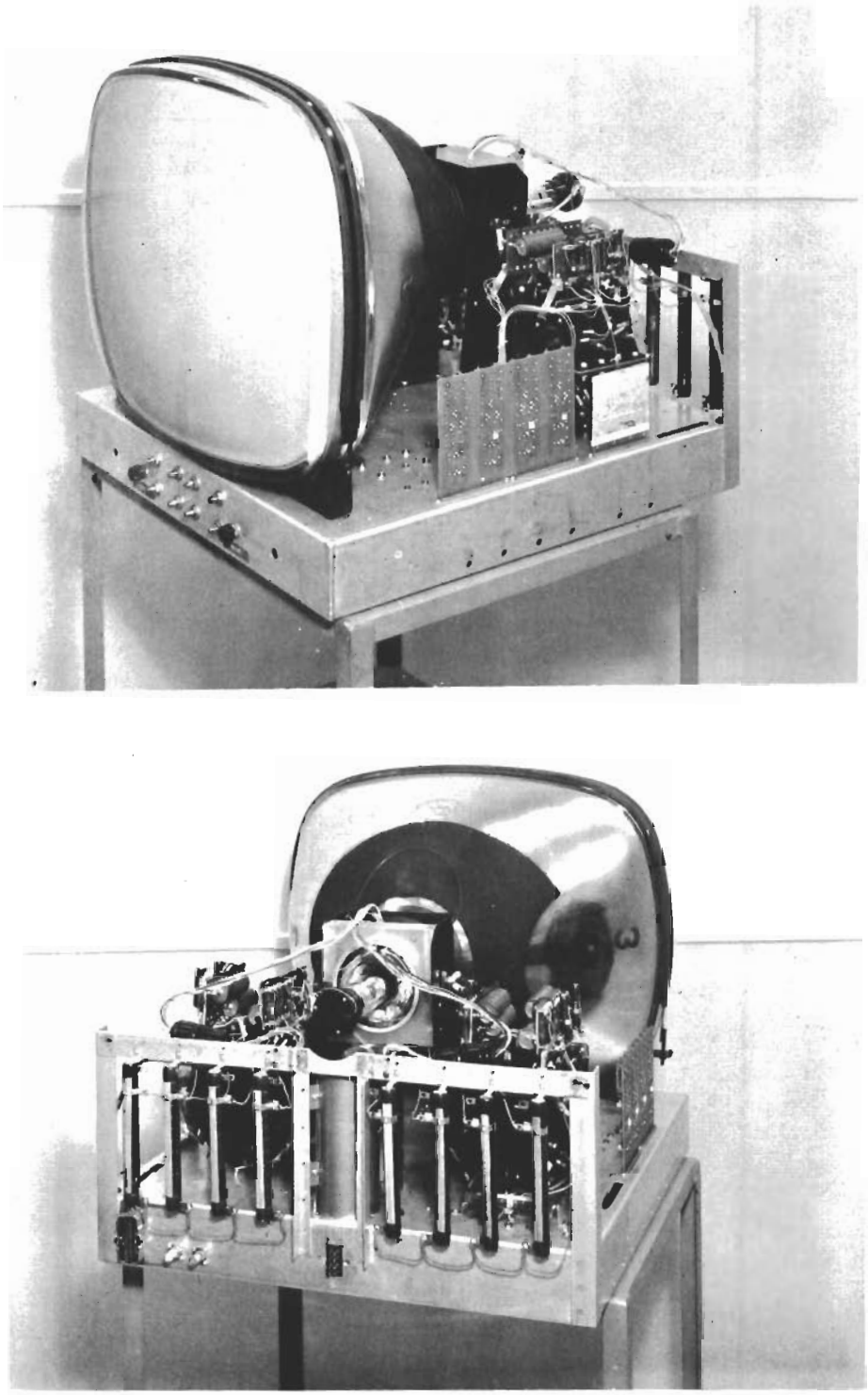


Figure 25. 21" DISPLAY SCOPE

SECTION V

DISCUSSION AND CONCLUSIONS

Figures 26 through 29 illustrate the complete system in operation.

The system has been proven to be extremely flexible. Typically, it may be programmed within one half-hour when changing configurations. The CRT ISS has been used to present a wide variety of display formats. Specific comments arising from checkout and usage of the system follow:

1. An adjunct to programming which has proven useful is the availability of buffer pedestals at the front panel. During checkout of the system it was possible to determine the condition of the operation by examining these pedestals. These pedestals have been used to supply accessory equipment via the console trunk lines.

2. Sequenced deflection output rise times were between one and five microseconds on either X or Y output lines.

3. The intensity modulation feature has permitted the intensity of all the display elements to be matched to each other.

4. Checkout and programming of the unit has been aided by employing the IM and blanking circuitry to indicate the presence of a channel whose location was unknown.

5. The line lock circuitry has kept the displayed images from shimmering due to stray 60 and 120 cps ripple fields in the presence of the display CRT.

6. The legibility of the five-stroke character has been satisfactory in practice especially for characters under 1/2 inch in the vertical dimension.

7. The flexibility of the character generation scheme has remained high in that it has been possible to remove, insert, or trade characters independently without regard to plug locations or any effects upon the rest of the system.

8. The output amplitude has proven sufficient for all of the various laboratory scopes that have been used to date.

9. With the high frequency carrier employed (10 megacycles), the output load consisting of a cable and scope Z input axis became a transmission line problem and it was necessary to provide an adjustable LC tuning arrangement so that the proper VSWR might be arrived at in reconnecting from one scope to another.

10. The constant current generator approach to the output stage has eliminated many of the operating hazards inherent in high power direct-coupled amplifiers.

11. No problem has arisen due to thermal environment and the differential drive of each pole has divided the total power in the yoke load among many amplifiers.

12. With regard to the 21-inch CRT, it has been found that a 15 kv accelerating potential yields the best compromise between display brightness and spot shape.

13. Polaroid filter glass has been helpful in reducing the effects of ambient lighting and 35 ft.-Lamberts trace brightness has been readily achieved with no appreciable increase in spot size.

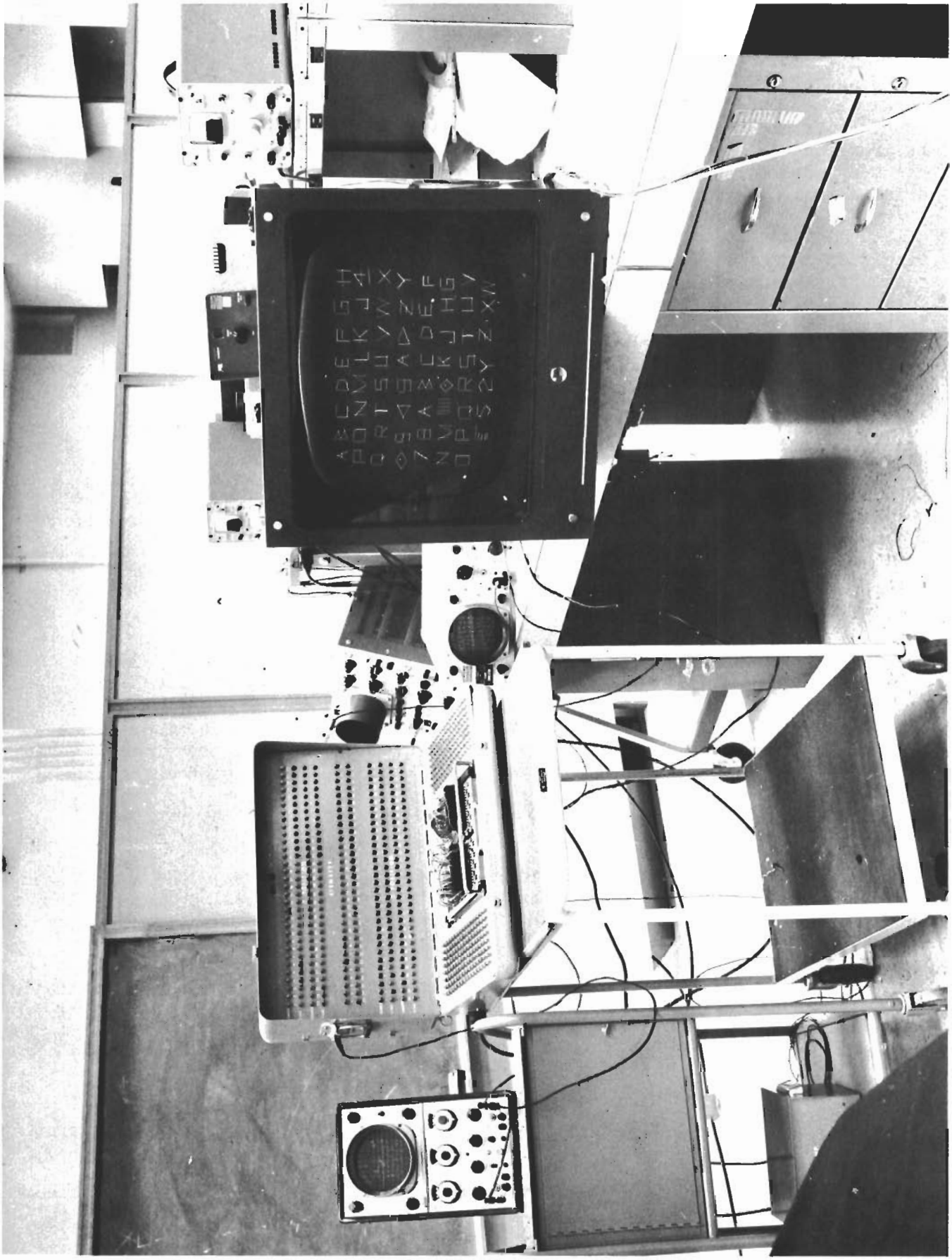


Figure 26. CRT - ISS OPERATION

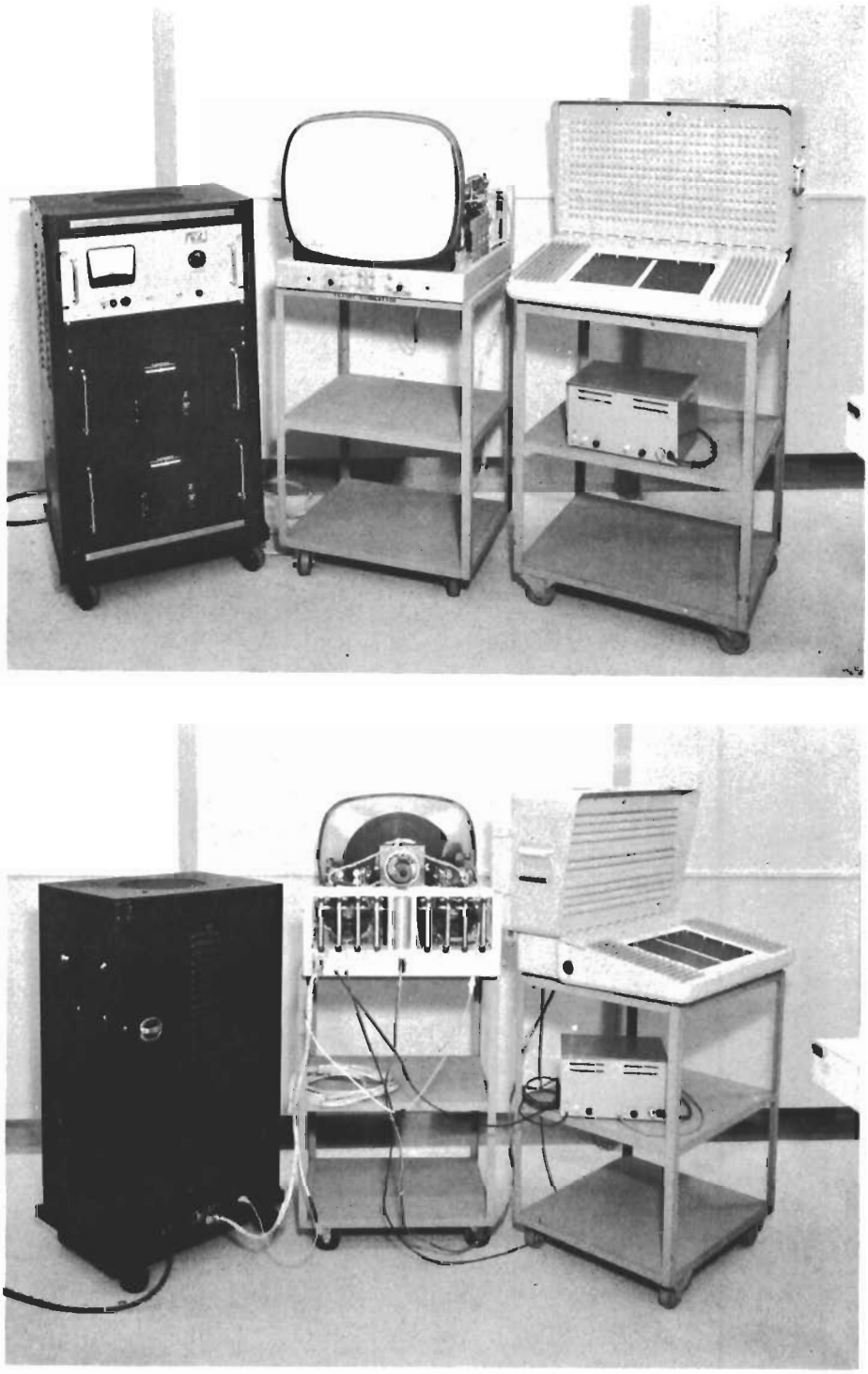
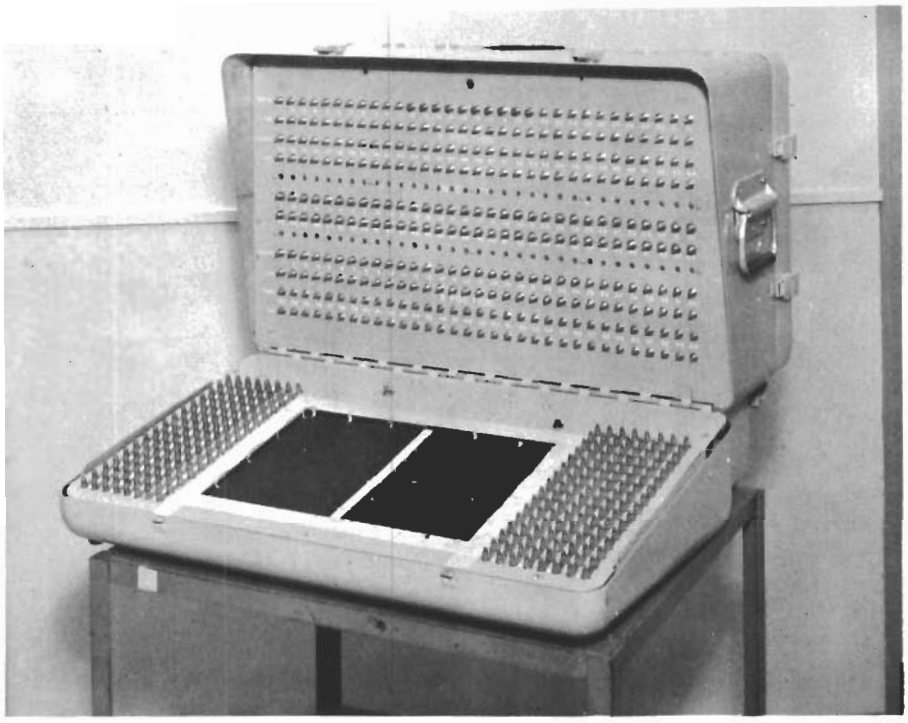


Figure 27. CRT - ISS COMPONENTS



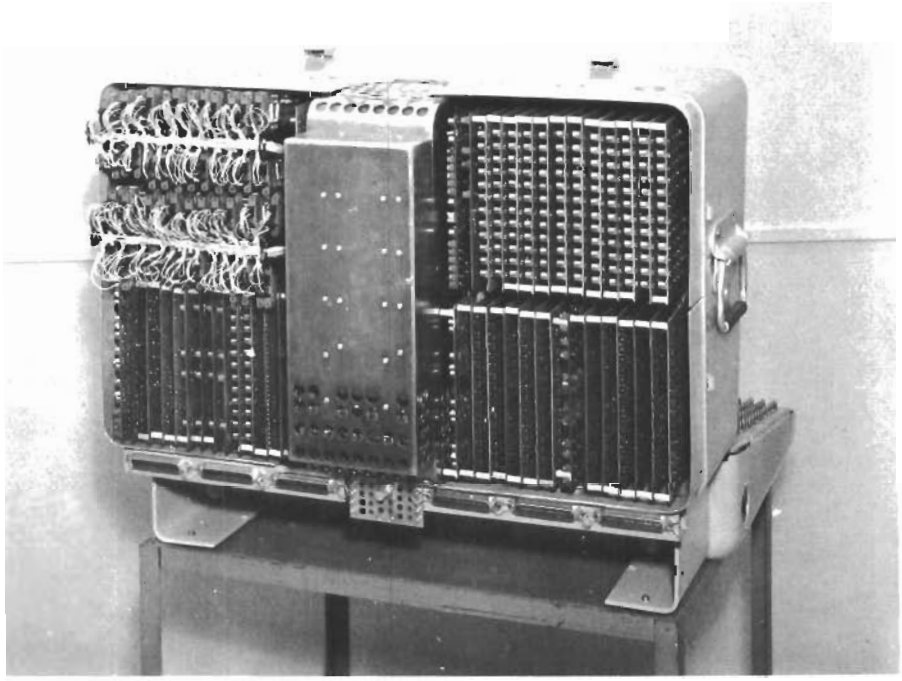


Figure 28. CRT - ISS CONSOLE

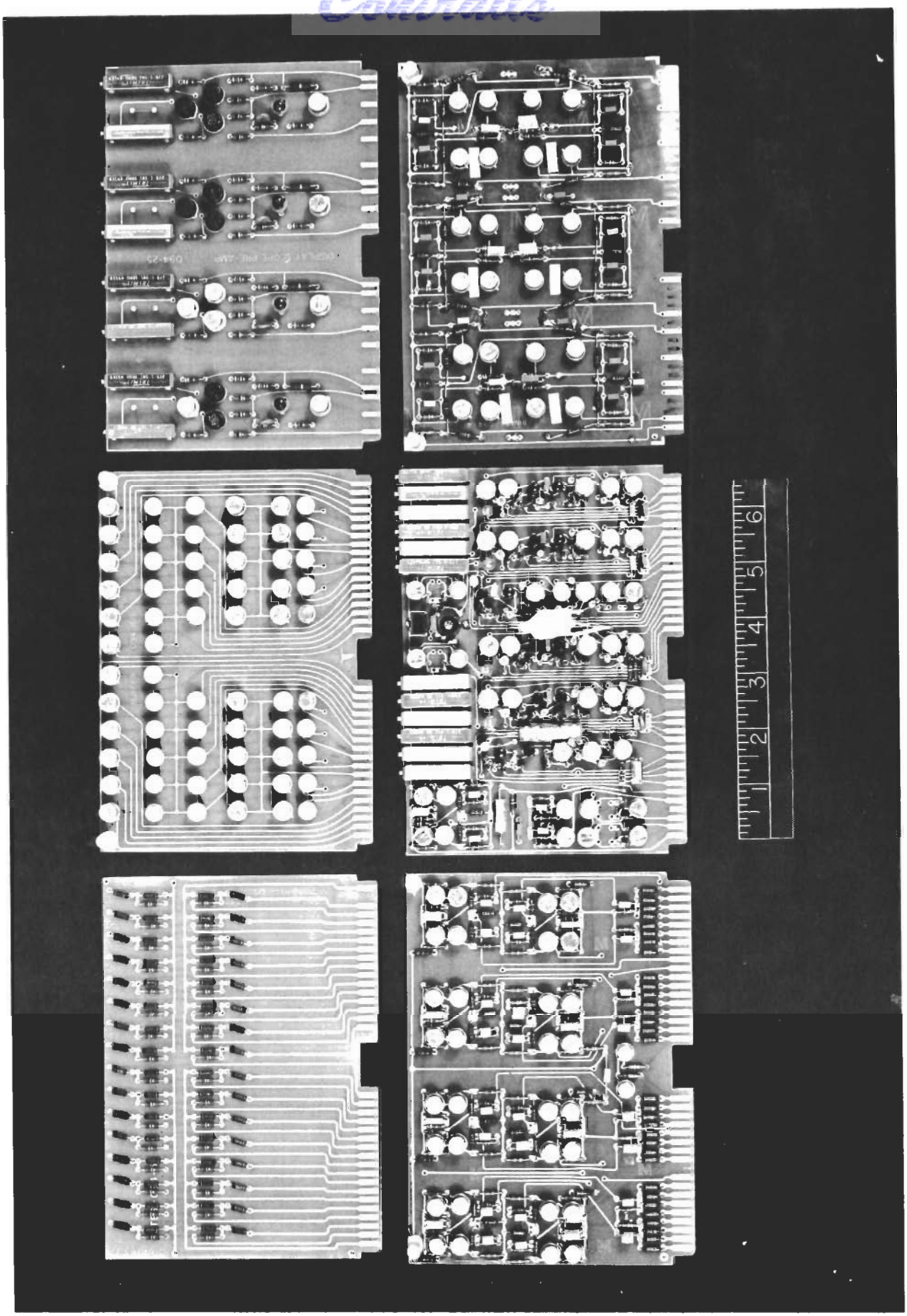


Figure 29. TYPICAL PRINTED CARD

SECTION VI

TECHNICAL RECOMMENDATIONS

With regard to the system layout, it is suggested that future systems be constructed with fixed patch panels and rack mounting so that more room will be available for added display functions.

It is further recommended that the intensity modulation printed circuit cards be repackaged for greater terminal clearance as the present layout is subject to flashover unless very careful cleanup is followed subsequent to soldering.

An aid to programming and troubleshooting would be the addition of a "one-shot" trigger pushbutton so that the sequencer could be advanced from channel to channel at will. In order to make this function more useful it would be desirable to have indicator lamps. Both buffer protection and channel indication could be accomplished by utilizing two lamps per channel.

One lamp could be installed in series with the NPN buffer emitter and the other lamp in series with the PNP emitter.

The NPN lamp would indicate the system sequence and the PNP lamp would indicate a system overload by continuous illumination.

With this type of protection it would be feasible to utilize the buffer pedestals to drive other circuits without danger of catastrophic buffer failure due to accidental shorting of external wiring.

The problem of switching noise causing occasional mis-triggering of the divisible outputs might be solved by connecting an inhibit gate driven by a blanking pulse on the eight trigger input lines.

Logarithmic taper intensity modulation controls substituted for the present linear units would be helpful in extending intensity adjustment range.

Elimination of program control of inter-character blanking should be worth the saving in patch panel space.

A definite improvement to character stroke position, sequencer switching time and intensity modulation delay could be effected by choosing silicon planar diodes with a selected forward characteristic. The type HD4636 has been found to be adequate for every location in the system where IN627's are presently used.

Character legibility could be vastly improved and system complexity could likewise be reduced by employing the presently developed modules in the following variations.

1. Substitute a generator similar to the range-circle amplifier for the triangular wave generator. Gate the output of this generator so that circle quadrants are available during the existing character stroke time periods.

2. Classify all character strokes into a minimum number of coordinate locations and stroke sizes.

3. Form characters by combinations of straight lines and curved segments using a four-stroke scheme.