PRELIMINARY DEVELOPMENT OF A SOLID-STATE MATRIX DISPLAY

B. J. LECHNER, et al.

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FOREWORD

This program was initiated by the Control Systems Research Branch, Flight Control Division, AF Flight Dynamics Laboratory, under Task 619009 "Advanced Display Generation Techniques" of Project 6190 under the direction of Mr. J. H. Kearns, III, and Mr. E. Warren. Captain C. J. Peterson served as the Task Scientist and Contract Monitor throughout the duration of the contract.

This report, describing the first of two efforts for the AF Flight Dynamics Laboratory, covers work conducted from April 1, 1964 to April 30, 1965 under Contract No. AF33(615)1493 by the Radio Corporation of America. The work was conducted in the Computer Research Laboratory, J. A. Rajchman, Director. B. J. Lechner was the Project Engineer and is responsible for the preparation of this report. A. G. Samusinko, G. W. Taylor, and J. Tults contributed to the contract during the work period. Most of the work on ferroelectric materials described in Section II-B was performed by G. W. Taylor and a substantial part of Section II-B of this report was written by him. A. G. Samusenko was responsible for many of the results reported in Section II-D. The electronics for the main 120-element model were designed by J. Tults, and he prepared the material for Appendix I. Also, J. Bowers and J. Horvath aided in the fabrication and testing of the ferroelectric samples, display circuits, and model displays.

This report was submitted by the authors in September 1965.

This report has been reviewed and is approved.

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ABSTRACT

The use of ferrolectric transchargers as storage and control elements in an electroluminescent matrix display has been studied. The research on display panel circuitry has led to the development of a new family of ferroelectric control circuits useful for solid-state matrix display and also for bar graph and other special-purpose displays. In these circuits, the ferroelectric elements provide analog storage and control the energization of the electroluminescent cells in accordance with the stored analog signals. The ferroelectric in conjunction with a diode provides a selection threshold which permits the element to be addressed in a matrix by voltage coincidence. The circuits developed under this program give greatly improved brightness and contrast compared with previous ferroelectric control circuits.

The ferroelectric material used in these studies is a ceramic with composition $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$. Detailed material studies under a concurrent program showed this composition to give the best compromise of low coercivity, high squareness, and stability with life. Ceramic ferroelectrics may be fabricated by doctor-blading, a technique which permits the simultaneous batch fabrication of an integrated array of transchargers for a matrix display.

The scanning and addressing of ferroelectric electroluminescent displays has also been studied. Techniques for both spot-addressing and line-addressing of matrix displays have been developed. Transcharger circuits with logic capability have also been developed; such circuits are especially useful for controlling bar graph, moving pointer, rate field, and alphanumeric displays.

Using the circuits and scanning techniques developed, three experimental model displays were constructed and tested. Taken together, these models demonstrate brightness as high as 48 ft-L; contrast ratio in excess of 100 to 1; geometric resolution as great as 10 elements per inch; capability for producing a gray scale; and a frame rate which allows continuity of motion without blurring or flicker. One of the models has 120 elements arranged as ten rows of 12 elements each and obtains its input signals from a vidicon camera, thus demonstrating the ability to reproduce moving images. The performance of these models clearly demonstrates the potential of using ferroelectric control circuits and electroluminescent elements for high-brightness, high-resolution, solid-state matrix displays.

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ILLUSTRATIONS

ILLUSTRATIONS (Cont'd.)

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ILLUSTRATIONS (Cont'd.)

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SYMBOLS

A	Constant
a_1	Area of ferroelectric FE_1
a_2	Area of ferroelectric FE_2
a_3	Area of ferroelectric FE_3
B	Brightness in ft-L
C	Capacitance in farads
C*	Contrast = $\frac{\text{on brightness}}{\text{off brightness}}$ measured in a dark room
d_1	Thickness of ferroelectric FE_1
d_2	Thickness of ferroelectric FE_2
d_3	Thickness of ferroelectric FE_3
dq	Differential charge in coulombs
dv	Differential charge in volts
dt	Differential charge in seconds
E	Electric field in V/cm
E_c	Nominal 60-Hz coercive field in V/cm
I	Current in amperes
I_{co}	Diode reverse saturation current
j	Integral factor of n
K	Constant
k	Constant
m	Number of elements in a line in a matrix display
N_1	Number of turns on transformer winding #1
N_2	Number of turns on transformer winding #2
N_3	Number of turns on transformer winding #3
n	Number of lines in a matrix display
P_r	Remanent polarization measured at zero field in $\mu coul/cm^2$
P_s	Saturation polarization measured at $3E_c$ in $\mu coul/cm^2$
Q_U	Total charge switched by an unblocked transcharger
Q_B	Total charge switched by a blocked transcharger
q	Charge in coulombs
S	P_r/P_s
T_F	Frame time in seconds
T_L	Addressing time in seconds in a line-addressed display

T_S	Addressing time in seconds in a spot-addressed display
u	Number of columns in a storage scanner
V	Voltage in volts
v	Number of rows in a storage scanner
x	Fraction of zirconium in $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$
y	Fraction of tin in $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$
z	Fraction of titanium in $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$
Φ	Magnetic flux
α	Constant

SECTION I

INTRODUCTION

The objective of this research program was to perform the preliminary work on a solid-state matrix display capable of presenting two-dimensional video information. The work has been directed toward proving the feasibility of a solid-state matrix display based on an advanced form of control circuitry using ferroelectric transchargers. The work included studies of panel design, development of the required fabrication techniques, selection of electroluminescent phosphors for maximum brightness, studies of scanning and driving circuitry, construction of model displays, and the evaluation of the performance of a complete system based on the techniques studied. Ultimate performance goals included a geometric resolution of 10 elements per inch, a uniform time average highlight brightness in excess of 15 ft-L, a contrast ratio of 100 to 1, capability through control circuitry for producing a gray scale (halftones) by independently controlling the brightness of any display element, and a frame rate which allows continuity of motion without objectionable blurring or perceptible flicker.

Previous attempts to achieve such a display have been unsuccessful for a variety of reasons. From a survey of earlier work,[1] it was evident that certain minimum requirements must be satisfied by the elements of a solid-state matrix display if it is to meet the above objectives. These requirements are: the element must produce visible light; the element must provide storage (analog storage if gray scale is required); the light must be controlled in accordance with the stored video signal; and the element must exhibit a well-defined selection threshold. In addition, if the display is to have practical importance, the elements must be economical of power and be amenable to batch fabrication in geometries that may be assembled into display panels.

Work[2] done on a previous program supported in part by Contract No. AF33(657)8725, and reported in "Solid State Display", TDR No. RTD-TDR-4033, Part II, April 10, 1964, established the basic feasibility of using ferroelectric transcharger controlled electroluminescent elements to meet these requirements for a solid-state matrix display. As a part of the previous program, a 7-element experimental model display using transcharger-controlled electroluminescent elements was constructed and tested. The successful operation of this model demonstrated the basic feasibility of the approach, but at the same time indicated that considerable additional research on ferroelectric materials, display panel fabrication techniques, and display panel circuitry would be required before one could hope to build a high-brightness, high-resolution, all solid-state display panel for moving halftone images.

The aforementioned research effort established that ceramic ferroelectrics from the ternary system, lead zirconate stannate titanate, offered the greatest promise for use in transchargers for controlling electroluminescent elements. Consequently, a research program[3] under Contract No. AF33(615)1193, reported in "Solid-State Raster Scanning for Display," TR No. AFAL-TR-65-106, May 1965,

running concurrently with the work reported here, has been devoted to research studies of these materials and to finding techniques for batch-fabricating ceramic ferroelectric materials in geometries suitable for constructing an entire line of a display panel at once.

The principal emphasis in the work reported here has been given to a thorough study of display panel circuitry and peripheral addressing circuitry. This work has led to the invention of a new family of transcharger control circuits which give greatly improved performance compared with previously devised circuits. Using these new circuits, three experimental model displays have been constructed and tested during the contract period. Taken together, these models demonstrate brightness as high as 48 ft-L, contrast ratio in excess of 100 to 1, geometric resolution as great as 10 elements per inch, capability for producing a gray scale, and a frame rate which allows continuity of motion without blurring or flicker. One of the models has 120 elements arranged as 10 rows of 12 elements each and obtains its input signals from a vidicon camera, thus demonstrating the ability to reproduce moving images. These models show a tenfold improvement in brightness and contrast over previously constructed experimental models, and therefore clearly demonstrate the potential of using ferroelectric transcharger controlled electroluminescent elements for high-brightness, high-resolution, all solid-state matrix displays.

Although the results of the present program are very encouraging indeed, it is nevertheless necessary that further research be accomplished on ferroelectric materials, fabrication techniques, display panel circuitry, and especially peripheral addressing circuitry.

SECTION II

DISCUSSION

A. GENERAL

The basic balanced transcharger circuit developed under Contract No. AF33(657)8725 (reported in "Solid-State Display", TDR No. RTD-TDR-4033, Part II, April 10, 1964) is shown in Figure 1.[2] This display panel element, consisting of a ferroelectric transcharger and an electroluminescent cell, formed the basis for the investigation carried out under this research program. Arrays of these elements would normally be arranged in a matrix as shown in Figure 2 and be addressed by voltage coincidence on the row and column lines. In addition to providing a selection threshold, the transcharger at each matrix location stores an analog value of video information and controls the excitation of the electroluminescent cell in accordance with this stored analog value. The display panel is in effect an analog memory with a continuous visual output of the information stored at each memory location.

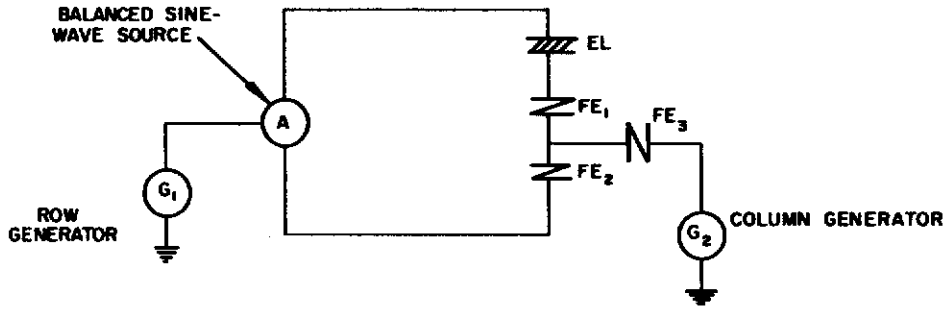

Figure 1. Balanced Transcharger Circuit.

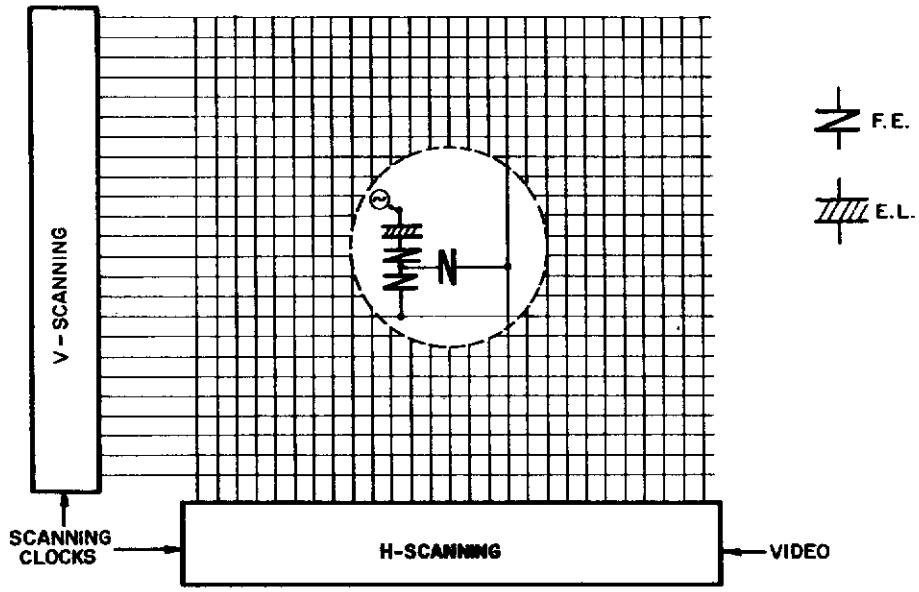

Figure 2. Transcharger Electroluminescent Matrix Display.

As with a conventional computer memory, the display may be bit-organized or word-organized. In the bit-organized mode the panel is addressed sequentially element by element. All elements are addressed once in each frame time and the process is then repeated.

In the word-organized mode each row of the display panel constitutes one word. The panel is addressed sequentially line by line with all elements in each line being addressed simultaneously by the horizontal storage and scanning register. All lines are addressed once in each frame time and the process is then repeated.

The basic feasibility of both the balanced transcharger circuit and the proposed panel organization were demonstrated under Contract No. AF33(657)8725.[2] The results of this previous work, however, indicated clearly the need for further research on ferroelectric materials, electroluminescent cells, display panel circuitry, panel fabrication techniques, and peripheral scanning and driving circuitry. The details of the efforts in these areas are presented in Sections II-B through II-F.

Since the ferroelectric transcharger is the key element in the proposed display system a substantial part of the concurrent research effort under Contract No. AF33(615)1193 (reported in "Solid-State Raster Scanning for Display", TR No. AFAL-TR-65-106, May 1965) was devoted to a detailed study of ferroelectric materials and particularly to methods of batch-fabricating ferroelectric transchargers. This related work is summarized in Section II-B.

The principal effort under Contract No. AF33(615)1493 was devoted to research on display panel circuitry. This work led to a new family of ferroelectric control circuits and is described in detail in Section II-D.

Also, during the latter half of the contract period, three experimental model transcharger-controlled electroluminescent displays were constructed and tested. These models and the results of the tests made on them are described in Section II-G. A detailed description of the electronic circuitry designed and constructed to exercise the display models can be found in the Appendices.

B. FERROELECTRIC MATERIALS*

1. Requirements and Measurements

Previous investigations[2] of several ferroelectric materials showed that, for transcharger applications to display matrices, ceramic ferroelectrics from the ternary system $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$ (where x, y, and z

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* A major portion of the material presented in this section previously appeared in the Final Report under Contract No. AF33(615)1193, "Solid-State Raster Scanning for Display". Inclusion of this material here is considered essential for proper understanding of the work accomplished under Contract No. AF33(615)1493.

represent the fractions of zirconium, tin, and titanium, respectively) offered the most promise of providing satisfactory electrical properties combined with a fabrication method amenable to the simultaneous batch-fabrication of many transchargers. Therefore the investigation under Contract No. AF33(615)1193 was limited solely to these materials. This materials work was done in part by the Clevite Corporation of Cleveland, Ohio, under subcontract from RCA. To evaluate the materials, three sets of measurements were made: Ferroelectric hysteresis loops were measured at 400 cps; pulse measurements of the switching characteristics of the ferroelectric were made; and actual transchargers were tested. The hysteresis loop measurement is by far the simplest measurement to make and at the same time gives much information about the ferroelectric. Figure 3 shows a polarization versus field hysteresis loop for a ferroelectric. The important parameters, coercive field (E_c), saturation polarization (P_s), remnant polarization (P_r), and squareness (S) may be measured directly from the loop. The definition of P_s in Figure 3, different from that sometimes found in the literature, has the advantage that it is easily measured and has been used consistently throughout the work reported here.

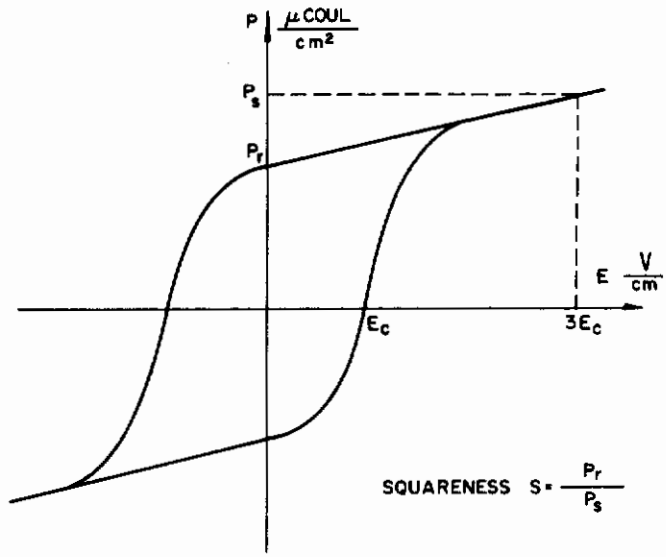


Figure 3.
Ferroelectric Hysteresis Loop.

The use of ferroelectric transchargers in a matrix display requires that the ferroelectric have a sufficiently high Curie temperature, switch in a few tens of microseconds, tolerate well the deleterious effects of hundreds of half-amplitude disturb pulses, have a $P_r > 0.5$ μcoul/cm^2, have as low an E_c as possible, have as high an S as possible, and be stable with operation for hundreds of hours. All of the ceramics investigated which showed hysteresis loops at all met the requirements on Curie temperature, switching time, tolerance to disturbs, and polarization. The studies therefore were concentrated on E_c, S, and stability with life.

2. Compositional Studies

Previous research efforts on ferroelectric materials have led to the development of a range of rhombohedral ferroelectric Pb(Zr, Ti, Sn)O_3 ceramic compositions that have a relatively low coercive field and that switch rapidly. This behavior is unusual in ferroelectric ceramics consisting, as they do, of varying sizes and orientations of domains and crystallites. These compositions display relatively square hysteresis loops for ceramics, particularly

under slow loop conditions. They are rhombohedral ferroelectrics near in composition to antiferroelectrics.

For preliminary evaluation, two prototype compositions were chosen on the basis of slow-loop properties. They were $Pb_{.99}[(Zr_{.80}Sn_{.20})_{.93}Ti_{.07}]_{.98}Nb_{.02}O_3$, which had a very square loop with very steep sides (sharply defined E_c), and $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.85}Ti_{.15}]_{.98}Nb_{.02}O_3$, which had a loop with slightly lower squareness but had low E_c and very low rhombohedral distortion.

It had been observed that the prototype ceramic ferroelectrics suffered a deterioration of properties, both "on the shelf" and with "excitation", in the form of increasing coercive voltage and decreasing polarization. Extensive tests, including spectrographic examination of decayed samples, confirmed that the decay was due, in large part, to migration into the ceramic of silver ions from the silver paste used to make connections to the evaporated gold electrodes on the ceramic. By keeping the silver paste physically remote from the active area of the ferroelectric, decay from this cause is eliminated. Although the remaining "excitation" decay is in some cases quite severe (as much as 30-percent decrease in polarization and as much as 100-percent increase in coercive field) there are some ceramic compositions which show substantially no decay after hundreds of hours of continuous operation at 400 Hz.

To study this decay as well as to explore in detail the effects of composition on E_c and S, 27 different ceramic compositions were prepared. The objective of the compositional studies was to find that material having the lowest coercive field E_c, the highest squareness ratio $S = P_r/P_s$, and the best stability with life. The following shorthand system has been used to designate the compositions tested:

40/60-12-2Nb means $Pb_{.99}[(Zr_{.40}Sn_{.60})_{.88}Ti_{.12}]_{.98}Nb_{.02}O_3$

The following are the 27 compositions which were tested:

40/60-12-2Nb
40/60-15-2Nb
40/60-18-2Nb
40/60-21-2Nb

45/55-15-2Nb

50/50- 9-2Nb
50/50-10-2Nb
50/50-11-2Nb
50/50-12-2Nb
50/50-13-2Nb
50/50-14-2Nb
50/50-15-2Nb
50/50-18-2Nb
50/50-21-2Nb

55/45-15-2Nb

60/40- 8-2Nb
60/40- 9-2Nb
60/40-10-2Nb
60/40-12-2Nb
60/40-15-2Nb

73/27- 7-2Nb

80/20- 4-2Nb
80/20- 5-2Nb
80/20- 6-2Nb
80/20- 7-2Nb
80/20-10-2Nb
80/20-13-2Nb

The samples were prepared by conventional dry-pressing techniques in the form of 5/8-in.-diameter discs which were lapped to a nominal thickness of 3 mils. For testing, the samples were electroded with evaporated gold. The measurements made on these 27 different compositions included the initial values of E_c, P_r, P_s, $S = P_r/P_s$, and the decay behavior of these four loop parameters under prolonged (1000 hours) excitation with a 400-Hz sine wave of peak amplitude approximately equal to $3E_c$.

Since $x + y = 1$ in the formula for the materials, only two parameters are required to specify a particular composition. It is convenient to choose these to be x/y and z. Figures 4, 5, 6, and 7 show the initial values of E_c, P_s, P_r, and S, respectively, as functions of x/y for the 27 materials. In these curves z is a parameter and at any value of x/y the spread along the abscissa encompasses the entire range of values of z. The data have been plotted in this fashion because at certain values of x/y, there were only one or two values of z available. Furthermore, it has not been possible to detect systematic variations with z.

From Figures 4 through 7, it can be seen that the requirements of low E_c and high S are contradictory since E_c is lowest for small x/y and S is highest for large x/y. A compromise must, therefore, be made.

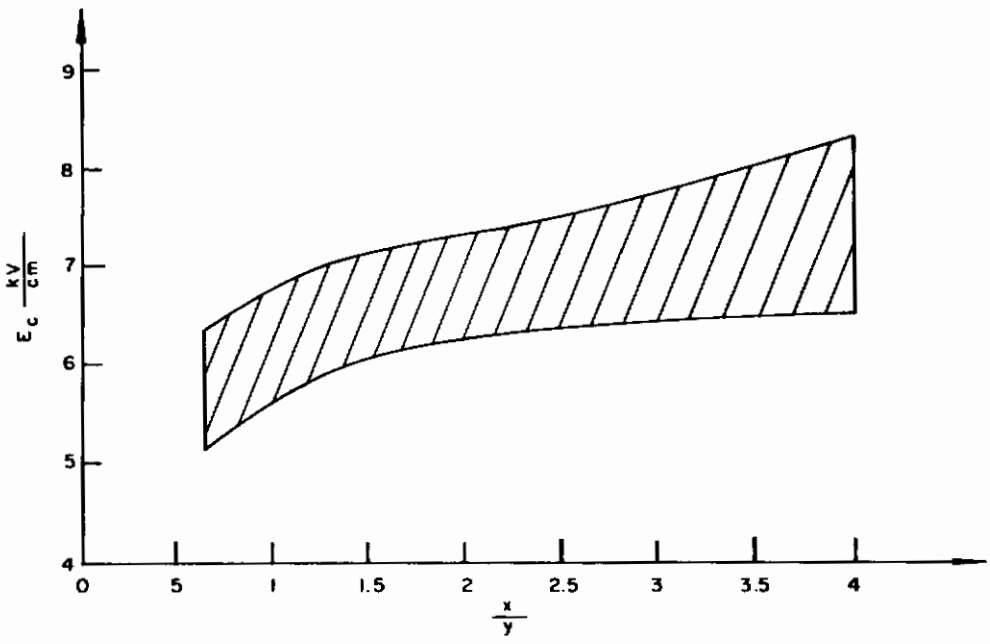


Figure 4. E_c vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

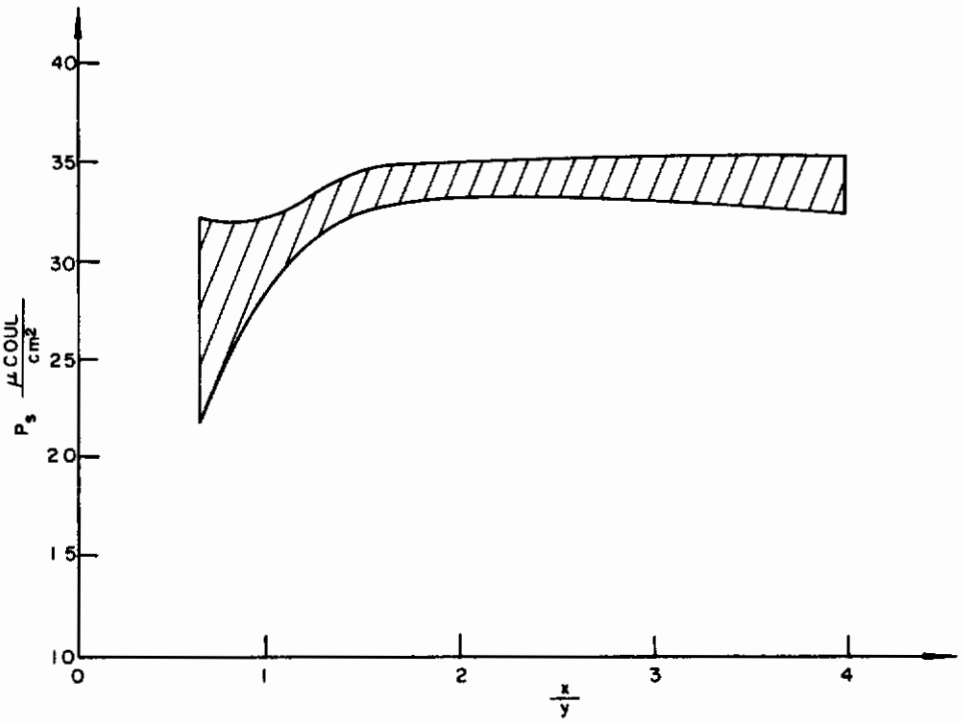


Figure 5. P_s vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

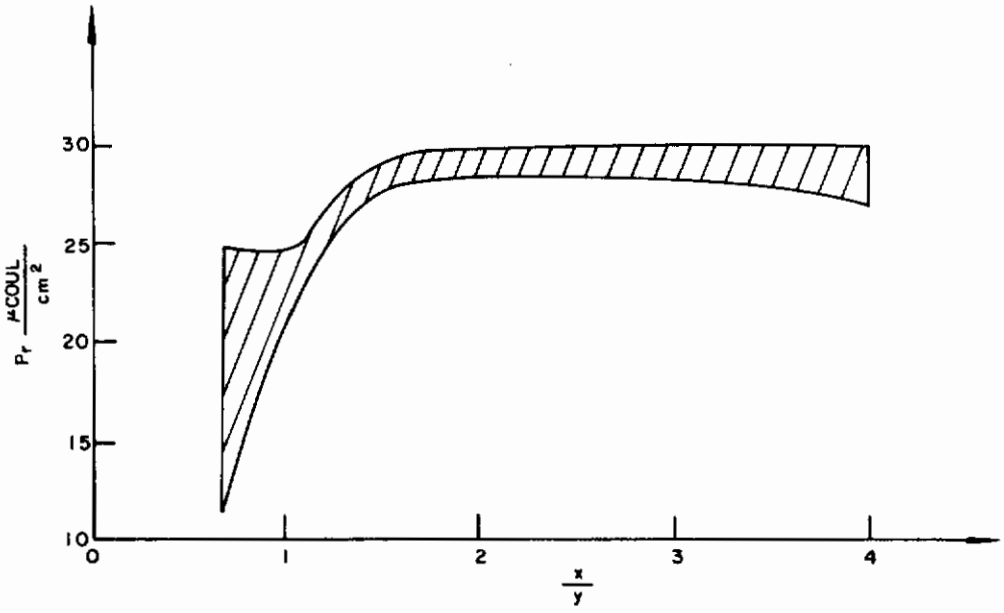


Figure 6. P_r vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

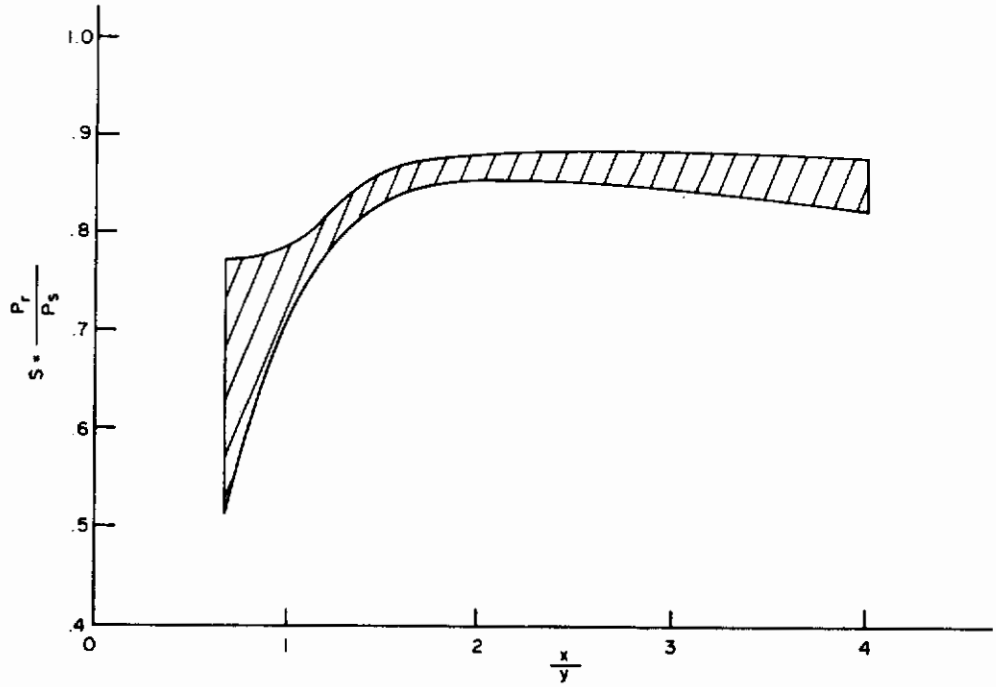


Figure 7. Squareness vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

To examine the performance with life of the 27 different compositions, refer to Figures 8 through 11. Here the loop parameters E_c, P_s, P_r, and S after 500 hours of continuous 400-Hz excitation at approximately $3E_c$ peak have been plotted as functions of x/y. E_c, P_s, P_r, and S have all been normalized to their initial values and in each case are plotted as fractions of the initial values. As in Figures 4 through 7, z is a parameter in these curves and at any value of x/y the spread along the abscissa encompasses the entire range of values of z. It can be seen from Figure 8 that the decay in E_c increases monotonically with increasing x/y. From Figures 9 through 11 it can be seen that the decay in P_s, P_r, and S is minimal for x/y = 1. The data of Figures 4 through 11 suggest that a best compromise among E_c, S, and performance with life would be a material with x/y = 1.

But what value of z should be chosen? Careful examination of E_c, P_s, P_r, and S as functions of z and time for $Pb_{.99}[(Zr_{.50}Sn_{.50})_{1-z}Ti_z]_{.98}Nb_{.02}O_3$, i.e., for the x/y = 1 materials, shows clearly that z = 0.14 represents the optimum choice. Slightly higher squareness would result for z = 0.13 and slightly lower E_c would result for z = 0.15, but in both cases the performance with life would be poorer than that for z = 0.14. It was therefore decided to choose $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$ or, for short, 50/50-14-2Nb, as the material to be used in fabrication and circuit studies and in the experimental model displays which were constructed.

The 50/50-14-2Nb material has an initial E_c = 6.7 kV/cm and an initial S = 0.75. After 1000 hours of continuous operation E_c = 7.7 kV/cm, an increase of about 15 percent; the 1000-hour values of P_r, P_s, and S are negligibly different from the initial values. Figures 12, 13, and 14 show E_c, P_s and P_r, and S, respectively, as functions of time for this material.

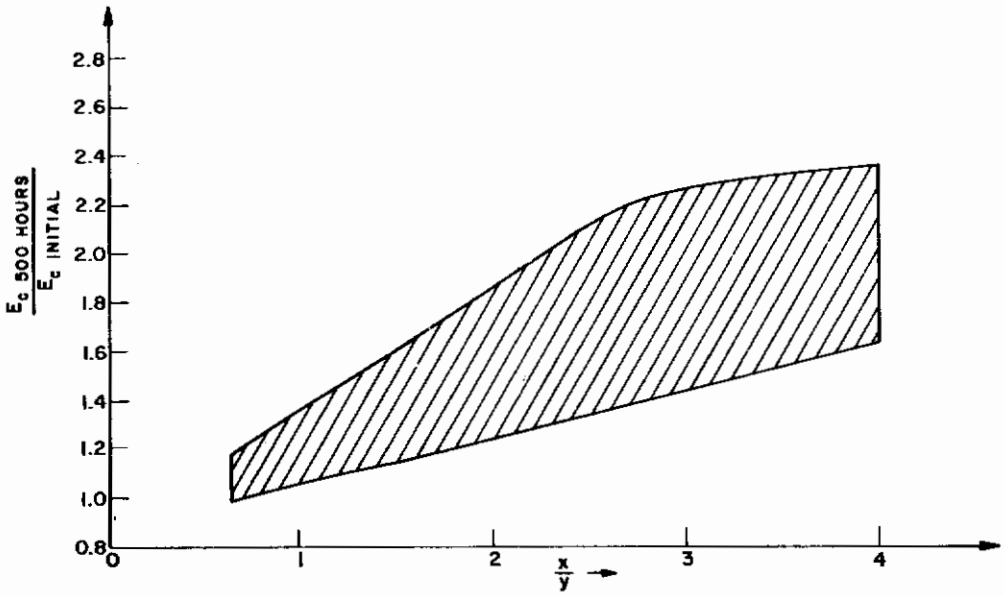


Figure 8. $E_{c_{500 \text{ hours}}}/E_{c_{\text{initial}}}$ vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

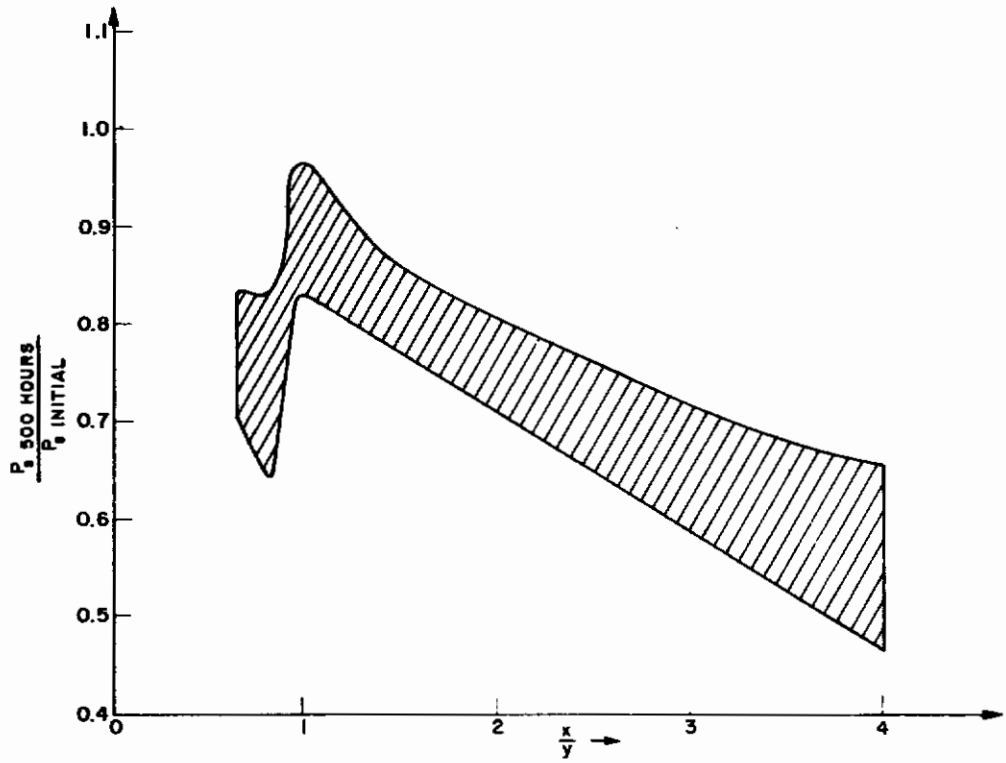


Figure 9. $P_{s_{500 \text{ hours}}}/P_{s_{\text{initial}}}$ vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

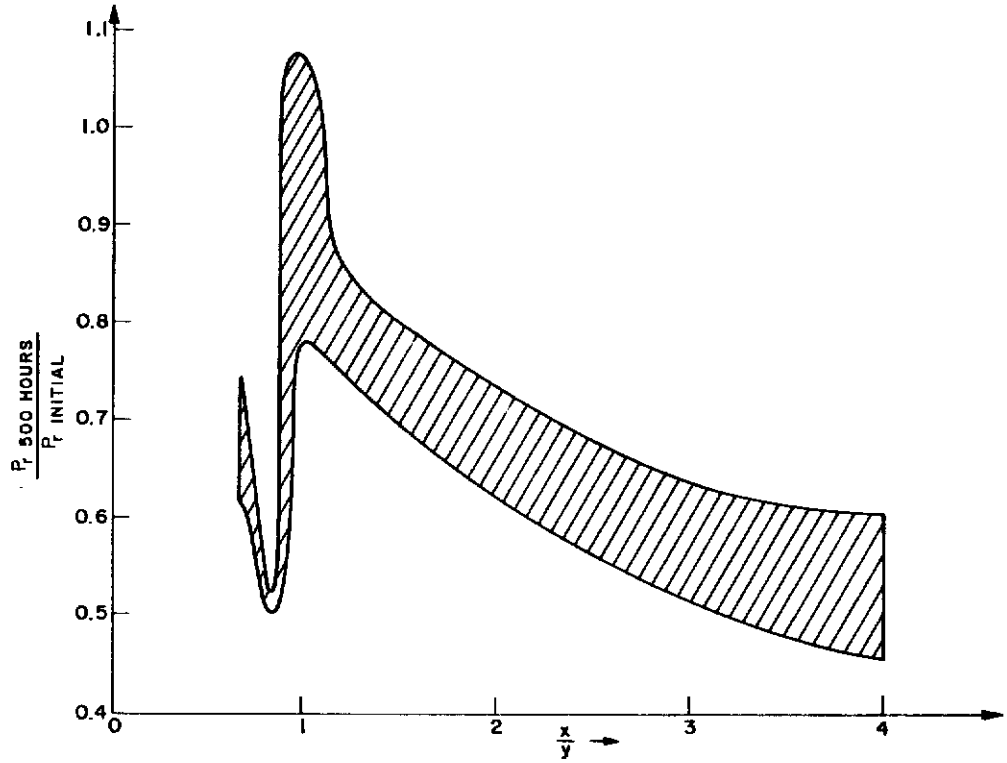


Figure 10. $Pr_{500\ hours}/Pr_{initial}$ vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

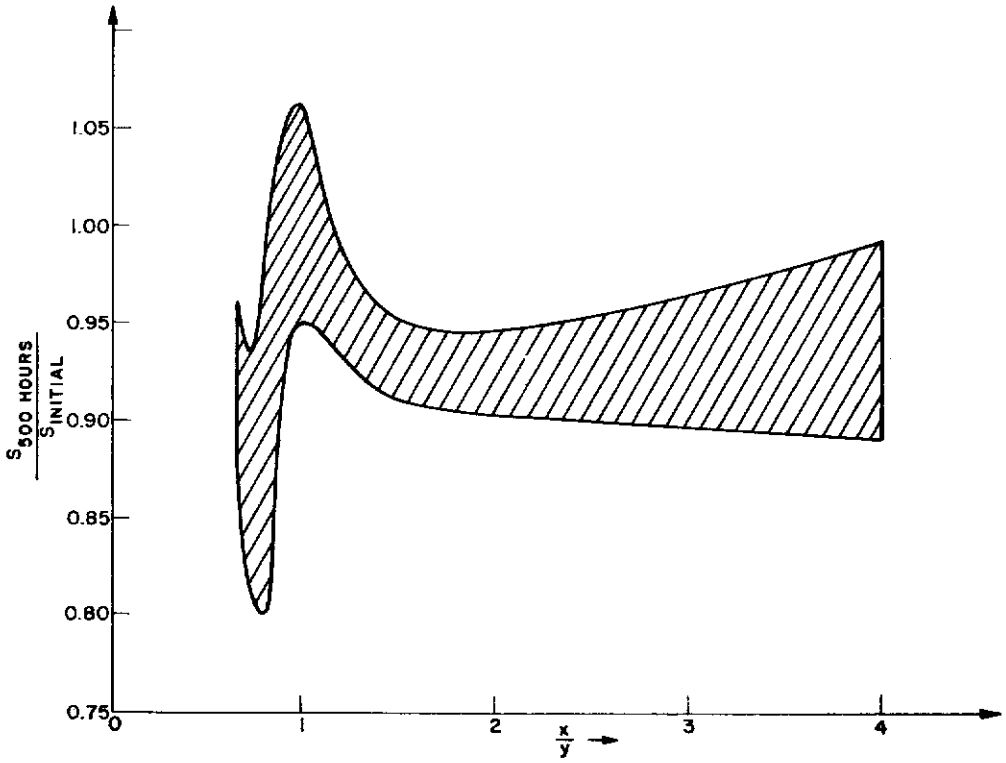


Figure 11. $S_{500\ hours}/S_{initial}$ vs x/y for $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$.

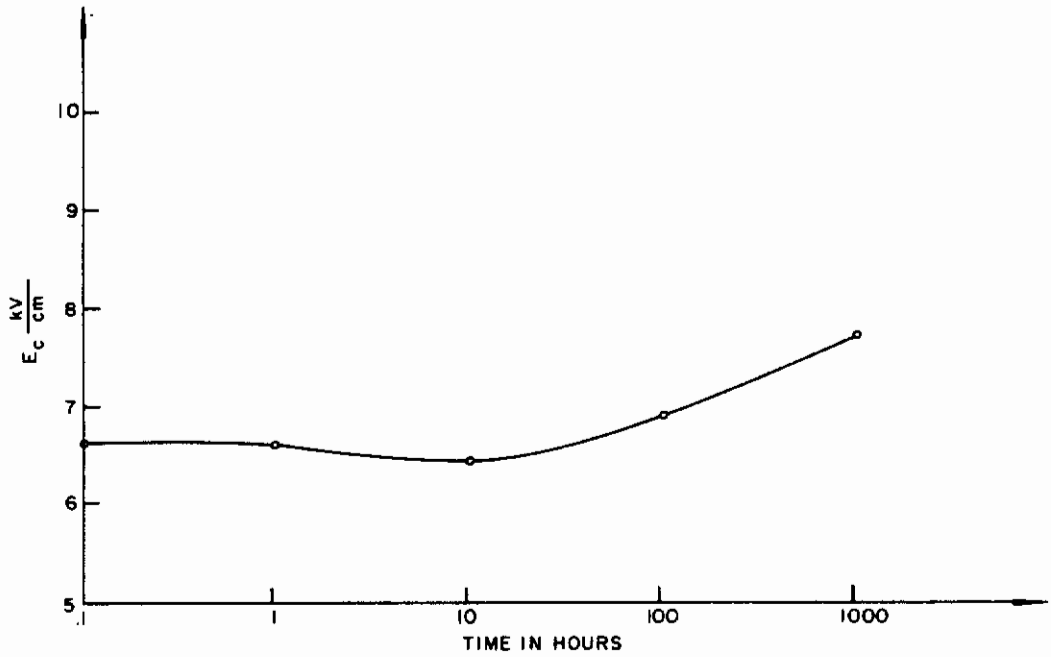


Figure 12. E_c vs Time for $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$.

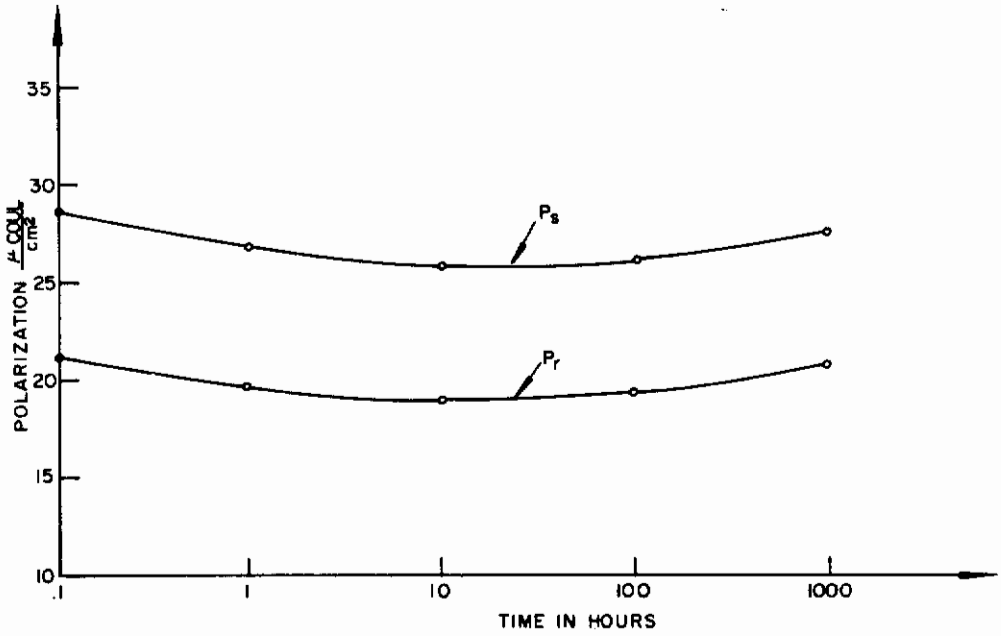


Figure 13. P_s and P_r vs Time for $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$.

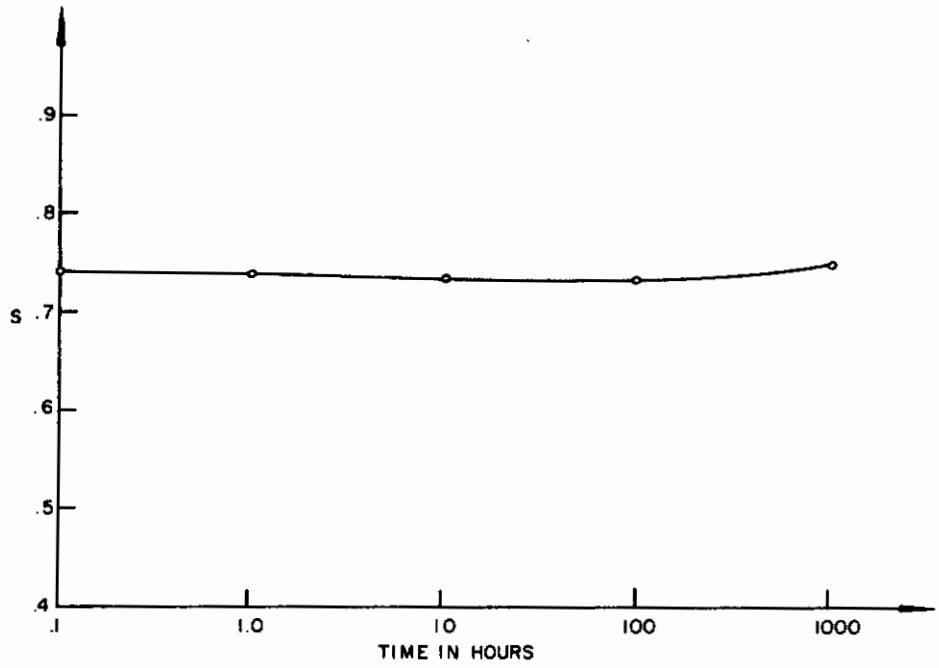


Figure 14. Squareness vs Time for $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$.

3. Use of Nb and Other "Donor" Additives

Although most of the work done on this program was with niobium-doped materials as indicated in Paragraph II-B-2, 19 ceramic compositions with additives other than niobium were prepared and their ferroelectric properties were studied.

The general conclusion is that the niobium-doped materials are superior to those materials with other additives. However, the number of samples with other additives was limited and, therefore, it cannot definitely be stated that niobium is the optimum additive.

4. Surface Preparation

In addition to the compositional studies, a study of ceramic surface preparation has been carried out. A detailed comparison of samples having a very finely polished surface with samples of identical composition but having conventionally lapped surfaces has shown that the fine polishing reduces the coercive field, increases the squareness, and reduces the decay. The finely polished samples were prepared by slow, careful polishing with 5-Å paper. Using this technique it was possible to reduce the thickness to 1.5 mils. Seventeen samples from the group of 27 compositions listed on page 9 were so prepared and have been tested for 500 hours at 400 Hz.

Table I gives a comparison of initial loop parameters and life performance of polished and lapped 50/50-14-2Nb material. The life data have been normalized to the 10-hour values to eliminate the effects of initial aging. Parameters of a doctor-bladed sample (see Paragraph II-B-9) have been included in the table for comparison.

TABLE I

COMPARISON OF PROPERTIES OF LAPPED, POLISHED, AND DOCTOR-BLADED $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$ CERAMIC SAMPLES

PARAMETER	SAMPLES		
	LAPPED	POLISHED	DOCTOR-BLADED
$E_{c_{initial}}$	6.7 kV/cm	5.4 kV/cm	5.5 kV/cm
$P_{s_{initial}}$	28.7 μcoul/cm^2	33 μcoul/cm^2	34.8 μcoul/cm^2
$P_{r_{initial}}$	21.3 μcoul/cm^2	28.2 μcoul/cm^2	29 μcoul/cm^2
S	0.75	0.86	0.84
$\frac{E_{c_{1000\ hours}}}{E_{c_{10\ hours}}}$	1.20	1.15	1.14
$\frac{P_{s_{1000\ hours}}}{P_{s_{10\ hours}}}$	1.08	1.00	0.98
$\frac{P_{r_{1000\ hours}}}{P_{r_{10\ hours}}}$	1.12	0.96	0.94
$\frac{S_{1000\ hours}}{S_{10\ hours}}$	1.04	0.96	0.96

The overall conclusion is that polishing is a distinct advantage for transcharger applications since it increases the squareness, reduces the decay in E_c and, if a suitable pre-aging treatment is given, also reduces the decay in P_r and P_s. The practical difficulty of polishing large areas of ceramics must be weighed against this.

5. Effect of the Magnitude of the Applied Field

The main effect of the magnitude of the applied driving field (E) on the ceramic characteristics is that an increase in E causes an increase in the amount of decay in E_c. As might be expected, the amount of increase is sharply dependent on both the composition of the ceramic and the surface treatment the material has received. Since the amount of data on the effect

of varying E is limited, it is not possible to determine the extent of these dependencies. However, some idea of the importance the magnitude of E has on the decay of E_c can be gained from the fact that for a lapped sample of composition x/y = 2.7, z = 0.07, a 27-percent increase in the magnitude of the applied E causes the amount of decay in E_c, after 500 hours of excitation, to increase by 38 percent. This is illustrated in Figure 15 where E_c has been plotted as a function of time for two different applied driving fields.

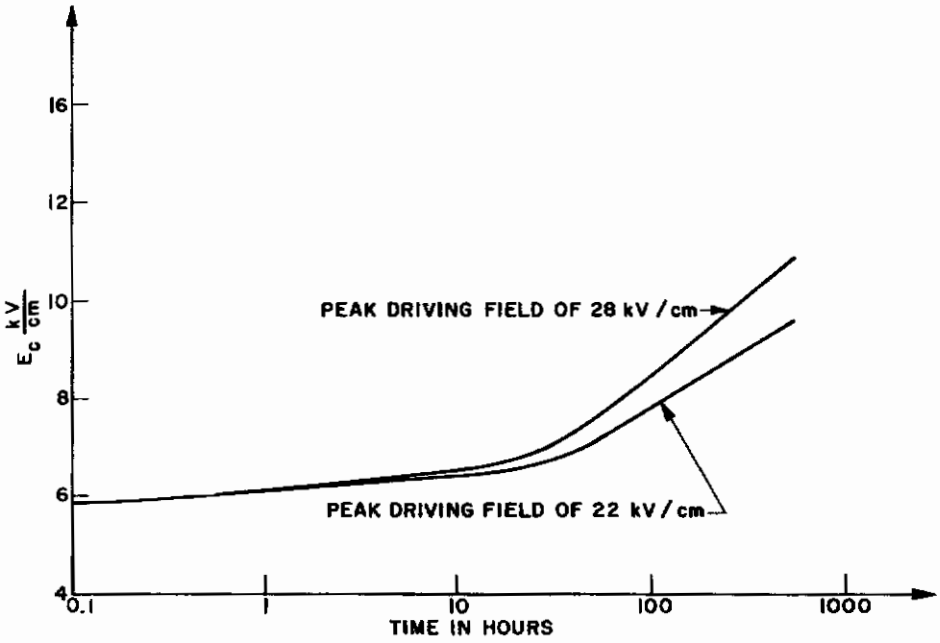


Figure 15. E_c vs Time for $Pb_{.99}[(Zr_{.73}Sn_{.27})_{.93}Ti_{.07}]_{.98}Nb_{.02}O_3$ at Two Different Driving Fields.

These results indicate that to minimize the decay in E_c, the applied E should be reduced to as low a level as is consistent with successful transcharger operation.

6. Fringing Effects

Some work was done to study closely the effects of electrode area on the hysteresis loop parameters. Measurements made on a series of different size square electrodes showed that once the electrode area becomes less than about 2×10^{-4} in.^{2}, the values of E_c, P_r, and P_s begin to rise very steeply. Because P_s rises faster than P_r there is a resultant decrease in $S = P_r/P_s$ as the electrode area becomes very small. Figure 16 shows E_c, P_r, and P_s as functions of the electrode size for a 2.6-mil-thick 80/20-8-2Nb sample. All these effects are due to fringing fields which become increasingly important as the electrode area decreases. Experiments indicate that the fringing, approximately the same on all compositions, extends about 2 mils beyond the electrode boundary. The fringing effect could increase the tolerance problem in a high-resolution display which requires very small ferroelectric transcharger areas.

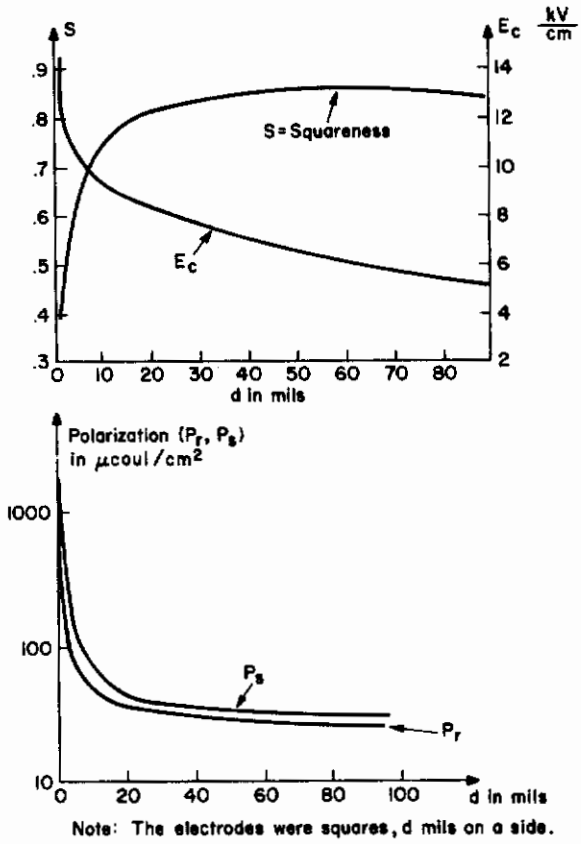


Figure 16. E_c, P_r, P_s, and S as Functions of Electrode Size for a 2.6-mil-Thick 80/20-7-2Nb Ceramic Ferroelectric.

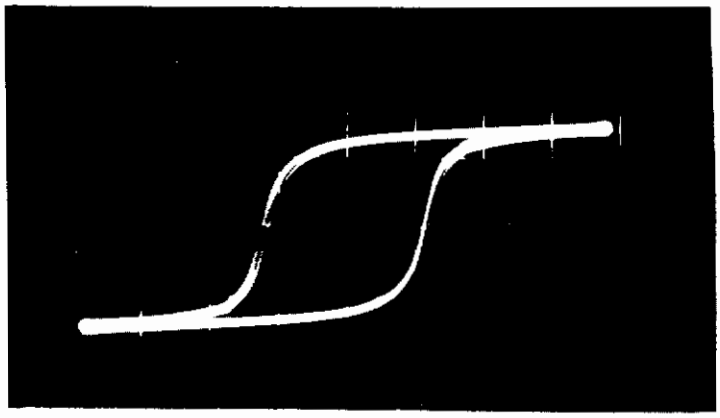
7. Uniformity

Since, in a display, many ferroelectric capacitors will be formed by appropriately electroding a single piece of ferroelectric material, it is important that the ferroelectric properties of the material be uniform so that the capacitors, and thus the transchargers formed by interconnecting the capacitors, will have identical properties. To test the uniformity of ceramic ferroelectric material, a single piece of 50/50-14-2Nb ceramic was electroded to produce seven geometrically identical capacitors. The capacitor electrodes were squares, 30 mils on a side. Figure 17 is a multiple-exposure photograph which shows, superimposed on each other, the 400-Hz hysteresis loops for these seven capacitors. As can be seen from the photograph, the seven loops are very nearly identical. This indicates that there should be little, if any, tolerance problem in a large-scale display.

8. Parameter Decay

Observations on hysteresis loops before and after repeated cycling show that the loop character gradually changes. The coercive field increases, the

magnitude of the saturation and remnant polarization decreases, and the loops become progressively less square. Although from a practical viewpoint ceramic compositions are available which suffer a minimum amount of excitation decay, the mechanism of this decay, and the larger decay which occurs in other compositions is not well understood. Were the mechanism known, it is likely that improved materials could be developed; therefore, efforts were made to discover the mechanism of the decay.



SCALES: HORIZONTAL — 5.22 $\frac{kV}{cm}$ /DIV.
VERTICAL — 24.6 $\frac{\mu coul}{cm^2}$ /DIV.

Figure 17. Multiple Exposure of 7 Hysteresis Loops for 7 Ferroelectric Capacitors Formed on a Single Piece of 50/50-14-2Nb Ceramic.

It is well known that with DC fields most ceramic dielectrics blacken and degrade in electrical resistivity if exposed for long intervals at elevated temperature. It is generally believed that this action is electrochemical in nature, with valency change and loss of oxygen from the crystal lattice the probable mechanism. There has, however, been little emphasis on the effects of long-duration AC fields. These have been considered ineffective in causing decay in ceramic dielectrics, except for fields sufficient to cause breakdown. It is considered improbable that AC fields would cause electrolysis unless some DC components were present. However, the experience in this project makes it plain that the hysteresis loop tends to widen and collapse very slowly under strong AC excitation.

Berlincourt[5,6] has considered this effect. He compares crystal distortion for ferroelectric samples near the antiferroelectric boundary with different $PbSnO_3$ content. He also presents measurements of strain versus field for these specimens. The magnitude of the switching strain appears to vary with the crystal distortion.

If only 180° switching took place, as with an oriented crystal, the switching strains would be accounted for completely by the piezoelectric effect. In fact, however, they are substantially larger, and Berlincourt compares the "strain hump", the nonpiezoelectric contribution to strain, for these compositions. The true strains are quite severe, and it is implicit in Berlincourt's approach that the degradation is either caused by or accompanied by microcracks. The dielectric behavior is consistent with this supposition. Some of the field would be concentrated across those cracks parallel to the electrodes. This would raise the apparent E_c and lower the switched polarization.

To test these ideas, a number of experiments and observations were made. These included microscopic observation of samples which had been subjected to alternating fields for various periods of time and measurements of strain-field characteristics before and after operation with alternating fields. Although time did not permit as thorough an investigation as desired, the results do show that degradation of these ferroelectrics involves several simultaneous effects. They are as follows:

a. Initially large strain-field effects occur. These diminish with time. This represents assumption of a more stable domain pattern with mostly 180° switching.

b. Microcracks occur at the electrode edge or at other regions of field concentration.

c. The ceramic darkens with exposure to AC field.

d. The switched polarization diminishes, and the coercive field increases. Generally, the loop becomes less "square" and more "slanted."

The electrical behavior is compatible with the observed phenomena and must represent their combined effects. The initially high reversible strain is consistent with the formation of the microcracks at stressed zones. The progressive lowering of the reversible strain and of the reversible polarization denotes the assumption of a more stable domain pattern. Eventually, mostly 180° switching takes place, with minimum strain. The microcracked region represents an array of series-parallel leakages that would tend to lower the switched polarization at a given field, perhaps by bypassing regions of crystallites. The darkening, if it can be presumed to represent lowered resistivity, would be connected with similar leakage effects.

These effects may be ameliorated by using electrodes of other material or other geometry. Also, it may be possible to reduce the decay by controlling the microtexture, particularly the grain size and porosity, of the material.

9. Ferroelectric Material Fabrication Techniques

There are three basic fabrication techniques available for the production of ceramic ferroelectric materials. They are:

1. Dry-pressing, firing, slicing, and lapping.
2. Hot-pressing, slicing, and lapping.
3. Doctor-blading or other thin-sheet process and firing.

Since it is at present the best-controlled process, dry-pressing has been used to prepare the various samples used in the compositional studies. The disadvantage of this process is that it is not directly applicable to the production of the long thin strips that are required for the batch-fabrication of transchargers. It is, of course, possible to assemble individual transchargers, made by dry-pressing, onto a substrate to produce a display panel. This would require fabricating bar or rod stock by dry-pressing, slicing into blanks, lapping to thickness, electroding and mounting. This, in fact, is precisely the process used to prepare the samples for the compositional studies discussed above and to produce transchargers for the circuit studies and the experimental models discussed in Sections II-D and II-G.

Hot-pressing differs from dry-pressing only in that, when a sample is made by hot-pressing, the forming and firing steps are carried out simultaneously. Since the hot-pressed materials are denser (very nearly theoretical density) than dry-pressed materials, it might be expected that they would have superior electrical characteristics. Limited electrical tests of hot-pressed 73/27-7-2Nb samples showed that the hot-pressed material was indeed slightly superior to the dry-pressed samples of the same composition.

The doctor-blading technique is by far the most attractive fabrication method. This technique has been successfully used to fabricate magnetic materials and promises to provide a means of inexpensive batch-fabrication of transchargers for use in a matrix display. To make a ceramic by doctor-blading, the ceramic powder is mixed with a liquid binder, poured onto a piece of glass, and then bladed into a uniform layer with a precision coating knife. After it has dried, the bladed layer is peeled from the glass. In this state, the "green" ceramic is easily handled and may be cut, punched, etc. It is then fired in similar fashion to the conventional dry-pressed ceramic; however, the large, thin pieces obtained by doctor-blading have a great tendency to warp and wrinkle when fired. This has been a severe problem with all samples made thus far. Two firing techniques — batch-firing and continuous-firing — have been explored. Batch-firing is the conventional ceramic firing process. The green material is placed between setter pieces in a firing box and the firing box is placed in a standard fire brick kiln. The continuous-firing process used a special kiln containing a long platinum muffle. A continuous platinum belt passes through the muffle and is advanced slowly by an electric motor. The green ceramic is placed on the platinum belt outside the furnace and is carried through the muffle by the moving belt.

Initial experiments with doctor-bladed materials were done on 73/27-7-2Nb ferroelectric ceramics. Early batch-fired samples of 73/27-7-2Nb material were badly warped and wrinkled, but, nevertheless, it was possible to make

some electrical measurements. These measurements show that one of the five 73/27-7-2Nb samples tested gave performance equivalent to that of conventionally-fabricated 73/27-7-2Nb material.

The next effort was done with an available piezoelectric composition, PZT-5H, to develop skill in blading and to try different firing techniques. Bladed samples of this material were continuous-fired under varying conditions. The best results yielded high-quality flat strips of excellent appearance, 2-in. wide and as long as 8 in. after firing.

When it became apparent from the compositional studies that 50/50-14-2Nb material represented the best compromise choice for transchargers to be used in a display, a large batch of 50/50-14-2Nb powder was prepared and all doctor-blading experiments thereafter have used this material. It was substantially the same as PZT-5H in the way it behaved in blading, and no special problems were found. However, great difficulties were encountered in firing these sheets. Attempts were made with both the batch-firing and continuous-firing techniques. In both cases there was a strong tendency toward severe warpage.

A systematic study showed that for this composition, shrinkage occurred more abruptly than for most other normal $Pb(Zr,Ti,Sn)O_3$ compositions. There seemed to be a step in shrinkage and density near 1240°C. This was strikingly illustrated by the observation of both opaque, yellow areas and shrunken translucent amber areas in the same sheet. Samples fired at temperatures just under 1240°C were flat but immature. Samples fired at temperatures above this were mature but wrinkled.

Some experimentation was done on improving the firing schedule for batch-fired pieces. In some trials, a very slow rise through the 1230° to 1260°C temperature range was tried, followed by a subsequent rise to 1320°C or 1340°C and a soak period of 1/2 to 1-1/2 hours at the peak temperature. This seemed to be beneficial for flatness but favored the undesired adhesion of sheets.

All in all, the batch-firing process can probably be perfected but it will require further experimentation. The key problem is to find the right setter material and the right firing schedule to eliminate warping and sticking while achieving maturity of the ceramic. The continuous-firing process also looks promising, but it too requires further experimentation.

Detailed electrical measurements have been made on five batch-fired samples of 50/50-14-2Nb doctor-bladed ceramic material. The measurements made included life tests of 1000-hour duration. Although the samples had been fired at different temperatures for varying periods of time and had different thicknesses, there were only small differences in the properties; e.g., E_c varied from 5 to 5.7 kV/cm, P_r from 27 to 30.5 $\mu coul/cm^2$, P_s from 31.8 to 35.7 $\mu coul/cm^2$, and $S = P_r/P_s$ from 0.84 to 0.86.

A comparison was made between the properties of the best doctor-bladed sample and the lapped and polished samples of the same composition and the same thickness. Results show that the doctor-bladed samples have a considerably superior performance to the lapped samples, in that their E_c is smaller,

and, P_r, P_s, and $S = P_r/P_s$ are higher. These results have been included in Table I to permit comparison with lapped and polished 50/50-14-2Nb samples. It can be seen that the performance of the doctor-bladed sample is, in fact, only slightly inferior to a polished sample. This might be expected, since the doctor-blading produces a very smooth surface. Figures 18, 19, and 20 show E_c, P_s and P_r, and S, respectively, as functions of time for a doctor-bladed 50/50-14-2Nb sample. Neglecting the initial decay which occurs during the first few hours of operation, the life performance of the doctor-bladed material is comparable to that obtained with conventionally fabricated 50/50-14-2Nb material.

Although doctor-blading promises ultimately to be the best fabrication technique for ceramic ferroelectric transchargers, further research is necessary before doctor-bladed transchargers can be incorporated into display models. Therefore, conventional dry-pressed 50/50-14-2Nb material was ordered from Clevite in sufficient quantity for the experimental models described in Section II-G.

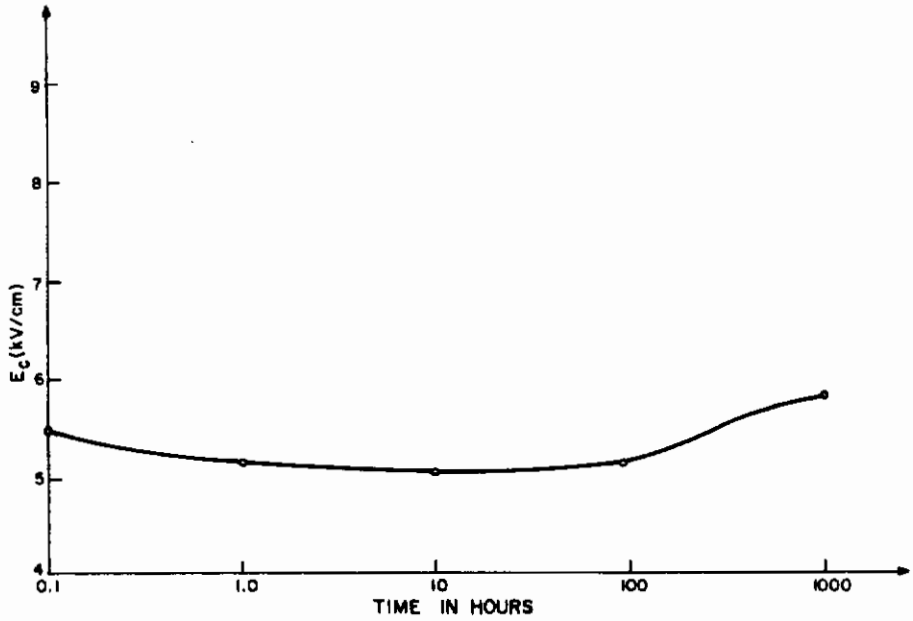


Figure 18. E_c vs. Time for Doctor-Bladed $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$.

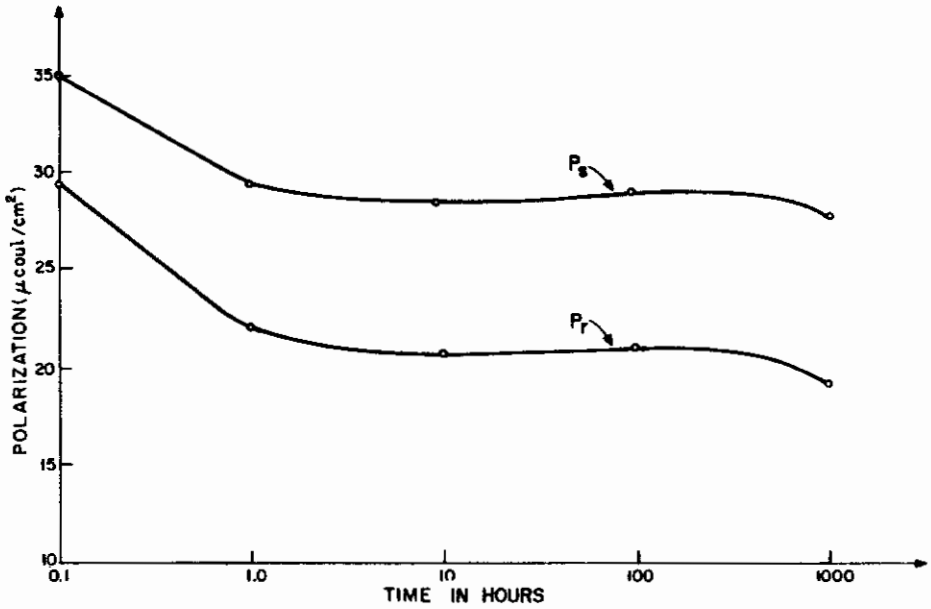


Figure 19. P_s and P_r vs Time for Doctor-Bladed $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$.

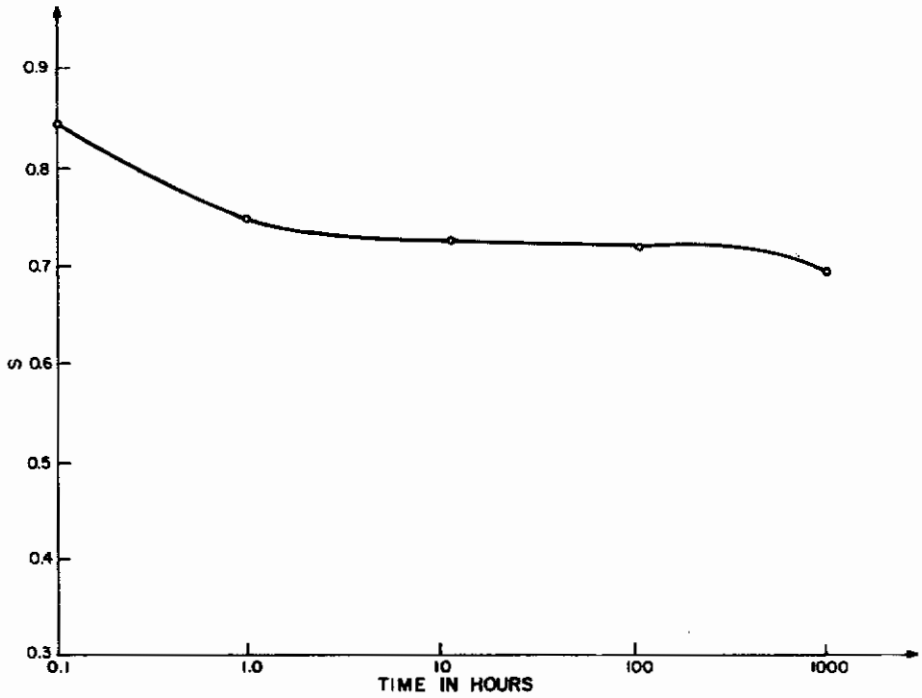


Figure 20. S vs Time for Doctor-Bladed $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$.

C. ELECTROLUMINESCENT CELLS

The program did not include research on electroluminescent cells. However, a variety of cells was obtained from RCA Lancaster* for evaluation and for use in display circuit experiments. The cells all had a nominal brightness of 10 ft-L when operated from a 400-Hz sine-wave source. The cells were made with three voltage ratings (400-Hz rms voltage required to produce 10 ft-L): 50 V, 125 V, and 250 V. Cell areas ranged from 0.01 in.^{2} to 0.25 in.^{2}

Display panel circuit experiments (see Section II-D) indicated that best performance was obtained with the 50-V cells. Figures 21 and 22 show brightness vs frequency and brightness vs voltage characteristics, respectively, for these cells. Life tests conducted at RCA Lancaster show that these electroluminescent cells have a half-life** of approximately 750 hours when operated at 50-V rms, 400 Hz.

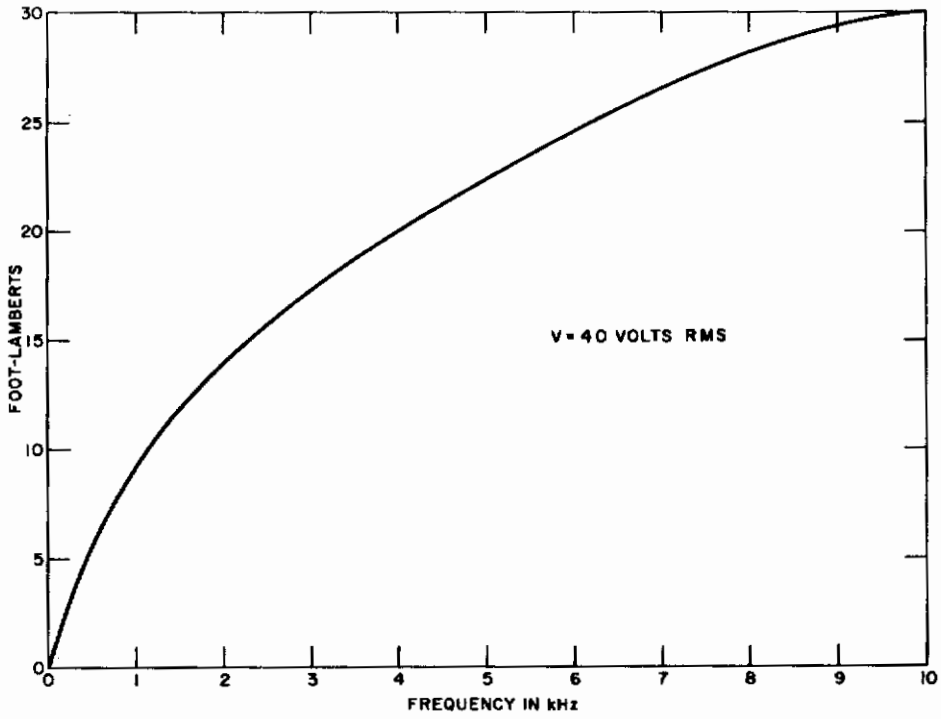


Figure 21. Electroluminescent Cell Brightness vs Frequency.

* RCA Electronic Components and Devices, Special Electronic Components Division, Lancaster, Pa.

** The half-life of an electroluminescent cell is defined as the time required for the brightness to diminish to one half of its initial value under continuous excitation.

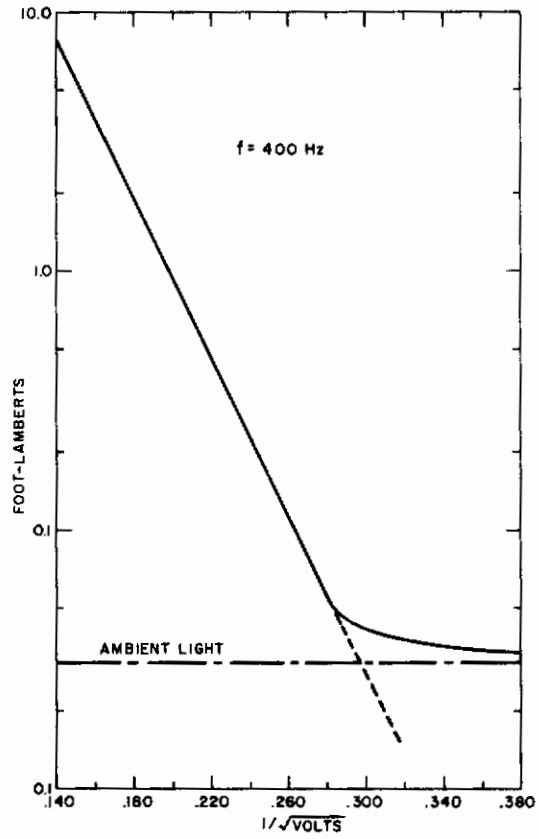


Figure 22. Log Brightness vs $1/\sqrt{V}$.

Once the 50-V rating had been chosen on the basis of the circuit experiments, RCA Lancaster fabricated 50-V panels for use in the experimental models (see Section II-G). The panels were made on glass substrates with semitransparent TIC* front electrodes. For the 120-element and 36-element panels a separate TIC electrode was used for each horizontal row of the panel. The electroluminescent powder in a high dielectric resin (HDR) binder was then applied by spraying or doctor-blading. Aluminum back electrodes were applied by vacuum evaporation and were structured to define the elements of the panel. Gold-plated female connectors were then pressure-bonded with indium to each of the back electrodes and to the TIC electrodes, and the entire panel was then encapsulated in epoxy resin to provide a moisture seal.

Some difficulty has been experienced with the bond between the pin and the aluminum back electrode. The pressure that may be used is limited by the strength of the back electrode and the electroluminescent layer, and, consequently, a good bond is not always obtained. A number of these bonds have failed within the first few hours of operation. It is clear that a better technique will have to be developed in the future.

* Fired-on tin oxide.

D. DISPLAY PANEL CIRCUITRY

The balanced transcharger circuit shown in Figure 1 and first developed[2] under Contract No. AF33(657)8725 formed the basis for the present investigation. The principal shortcoming of this circuit is the lack of adequate contrast. It has been shown[2] that, for this circuit, if the electroluminescent cell characteristic is approximated by

$$B = AV^{\alpha}$$

where B = brightness
V = voltage
A and α are constants

the contrast C^* for a transcharger-controlled electroluminescent display is given by

$$C^* \simeq \left(\frac{2}{1-S}\right)^{\alpha}$$

where S = ferroelectric squareness.

Since it appears from the compositional studies that an S greater than 0.75 is not likely to be achieved with materials that are otherwise satisfactory, it is imperative that other means be found to improve the contrast.

Two potential means for achieving an improvement were investigated[3] under Contract No. AF33(615)1193. The first technique involves increasing the exponent α in the expression above either by tailoring the characteristic of the electroluminescent cell or by including a nonlinear resistor in series with the electroluminescent cell. Experiments with this technique showed that a considerable improvement in performance can be obtained. The improvement, however, is obtained at the expense of increased power dissipation and considerably tighter component tolerances.

The second means proposed to improve the contrast is to substantially cancel the undesired signal coupled through a blocked transcharger because of poor squareness in the hysteresis loop of the ferroelectric by capacitively coupling an out-of-phase signal to the electroluminescent cell. Initial experiments demonstrated that a contrast improvement of at least an order of magnitude could be obtained with only a slight loss in brightness.

The initial experimental success with this technique prompted a more detailed investigation; the experiments led to the invention of a new circuit, known as the doubly balanced transcharger, which gives superior performance.

1. Doubly Balanced Transcharger

The doubly balanced transcharger circuit is shown in Figure 23; operation is as follows: Center-tapped sine-wave generator A_1 and ferroelectrics FE_1, FE_2, FE_3, and FE_4 constitute a balanced bridge with the electroluminescent cell EL connected between the points of balance. Generators G_1 and G_2 are the

row and column pulse generators, respectively (consider them inactive for the present), and battery E keeps diode D reverse-biased. Suppose that initially ferroelectrics FE_1, FE_2, FE_3, and FE_4 are all polarized upward; they will thus switch in unison under the signal applied by generator A_1; since the bridge is balanced, no voltage appears across the electroluminescent cell and it remains dark. To address the cell, generator A_1 is disabled momentarily and generators G_1 and G_2 are activated in coincidence. The row generator G_1 produces a positive pulse and the column generator G_2 produces a negative pulse. Neither generator alone has sufficient amplitude to overcome the back-bias on diode D; in fact, G_1 has a fixed amplitude just equal to E while G_2 is amplitude-modulated by the video signal. G_1 and G_2 in coincidence forward-bias the diode D and charge is drained from point X to ground through D and the internal impedance of G_2 switching ferroelectric FE_3 or FE_4. Thus FE_3 and FE_4 will be left polarized oppositely. When A_1 is energized again, FE_1 and FE_2 (which were not disturbed by the pulses from G_1 and G_2) constitute an unblocked pair and their "impedance" is low while FE_3 and FE_4 now constitute a blocked pair and their "impedance" is high. The bridge is thus unbalanced and a voltage is impressed on the electroluminescent cell which lights.

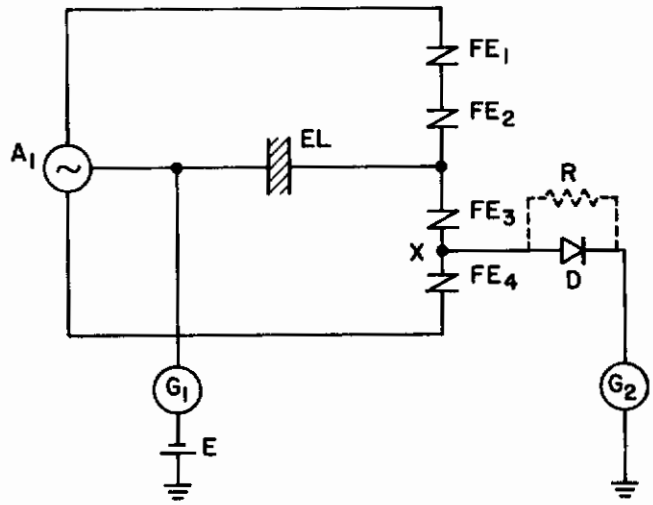


Figure 23. Doubly Balanced Transcharger Circuit.

The voltage on the cell, and hence its brightness, depends on the degree of unbalance of the bridge which in turn depends on the degree to which FE_3 and FE_4 have been blocked. This depends on the charge drained from point X and hence on the amplitude of the pulse from G_2. Thus partial switching for a halftone display is possible. FE_3 and FE_4 do not remain blocked indefinitely but rather, unblock slowly as charge returns to point X via the reverse leakage current of diode D. By controlling this leakage so that FE_3 and FE_4 return to their unblocked state in one frame time, the need for a reset pulse is eliminated.

The circuit of Figure 23 was constructed and tested experimentally. 50/50-14-2Nb ceramic ferroelectrics were used for FE_1, FE_2, FE_3, and FE_4; the 1N484 diode D was paralleled by a 22-MΩ resistor to achieve the desired reverse leakage. Brightness approaching 10 ft-L was obtained with a contrast ratio

too high to measure easily (certainly in excess of 100 to 1). The excellent performance of this circuit and the advantage of not needing a reset pulse make it especially attractive for use in a display matrix. The drawback, of course, is the diode which, from the point of view of fabrication, adds complexity.

Figure 24 illustrates how the circuit of Figure 23 is incorporated in a display matrix; for simplicity, only two rows of three elements each are shown. Generator A is a common sine-wave source for all rows; the required balanced source is obtained at each row by using a center-tapped transformer. Generators G_{11} and G_{12} are the row generators and generators G_{21}, G_{22}, and G_{23} are the column generators. As can be seen, the connections are similar to those for the conventional balanced transcharger of Figure 1.

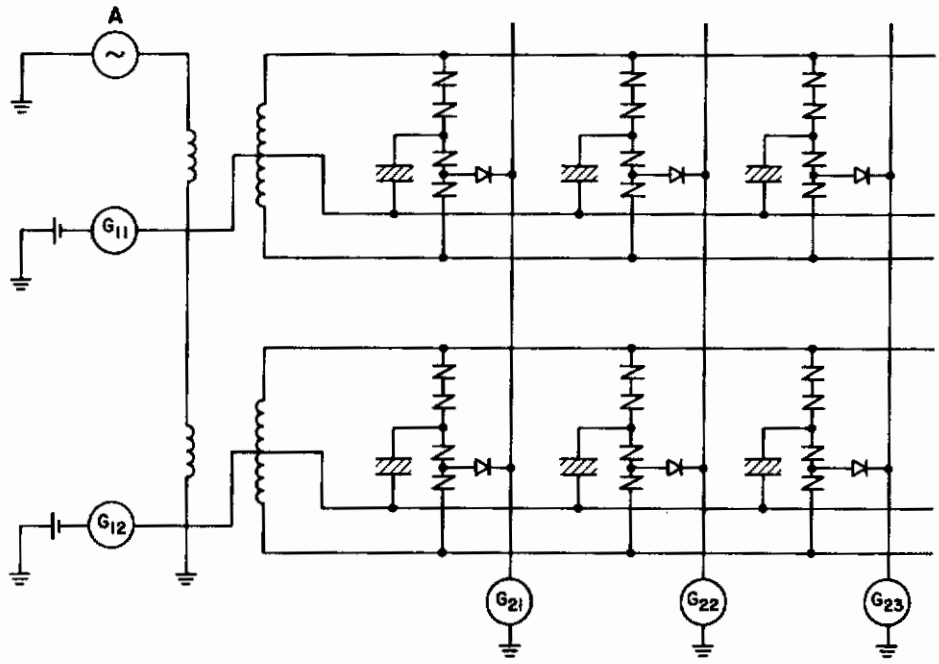


Figure 24. Illustrating the Circuit of Figure 23 in a Matrix.

Attempts to replace the diode D with a ferroelectric capacitor have been only partially successful. To prevent severe unblocking by the sine-wave signal, it has been necessary to use two or three ferroelectric capacitors in series to replace D. Under these conditions operation has been achieved with a brightness of about 3 ft-L and excellent contrast.

Considerable effort has been directed to understanding the reasons for poorer performance when a ferroelectric capacitor is used instead of a diode in the column bus connection to the circuit. The basic circuit investigated is shown in Figure 25, with element X being either a diode or a ferroelectric capacitor. A single pulse generator G was used for experimental convenience. Operation of the circuit has been analyzed as follows:

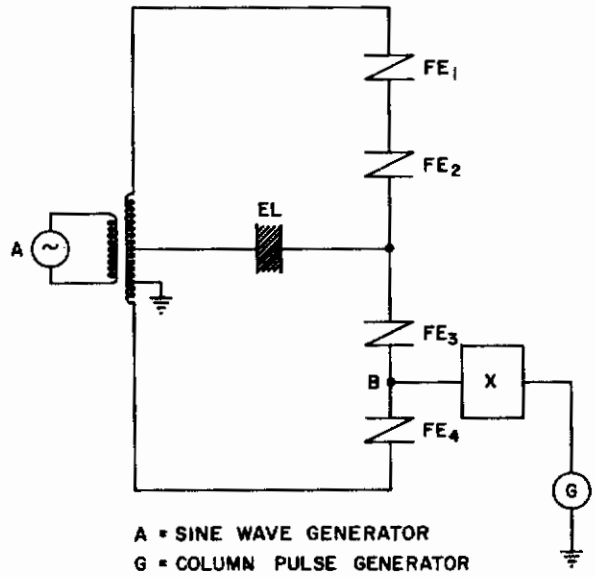


Figure 25. Experimental Transcharger Circuit.

When a ferroelectric capacitor is used at X, the operation of ferroelectrics FE_3 and FE_4 is as illustrated in Figure 26(a). FE_3 and FE_4 are shown in the blocked state, i.e., the "on" state for the electroluminescent cell. Note that the initial operating point is on the charge axis (V = 0). To prevent spurious unblocking of the pair FE_3 and FE_4, the voltage from generator A must be limited so that the peak-to-peak voltage excursion applied to FE_3 and FE_4 does not exceed approximately $2V_c$. If the AC voltage is so limited, then ferroelectrics FE_1 and FE_2, which are an unblocked pair, will operate on minor loops as shown in Figure 26(a) and the net current delivered to the electroluminescent cell will be relatively small. Consequently, the cell brightness will be relatively low. When a diode is used at point X in the circuit of Figure 25, the operation is as illustrated in Figure 26(b). Here again, ferroelectrics FE_3 and FE_4 are shown in the blocked state. Note that the initial operating points are displaced considerably from the charge axis ($V = \pm V_1$). The presence of the diode permits this displacement of the operating points. In effect, excess charge has been delivered to node B and cannot return through the reverse-biased diode at X. Consequently, the AC generator A can drive FE_3 and FE_4 with a peak-to-peak voltage well in excess of $2V_c$ without causing spurious unblocking. This larger voltage will also drive FE_1 and FE_2 over their full loops as shown in Figure 26(b) and, consequently, deliver a maximum current to the electroluminescent cell producing high brightness.

The above analysis is difficult to verify experimentally in the case when X is a ferroelectric capacitor, since it is not then possible to monitor the voltage at point B. However, measurements of the currents in the various branches of the circuit tend to confirm the above explanation. Therefore, it appears that the diode is essential for high-performance (high brightness and high contrast) operation of the circuit.

From a fabrication point of view, this is a severe disadvantage, since a diode will be required for each element location in the display. Not only

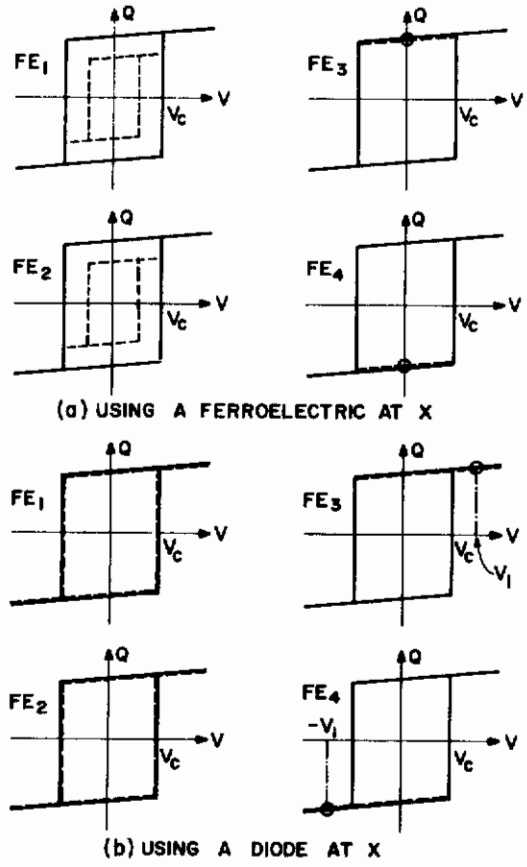


Figure 26. Illustrating the Operation of the Circuit of Figure 25. Operating Paths Shown Dotted.

does this introduce an additional technology to the panel fabrication, but will also add significantly to the ultimate cost of a display panel. The lower capacitance of the diode compared with the ferroelectric capacitor is, however, a definite advantage as far as addressing the display is concerned. The use of a diode will substantially reduce the capacitance "seen" by the column pulse driver circuitry and may thus permit a significant simplification of the required addressing circuitry. It is clear that further research efforts are necessary to seek possible means of eliminating the diode from the circuit without destroying the advantages which accrue from its presence. However, even if the diode were essential, present advances in integrated semiconductor technology may soon permit integrated fabrication of the necessary diodes in a geometry suitable for incorporation into a display panel.

Despite its shortcomings the circuit of Figure 23 is at present the best performing transcharger display circuit and was therefore chosen for use in the experimental models constructed under this Contract. Following the initial success with this circuit, a detailed investigation was undertaken to confirm the decision to use it in the experimental models and to determine the optimum operating conditions. A series of experiments were made on the circuit of Figure 23 with various electroluminescent cells of different voltage rating,

with various diode-resistor combinations, with various EL/FE area ratios, and with various driving signals. In all cases, 50/50-14-2Nb ferroelectric material was used. To provide the signals required from generators A_1, G_1, and G_2 in Figure 23, either standard laboratory signal generators or the electronic circuitry constructed for the models (see Appendices) were used.

Electroluminescent cells with nominal voltage ratings of 50, 125, and 250 V were tested in the circuit. As was expected, the highest brightness was obtained with the 50-V cells, but the light output was not proportionately lower for the 125-V and 250-V cells. This seemingly surprising result is easily explained when it is remembered that the transcharger is a charge-limited device that delivers a fixed charge to the load in any case. Since the higher voltage electroluminescent cells are thicker and therefore have lower capacitance, the same delivered charge results in a higher voltage across these electroluminescent cells ($V = q/C$) which results in nearly the same brightness obtained from the lower voltage cells. Of course, the voltage delivered from generator A_1 must be large enough in all cases to support the total drop in the circuit. Since the 50-V electroluminescent cells provided the highest brightness and permitted a lower operating voltage for generator A_1, these cells were chosen for the experimental models.

The requirements for the diode are not critical: the breakdown voltage must be 300 V or more, the front-to-back ratio must be greater than 10^4, and the reverse saturation current should be less than 1 μA. The 1N488 diode easily satisfies these requirements and was therefore chosen for use in the models. With no resistor paralleling the diode, the self-resetting time of the circuit, determined only by the I_{co} of the diode, was approximately two minutes. By paralleling the diode with 22 MΩ the resetting time is reduced such that the current through the electroluminescent cell has decreased by one-third in one frame time (33 msec). This proved to be an optimum choice for maximum brightness without perceptible smear of moving images.

To choose the optimum addressing pulse width for the circuit of Figure 23, the data of Figure 27 were obtained. Since generators G_1 and G_2 are series-aiding, only generator G_2 was used for the tests. The bias E was set to 50 V. For pulse amplitudes of less than 60 V, the electroluminescent cell brightness was less than 0.2 ft-L for all pulse widths. As can be seen from Figure 27, at all pulse voltages, the brightness is independent of pulse width for pulse widths greater than 30 μsec. It was therefore decided to use pulse widths between 30 and 50 μsec in the experimental models (see Section II-G). It should be noted that a display could be designed on the basis of width-modulating the addressing pulse to convey the video information. Although exhaustive tests were not made, it is felt that this mode of operation would suffer more from tolerance problems than the amplitude-modulation scheme emphasized here.

To determine the optimum EL/FE area ratio a number of transchargers were prepared with different electrode areas. These were 46 x 46 mils, 52 x 52 mils and 57 x 57 mils. The electroluminescent cell used was in all cases a nominal 50-V cell, 0.2 x 0.2 in. The resulting EL/FE area ratios were thus 18.9, 14.8, and 12.5, respectively. To provide the signals required from generators A_1, G_1, and G_2 in Figure 23, the electronic circuitry used for the auxiliary model to demonstrate high resolution (see Appendix III) was used.

Generator A_1 provides a 900-Hz sine wave of adjustable amplitude; the sine wave is interrupted for 250 μsec at a 30-Hz rate to allow addressing. During the 250 μsec that A_1 is blanked, G_1 provides a positive 30-μsec pulse of adjustable amplitude and, coincident with the pulse from G_1, G_2 provides a negative 30-μsec pulse of adjustable amplitude. G_2 also provides negative 30-μsec disturb pulses at a 12.5-kHz rate during the interval when A_1 is not blanked. The DC bias E was adjustable to 125 V.

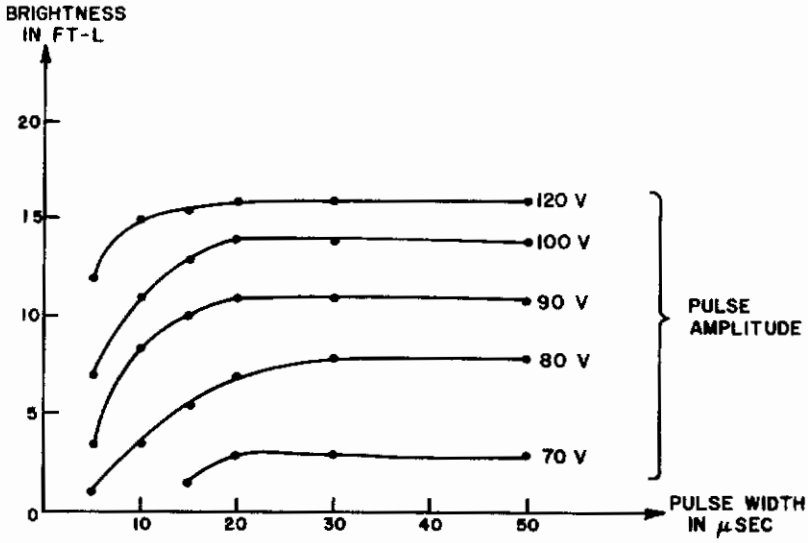


Figure 27. Brightness vs Addressing Pulse Width for Various Addressing Pulse Amplitudes.

The 900-Hz sine-wave generator A_1 was set to 350 V rms for all tests. With G_1 and the coincident pulse from G_2 turned off, full 60-V disturb pulses were applied and the bias E was adjusted to the point where the electroluminescent cells were just extinguished. Next, the amplitude of G_1 was increased to just below the value at which the cells start to light. Then the brightness was measured as a function of the amplitude of the coincident pulse from G_2. The results are plotted in Figure 28 from which it can be seen that the "off" brightness is always 0 ft-L and that the maximum "on" brightness obtained with a pulse amplitude of 60 V increases from 3.5 ft-L for an EL/FE area ratio of 18.9 to 11 ft-L for an area ratio of 12.5. The slope of the transfer characteristic measured at a pulse amplitude of 30 V also increases from 0.1 ft-L/V for an area ratio of 18.9 to 0.8 ft-L/V for an area ratio of 12.5.

Although high brightness is desired, it is also desired, in a halftone display, to have a transfer characteristic with a small slope to minimize the sensitivity to component tolerances. Since the data of Figure 28 show that the transfer slope increases more rapidly than the "on" brightness with increasing transcharger area, it is necessary to make a compromise when designing a particular display. Since gray-scale capability was of secondary importance for the main 120-element model, it was decided to use an EL/FE area ratio of 12.5 to achieve high brightness. This ratio yields a maximum "on" brightness of 11 ft-L with a transfer slope at 30 V of 0.8 ft-L/V. For the auxiliary model to show high resolution an EL/FE area ratio of 14.8 was chosen to obtain

better gray-scale uniformity at the expense of some brightness. This area ratio yields a maximum "on" brightness of 7.5 ft-L and a transfer slope at 30 V of 0.3 ft-L/V.

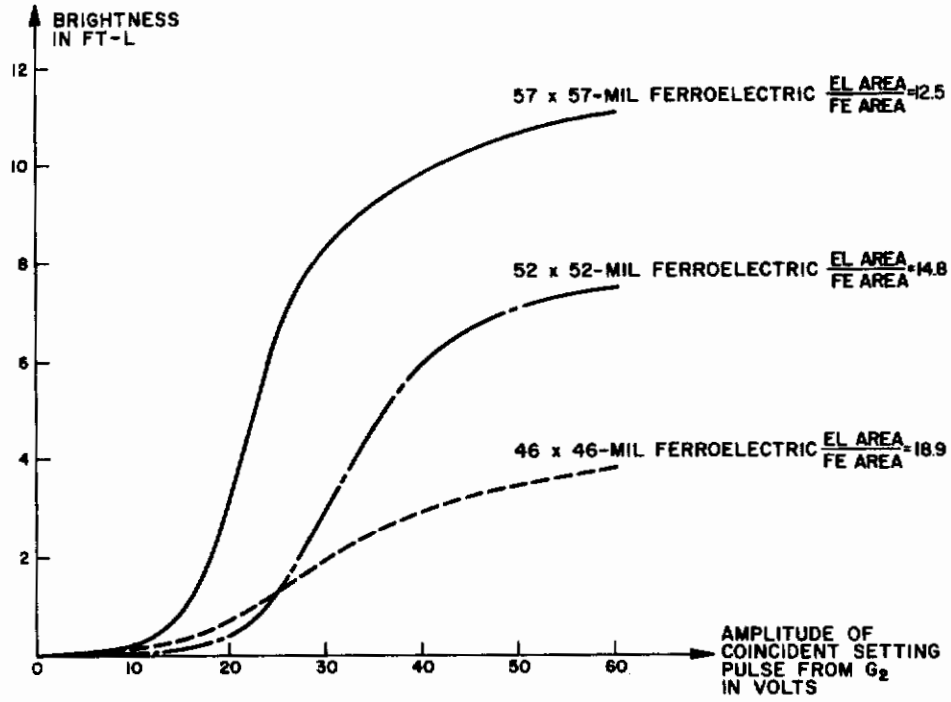


Figure 28. Brightness vs Setting Pulse Amplitude for Three Different Transcharger Areas (with disturb pulses).

To test for crosstalk in a display, the disturb pulses were turned off and, without changing any other parameters, the brightness was again obtained as a function of the amplitude of the coincident pulse from G_2. The result for the 52 x 52-mil transcharger is plotted in Figure 29. Except at very low brightnesses (where measurement accuracy is poor), the difference is less than 10 percent which is not discernible by eye.

Some measurements were made on the 52 x 52-mil transcharger to determine the extent of the tolerance problem. The complete transfer characteristics were measured against a standard electroluminescent cell for three supposedly identical 52 x 52-mil transchargers. Each characteristic was measured for the two extreme cases of no disturb pulses present and of the disturb pulses present in maximum number and amplitude. The total variation among the six measured characteristics reached its maximum value of $\pm$ 1.2 ft-L near the mid-region (30 V) of the transfer characteristic. By comparison, the deviation from the maximum "on" brightness of 7.5 ft-L was only $\pm$ 0.5 ft-L. Part of this variation was due to small differences in the dimensions and, hence, the areas of the ferroelectric cells which comprise the transchargers. These differences were due to differential rates of etching in the copper used for making the evaporation masks. In the future, closer control will be needed on the mask manufacture. Clearly, the tolerance studies must be extended to determine the statistical

variation of both the transcharger and electroluminescent characteristics over a much larger number of samples. Such studies will be paramount in determining the performance of a large display.

Most of the tests discussed above were made with a sinusoidal excitation signal at a frequency of approximately 1 kHz. When it became apparent from the scanning and driving circuit studies (see Section II-F) that the system design would be greatly simplified by using a continuously gated excitation signal, tests were made on the circuit of Figure 23 using such signals.

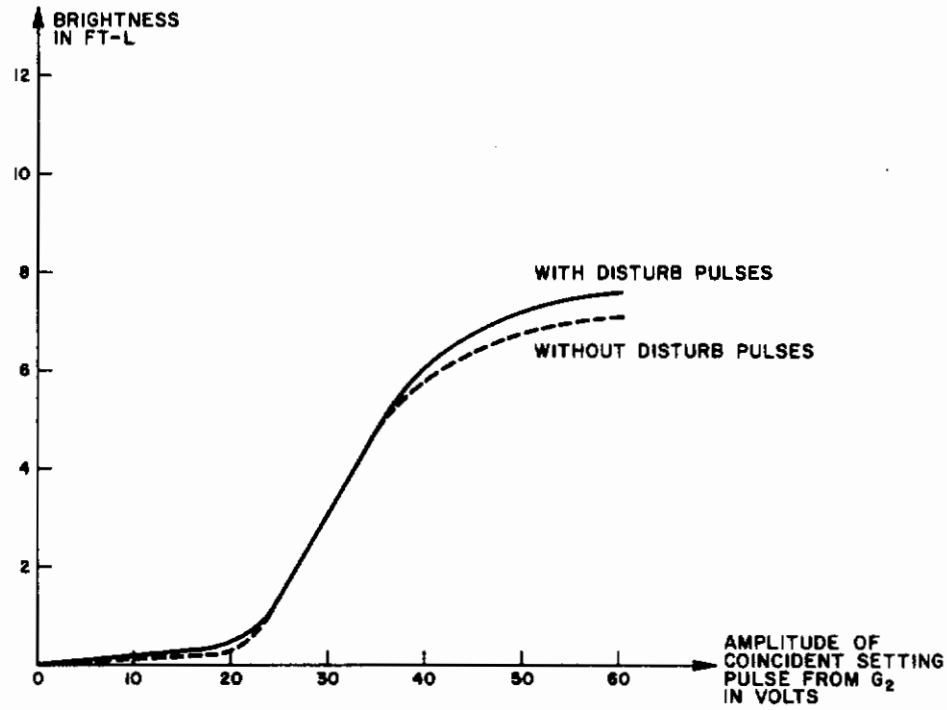


Figure 29. Brightness vs Setting Pulse Amplitude for 52 x 52-mil Transcharger with and without Disturb Pulses.

Figure 30 shows the excitation waveforms used for the tests. Figure 30(a) is the conventional sine-wave excitation signal interrupted briefly each frame time to allow addressing. Figure 30(b) shows the continuously gated sine wave. Here, single cycles of a 2-kHz sine wave alternate with off periods of 500 μsec ($\frac{1}{2\ \text{kHz}}$). The cell thus "sees" 1000 cycles of sine wave each second, and yet half of the total time is available for addressing. Since electroluminescent cell brightness and life are approximately dependent only on the total number of cycles of excitation, one would expect essentially the same performance from the excitation signals of Figures 30(a) and 30(b). Or, to look at it in another way, the 2-kHz sinusoid of Figure 30(b) produces a brightness of about 1.6 times that of the 1-kHz sinusoid of Figure 30(a) (see Figure 21 for electroluminescent cell brightness vs. frequency), but since the 2-kHz signal is present for only 50 percent of the time, the actual brightness for the waveform of Figure 30(b) is approximately 0.8 of the brightness for the waveform of Figure 30(a). Experimental measurements have confirmed this relationship.

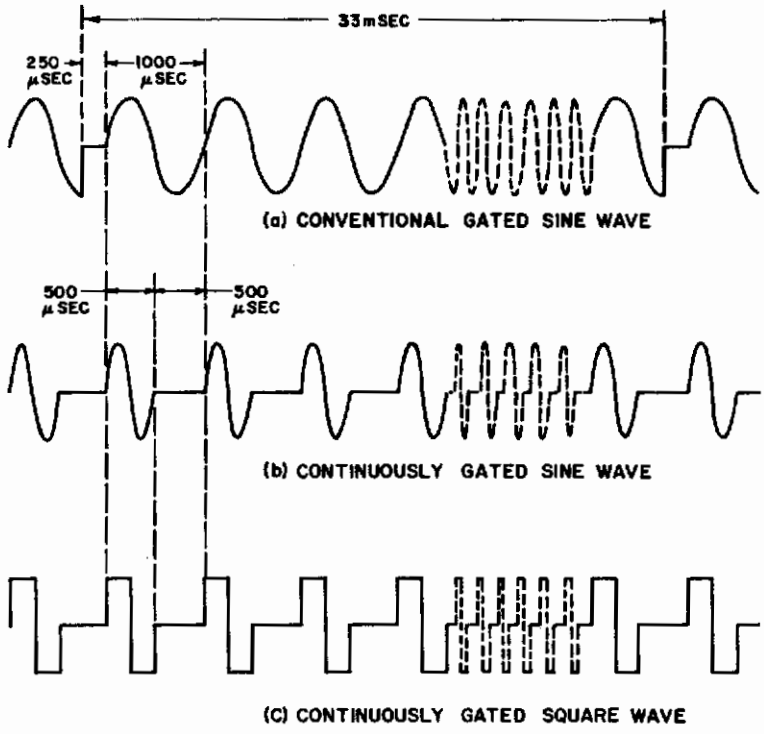


Figure 30. Excitation Waveforms.

The waveform of Figure 30(c) is similar to that of Figure 30(b) except that the signal is a square wave rather than a sine wave. From a practical standpoint, the square wave is preferred since it is easier to generate and can be amplified with greater efficiency. Also, since the ratio of rms to peak value is higher for a square wave than it is for a sine wave one would expect higher brightness for a square wave than for a sine wave of the same peak value. This has also been confirmed experimentally. Figure 31 shows the brightness vs set pulse amplitude transfer characteristics for the circuit of Figure 23 for three different peak-to-peak values of the excitation waveforms of Figures 30(a) and 30(c). As can be seen, for the same peak-to-peak voltage, the waveform of Figure 30(c) gives approximately 50 percent more brightness than the waveform of Figure 30(a). The waveform of Figure 30(c), therefore, not only simplifies the system design, but also, for a given peak-to-peak excitation, increases the brightness about 50 percent; or, alternately, for a given brightness permits a lower peak-to-peak excitation signal to be used. The excitation waveform of Figure 30(c) was chosen for the main model described in Section II-G.

2. Asymmetrical Doubly Balanced Transcharger

Experimentation with the circuit of Figure 23 has led to the slightly different version shown in Figure 32. In this circuit, the sine-wave signal is supplied via transformer T which has its secondary tapped such that $N_1 = N_2 = N_3$. This arrangement halves the voltage applied to the upper half of the circuit and allows one ferroelectric capacitor to be eliminated from this

part of the circuit and yet maintain a balanced-bridge configuration. This modification has been tested experimentally, and performance nearly equivalent to that of the original circuit was achieved. The new arrangement not only simplifies the circuit by eliminating one ferroelectric capacitor, but also reduces the power consumption by about 25 percent.

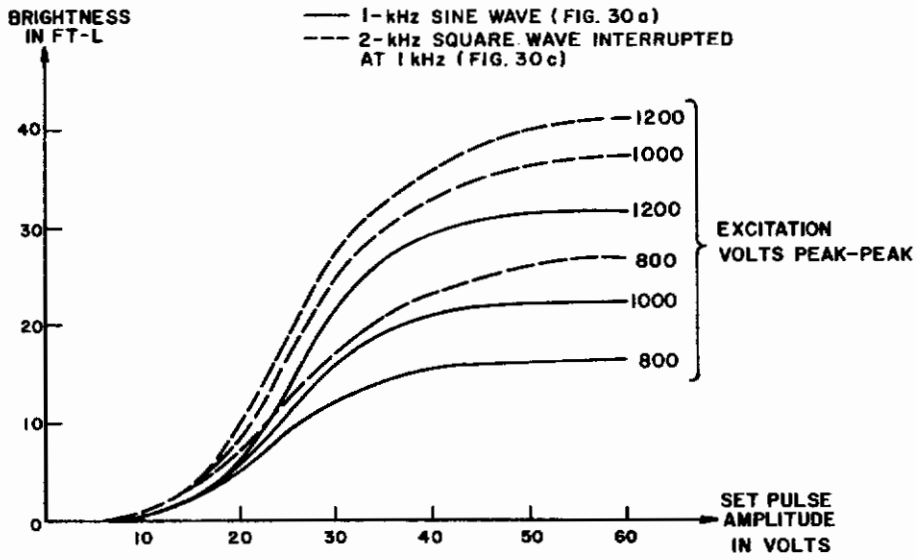


Figure 31. Brightness vs Set Pulse Amplitude For Various Amplitudes of Two Different Excitation Waveforms.

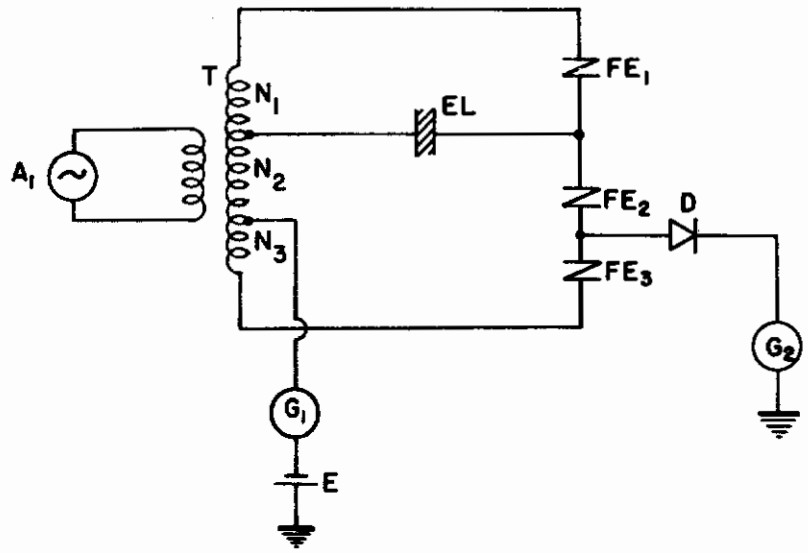
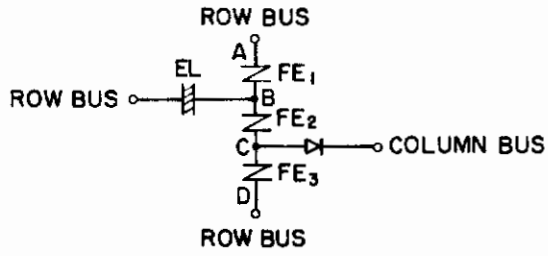


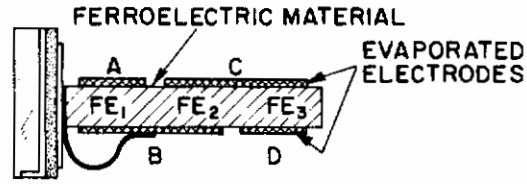
Figure 32. Modified Transcharger Circuit.

The second modification evident in Figure 32 is the connection of the row generator G_1 to a tap on the transformer lower than the tap to which the electroluminescent cell is connected. This makes the lower half of the circuit more nearly a balanced bridge and permits a substantial reduction in the bias voltage E. Otherwise, operation is identical to the original circuit. Not only is the circuit of Figure 32 more economical of power, but it is also topologically more suitable for integrated fabrication. Figure 33 illustrates how the circuit of Figure 32 may be fabricated.

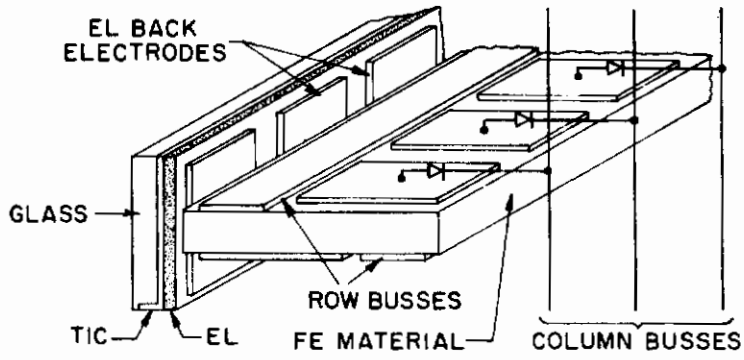
Although the circuit of Figure 32 is simpler and more economical of power than that of Figure 23, the bridge is not symmetrical and, therefore, the balance conditions are more critical. This means that, in practice, the circuit of Figure 32 will require tighter component tolerances to achieve comparable performance.



(a) BASIC CIRCUIT



(b) INTEGRATED CONSTRUCTION OF FE_1, FE_2, AND FE_3



(c) ONE ROW OF A DISPLAY MATRIX

Figure 33. Method of Fabrication of the Circuit of Figure 32.

The circuits of Figures 23 and 32 achieve their improvements over the circuit of Figure 1 by connecting two additional elements — a generator in series with a ferroelectric capacitor — across the electroluminescent cell. These elements serve to deliver to the electroluminescent cell an out-of-phase current which cancels the current which would otherwise be present due to the relatively poor squareness of the ferroelectric material. An alternate scheme is to connect an element in parallel with the electroluminescent cell which will carry the unwanted current but which will not affect the desired current. What is wanted is an element having a low impedance at low applied voltages and a high impedance at high applied voltages. A ferroelectric capacitor behaves in somewhat this fashion. For applied voltages slightly in excess of the coercive voltage, the ferroelectric switches and current flows; if the voltage is then further increased, little additional current will flow because the ferroelectric is already saturated.

A display circuit based on this scheme is shown in Figure 34. Operation is as follows: Center-tapped generator A supplies a sinusoidal excitation

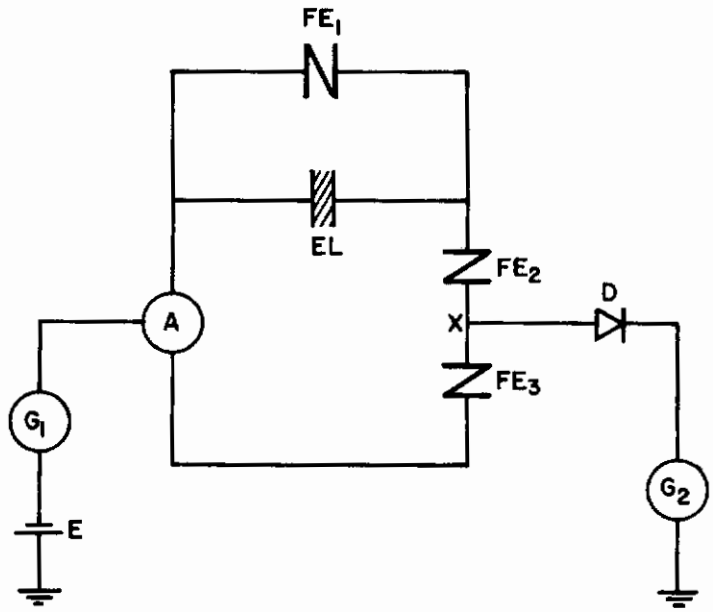


Figure 34. Transcharger Display Circuit.

signal for the circuit. Generators G_1 and G_2 are the row and column pulse generators, respectively (consider them inactive for the present), and battery E keeps diode D reverse-biased. Ferroelectrics FE_2 and FE_3 are identical. Ferroelectric FE_1 has lower polarization and lower coercivity than FE_2 and FE_3. Suppose that initially FE_2 and FE_3 are poled alike (in the unblocked state); they will then switch in unison under the signal applied by generator A supplying a charge Q_U each time they switch. FE_1 will also switch in unison with FE_2 and FE_3, absorbing a charge Q_B. The difference charge Q_U-Q_B will flow to the electroluminescent cell causing it to light. To address the cell, generator A is momentarily disabled, and generators G_1 and G_2 are activated in coincidence. The row generator G_1 produces a positive pulse and the column generator G_2 produces a negative pulse amplitude-modulated by the video signal.

Neither generator alone has sufficient amplitude to overcome the back-bias on diode D, but in coincidence G_1 and G_2 forward-bias the diode and charge is drained from point X to ground through diode D and the internal impedance of generator G_2, switching ferroelectric FE_2 or FE_3. Thus, FE_2 and FE_3 will be left polarized oppositely. When generator A is again energized FE_2 and FE_3 constitute a blocked pair and pass only a small charge Q_B. FE_1 continues to switch, however, and in doing so absorbs this charge Q_B, thus preventing current flow through the electroluminescent cell. Of course, since there must be a voltage drop across FE_1 for it to switch, there will be a voltage drop across the electroluminescent cell and some current will flow through the electroluminescent cell; however, the presence of FE_1 will markedly reduce this current by absorbing most of the charge Q_B.

As with the other circuits, the brightness of the electroluminescent cell depends on the degree to which FE_2 and FE_3 are blocked. This depends on the charge drained from point X and hence on the amplitude of the pulse from G_2. The circuit is self-resetting since FE_2 and FE_3 do not remain blocked indefinitely but rather unblock slowly as charge returns to point X via the reverse leakage current of diode D. Note that the video signal must be inverted since pulses from G_2 make the cell go dark; the relaxed state is with FE_2 and FE_3 unblocked and the cell "on". This is a disadvantage of the circuit, since if video information is removed, the panel will fade to white rather than black.

Figure 35 shows a brightness vs set pulse amplitude transfer characteristic for the circuit of Figure 34. The bias E was 60 V. Since generators G_1 and G_2 are series-aiding, a single generator providing 40-μsec pulses was used for the tests. Generator A provided a 1-kHz sine wave of 425 V rms.

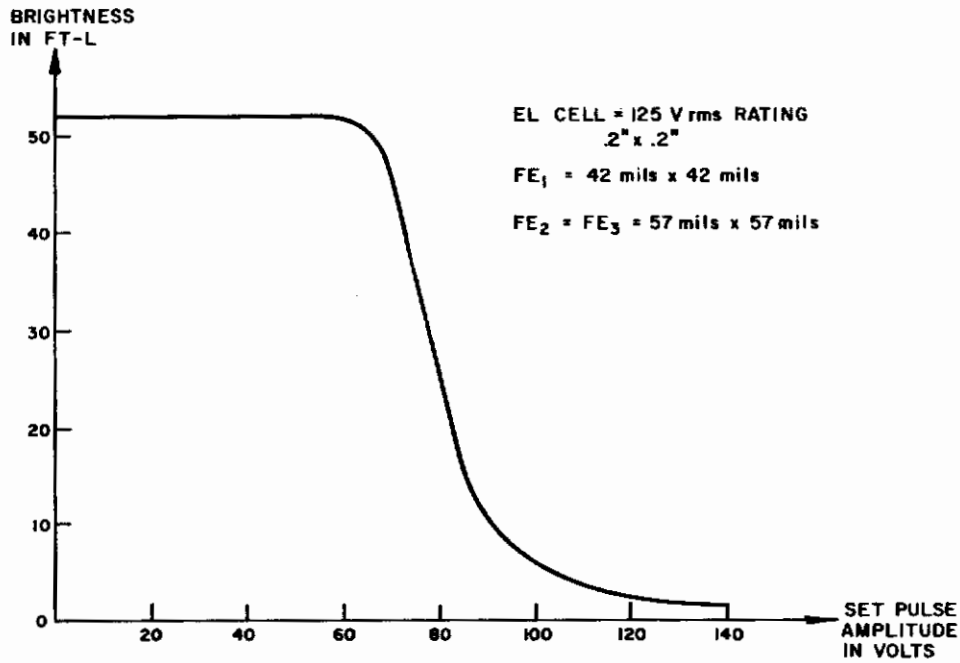


Figure 35. Brightness vs Set Pulse Amplitude Transfer Characteristic for the Circuit of Figure 34.

The invention and study of the circuits of Figures 1, 23, 25, 32, and 34 led to the realization that they are all special cases of the general circuit shown in Figure 36. The circuit of Figure 36 becomes that of Figure 1 if $N_1 = 0$, $d_1 = \infty$, $N_2 = N_3$, $d_2 = d_3$, $a_2 = a_3$, $E = 0$, and the isolating element is a ferroelectric capacitor. The circuit of Figure 23 is obtained if $N_2 = 0$, $N_1 = N_3$, $a_1 = a_2 = a_3$, $d_1 = 2d_2 = 2d_3$ and the isolating element is a diode. The circuits of Figures 25 and 32 are obtained similarly. For the circuit of Figure 34, $N_1 = 0$, $a_1 < a_2 = a_3$, and $d_1 < d_2 = d_3$.

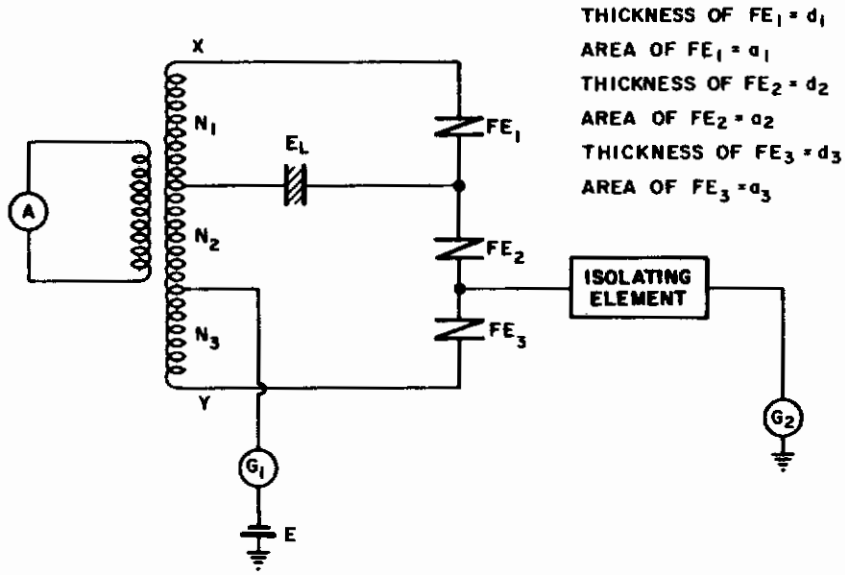


Figure 36. General Transcharger Circuit.

Figure 36 thus represents a whole family of circuits, certain members of which have been rather thoroughly investigated. Since there are many parameters in the circuit of Figure 36, time has not permitted an exhaustive investigation of all possibilities. At first thought, it might appear that, other than the degenerate cases, the only cases of interest would be those in which the bridge is balanced [$N_1/d_1 = (N_2 + N_3)/(d_2 + d_3)$ and $a_1 = a_2 = a_3$]. This would be true if we were dealing with linear elements, but the ferroelectrics and the electroluminescent cell as well are highly nonlinear elements.

It is possible, for example, to achieve good performance with

$$\frac{N_1}{d_1} > \frac{N_2 + N_3}{d_2 + d_3}$$

provided $a_1 < a_2 = a_3$. Figure 37 shows the brightness vs set pulse amplitude transfer characteristic for the circuit of Figure 36 with $N_2 = 0$, $N_1 = N_3$, $E = 50$ V, $d_1 = d_2 = d_3$, a diode isolating element and $a_1 = ka_2 = ka_3$ ($k \leq 1$) for three values of k. For these conditions

$$\frac{N_1}{d_1} = 2\left(\frac{N_2 + N_3}{d_2 + d_3}\right)$$

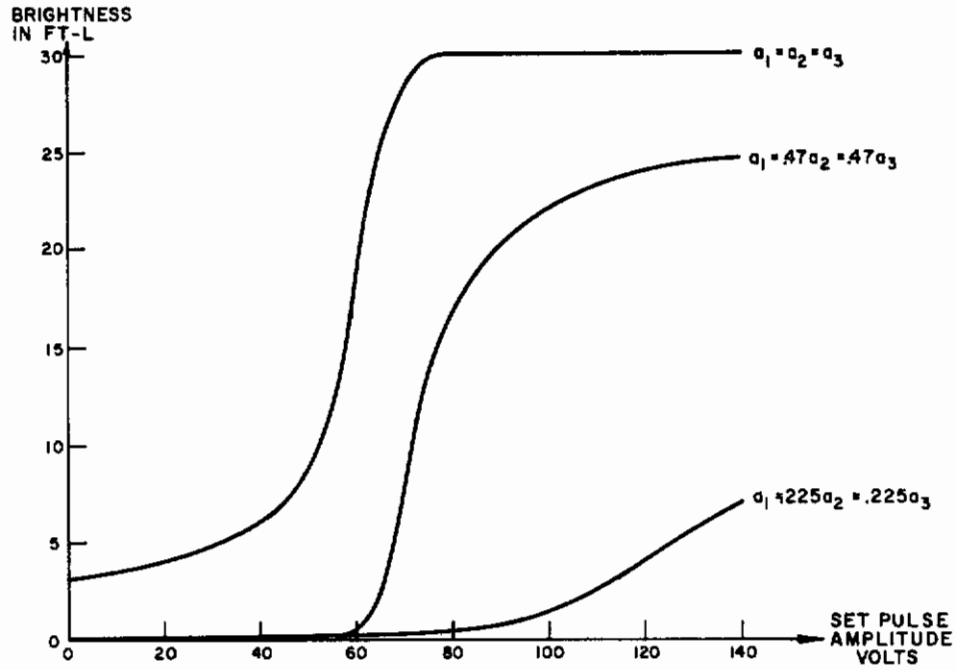


Figure 37. Brightness vs Set Pulse Amplitude for an Unbalanced Version of the Circuit of Figure 36.

The electroluminescent cell was 0.2 x 0.2 in. and had a nominal rating of 50 V and $a_2 = a_3 = 0.009$ in.^{2} Generator A provided a 1-kHz sine wave and the amplitude between points X and Y in Figure 36 was 285 V rms. Since generators G_1 and G_2 are series-aiding a single generator producing 40-μsec pulses was used for the tests.

The data of Figure 37 show that for small values of k, the performance is poor because of low brightness and that for large values of k, the performance is also poor because of poor contrast. Good performance results from intermediate values of k. It appears on the basis of this and other limited data that the best performance is obtained when $k \approx 1/K$ where

$$K = \frac{N_1/d_1}{(N_2 + N_3)/(d_2 + d_3)}$$

or for the case where $N_2 = 0$ and $d_1 = d_2 = d_3$,

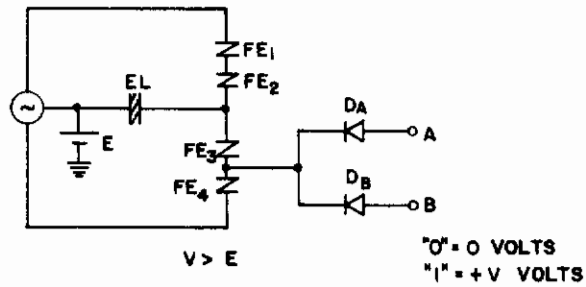
$$K = 2\,\frac{N_1}{N_3}$$

As a part of any future effort, a thorough investigation of the circuit of Figure 36 should be undertaken to determine the optimum circuit parameters. The various circuit parameters should be varied systematically and the circuit behavior as a function of the parameters be thus determined.

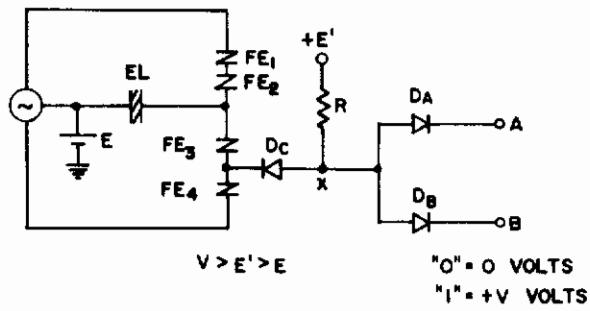
3. Transcharger Circuits with Logic Capability

The basic ferroelectric transcharger control circuit is useful not only for electroluminescent matrix displays, but is equally well suited for other types of electroluminescent displays such as pointers, bar graphs, and alpha-numeric indicators. This is especially true of the transcharger circuits of Figures 23 and 32 which are particularly suited to operation with the logically derived level inputs usually associated with pointers, bar graphs, etc.

Figure 38 illustrates the way in which the transcharger circuit can be modified to include logic capability. Figure 38(a) shows an "OR" gate transcharger; the circuit will be recognized as essentially that of Figure 23 with two input diodes. If both inputs A and B are "0", both diodes will be held back-biased by battery E and FE_3 and FE_4 will be unblocked; thus the cell will be dark. If either A or B or both are "1", one or both of the diodes will be forward-biased, FE_3 and FE_4 will block and the cell will light. If the inputs A and B are levels, the cell will stay lit as long as the input is present and will "go out" (by the unblocking of FE_3 and FE_4 through the reverse leakage of the diodes) when the input is removed.



(a) "OR" GATE TRANSCHARGER

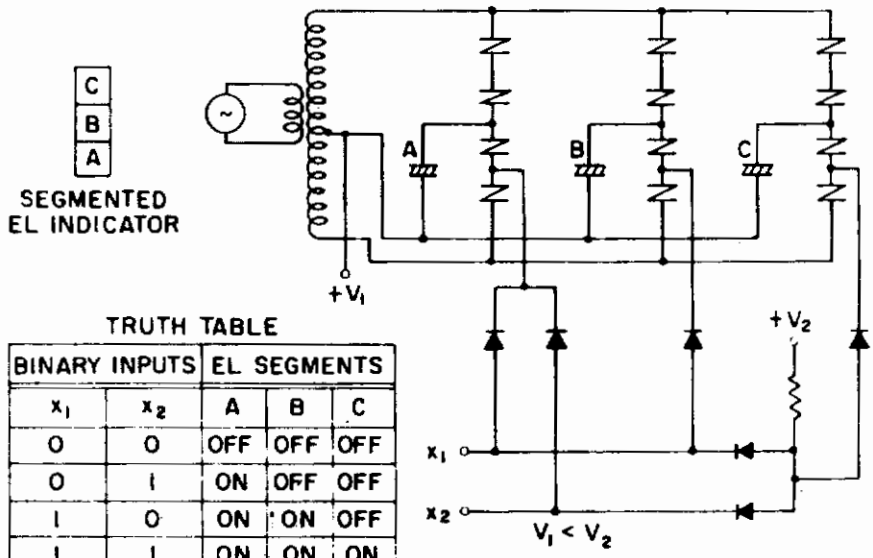


(b) "AND" GATE TRANSCHARGER

Figure 38. Illustrating the Logic Capability of the Transcharger Circuit.

Figure 38(b) shows an "AND" gate transcharger; again, the circuit is basically that of Figure 23. When either or both of the inputs A and B are "0", either or both of the diodes D_A and D_B conduct, and point X is maintained at 0 V. Diode D_C is thus reverse-biased by battery E, FE_3 and FE_4 are unblocked, and the cell is dark. Only when both inputs A and B are "1" will both diodes D_A and D_B be reverse-biased. This allows point X to rise to E' volts, and since $E' > E$, diode D_C will be forward-biased. This will block FE_3 and FE_4 and the cell will light. Again assuming level inputs, the cell will stay lit while the proper input is present and will "go dark" when the input is removed.

Since both the "AND" and "OR" functions can be performed, if double-rail (complementary) input signals are available, any desired logic function can be implemented. Thus pointers, bar graphs, segmented alphanumerics, etc., can be built and any desired input code may be used. Figure 39 shows how this may be done for a bar graph indicator. It is assumed that the input is a linear variable and that the length of the illuminated portion of the bar graph is to be proportional to the input variable. Thus, when the input is 0 (binary 00) none of the bar graph segments are lit; when the input is 1 (binary 01) segment A is lit; when the input is 2 (binary 10) segments A and B are lit; and when the input is 3 (binary 11) segments A, B, and C are lit. Although only three segments are shown in the bar graph of Figure 39, the extension to a larger number of segments is straightforward. Similar logical decoders can be designed for pointers, segmented alphanumerics and other similar displays using any desired input code.



TRUTH TABLE

BINARY INPUTS		EL SEGMENTS		
x_1	x_2	A	B	C
0	0	OFF	OFF	OFF
0	1	ON	OFF	OFF
1	0	ON	ON	OFF
1	1	ON	ON	ON

$A = x_1 + x_2$
$B = x_1$
$C = x_1 x_2$

Figure 39. Transcharger Controlled EL Bar Graph Indicator.

Although there are other ferroelectric logic circuits, it is felt that those illustrated in Figures 38 and 39 are the simplest circuits which are capable of giving reliable high performance in display applications. The virtue of these circuits lies in their simplicity and their adaptability to any desired input code. The "OR" gate circuit, in fact, requires only one additional component above and beyond the normal components of the basic transcharger circuit itself. The fact that the doubly balanced transcharger circuit accepts a DC level input and controls the AC energization of the electroluminescent cell in accordance therewith makes this simplicity possible. Compared with other means for decoding level inputs and controlling electroluminescent cells, such as neon bulb-photoconductor circuits or transistor-silicon controlled rectifier circuits, this diode logic-ferroelectric transcharger circuit should be more reliable and ultimately less expensive. The necessary diodes and resistors for the decoding circuitry are readily amenable to fabrication by any of the means common to integrated-circuit technology. Thus, a single strip of ferroelectric material and a single wafer of semiconductor material would constitute the entire decoding and controlling circuit for a solid-state bar graph, pointer, or alphanumeric display.

E. PANEL FABRICATION TECHNIQUES

A semi-integrated modular construction technique is essential to the construction of a practical solid-state display panel. Construction of the panel element by element would be prohibitively expensive, and attempts to fabricate the entire panel in a single piece would result in yield problems. Since a display panel is an assembly of lines of elements, a single line of the display is a logical choice for a module. It is felt that the assembly of a panel from lines that have been batch-fabricated and pre-tested will give an optimum construction technique.

Two specific means of constructing a line of a display are illustrated in Figures 40 and 41. Figure 40 shows a long ribbon of ferroelectric material on which transchargers have been formed side by side at regular intervals by proper electrode placement. It had been hoped that the doctor-blading technique studied under Contract No. AF33(615)1193 would be sufficiently perfected to make ferroelectric strips as shown in Figure 40 for use in the experimental models constructed under this program. Although, as outlined in Section II-B, considerable progress was made on the doctor-blading process, further work is required before it will be possible to use the technique in constructing experimental models.

The fabrication scheme illustrated in Figure 41 preserves the line-at-a-time philosophy without requiring long flat strips of ferroelectric material, and it is this scheme which was used to construct the experimental models. Since the experimental models required only a relatively small number of elements, the electroluminescent cells were not constructed a line-at-a-time but were simply fabricated all at once on a single glass substrate. The transchargers were fabricated a line at a time by electroding individual ceramic chips for two or more transchargers and then assembling these chips onto substrate carrier strips to form a complete line as shown in Figure 41. The ceramic chips were 0.4 x 0.5 in. x 3-mil-thick, dry-pressed, lapped

50/50-14-2Nb ferroelectric material obtained from Clevite Corporation. They were electroded by evaporating gold through appropriately designed masks. The electroded chips are mounted on substrate carrier strips which are made from standard printed-circuit board stock. The carrier strips have copper paths leading from the edges of the ceramic chip to the edges of the carrier strip where contact is made to the electroluminescent cells and to the column busses. Connections between ceramic chips and from the ceramic chips to the conductive paths on the substrate were made with wire leads attached with silver paste. The ceramic chips were not in any way attached to the substrates but were simply held in place by the wire leads connected to them. The details of how the technique of Figure 41 was applied to each of the experimental models are given in Section II-G.

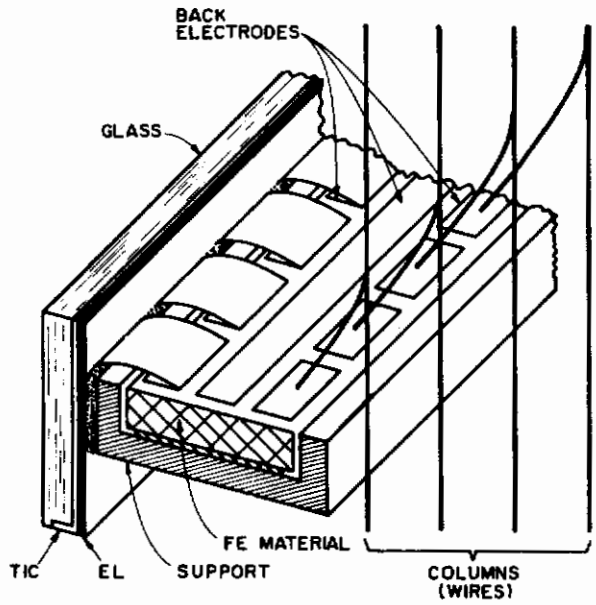


Figure 40.

One Line of Display Panel.

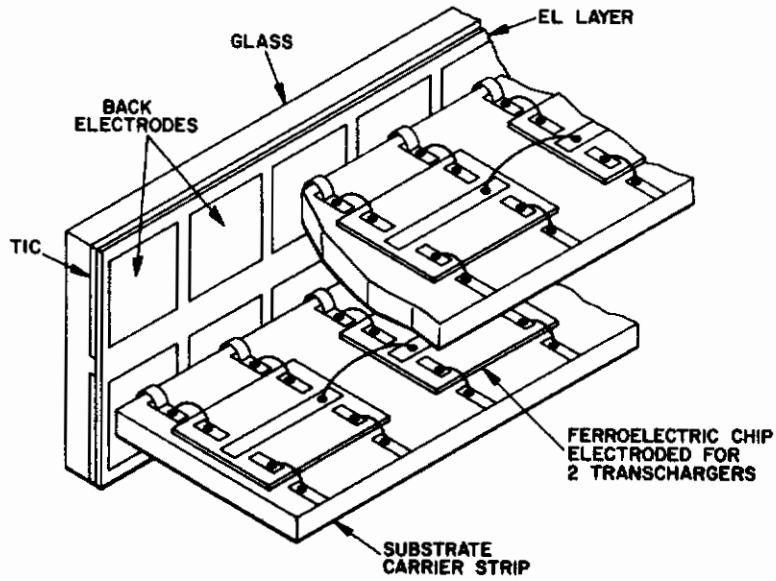


Figure 41.

Display Panel Fabrication Scheme.

Although the fabrication scheme of Figure 41 was entirely satisfactory for the construction of the experimental models, the method illustrated in Figure 40 of using doctor-bladed ferroelectric material is naturally to be preferred as a mass-fabrication technique for full-scale displays. And it is fully expected that the doctor-blading technique will be perfected and will ultimately be used to fabricate transchargers for matrix displays. However, if necessary, the technique of Figure 41 could, of course, be automated by using appropriate machinery to fabricate, electrode, and test the ceramic chips and then to use machinery similar to that presently used for computer memory cores to orient the chips and put them in place on the substrate carrier strips. The connections between chips and to the substrate would then be made by evaporation or silk-screening.

In both the technique of Figure 40 and that of Figure 41, it is necessary to make connections from the ferroelectric carrier substrate to the electroluminescent cells and to the column busses. Pin connectors were used for this purpose in the experimental models to facilitate assembly and disassembly for experimentation. In a practical display, the pin connectors would be neither necessary nor economical. Preferred methods would be to use spring connectors, such as phosphor bronze fingers or conductive rubber buttons or to make the connections by gang-soldering. To use gang-soldering, the parts to be connected are first tinned with a solder of appropriate melting temperature; the parts are then held in contact with a jig and the entire assembly is placed in an oven and raised to a temperature above the melting point of the solder, thus simultaneously soldering all of the connections. Since both the electroluminescent cell and the ferroelectric can easily withstand temperatures of 150°C or more, there should be no difficulty in applying this technique.

F. SCANNING AND DRIVING CIRCUITRY

In order to scan a ferroelectric electroluminescent display panel, electronic circuitry is required to provide both horizontal and vertical scanning pulses, to convert the video signal information into the proper form and to deliver it to the panel. Also, a supply of AC energizing power is necessary for the electroluminescent cells.

1. Scanning Circuitry

The exact form of the scanning circuitry is, of course, dependent on the type of information that the display is to present and upon the form in which this information is to be presented. There are, however, certain general principles which apply in any event. Since the transcharger provides local storage, the electroluminescent elements are energized continuously and a high frame rate is not required to prevent flicker. The presentation of dynamic information does, however, require periodic updating of the display to preserve continuity of motion; it has been found that a frame rate of 15 frames per second is adequate for this purpose in most instances, but higher frame rates can, of course, be used if desired.

There are two basic methods of addressing a matrix display: spot-addressing in which a single element is addressed at a time and line-addressing in

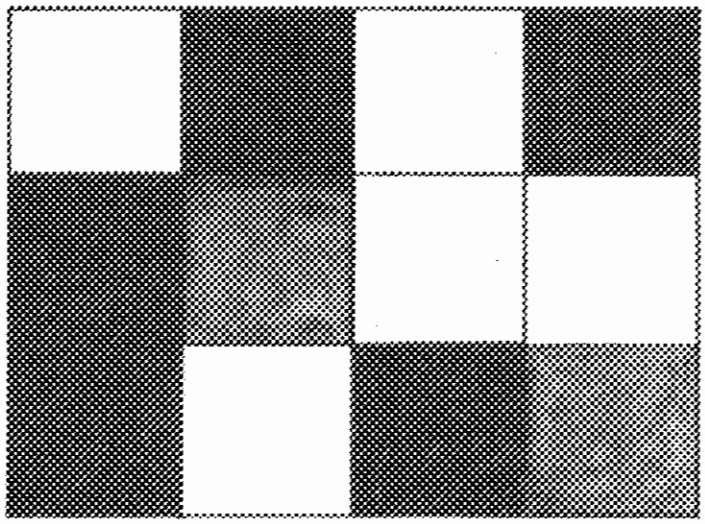
which all elements of a given line are addressed at a time. These methods are, respectively, analogous to bit-organized and word-organized computer memories. Spot-addressing is practical only for low-resolution displays; high-resolution displays must employ a form of line-addressing. Consider a display having n lines of m elements each. For a frame rate of 15 frames per second, if spot-addressing is used, the maximum time available to address each element is $T_S = \frac{1}{15\ nm}$ seconds, but if line-addressing is used, the maximum time available to address each element is $T_L = \frac{1}{15n}$ seconds. If, for example n=60 and m=75, $T_S = \frac{1}{15x60x75} = 14.8$ usec, a reasonable time in which to reset and set a storage element; but if n = 600 and m = 750, $T_S = 0.148$ μsec, a goal which is not in sight for transcharger switching with presently known ferroelectrics. However, for n = 600 and m = 750, $T_L = 111$ μsec, which is a switching time easily achieved with present transchargers. Even if it were possible to switch the transchargers in a fraction of a microsecond, the practical problems of distributing such high-speed signals within the display panel itself would make the use of line-addressing preferable. It should be noted that the principle of line-addressing is not confined solely to addressing lines of the display in parallel. Line-addressing is really a particular case of parallel-addressing. Certain display applications might make it preferable to address all elements of a given column in parallel or all elements in a square or rectangular segment of the display, or in the case of bar graph or alphanumeric displays, all elements of the entire display.

To illustrate the differences between spot-addressing and line-addressing consider a 12-element display arranged as three rows of four elements each (n = 3, m = 4). Suppose this display is reproducing the halftone image shown in Figure 42(a); if the image is scanned in the usual manner (left to right, top to bottom) the video waveform will be as shown in Figure 42(b) (positive going video represents white). If a frame rate of 15 frames per second is assumed, the frame time $T_F = \frac{1}{15} = 67$ msec, $T_L = \frac{1}{3x15} = 22$msec, and $T_S = \frac{1}{3x4x15} = 5.5$ msec.

The row and column addressing waveforms for spot-addressing are shown in Figure 43. The row pulses are negative-going and of width T_L and repetition rate $1/T_F$. The column pulses are positive-going (amplitude-modulated by the video signal) and of width T_S and repetition rate $1/T_L$. During the time that each row pulse is present, pulses appear sequentially on each of the columns.

The row and column addressing waveforms for line-addressing are shown in Figure 44. The row pulses are identical to those shown for spot-addressing in Figure 43. The column pulses, however, are of width T_L. During the time that each row pulse is present, all of the columns are pulsed simultaneously.

Figure 45 shows a block diagram of a spot-addressed display. The operation of the display is as follows: Incoming composite video information is separated into synchronizing information and video information. The synchronizing information controls the scanning clocks which provide timing signals to the vertical and horizontal scanners. The vertical scanner is a shift



(a) HALFTONE IMAGE

Figure 42. Halftone Image on a Twelve-Element Display and the Corresponding Video Waveform.

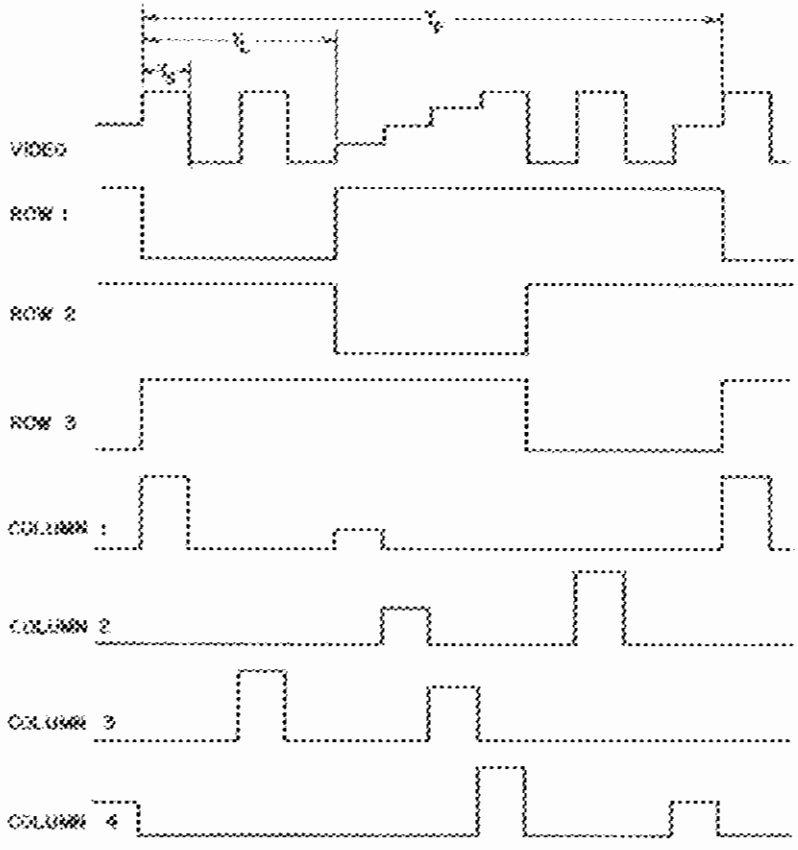


Figure 43. Video Signal and Row and Column Signals Corresponding to the Image of Figure 42 When Spot-Addressing is Employed.

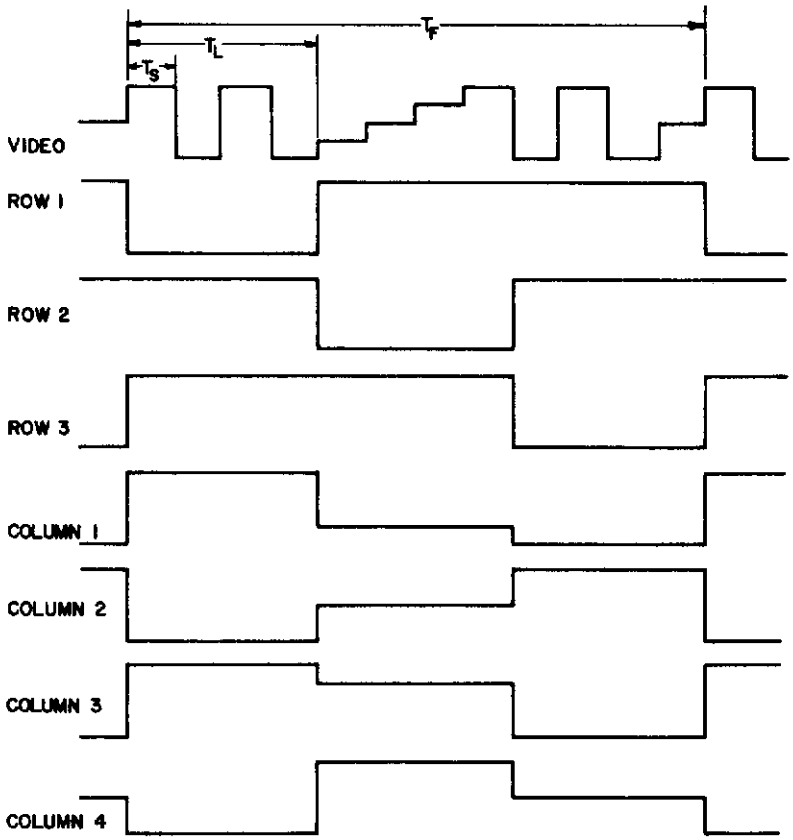


Figure 44.

Video Signal and Row and Column Signals Corresponding to the Image of Figure 42 When Line-Addressing is Employed.

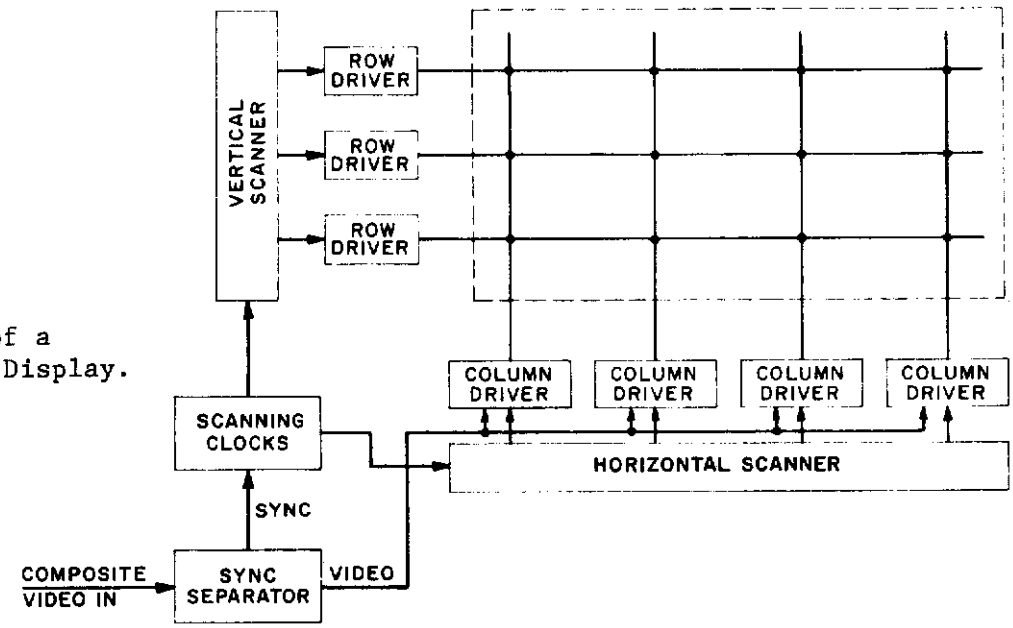


Figure 45.

Block Diagram of a Spot-Addressed Display.

register and for an n-line display provides n outputs, each of which is energized in sequence for a time T_L. These outputs trigger the row drivers which provide half-select row pulses. Like the vertical scanner, the horizontal scanner is also a shift register and provides m outputs, each of which is energized in sequence for a time T_S. These outputs energize the column drivers which produce column pulses of width T_S, amplitude-modulated by the video signal present at the input to the column drivers at the time they are energized.

Figure 46 shows a block diagram of a line-addressed display designed to accept parallel video inputs. The operation of the display is as follows: The synchronizing input controls the scanning clocks which provide timing signals to the vertical scanners and to the column drivers. The vertical scanner is a shift register and for an n-line display provides n outputs, each of which is energized in sequence for a time T_L. These outputs trigger the row drivers which provide half-select row pulses. Simultaneous with the operation of the row drivers, all m column drivers are energized to produce column pulses of width T_L, amplitude-modulated by the m video inputs.

Although it may be possible in some display applications to arrange to have the video input supplied a line-at-a-time in the form of m simultaneous parallel signals as indicated in Figure 46, it is more usual to have the video input supplied a bit at a time in the form of one serial real-time signal. In this case, line-addressing implies staticizing or temporary storage of the video information.

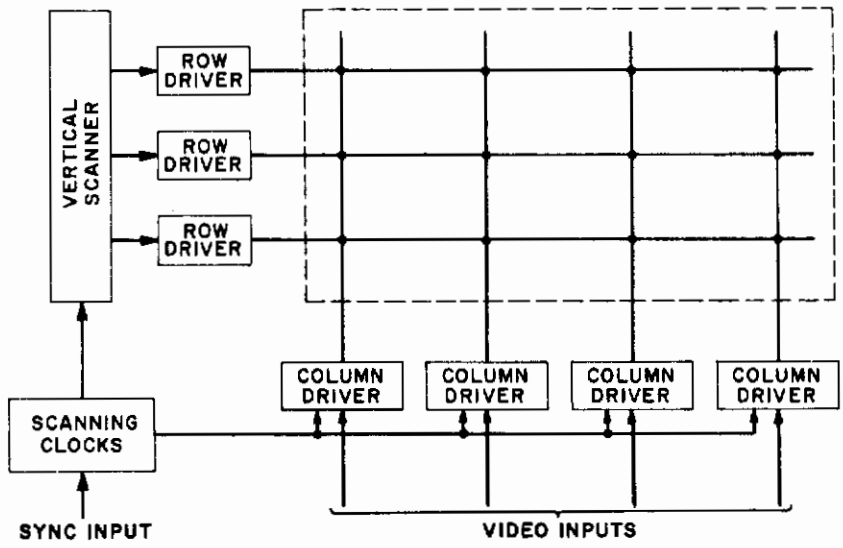


Figure 46. Block Diagram of a Line-Addressed Display (parallel video input).

Figure 47 shows a block diagram of a display designed to accept serial video information in real time, store it temporarily and then transfer it in parallel to all elements in a given line of the display. The operation of the circuitry is as follows: Incoming composite video information is separated into synchronizing information and video information. The synchronizing

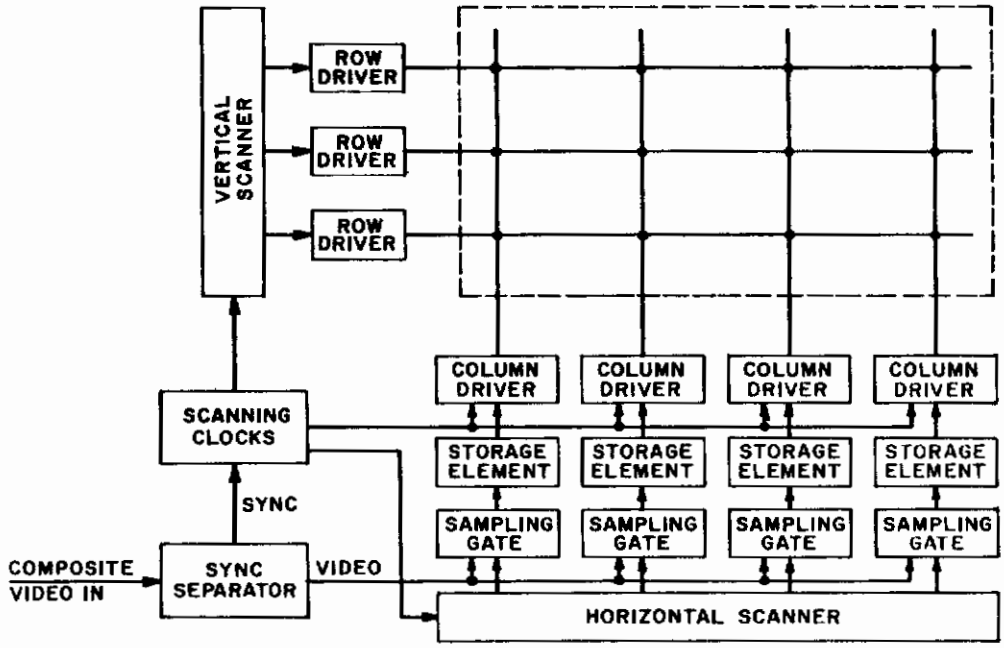


Figure 47. Block Diagram of a Line-Addressed Display (serial video input).

information controls the scanning clocks which provide timing signals to the vertical and horizontal scanners, and to the column drivers. The vertical scanner is a shift register and for an n-line display provides n outputs, each of which is energized in sequence for a time T_L. These outputs trigger the row drivers which provide the half-select row pulses. Like the vertical scanner, the horizontal scanner is also a shift register and provides m outputs, each of which is energized in sequence for a time T_S. These outputs energize the sampling gates thus "trapping" the video information in the storage elements. After a complete line of video information has been trapped, a timing signal energizes the column drivers. The column drivers produce pulses whose amplitudes are dependent on the stored video signal and whose time of occurrence is synchronous with the half-select pulse from the row driver. It is the coincidence of these row and column signals that writes a whole line of video information into the panel at once.

The practical realization of the horizontal scanning and driving circuitry for the system of Figure 47 presents difficulties on two counts: (1) The horizontal scanner must operate at $\frac{1}{T_S}$ Hz which means MHz rates for a large display ($\frac{1}{T_S} = \frac{1}{0.148\ \mu sec} = 6.75$ MHz for a 15 frame per second display with

n = 600 and m = 750). (2) The sampling gates, storage elements, and column drivers are required in large quantity (one set of circuits for each of m columns).

A novel and rather elegant solution to these difficulties has been proposed,[7] wherein transfluxors are used to perform not only the scanning but also the gating and storage of sampled video. Figure 48 shows in block diagram form how such a system will perform. Video information is supplied alternately to registers #1 and #2. Each register consists of m elements, each capable of accepting information in a time T_S and storing its analog value for a time T_L. After a line of video information has been stored in one of the registers it is transferred in parallel to the display panel. The row location into which the information is written is determined by energizing the appropriate row driver. The two registers thus alternately accept serial video input information and then transfer it in parallel to a row of the display.

Each element of the registers must provide the following functions:

1. Accept video information on command from a sequencing signal in a time T_S.

2. Store the analog value of this video information for a time T_L.

3. Produce, on command from a transfer signal, an output signal whose amplitude is proportional to the value of the stored video information.

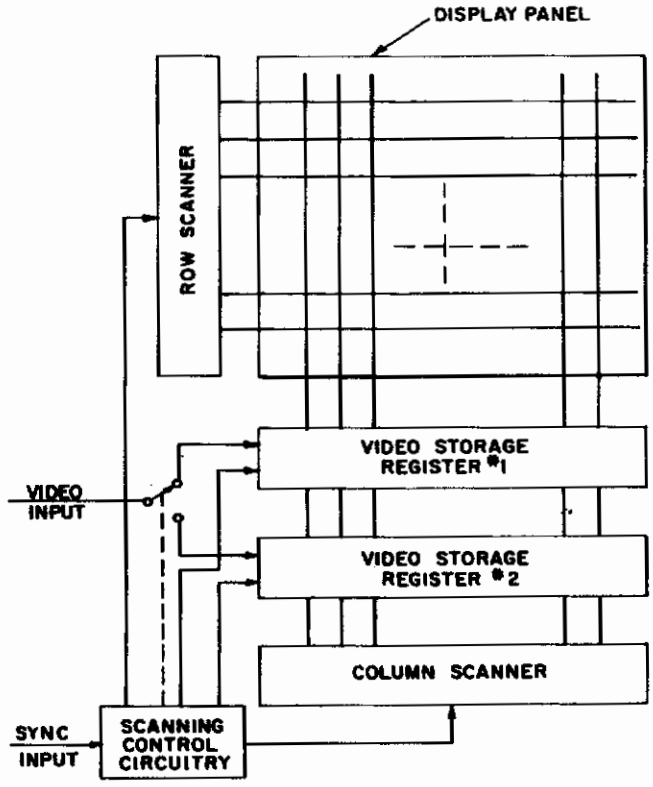


Figure 48. Block Diagram of Panel-Display Scanning System.

The transfluxor[8] is an element which is capable of performing all of these functions. Figure 49 shows the Φ-I characteristic of the transfluxor. The video signal alone is not of sufficient amplitude to set the transfluxor. The

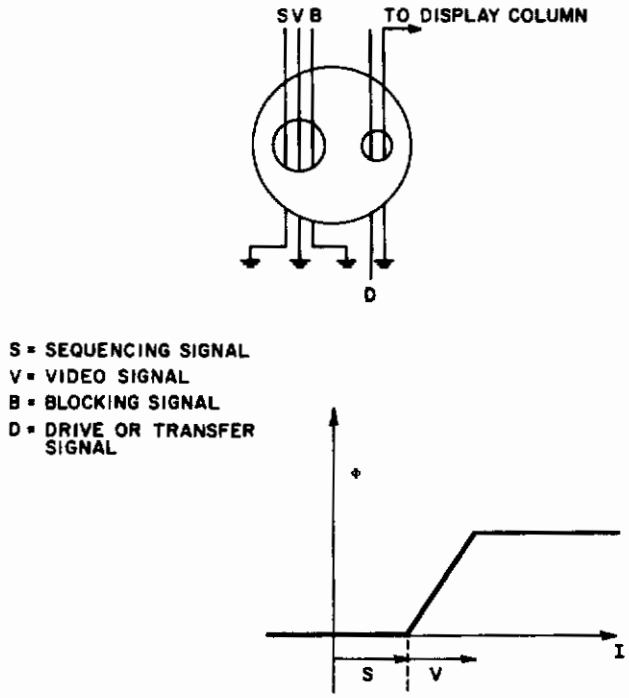


Figure 49. Illustrating Transfluxor Storage and Transfer of Analog Video Information.

sequencing signal S biases the transfluxor to its knee, allowing the video signal to set the transfluxor to a value proportional to the instantaneous amplitude of the video signal. The sequencing signal thus samples the video signal and the transfluxor stores the analog value of this sample. If the small aperture of the transfluxor is then used as a pulse transformer, the degree of coupling and, hence, the amplitude of the output signal will be linearly related to the amplitude to which the transfluxor was previously set by the video signal. A negative blocking signal B then resets the transfluxor to its original state and the process may be repeated.

Figure 50 illustrates the basic principle of using transfluxors for the elements of the storage registers. Assume that V_1 is supplying video information to register #1. The sampling lines S_{1i} are pulsed in sequence with pulses of width T_S to sample the video signal and to store its analog value in the transfluxors of register #1. While this process is taking place, the drive line D_2 of register #2 is pulsed, and the video information previously stored in register #2 is transferred to the panel. Blocking pulse B_2 then resets register #2 and the video input signal is switched from V_1 to V_2. The roles of registers #1 and #2 have thus been interchanged and the process is repeated.

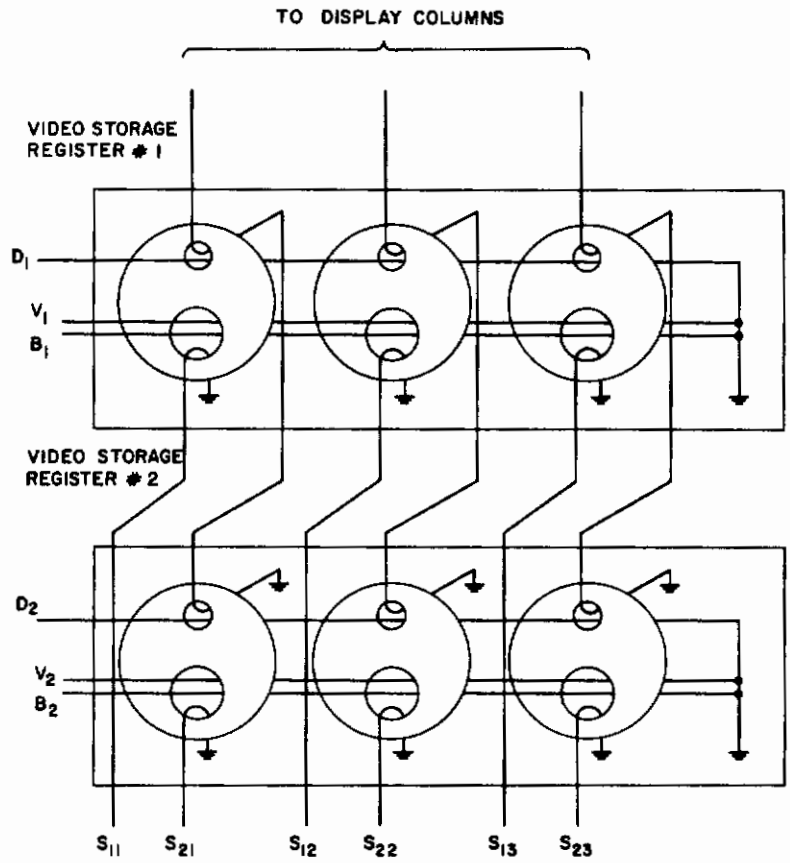


Figure 50. Use of Transfluxors as Elements of Video Storage Registers.

To simplify the process of providing the sequencing signals S_{1i} and S_{2i}, the video storage registers may be arranged in a matrix u x v with u and v chosen to be relatively prime. If u and v are then sequenced simultaneously, the matrix location at which u and v are coincident will progress diagonally through all possible matrix locations. Figure 51 illustrates this for u = 25, v = 28, and m = 700 elements. The pulse signals u and v must have a width T_S and must each have amplitudes equal to the peak-to-peak video signal. The transfluxors must be biased so that they will be brought to the knee of the Φ-I characteristic only upon the coincidence of u and v. The sequential scanning of u and v may be achieved in a variety of ways; the simplest is to use conventional high-speed semiconductor shift registers.

The transfluxor approach has been investigated in detail. These studies indicate that the transfluxor is entirely capable of performing the required functions at low speeds, but that, at submicrosecond writing times, prohibitively large driving currents are required. Also, when the transfluxor geometry is chosen to minimize the required writing currents, read outputs large enough to drive the transcharger matrix can be obtained only marginally and only by using multiple-turn windings on several transfluxors. It is evident that, in practice, an amplifier will be required between the transfluxor and the display column busses.

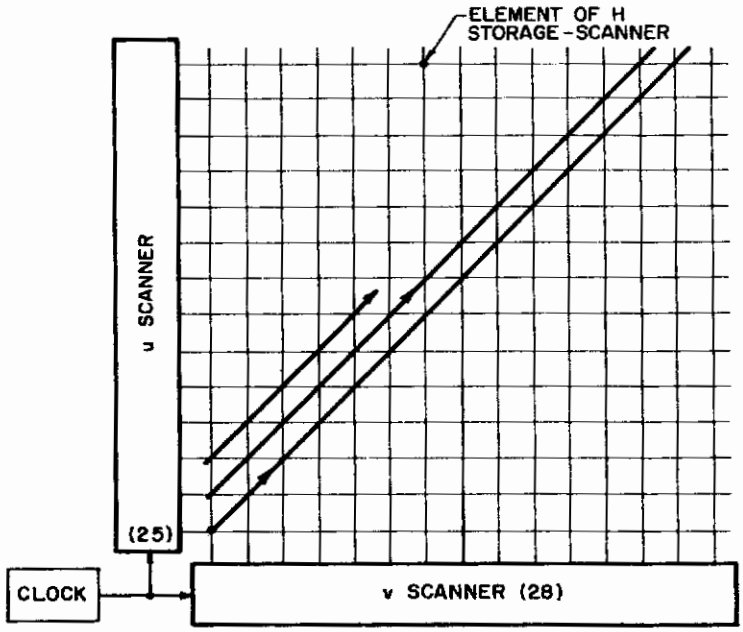


Figure 51. u x v Scan for H Scanner.

If an amplifier is to be used, one is led to consider capacitive storage as an alternative to magnetic storage. Capacitive storage is somewhat simpler and also lends itself better to use with semiconductor circuitry. Several circuits using capacitive storage have been devised and breadboard tested at submicrosecond writing times. Although they meet all of the basic requirements, an analysis of the tolerances on circuit components (typically two transistors, a capacitor, and a few resistors) indicates that extremely close tolerances must be kept to achieve acceptable circuit uniformity. These tight tolerances arise because the circuits operate as open-loop linear amplifiers to produce a gray scale. For on-off operation of a display, uniformity of the transfer characteristic is, of course, not required and hence the tolerances can be relaxed considerably. But for a gray-scale display further research is necessary to find circuits which are less sensitive to parameter variations.

The use of line-at-a-time addressing and the therefore-required storage register is based on the inability of the ferroelectric transcharger to switch rapidly enough for real-time addressing of a large display. It is, however, possible to address the column busses of the display in real time and then to use the parasitic capacitances of the column busses as storage elements. To illustrate the scheme consider a 525-line, 15-frame per second display. The time per line, T_L, in such a display would be 127 μsec, and, assuming 650 elements per line, the time per element, T_S, would be 0.2 μsec. Suppose row one is being addressed. The column busses would be sequentially addressed for 0.2 μsec. During this interval the capacitance of the column busses would be charged to a voltage proportional to the analog video signal. At some point during the 127-μsec interval between successive energizations of the column busses the row bus would be energized for 20 to 30 μsec to allow the ferroelectrics for row number one to switch. This method is attractive because a

special storage register is not required. However, for a large display, the column drivers must have a large current capability at megahertz frequencies.

Let us calculate this current for a 525-line display having elements 0.1 in. square; such a display would measure approximately 4 x 6 feet. With present ceramic ferroelectrics, the required switching voltage is about 60 V and the required charge is about 0.2 μcoul for display elements 0.1 in. square. If the applied voltage (stored on the parasitic capacitance of the column bus) is to fall no more than 10 percent when the selected cell switches, we have:

$$dv = 0.1 \times 60 = 6 \text{ volts}$$

and since

$$C = \frac{dq}{dv}$$

we find the required parasitic capacitance to be

$$C = \frac{0.2 \text{ μcoul}}{6 \text{ volts}} = 33000 \text{ pF}$$

If the doubly balanced transcharger circuit of Figure 23 is used, the parasitic capacitance of the column bus is essentially the total capacitance of the diode isolating elements. Assuming a diode capacitance of 10 pF per diode, we have, for our 525-line display, 525 x 10 pF = 5250 pF. Thus, additional capacitance must be added if the voltage drop is to be less than 10 percent. For a parasitic capacitance of 33000 pF, the current required from the column driver to charge this capacitance to 60 V in 0.2 μsec is

$$I = C \frac{dv}{dt} = 0.033 \times 10^{-6} \left(\frac{60}{0.2 \times 10^{-6}} \right) = 10 \text{ amperes}$$

This is too large to be practical and it is therefore concluded that for large displays, the storage-register technique of Figure 47 must be used.

However, since the required current is proportional to the area of the display, it may be possible to use the direct-addressing technique for smaller displays. For example, for a display 12 x 16 in. the required drive current is only 500 mA.

2. Driving Circuitry

In addition to the scanning circuitry already discussed additional peripheral circuitry is required to provide the AC driving signals which energize the electroluminescent cells. Aside from the obvious requirements of voltage and current, the excitation signal must meet two important requirements:
(1) The driving signal must be interrupted during the time of addressing.
(2) Each row of the display must be provided with a center-tapped source which is DC-isolated from all other rows at the time of addressing.

In principle, the first requirement is easily satisfied by having a gate circuit associated with each row of the display which interrupts the excitation signal for an interval T_L at the time of addressing. The excitation waveforms for an n-line display operating at a frame rate $1/T_F$ would then be as shown in Figure 52. From a practical standpoint, this scheme is not at all satisfactory, since it requires, in effect, that a separate excitation signal be generated for each line of the display.

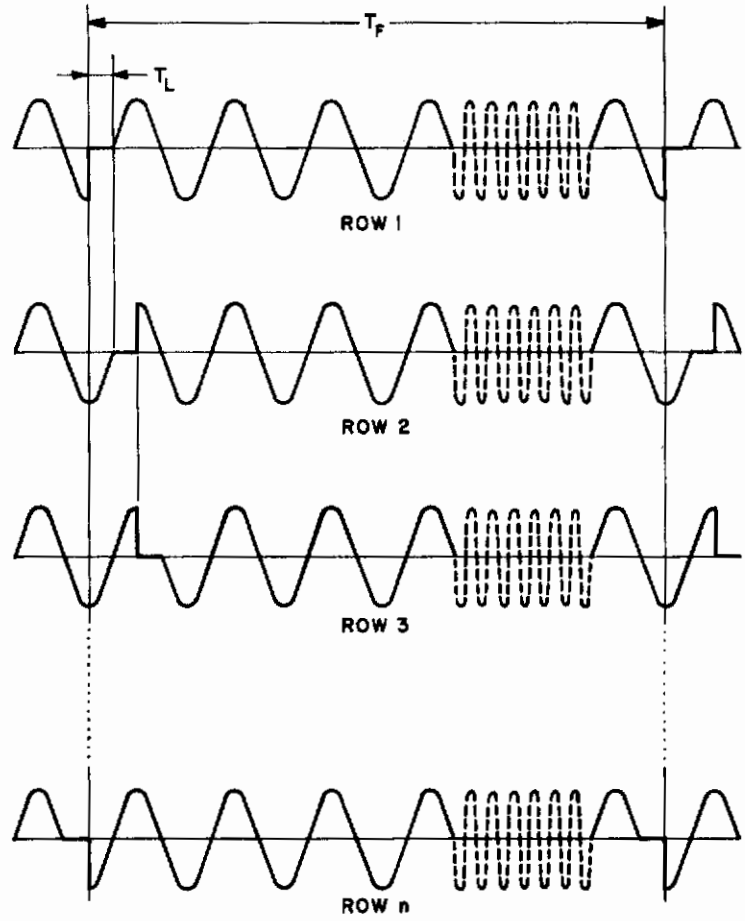


Figure 52. Excitation Waveforms for an n-Line Display (interrupt interval = T_L).

The number of separate excitation signals required can easily be reduced, however, by increasing the time that the excitation signal is interrupted. For example, if the interrupt interval is made equal to jT_L, where j is an integral factor of n, only n/j separate excitation signals are required. This is illustrated in Figure 53. With this arrangement each separate excitation signal drives j rows of the display. The simplification is, however, obtained at the expense of brightness, since the electroluminescent cells produce no light when they are not excited. For an appreciable economy in the number of excitation signals required, j must be a large fraction of n, and the brightness is reduced by precisely this fraction. For example, if $j = n/3$, only $n/j = \frac{n}{n/3} = 3$ separate excitation sources are required, but the brightness will be reduced by 1/3.

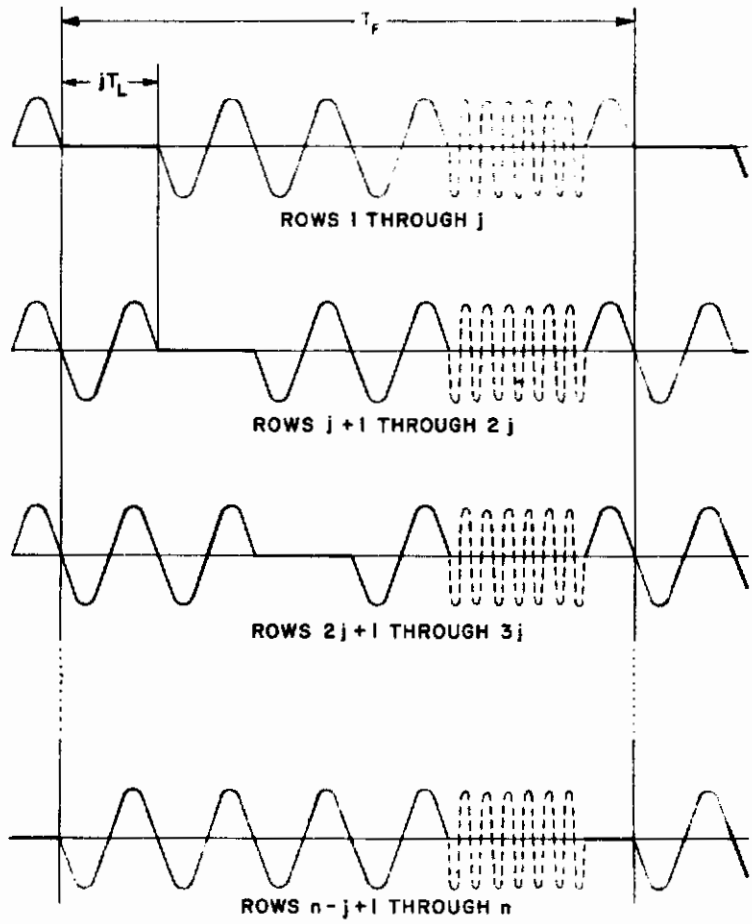


Figure 53. Excitation Waveforms for an n-Line Display (interrupt interval = jT_L).

However, since the brightness of an electroluminescent cell is approximately proportional to the frequency of the excitation signal, if the frequency is increased by a factor $\frac{1}{1-(j/n)}$, the brightness will remain nearly the same. For our example, $j = n/3$, this means a 50-percent increase in the excitation frequency. Notice that 3/2 as many excitation cycles will be present for 2/3 as long a time; thus, the total number of excitation cycles remains constant. This means that the life of the electroluminescent cells will be substantially unaffected since it is approximately dependent only on the total number of cycles applied.

Although Figure 53 shows the interruption of the excitation occurring all at once, this is not necessary and, in fact, from a practical standpoint, not desirable. Figure 54(a) shows the excitation waveforms for a system with $j = n/2$, wherein the gating is divided into $n/2$ segments, each of duration T_L. This has been called a continuously gated excitation signal since the gating intervals alternate equally with one cycle of excitation. These waveforms are easy to generate and amplify, and this is essentially the system used in the 120-element model described in Section II-G. Although sinusoidal driving

signals have been shown in Figures 52, 53, and 54(a), it is also possible to use other waveshapes, such as the square wave indicated in Figure 54(b). From a practical standpoint the square wave is preferred since it is easier to generate and can be amplified with higher efficiency. Also, since the square wave has higher ratio of rms to peak value, the brightness is higher for a given peak-to-peak excitation signal.

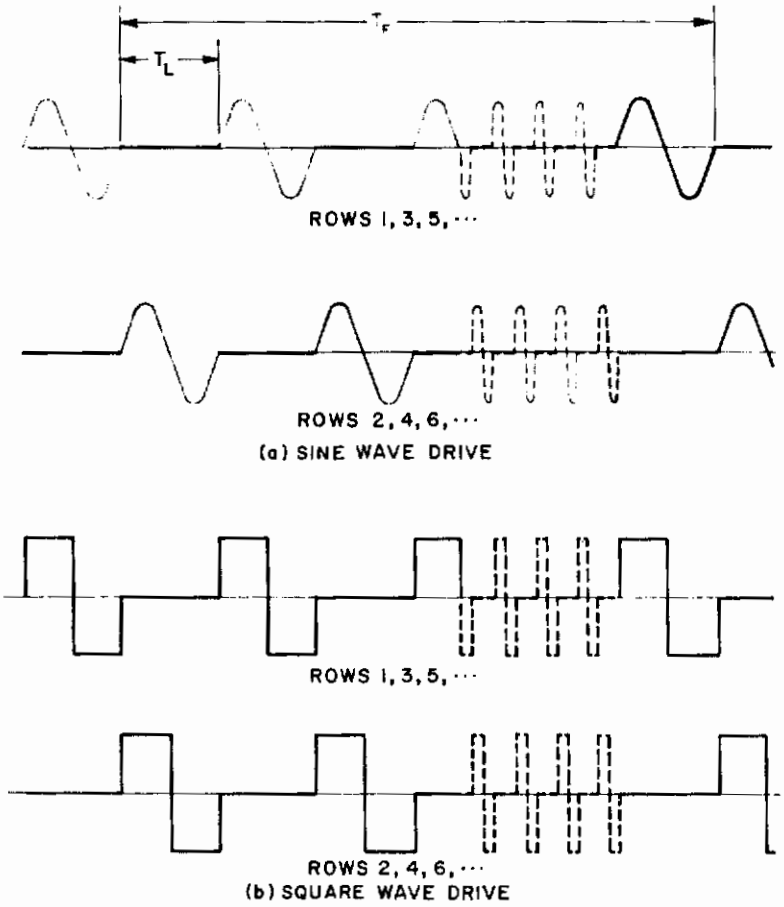


Figure 54. Continuously Gated Excitation Waveforms.

The second requirement on the excitation source (to provide a DC-isolated center-tapped source for each row) is easily satisfied by using a center-tapped transformer for each row. Although entirely satisfactory for small displays having but a few rows, this scheme is not practical for large displays.

Figure 55 illustrates a scheme which eliminates the need for center-tapped transformers at each row of the display. Figure 56 shows the waveforms for the circuit of Figure 55. Consider initially only the generators and diodes associated with row 1, namely, generators A_{11}, A_{12}, A_{13}, and A_{14}, and diodes D_{11}, D_{12}, D_{13}, and D_{14}. When the generators are inactive, bias supply E_1 maintains reverse-bias on diodes D_{11} and D_{14}, and bias supply E_2 maintains reverse-bias on diodes D_{12} and D_{13}. When generator A_{12} operates to produce a positive pulse and A_{14} operates to simultaneously produce a negative pulse,

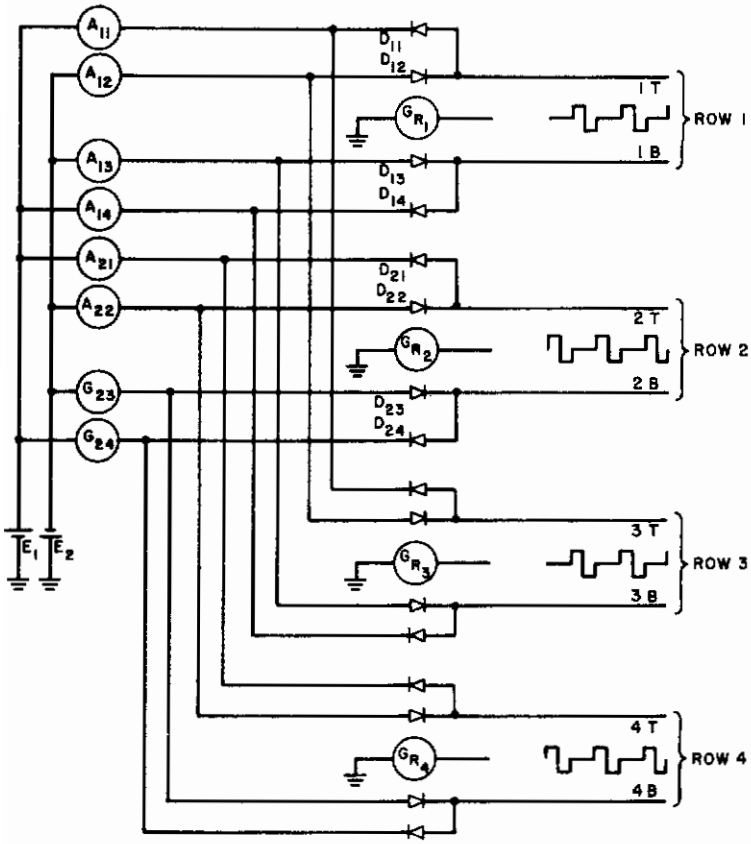


Figure 55.

Continuously Gated Square Wave Excitation System Not Requiring Center-Tapped Transformers.

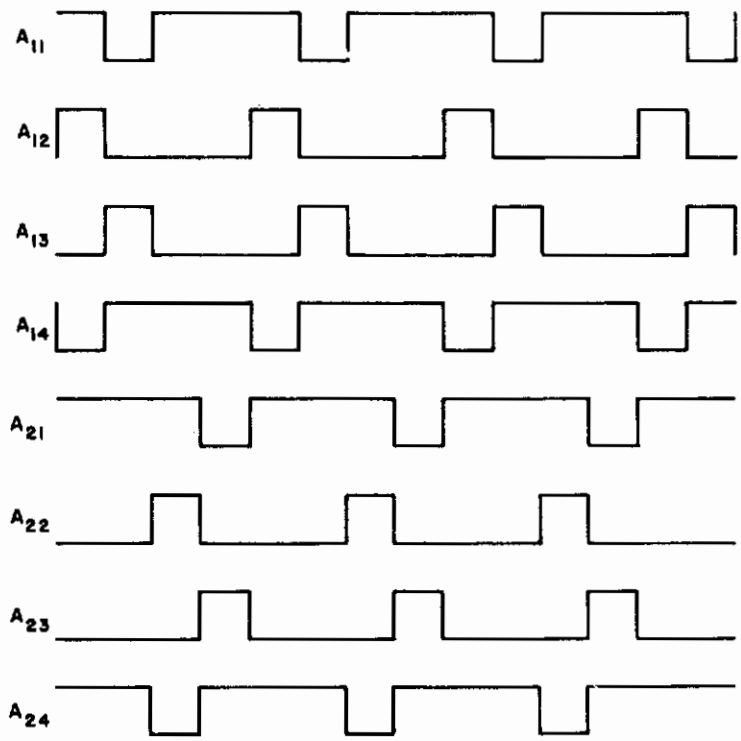


Figure 56.

Waveforms for the Circuit of Figure 55.

diodes D_{12} and D_{14} are forward-biased to produce a plus-to-minus signal from terminal 1T to terminal 1B. When generators A_{11} and A_{13} operate simultaneously with A_{11} thus producing a negative pulse and A_{13} a positive pulse, diodes D_{11} and D_{13} are both forward-biased and a minus-to-plus signal is produced between terminals 1T and 1B. Since row 3 is wired in parallel with row 1 the signal from 3T to 3B is identical with that from 1T to 1B. The operation for row 2 and row 4 is similar; when generators A_{22} and A_{24} operate, diodes D22 and D_{24} are forward-biased and a plus-to-minus signal is produced from 2T to 2B; and, when generators A_{21} and A_{23} operate, diodes D_{21} and D_{23} are forward-biased to produce a minus-to-plus signal between terminals 2T and 2B. Again, since row 4 is wired in parallel with row 2, the signals between 4T and 4B are identical to those between 2T and 2B. The separate sets of diodes for each row provide the required DC isolation between rows during the addressing intervals.

G. EXPERIMENTAL MODELS

To demonstrate the feasibility of fabricating and operating display panels based on the use of ferroelectric electroluminescent elements, the construction and test of three experimental model displays was planned as part of this contract effort. The main 120-element model incorporates all of the basic features of a complete display including the scanning and driving circuitry. Input signals for this display are obtained from a vidicon camera, thus permitting the real-time display of moving images. To help insure the success of the main model, the goals with respect to brightness and resolution were kept modest and two auxiliary models were constructed--one to show high brightness, and another to show high resolution.

1. Main 120-Element Model

The main 120-element display has the following characteristics:

a. Ten lines of 12 elements each.
b. A frame rate of 83.3 frames per second
c. An addressing time per bit of 41.6 μsec.
d. A geometrical resolution of 4 elements per inch resulting in a panel 3 x 2-1/2 in.
e. A contrast ratio in excess of 100 to 1.
f. A brightness of approximately 15 ft-L.
g. Capability for on-off operation of each separate element and the ability to demonstrate continuous control for the presentation of a gray scale.
h. Complete scanning and driving circuitry including a vidicon camera to provide input signals.

A photograph of the complete experimental 120-element model display system is shown in Figure 57. The 120-element display itself is in the lower left foreground of the picture. Behind the display is an illuminated easel and to its right is the vidicon camera. The 30-in. table-top relay rack at the right side of the photograph houses the electronics for the model display. Figure 58 is a close-up front view of the 120-element display and Figure 59 is a rear view of the display.

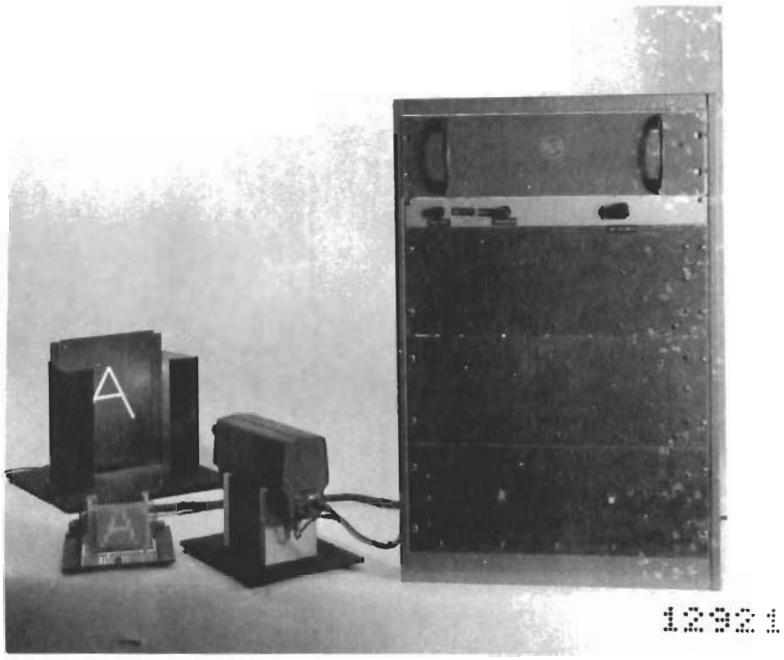


Figure 57. Complete 120-Element Experimental Model Display System.

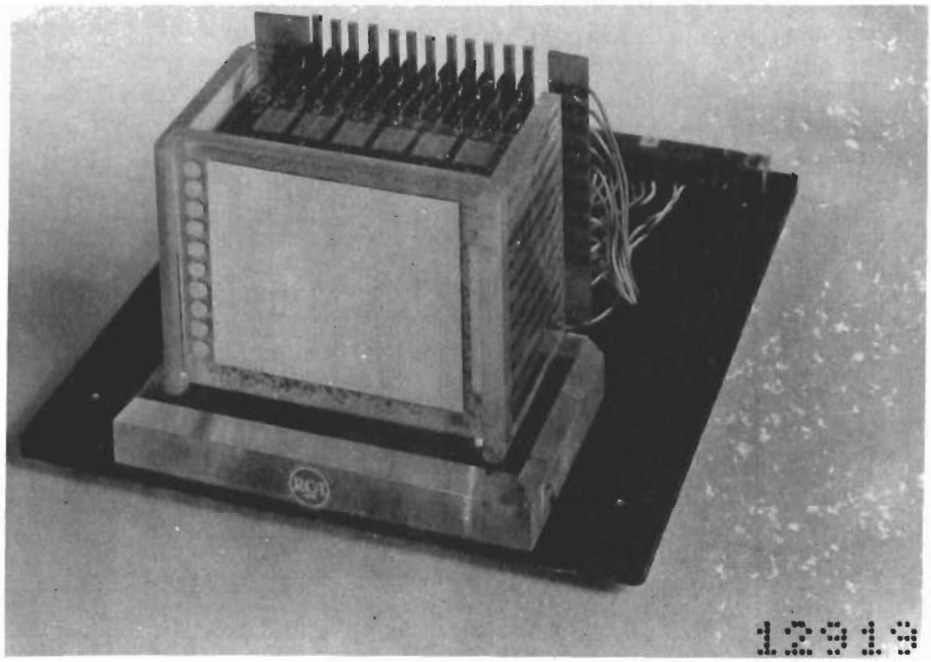


Figure 58. Front View of 120-Element Display.

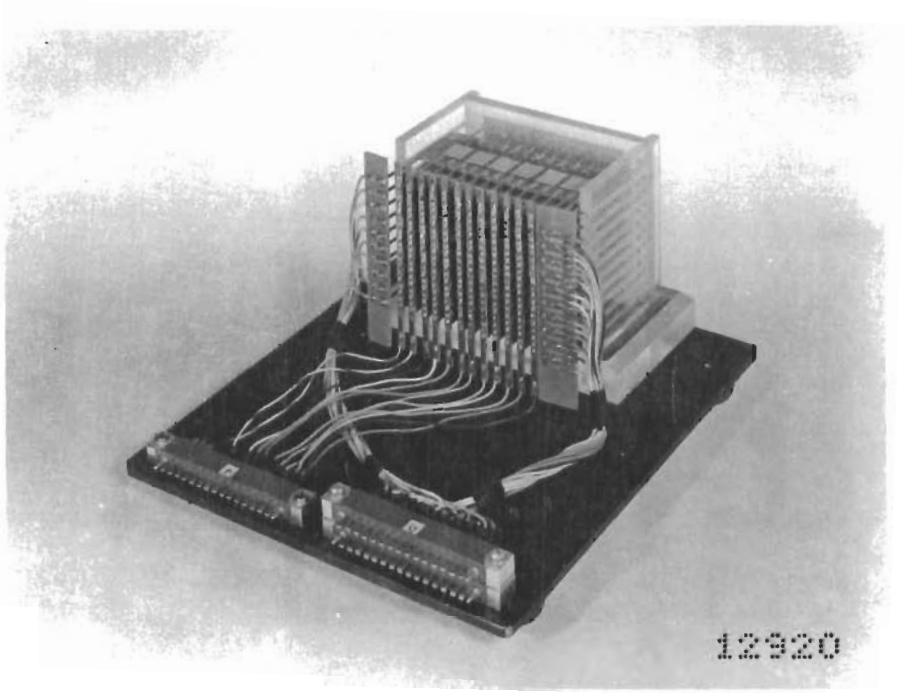


Figure 59. Rear View of 120-Element Display.

Figure 60 is a simplified schematic and block diagram of the 120-element model. For clarity, only two rows of three elements each are shown in the figure. The circuitry enclosed within the dotted block at the upper right of

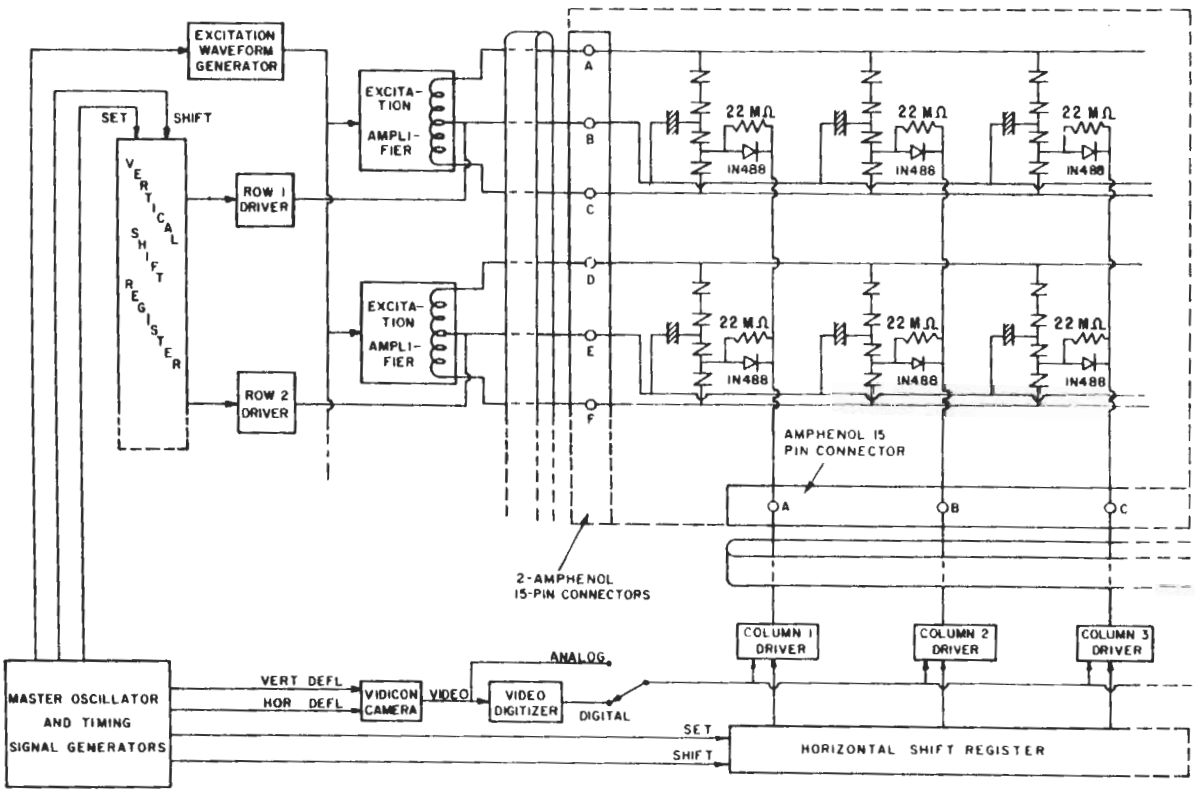


Figure 60. Diagram of Main 120-Element Model.

Figure 60 is the actual display as shown in the photographs of Figures 58 and 59. The remainder of Figure 60 constitutes the electronic system, designed and constructed to exercise the display model. The 120-element model is spot-addressed in the fashion of Figure 45 and as described in Section II-F. The electronic system employs conventional transistor circuits and is described in detail in Appendix I. As can be seen from Figure 60, the electronics consists of row drivers and column drivers which are energized sequentially by vertical and horizontal shift registers, respectively; an excitation waveform generator and its associated amplifiers; a vidicon camera and video digitizer; and a master oscillator and associated timing signal generators. A simplified timing diagram for the 120-element model is shown in Figure 61.

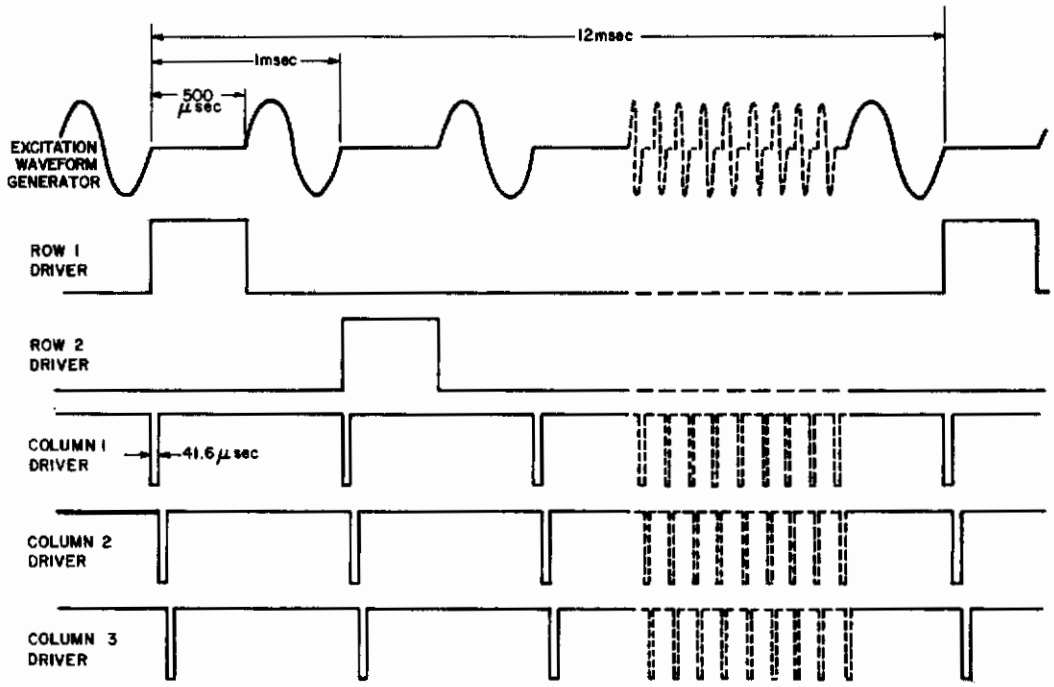


Figure 61. Timing Diagram for Main 120-Element Model.

Referring to Figures 60 and 61 the operation is as follows: The excitation waveform generator produces a 2-kHz continuously gated excitation signal; although shown as a sinusoidal signal in Figure 61, the generator output is actually a square wave, but the outputs of the excitation amplifiers are more nearly sine waves than square waves. The excitation amplifiers have center-tapped outputs and provide the energizing signal to the ten rows of the display. Since the model has a small number of rows, only a single phase of continuously gated excitation signal is used, and hence only half of the total available time is used for addressing. Except when energized, the row driver outputs are clamped to -100 V. This provides the necessary negative bias to keep the addressing diodes cut off. The outputs from the vertical shift register energize the row drivers sequentially for 500-μsec intervals (one line time, T_L) when the excitation waveform is blanked. The row drivers produce 100-V positive-going pulses to overcome the bias on the addressing diodes and to allow the column pulses to switch the selected cells. The outputs from the

horizontal shift register energize the column drivers sequentially for 41.6 μsec (one spot time, T_S) during the 500-μsec interval that a row driver is on. The column drivers produce negative-going pulses whose amplitude is controlled by the video signal from the vidicon camera. If the analog-digital switch is in the analog position the column pulse amplitude may be anywhere between 0 V (black level — cell not switched) and -100 V (white level — cell fully switched), and the model operates as an analog or gray-scale display. If the analog-digital switch is in the digital position the column pulse amplitude will be either 0 V or -100 V depending on whether the video signal is below or above the digitizer threshold, and the model operates as a digital or on-off display. In Figure 61, the column pulses have all been shown with amplitudes of -100 V. This corresponds to a white field. Note in Figure 61 that the frame time T_F is 12 msec (corresponding to a frame rate of $\frac{1}{12 \text{ msec}}$ = 83.3 frames per second). Since half of the total time is used for addressing and since the line time is 500 μsec this corresponds to a 12-line display, but the model has only ten lines. The other two lines are scanned but are not displayed. The vertical shift register has 12 stages but two of the outputs are not used. Also, the vidicon raster has 12 scan lines, but the two that occur during vertical retrace are not displayed. The master oscillator and associated timing signal generators provide synchronized timing signals for the vertical and horizontal shift registers, the excitation waveform generator, and the vertical and horizontal deflection of the vidicon camera. The model thus constitutes a complete television system capable of displaying in motion, the scenes scanned by the vidicon camera. Figure 62 illustrates the construction technique that was used for the 120-element model. The 120 electroluminescent cells (ten lines of 12 each) are fabricated on a single glass substrate. The cells have a nominal

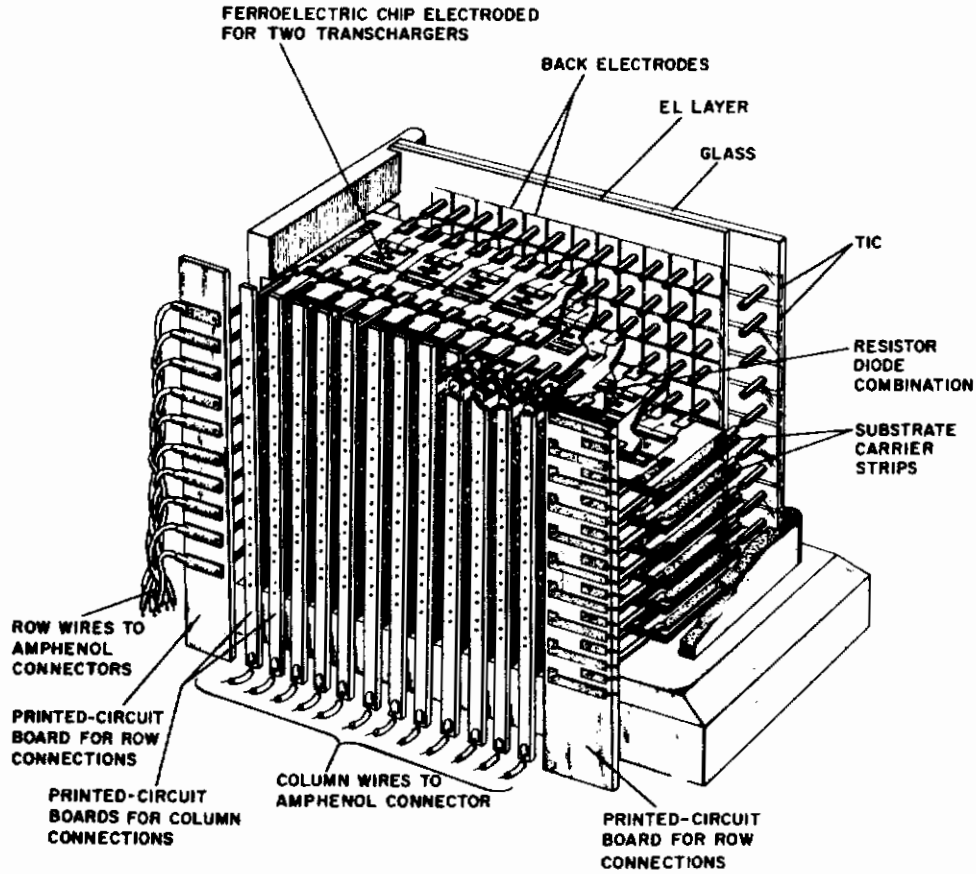


Figure 62.

Construction of Main 120-Element Model.

voltage rating of 50 V rms. Separate semitransparent TIC electrodes are provided for each of the ten rows. The 120 separate electroluminescent patches (each 0.25-in. square) are defined by structuring the back electrode. A gold-plated female connector placed orthogonal to the substrate is attached to each of the 120 back electrodes and to the ten semitransparent TIC electrodes. The entire electroluminescent panel is encapsulated in epoxy resin to provide a moisture seal.

To construct the transchargers for the model, a number of 0.4 x 0.5 in. x 3-mil-thick dry-pressed lapped 50/50-14-2Nb ferroelectric chips were prepared. The chips were each electroded for two transchargers as shown in the magnified photograph of Figure 63. Since the ceramic material is translucent, the bottom electrodes show as dark areas in the photograph. The electrode pattern forms two groups of four series-connected capacitors. The electrode areas were chosen to give an EL/FE area ratio of 12.1. As indicated in Section II-D, this favors brightness at the expense of gray-scale uniformity.

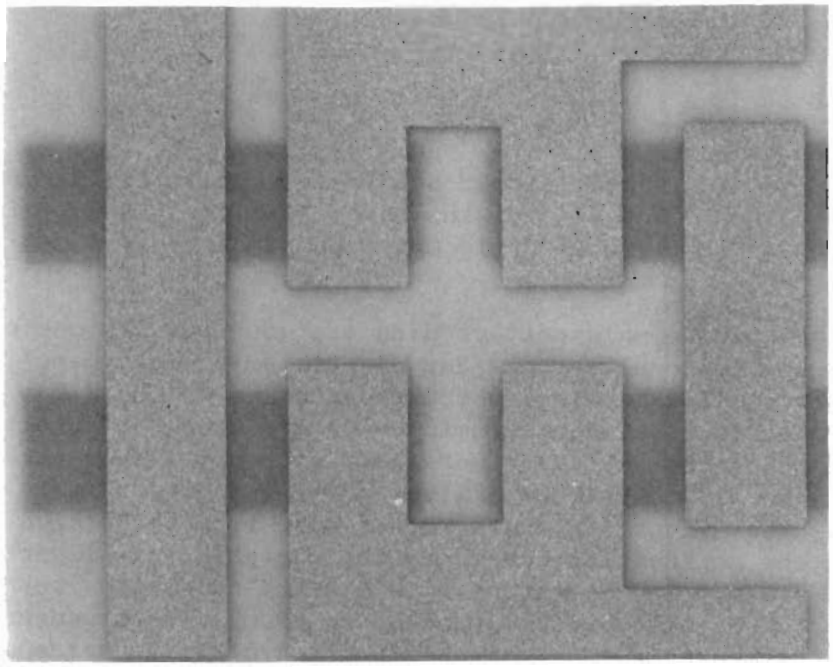


Figure 63. Magnified Photograph of Ferroelectric Chip Electroded to Form Two Transchargers.

The upper and lower horizontal top electrodes in the photograph are the row busses. The F-shaped electrodes form the midpoint of each of the groups of four capacitors and are connected to the electroluminescent cell. The F shape was used to ease the requirements on mask registration when the electrodes are evaporated. With this arrangement, small errors in mask registration do not affect the area defined by the cross-over of the electrodes. The electroded ceramic chips (six for each of the ten lines) are mounted on printed-circuit board substrate carrier strips as shown in Figure 64. The carrier strips have conductive paths leading from the edges of the ceramic chips to the edges of

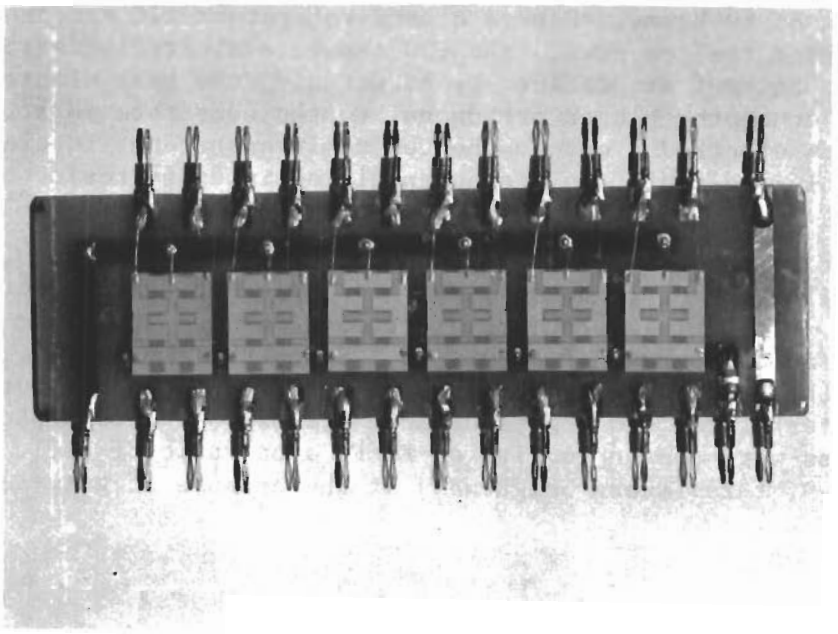


Figure 64. Ferroelectric Substrate Carrier Strip for One Line of the Main 120-Element Model with Ferroelectric Chips in Place.

the carrier strip where male contact pins are mounted. On one edge these pins mate with the female connectors on the electroluminescent panel, and on the other edge with similar female connectors attached to the diode resistor combination. Connections between ceramic chips and from the ceramic chips to the conductive paths on the substrate were made with wire leads attached with silver paste. In all cases where silver paste connections were made to the ceramic chips, the silver paste was kept remote from the active ferroelectric area to avoid the degradation caused by the migration of silver ions. The ceramic chips are not in any way attached to the substrates but are simply held in place by the wire leads connected to them. The necessary row and column connections are made by means of printed-circuit boards mounted parallel to the electroluminescent panel. The diodes and resistors are mounted in cordwood fashion on these printed-circuit boards and are fitted with female connectors. These mate with the male pin connectors on the rear edge of the substrate carrier strips.

With this construction technique both the electroluminescent panel and the transcharger strips could be easily assembled and disassembled to facilitate experimentation. The model was assembled row by row, and each row was tested before the substrate carrier strip for the next row was installed.

Operating tests of the completed model were extremely successful. All 120 elements worked initially with essentially perfect contrast, peak brightness of 15 ft-L, reasonable gray-scale control, negligible crosstalk, and smear-free moving images. The operating tests revealed two minor problems:

During the first few hours of operation four cells in the upper left corner of the display failed. The failure was traced to opening of the indium bond between the aluminum back electrode of the electroluminescent cells and the gold-plated female connector (see Section II-C). Clearly, a better connection technique is required. The second problem was the dissipation of the heat associated with the hysteresis loss of the ferroelectrics. It had been expected that convection cooling through the stack of substrate carriers would be adequate. It turned out, however, that most of the heat was dissipated by conduction to the electroluminescent panel which acted as a heat sink. This caused the electroluminescent cell temperature to rise substantially. Since operation at elevated temperature materially shortens the life of electroluminescent cells, a small fan was provided to prevent the temperature rise. Had this difficulty been anticipated, suitable mechanical design would have prevented the transfer of heat to the electroluminescent panel.

The brightness vs set pulse amplitude transfer characteristics were measured for each of the 120 elements in the display, and the average transfer characteristic is shown in Figure 65. The measurements were made by coupling each row of transchargers in turn to a standard row of 12 electroluminescent elements. By this means it was possible to quickly measure the transfer characteristic for each of the 120 display elements. Since the 12 electroluminescent cells had been selected to give the same light output for the same AC driving voltage, and since the excitation and driving signals were also standardized, the variations which occurred in the transfer characteristics were attributable primarily to the ferroelectric transcharger part of the circuit. These variations turned out to be greater than originally expected, especially at intermediate halftone levels.

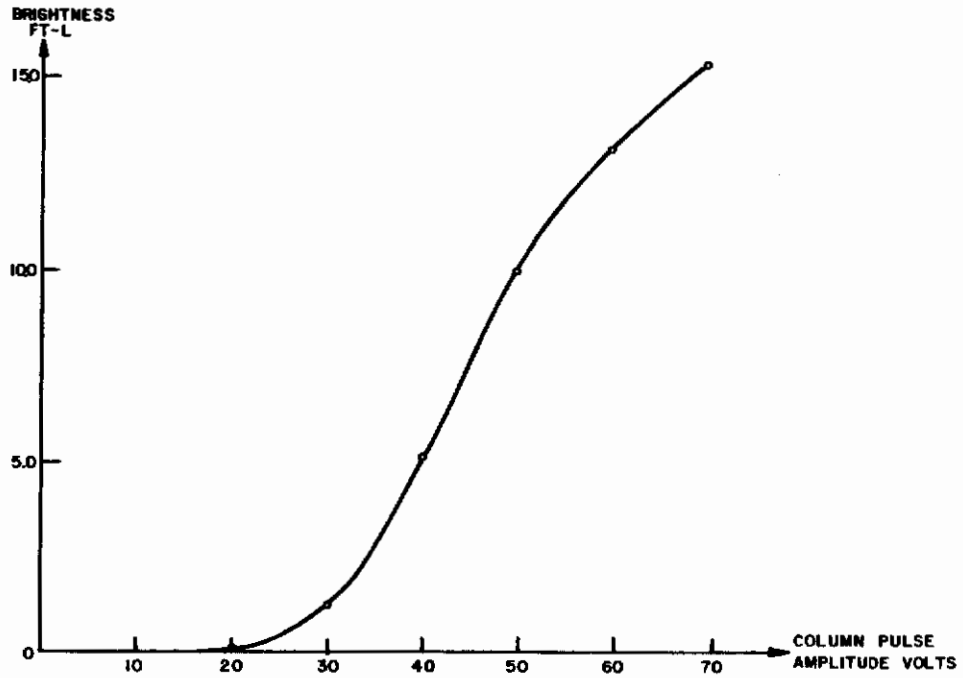


Figure 65. Brightness vs Column Pulse Amplitude for the 120-Element Model (averaged values for all 120 elements).

The maximum "on" brightness reached with a column pulse of 70 V varied over the 120 elements between 9.4 and 19 ft-L. The average value, as plotted in Figure 65, was 15 ft-L and the lower and upper decile points were 12.3 and 17.3 ft-L, respectively. For column pulses of 20 V or less, all cells had essentially zero brightness. At a halftone setting of 40 V the brightness varied between 0.5 and 15 ft-L, with an average value of 5 ft-L and a lower and upper decile of 1.3 and 10.3 ft-L.

These transfer characteristic variations were considerably greater than those obtained on the earlier 36-element display model built under Contract No. AF33(615)1193. Because of this it was decided to check on the hysteresis loop characteristics of the last 12 groups of ceramic chips received from the Clevite Corporation. Measurements showed that five of these groups had remanent and saturation polarizations 20 to 25 percent lower than the nominal 50/50-14-2Nb ceramic values. The probable reason for this is that not enough quality control was maintained when it became necessary to produce a large number of chips in a short period of time. In particular, it is suspected that some of the niobium oxide used contained impurities.

Unfortunately, because of lack of time and material it was possible to replace only the worst 10 of the 120 transchargers in the model. The replacement transchargers were made from ceramic known to have the standard properties. These replacements considerably reduced the variation in the transfer characteristics of the 120 elements. As a result, the display subjectively gave very satisfactory performance as a digital or on-off display. As an analog or gray-scale display, the performance was found to be less pleasing. This was partly expected since the EL/FE area ratio was originally chosen to give high brightness at the expense of gray-scale uniformity. Nevertheless, in the future, by better control of the ceramic manufacture an improved high-brightness analog display should be easily obtained.

Figures 66, 67, and 68 are unretouched off-the-screen photographs of the working 120-element model display. The photographs were taken with totally darkened room lighting. The display was operating at 15 ft-L in the digital mode. The variation in element brightness evident in the photographs is not entirely due to nonuniformities in the transchargers. Because of the limited resolution (120 elements) there is a rather severe aperture effect in the camera system (the electron beam in the vidicon was not defocussed and the ten-line raster is spread over most of the useful target area). This means that parts of the televised scene will not be "seen" or almost not be "seen" by the vidicon. In the digital mode of operation, residual 60-Hz hum in the camera circuits causes the video signal for such portions of the scene to oscillate about the threshold of the digitizer. This results in flicker of the particular element in the display (the flicker rate is the beat frequency between 60 Hz and the scanning frequency). For example, the first illuminated element in the second row of Figure 67 was flickering at the time the photograph was taken and, hence, appears dimmer than its neighboring elements which were not flickering. This effect is peculiar to low-resolution systems and would not be noticed in a full-scale display.

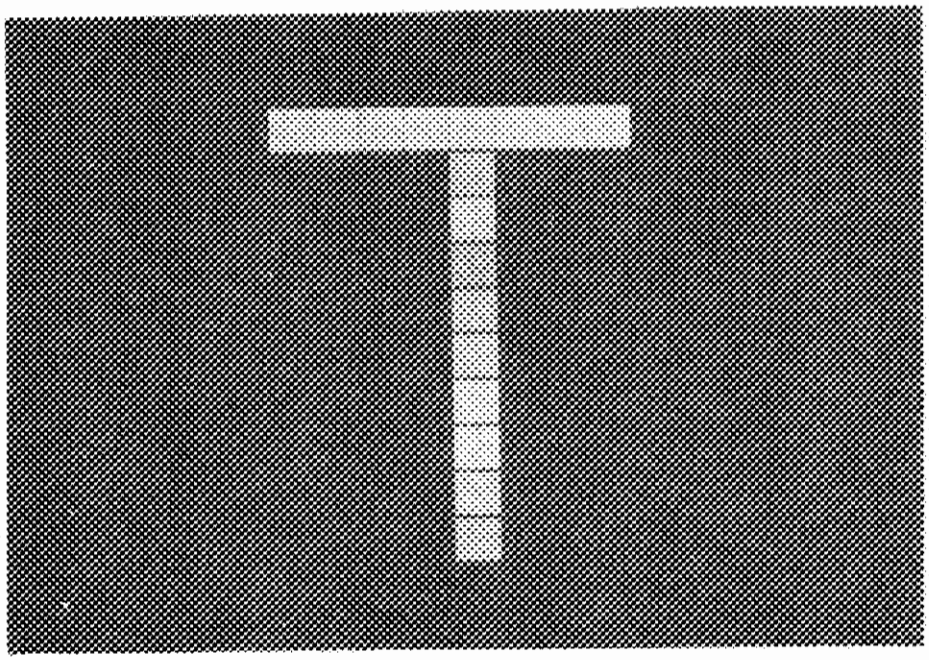


Figure 66. Off-the-Screen Photograph of 120-Element Model Displaying the Letter T.

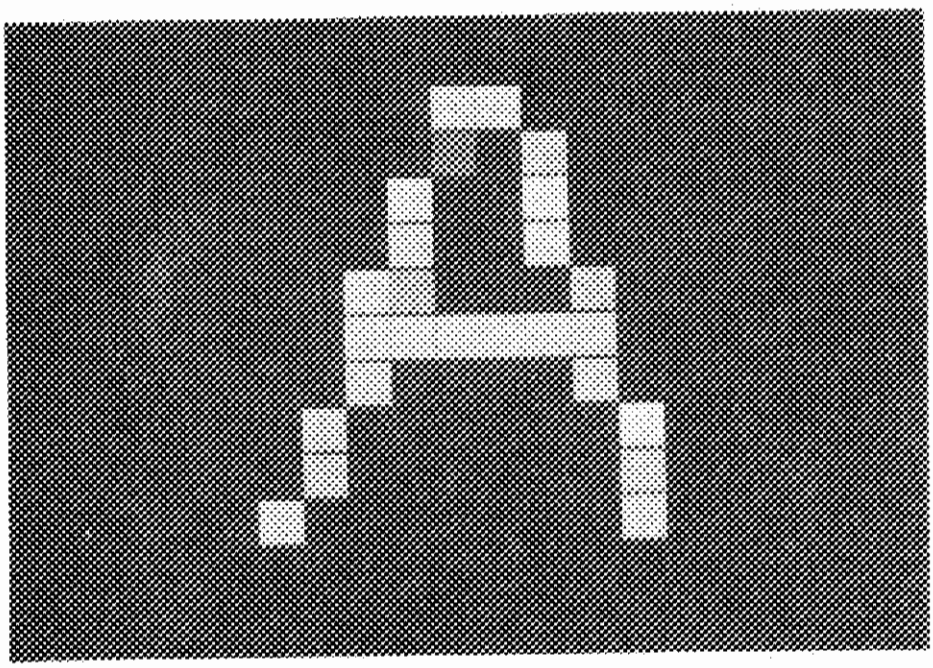


Figure 67. Off-the-Screen Photograph of 120-Element Model Displaying the Letter A.

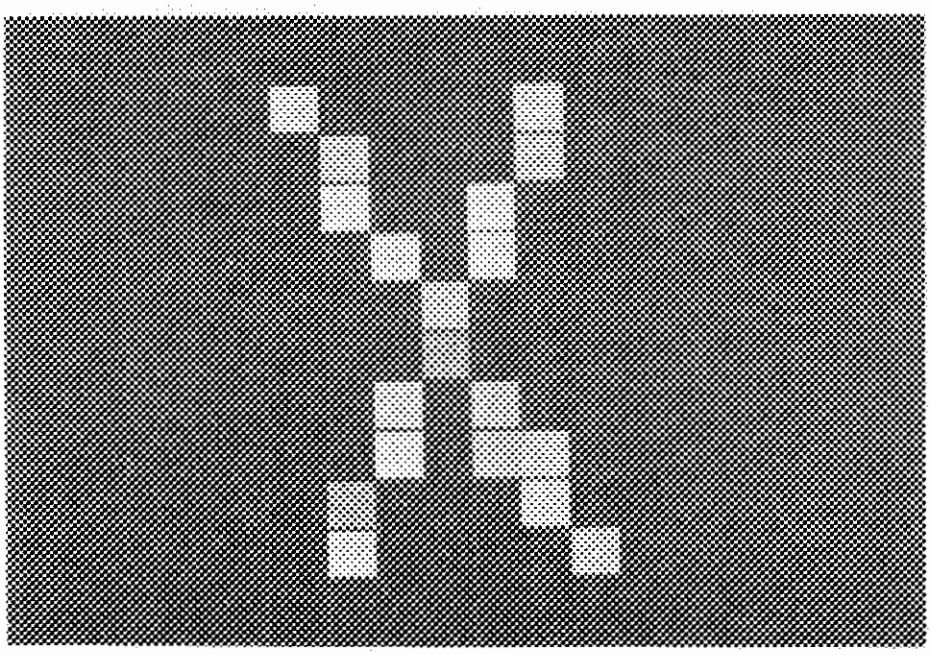


Figure 68. Off-the-Screen Photograph of 120-Element Model Displaying the Letter X.

Although it cannot be shown in the photographs of Figures 66 through 68, by moving either the screen or the vidicon camera the displayed images were made to move on the face of the display. Also, it was possible to place simple moving objects, such as a pendulum, in front of the camera and observe them in motion on the face of the display. Objects in motion did not blur or smear perceptibly. Despite the limited resolution, simple objects such as a human hand could be recognized when placed before the camera.

The highly successful operation of this 120-element model display to produce moving halftone images in real time without blurring or smearing and with good brightness and excellent contrast clearly demonstrates the feasibility of using ferroelectric electroluminescent elements in a matrix display.

7. Auxiliary Model to Show High Brightness

Since the main 120-element model had limited brightness, an auxiliary model was constructed to demonstrate the feasibility of fabricating and operating a high-brightness display using ferroelectric electroluminescent elements. The high-brightness model has the following characteristics:

a. Two elements.
b. An element size of 0.5-in. square.
c. A contrast in excess of 100 to 1.
d. A brightness in excess of 40 ft-L.
e. Simple electronics including the capability for either analog or digital addressing.

A photograph of the completed high-brightness model display is shown in Figure 69. The display circuitry itself is mounted on the plug-in board, and the associated electronics are housed in the utility box. Figure 70 is a closeup photograph of the plug-in board. The electroluminescent elements are at the top; the ferroelectric elements are mounted in the plastic boxes at the center; and the addressing diodes are in the plastic box at the bottom. The display operates in either of two modes — analog or digital — selected by a panel switch. In the analog mode the potentiometers give continuous independent control of the brightness of the top and bottom electroluminescent cells. In the digital mode, depressing either pushbutton causes the bottom electroluminescent element to light, and depressing both pushbuttons causes the top element to light.

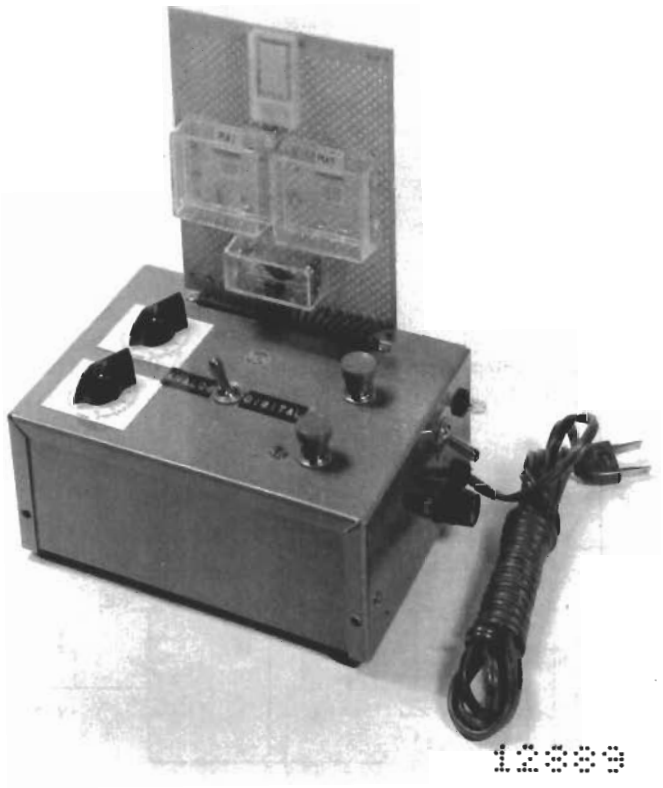


Figure 69. Photograph of Auxiliary Model to Show High Brightness.

Figure 71 is a simplified schematic of the high-brightness model in the analog mode. The portion of the circuitry within the dotted block of Figure 71 is the actual display mounted on the plug-in board. The remainder of Figure 71 is the electronic system used to exercise the model. It will be noted that the general transcharger circuit of Figure 36 has been used. The parameters of the circuit (see Section II-D) are as follows: $N_1 = N_3$; $N_2 = 0$; $d_1 = d_2 = d_3$; $a_1 = 0.47$ $a_2 = 0.47$ a_3. The electronic system employs conventional transistor circuits and is described in detail in Appendix II. Basically, the system consists of an excitation source, a bias source, and a source of addressing signals. Center-tapped generator A is the excitation source and it provides 2500-Hz square waves at approximately 900 V peak-to-peak. DC source E_1 provides reverse bias for the addressing diodes and DC source E_2 provides the

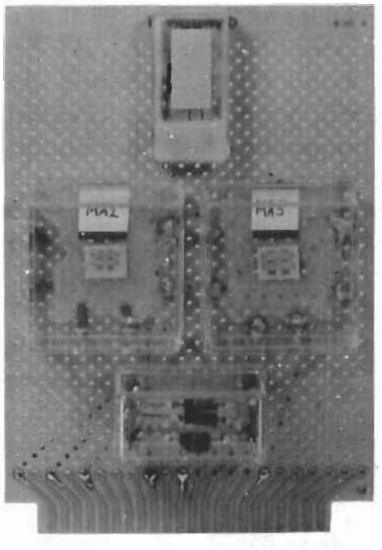


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Figure 70. Close-up Photograph of the Plug-in Board for the High-Brightness Model.

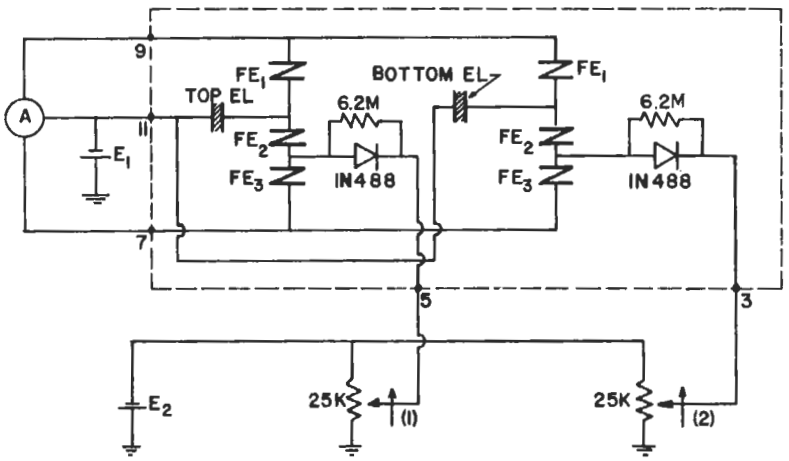

Figure 71. Simplified Schematic of the High-Brightness Model (analog mode).

addressing signals via potentiometers (1) and (2). When the potentiometers are at the minimum setting, the reverse-bias E_1 prevents the diodes from conducting. Thus, FE_2 and FE_3 remain unblocked and the electroluminescent cell is dark. Advancing either potentiometer forward-biases the corresponding diode, blocking FE_2 and FE_3 and causing the electroluminescent cell to light. The brightness depends on the degree to which FE_2 and FE_3 are blocked which, in turn, depends on the diode bias and hence on the potentiometer setting.

Figure 72 is a simplified schematic of the high-brightness model in the digital mode. Again, the circuitry within the dotted block is on the plug-in

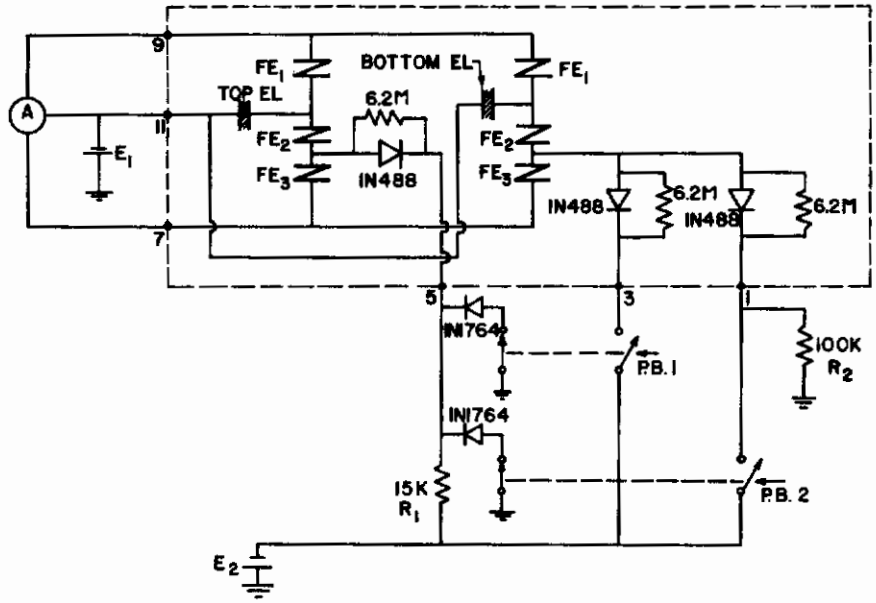

Figure 72. Simplified Schematic of the High-Brightness Model (digital mode).

board and the remainder is the electronic system. Center-tapped generator A and bias source E_1 perform as before. DC source E_2 provides the addressing signals via pushbutton switches 1 and 2 and their associated circuitry. Note that two 1N488 addressing diodes are associated with the bottom cell; depressing either pushbutton 1 or pushbutton 2 will supply the addressing signal to the bottom cell and cause it to light. The 100-kΩ resistor R_1 provides a DC return. The top cell receives its addressing signal via the 15-kΩ resistor R_2. The two 1N1764 diodes short-circuit this signal to ground and only when both pushbutton 1 and pushbutton 2 are depressed is the short circuit removed and the addressing signal applied, causing the top cell to light. These circuits will be recognized as essentially the "OR" gate and "AND" gate circuits of Figure 38 described in Section II-D. The construction technique used for the high-brightness model should be evident from Figure 70. The electroluminescent cells have a nominal voltage rating of 50 V rms, are fabricated on a single glass substrate and are sealed with epoxy resin for moisture protection. Two dry-pressed lapped 50/50-14-2Nb ferroelectric chips, 0.4 x 0.5 in. x 3-mils-thick, were used for the transchargers. The chip labeled MA-2 is electroded to form four capacitors 65 x 65 mils; these are used for FE_2 and FE_3 for both

the top and bottom cells. The other chip, labeled MA-5, is electroded to form four capacitors 95 x 95 mils; two of these are used for FE_1 for the top and bottom cells and the remaining two are not used.

Operating tests of the completed model were extremely successful. The contrast is essentially perfect; the peak brightness is 48 ft-L and there is no interaction between elements in either the analog or the digital mode. Figure 73 is a plot of the brightness vs addressing voltage for the high-brightness model. The curve was taken with the model in the analog mode and with a bias (E_1 in Figures 71 and 72) of 22.5 V. The small difference in brightness (about 10 percent) between top and bottom cells is not discernible by eye.

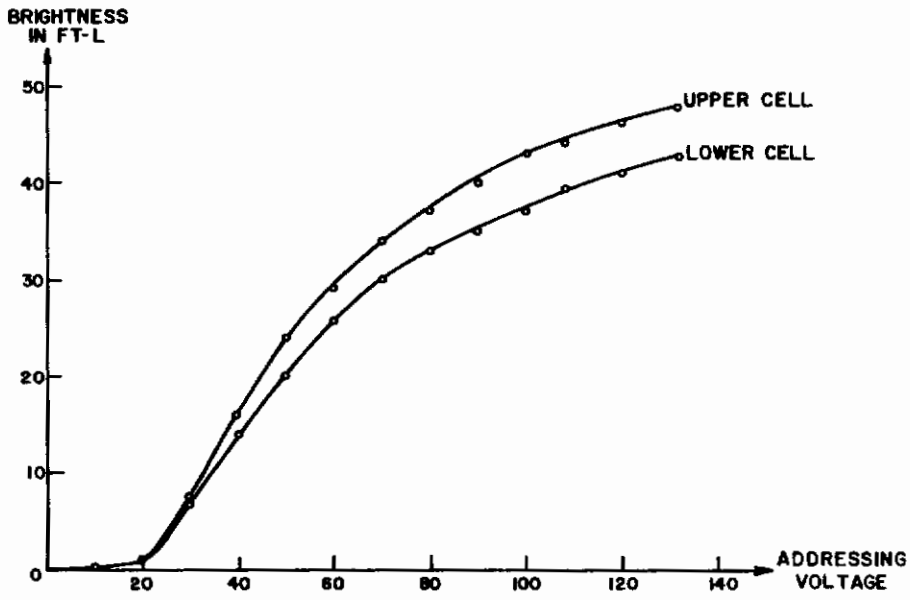

Figure 73. Brightness vs Addressing Voltage for the High-Brightness Model.

The successful operation of this model clearly demonstrates the capability of the basic transcharger circuit for use in high-brightness, high-contrast displays. The model also demonstrates the logic capability of the circuit and, hence, its usefulness in bar graph and other digitally controlled displays.

3. Auxiliary Model to Show High Resolution

Since the main 120-element model had a limited geometric resolution of four elements per inch, an auxiliary model with a geometric resolution of ten elements per inch was constructed to demonstrate the feasibility of fabricating

and operating a high-resolution display using ferroelectric electroluminescent elements. The high-resolution model has the following characteristics:

a. Two lines of 18 elements each.
b. A frame rate of 30 frames per second.
c. A line-addressing time of approximately 30 μsec.
d. A geometrical resolution of 10 elements per inch.
e. A contrast in excess of 100 to 1.
f. A brightness of approximately 4 ft-L.
g. Capability for presenting moving halftone images.
h. Complete semiconductor scanning circuitry to exercise the model.

A photograph of the completed high-resolution model display is shown in Figure 74; Figure 75 is a schematic diagram of the model. For clarity, only three of the 18 elements in each of the two rows are shown in the figure. As with the main 120-element model, the doubly balanced transcharger circuit of Figure 23 is used. The circuitry enclosed within the dotted block in Figure 75 is the actual display as shown in Figure 74. The remainder of Figure 75 constitutes the electronic system which was used to exercise the display model. The high-resolution model is line-addressed using parallel video input in the fashion of Figure 46, as described in Section II-F. Since the high-resolution model is electrically identical to the experimental model display constructed under Contract No. AF33(615)1193, the electronics constructed for that model were used to exercise the high-resolution model. The electronic system employs conventional transistor circuitry and is described in detail in Reference 3 and briefly in Appendix III.

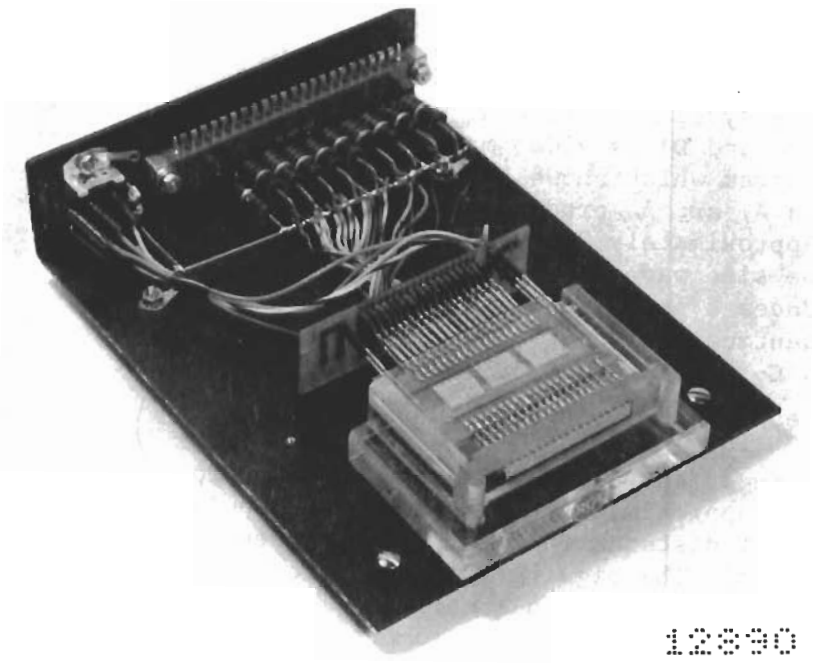

Figure 74. Photograph of the Auxiliary Model to Show High Resolution.

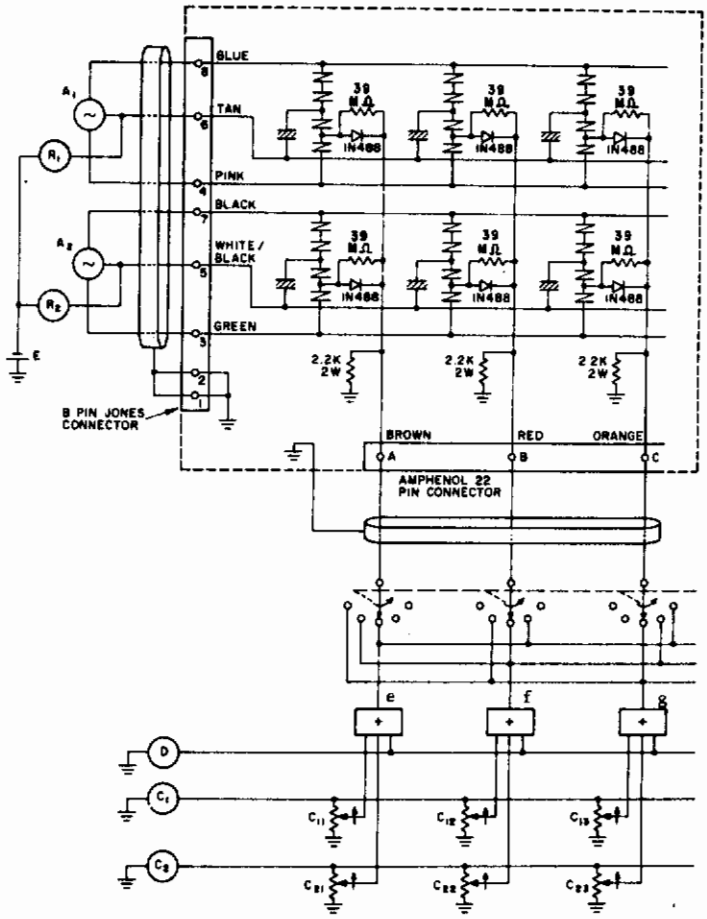

Figure 75.

Schematic Diagram of High-Resolution Model Display.

Basically, the system consists of seven signal sources (generators A_1, A_2, R_1, R_2, C_1, C_2, and D), a video matrix, and a mechanical scanner. Figure 76 is a timing diagram which shows the waveforms produced by the seven generators. Generators A_1 and A_2 produce identical waveforms, a 900-Hz sine wave interrupted for approximately 200 μsec at a 30-Hz rate. It is during this interval, when the sine wave is blanked, that row 1 and row 2 are addressed. Generator R_1 produces a positive pulse approximately 30-μsec wide; generator R_2 produces an identical pulse delayed from that of generator R_1 by 100 μsec. Generators C_1 and C_2 each produce 30-μsec pulses, coincident with the pulses from R_1 and R_2, respectively. During the 33-msec $\left(\frac{1}{30\ \text{Hz}}\right)$ interval between successive addressings, the disturb pulse generator produces 30 μsec disturb pulses at a rate of approximately 12.5 kHz. These pulses realistically simulate the half-select disturbs which would be present in an actual display having over 400 lines. The signals from generators C_1, C_2, and D are fed to the video matrix circuits shown in simplified form in Figure 75. Generators C_1 and C_2 each feed a bank of 18 potentiometers (for clarity only three are shown in the figure); 18 adder circuits (again only three are shown in the figure) derive signals from these potentiometers and from the disturb pulse generator D. The signals at points e, f, and g will thus be: a pulse at the time generator C_1 operates, a pulse at the time generator C_2 operates, and then a chain of disturb pulses. The amplitudes of the pulses that occur when the generators C_1 and C_2 operate depend on the setting of the 36 potentiometers;

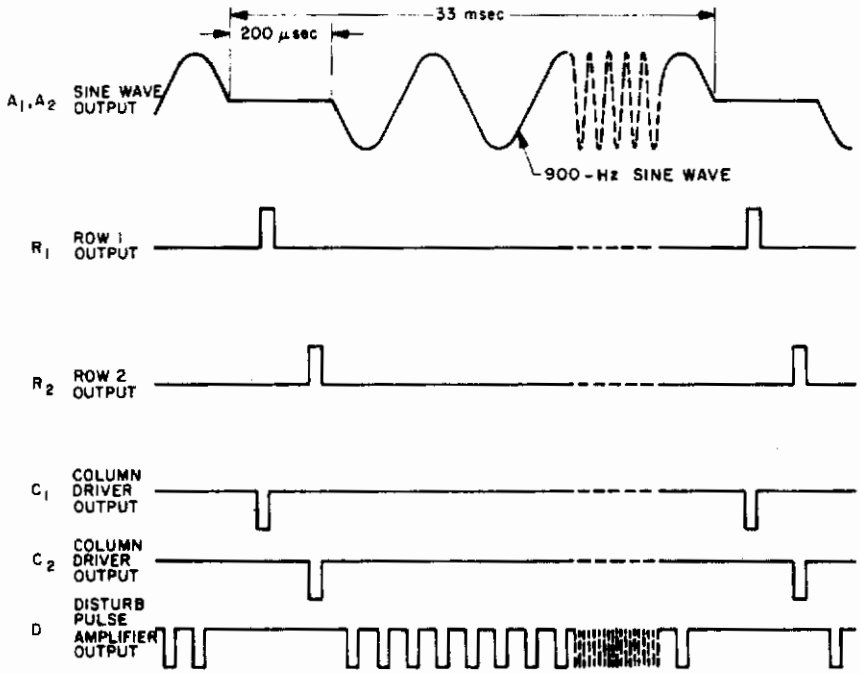

Figure 76.

Timing Diagram for High-Resolution Display Model.

the potentiometers thus establish a video halftone pattern. The outputs from the adder circuits, e, f, g, etc., are connected to an 18-gang, 18-position, solenoid-driven rotary switch (only 3 gangs and 5 positions are shown in the figure); rotation of the switch will cause the video pattern to move on the face of the display screen. With the switch in its initial position, e is connected to column 1, f to column 2, etc. When the switch is advanced one position, e is connected to column 2, f to column 3, etc. As explained in Appendix III, circuitry is provided to operate the switch automatically at rates adjustable from several seconds per step to several steps per second, thus permitting the continuous display of moving images. Manual operation and a homing position are also provided. Figure 77 shows the column bus waveforms for three typical test patterns. The waveforms are shown with the switch stationary. When the switch is stepping, the white field and black field waveforms will not change, but the checkerboard waveforms will alternate between odd and even column busses.

Figure 78 illustrates the mechanical construction technique that was used for the high-resolution model. The 36 electroluminescent cells (2 lines of 18 each) having a nominal voltage rating of 50 V rms are fabricated on a single glass substrate. Separate semitransparent TIC electrodes are provided for each of the two rows. The 36 separate electroluminescent patches (each 0.1-in. square) are defined by structuring the back electrode. A gold-plated female connector placed orthogonal to the substrate is attached to each of 36 back electrodes and to the two semitransparent TIC electrodes. The entire electroluminescent panel is encapsulated in epoxy resin to provide a moisture seal.

To construct the transchargers for the model a number of 0.4 x 0.5 in. x 3-mil-thick dry-pressed lapped 50/50-14-2Nb ferroelectric chips were prepared. The chips were each electroded for six transchargers as shown in the magnified photograph of Figure 79. Since the ceramic material is translucent,

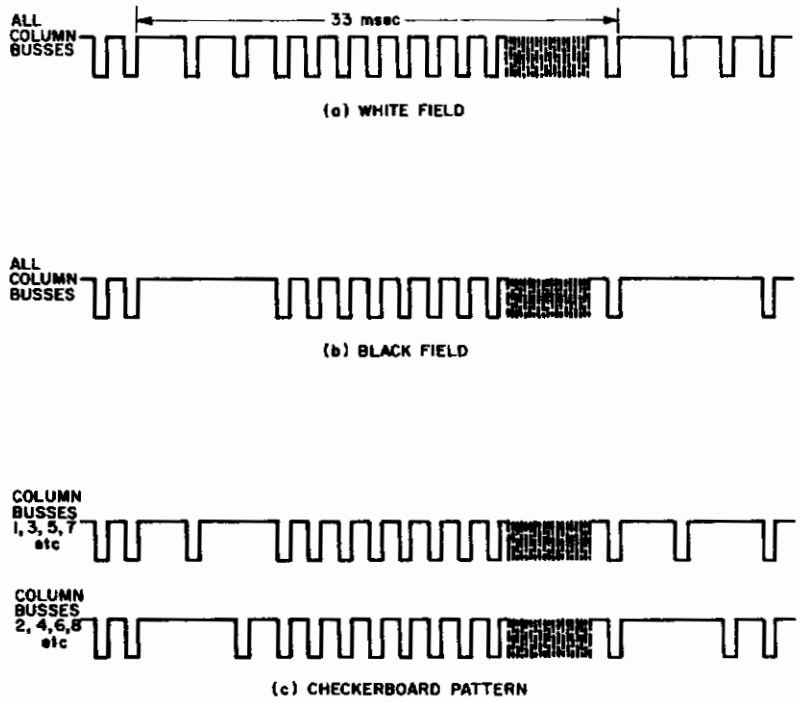

Figure 77. Column Bus Waveforms for Typical Patterns.

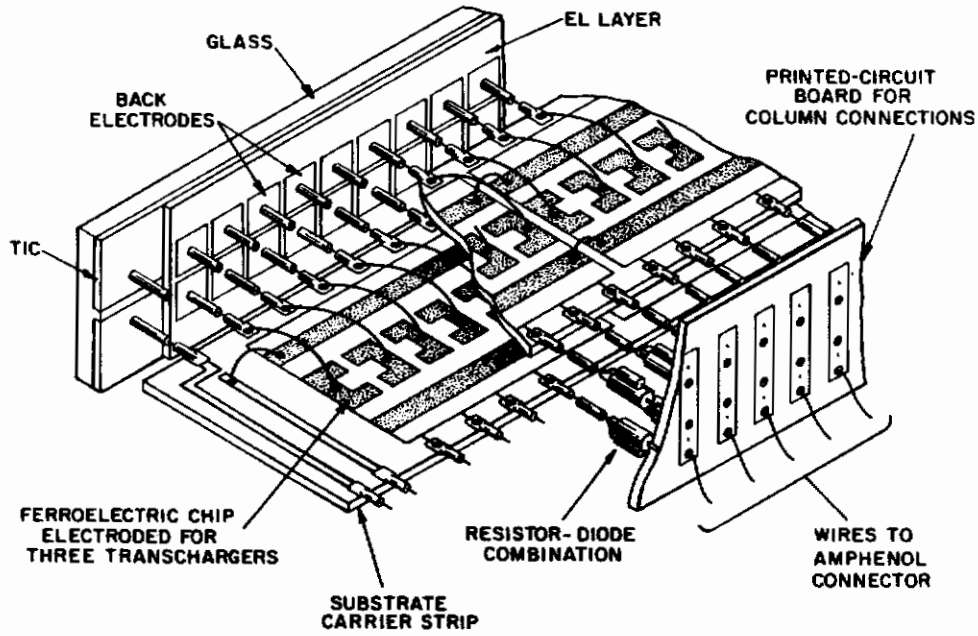

Figure 78. Construction of High-Resolution Experimental Model.

the bottom electrodes show as dark areas in the photograph. As can be seen in the photograph, the electrode pattern forms six groups of four series-connected capacitors. The upper and lower horizontal top electrodes in the photograph are the row busses. The horseshoe-shaped electrodes form the midpoint of each of the groups of four capacitors and are connected to the electroluminescent cell. The horseshoe shape was used to ease the requirements on mask registration when the electrodes are evaporated. With this arrangement, small errors in mask registration do not affect the area defined by the crossover of the electrodes. The electrode areas were chosen to give an EL/FE area ratio of 14.8. As indicated in Section II-D, this favors gray-scale uniformity at the expense of brightness. The electroded ceramic chips (three for each of the two lines) are mounted on printed-circuit board substrate carrier strips as shown in Figure 78. The carrier strips have conductive paths leading from the edges of the ceramic chips to the edges of the carrier strip where male contact pins are mounted. On one edge, these pins mate with the female connectors on the electroluminescent panel, and on the other edge with similar female connectors attached to the diode resistor combination. Connections between ceramic chips and from the ceramic chips to the conductive paths on the substrate were made with wire leads attached with silver paste. In all cases where silver paste connections were made to the ceramic chips, the silver paste was kept remote from the active ferroelectric area to avoid the degradation caused by the migration of silver ions. The ceramic chips are not in any way attached to the substrates but are simply held in place by the wire leads connected to them. The necessary row and column connections are made by means of a printed-circuit board mounted parallel to the electroluminescent panel. The diodes and resistors are mounted in cordwood fashion on this printed-circuit board and are fitted with female connectors. These mate with the male pin connectors on the back edge of the substrate carrier strips. With this construction technique both the electroluminescent panel and the transcharger strips could be easily assembled and disassembled to facilitate experimentation.

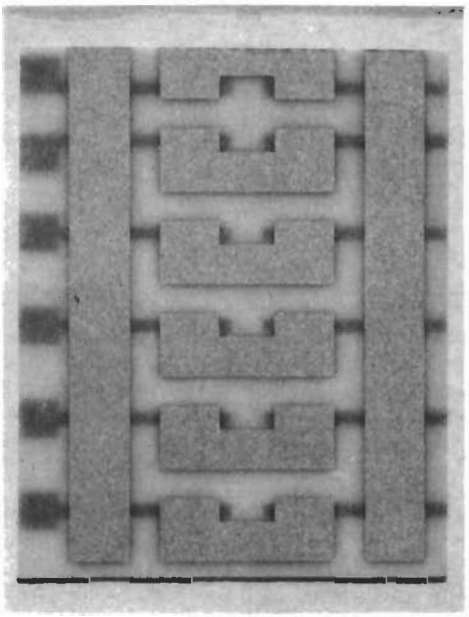

Figure 79. Magnified Photograph of Ferroelectric Chip Electroded to Form Six Transchargers.

Operating tests of the completed model were extremely successful. All 36 elements worked with essentially perfect contrast (in all cases the "off" brightness was less than 1 percent of the "on" brightness indicating a contrast ratio in excess of 100 to 1), peak brightnesses of approximately 4 ft-L, excellent gray-scale control, negligible crosstalk, and smear-free moving images. Figure 80 shows the brightness vs column pulse amplitude transfer characteristics for the 18 elements of the first (top) row. The elements are numbered 1 to 18 from left to right. Figure 81 shows the transfer characteristics for the second (bottom) row of elements and Figure 82 the average transfer characteristic for all 36 elements. These curves were taken with 350-V rms 900-Hz sine-wave excitation, row pulse amplitude of 125 V, bias voltage of -125 V and full 60-V disturbs at 12.5 kHz. The brightness scale in Figures 80, 81, and 82 is accurate on a relative basis but the absolute value should be taken as only approximate. Since the 0.1-in. square display elements were too small to fill the measuring area of the available spot brightness meter, it was necessary to derive a correction factor for the meter based on the measured brightness of a larger cell whose brightness had been matched by eye to the 0.1-in. square electroluminescent elements.

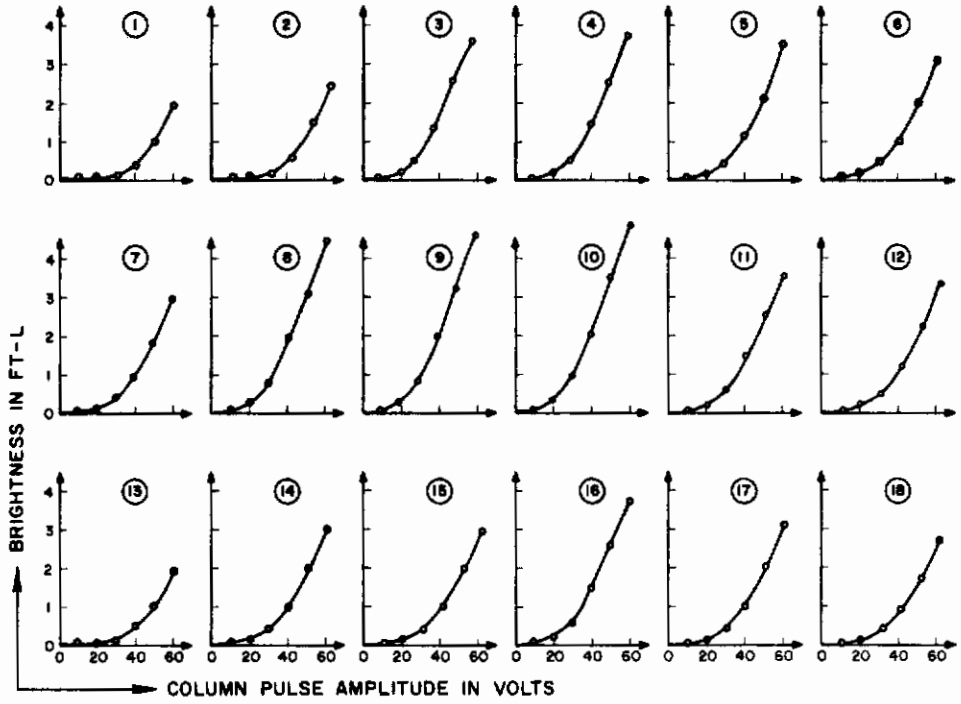

Figure 80. Brightness vs Column Pulse Amplitude for the 18 Elements in Row 1 of the High-Resolution Experimental Model.

The data of Figures 80 and 81 show a variation of a little more than 2 to 1 in peak brightness for the 36 elements. This variation is attributed to the cumulative effects of the mechanical tolerances on the cell area, the ferroelectric areas, and the thickness of the ferroelectric chips and to the effects

of fringing fields in the ferroelectric (the linear dimensions of the electrodes were in some instances only about four times greater than the thickness of the ferroelectric). It is clear that greater mechanical precision than was achieved here will be required to achieve good uniformity in high-resolution displays.

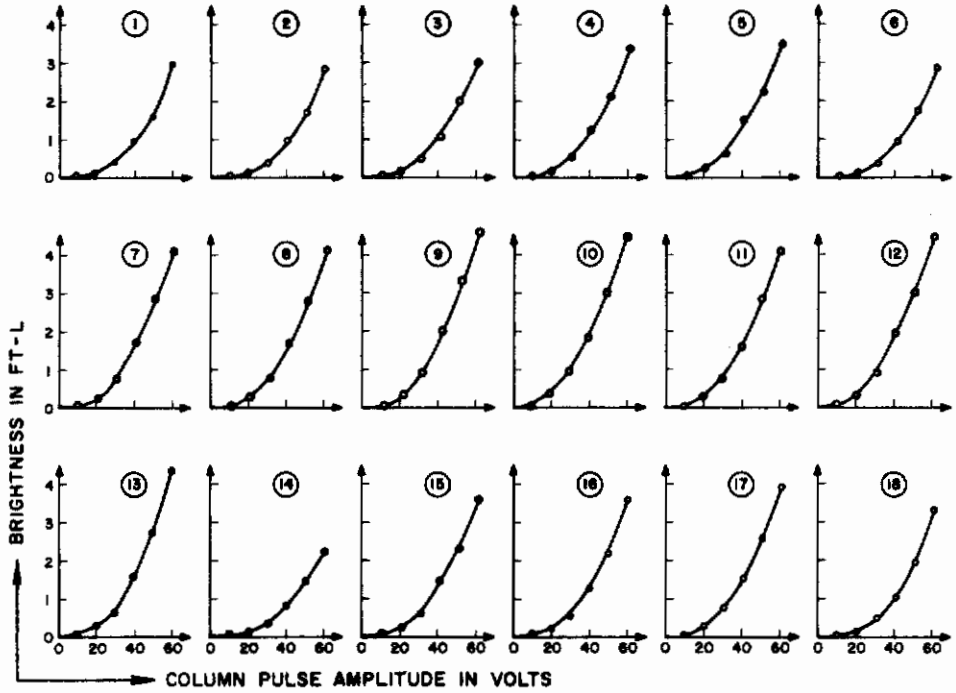

Figure 81. Brightness vs Column Pulse Amplitude for the 18 Elements in Row 2 of the High-Resolution Experimental Model.

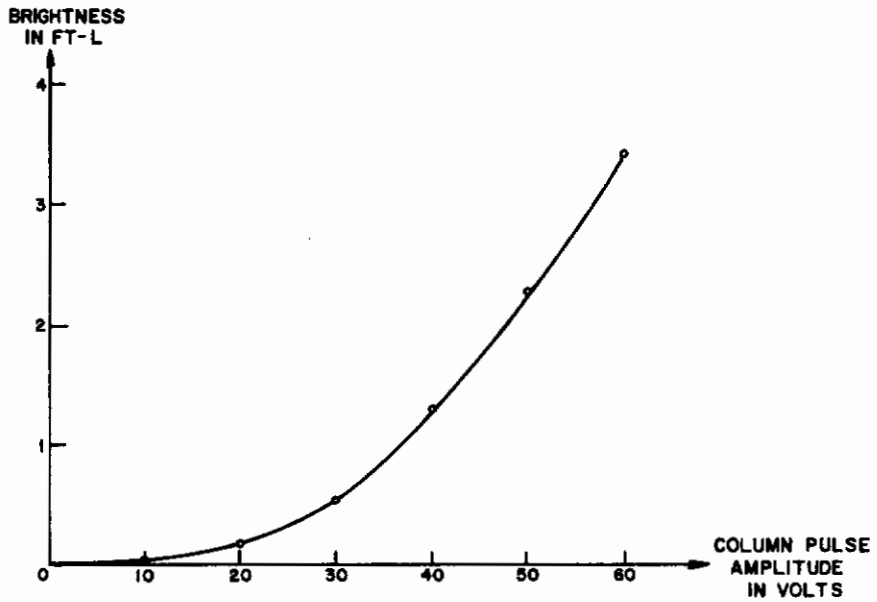

Figure 82. Brightness vs Column Pulse Amplitude for the High-Resolution Experimental Model (averaged values for all 36 elements).

Figures 83 and 84 are unretouched off-the-screen photographs of the working experimental model display. Figure 83 shows a geometric pattern with some cells fully on and others fully off. Figure 84 shows a gray-scale pattern with some elements fully on, some fully off, and some set to intermediate values of brightness. The photographs of Figures 83 and 84 were taken with subdued but not totally darkened room lighting. Some halation is noticeable in the photographs, especially adjacent to the bright end of the shading bar in Figure 84. This is due only to the scattering of light by the glass substrate on which the electroluminescent cell is fabricated; there is no electrical crosstalk. Although it cannot be shown in the photographs, by operating the stepping switch in the model, the patterns in Figures 83 and 84 (or any other patterns) were made to move from left to right along the face of the display. Even at the maximum rate of 8 steps per second, no smearing of the image was discernible.

Taken together these three models demonstrate brightness as high as 48 ft-L, contrast ratio in excess of 100 to 1, geometric resolution as great as 10 elements per inch, capability for producing gray scale, and a frame rate which allows the reproduction of moving images without blurring or flicker. Both spot-addressing and line-addressing have been demonstrated and one of the models demonstrated the usefulness of the basic transchanger electroluminescent circuit for bar graph type displays.

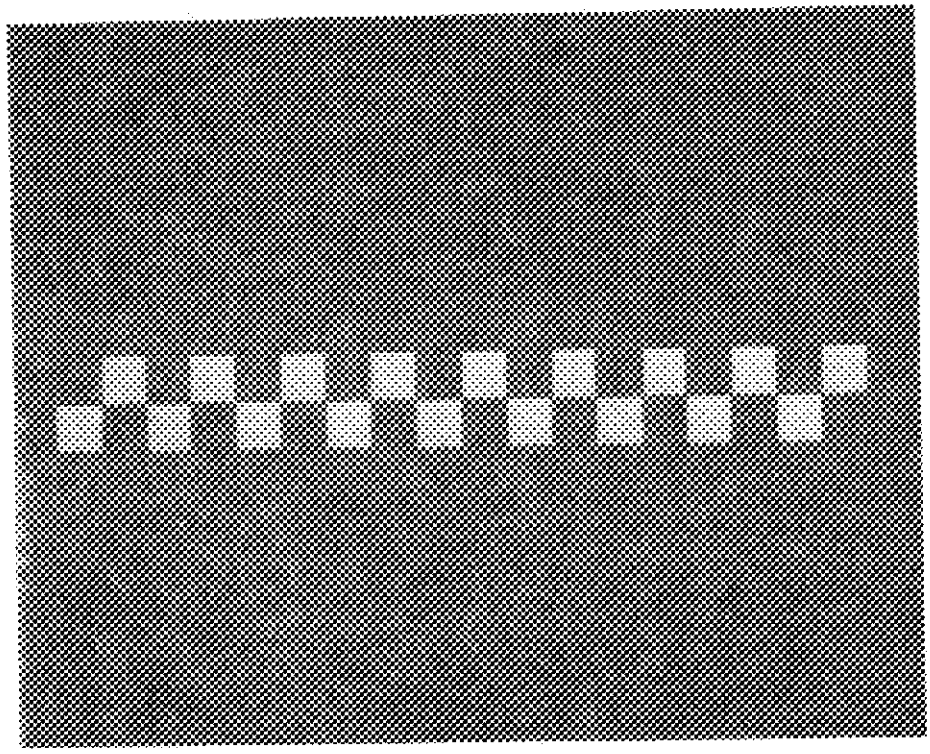

Figure 83. Off-the-Screen Photograph of High-Resolution Display Model Showing a Geometric on-off Pattern.

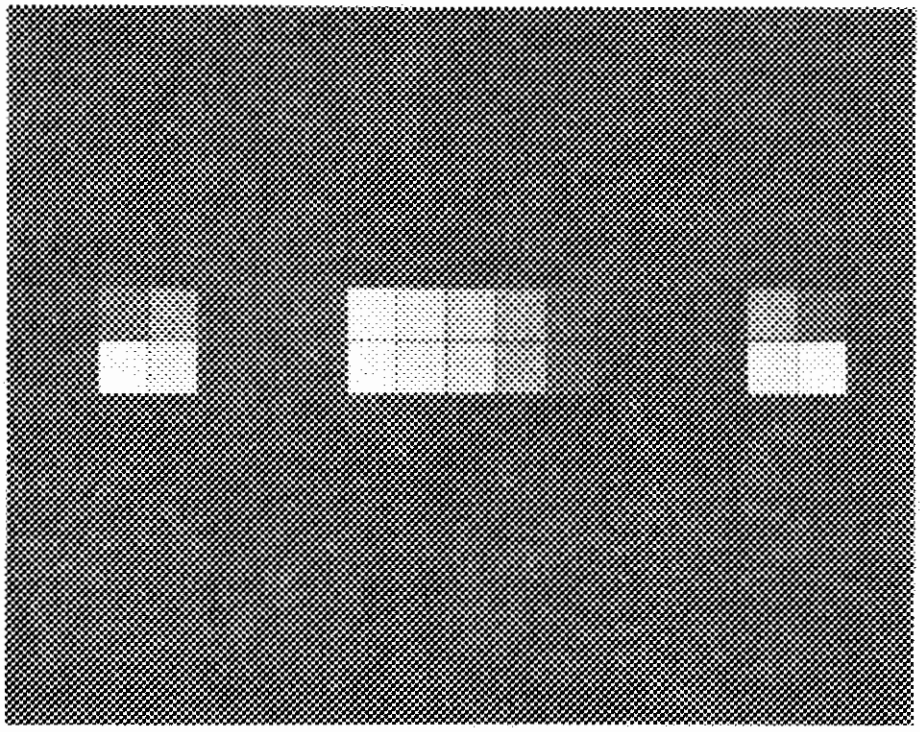

Figure 84. Off-the-Screen Photograph of High-Resolution Display Model Showing a Gray-Scale or Halftone Pattern.

The performance of the models clearly demonstrates the potential of using ferroelectric control circuits and electroluminescent elements for high-brightness, high-resolution all-solid-state matrix displays for moving halftone images, and for bar graph and other digital displays. At the same time, however, it indicates the need for further research to achieve better uniformity and improved fabrication methods.

SECTION III

SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

A. SUMMARY AND CONCLUSIONS

The key element in the proposed electroluminescent display matrix is the ferroelectric transcharger. Because of the importance of the ferroelectric, the major effort in a related program under Contract No. AF33(615)1193 was devoted to a thorough investigation of ceramic ferroelectrics from the ternary system $Pb_{.99}[(Zr_xSn_y)_{1-z}Ti_z]_{.98}Nb_{.02}O_3$. Twenty-seven different compositions from this system were studied in detail. The data from these studies indicate clearly that $Pb_{.99}[(Zr_{.50}Sn_{.50})_{.86}Ti_{.14}]_{.98}Nb_{.02}O_3$ is the best compromise choice for low coercivity, high squareness, and stability with life. This material, designated 50/50-14-2Nb, has an initial E_c = 6.7 kV/cm, a squareness S = 0.75, a 15-percent increase in E_c after 1000 hours, and negligible decay in polarization. A sufficient quantity of 50/50-14-2Nb material was obtained from the Clevite Corporation for use in circuit experiments and in the experimental models.

In addition to the 27 compositions already mentioned, 19 compositions with additives other than niobium were prepared and tested. Although some of the materials had high squareness ratios, none of the 19 samples was superior to the 50/50-14-2Nb material. Other material studies carried out under Contract No. AF33(615)1193 were concerned with surface preparation techniques, the effects of electrode area, and the uniformity of the ferroelectric properties.

Although, from a practical standpoint, the 50/50-14-2Nb material has satisfactory performance with life, the mechanism of the small decay which does occur (and the large decay which occurs in other materials) is not fully understood. Some experiments were conducted to bring out the nature of the degradation observed with repeated AC cycling. The experiments showed that the degradation could be ascribed to the formation of leakage paths and to domain changes. Were the decay mechanisms better understood, it is possible that improved materials could be developed.

The ceramic ferroelectrics may be fabricated in a variety of ways. All of the 50/50-14-2Nb samples used in the circuit studies and in constructing the experimental models were prepared by conventional cold-pressed ceramic techniques. A better process, known as doctor-blading, which permits the direct batch-fabrication of many transchargers at once, as is desired for a matrix display, has been investigated under Contract No. AF33(615)1193. Although the early doctor-bladed samples were badly warped and wrinkled, it was possible to make electrical tests which showed that the doctor-bladed material was superior electrically to the conventionally fabricated material. The firing techniques must still be perfected, however, to eliminate the warping and wrinkling.

The study and evaluation of display panel circuitry was carried out with the principal emphasis placed on techniques to improve brightness and contrast. This work led to the invention of a new transcharger circuit. Known as the

doubly balanced transcharger, the new circuit gives greatly improved performance. Brightnesses approaching 20 ft-L have been achieved with contrast ratios in excess of 100 to 1. Detailed studies of this doubly balanced transcharger circuit showed that both the peak brightness and the slope of the transfer characteristic are functions of the EL/FE area ratio. An EL/FE area ratio of about 15 was found to be optimum for a gray-scale display; a ratio of about 12 is preferred for an "on-off" display. In its present form the doubly balanced transcharger requires a diode at each element location in the display panel. From a fabrication point of view, this is a severe disadvantage, but from a system point of view the diode offers two distinct advantages. Since self-resetting is achieved through the reverse leakage of the diode, the need for reset pulses is eliminated, and since the diode has a much lower capacitance than a ferroelectric, the column driver current requirements are reduced.

The studies of the doubly balanced transcharger circuit showed it to be a specific member of a general family of transcharger circuits. Some other members of this family were investigated in detail, and one circuit was found to give a brightness of nearly 50 ft-L with a contrast in excess of 100 to 1. Tests showed that all of the circuits tolerated well the deleterious effects of half-select disturb pulses which would be present in a full-scale matrix display.

Transchargers with logic capability have also been developed; these circuits are especially suited for use in bar graph, pointer, and alphanumeric displays.

A thorough study of addressing techniques has led to the development of a number of means for addressing matrix displays. Low-resolution displays may be spot-addressed, whereas high-resolution displays must be line-addressed. In the latter case, if the video information is supplied serially in real time, a high-speed horizontal storage register is required. Techniques for scanning such a register have been developed, and the possibility of using transfluxors to realize the actual register elements has been studied. Although transfluxors can be used at low speeds, they are not satisfactory register elements at the submicrosecond speeds required for a high-resolution real-time display. The use of capacitive storage and semiconductor amplifying circuits promises, however, to provide a satisfactory realization of the required storage register.

To demonstrate the feasibility of a ferroelectric electroluminescent display, three experimental model displays were constructed. Taken together, the models demonstrate brightness as high as 48 ft-L, contrast ratios in excess of 100 to 1, geometric resolution as great as 10 elements per inch, capability for producing gray scale, and a frame rate which allows continuity of motion without blurring or flicker. The models all use the new doubly balanced transcharger circuit.

The main model has 120 elements, each 0.25-in. square, arranged as ten rows of 12 elements each. The model operates at a frame rate of 83.3 frames per second and is spot-addressed with a spot-addressing time of 41.6 μsec. Producing a brightness of 15 ft-L with a contrast in excess of 100 to 1, the model shows moving images with negligible crosstalk and no observable smear.

Although conventionally fabricated 50/50-14-2Nb ceramic was used in the model, a semi-integrated construction technique was employed with two transchargers formed on each 0.4 x 0.5 in. x 3-mil-thick ferroelectric chip. Simple electronics using conventional transistor circuitry were designed and constructed to exercise the display. To provide video signals for the display, the electronics include a vidicon camera. It is thus possible to display moving halftone images in real time.

A second model to demonstrate high brightness has two elements, each 0.5-in. square, and operates at a brightness of nearly 50 ft-L with a contrast in excess of 100 to 1. This model is provided with simple transistor electronics which include the capability for either analog or digital addressing of the display.

The third model, to demonstrate high resolution, has 36 elements, each 0.1-in. square, arranged as two lines of 18 elements each. The model operates at a frame rate of 30 frames per second and is line-addressed with a line-addressing time of 30 μsec. Producing a brightness of 4 ft-L with a contrast in excess of 100 to 1, the model shows moving halftone images with negligible crosstalk and no noticeable smear. Although conventionally fabricated 50/50-14-2Nb ceramic was used in the model, a semi-integrated construction technique was employed with six transchargers formed on each 0.4 x 0.5 in. x 3-mil-thick ferroelectric chip. Simple electronics, using conventional transistor circuitry, were designed and constructed to exercise the model display. To provide video signals for a moving halftone image, an adjustable resistor matrix and a simple mechanical scanner are provided. The electronics include circuitry to generate disturb pulses to realistically simulate the half-select disturbs which would be present in a display having over 400 lines.

The successful operation of these experimental models under realistic conditions clearly demonstrates the feasibility of using ferroelectric electroluminescent elements in a matrix display.

B. RECOMMENDATIONS

To achieve a practical ferroelectric electroluminescent display, it is recommended that future research be done on ferroelectric materials, electroluminescent cells, display panel circuitry, panel fabrication techniques, and peripheral scanning and driving circuitry.

Although the 50/50-14-2Nb ceramic material has proved very satisfactory for the circuit experiments and for the experimental models constructed thus far, there is considerable room for improvement. Higher squareness, lower coercivity, and better performance with life are desired. Toward this end, the compositional studies on ceramics should be extended. Materials having additives other than niobium should be studied further so that the effects of these additives may be thoroughly evaluated. Ceramic systems other than lead stannate zirconate titanate should also be explored. In particular, systems with lower crystal distortion should be studied.

The physical mechanism of the decay in ceramics should be studied further. Additional samples of representative compositions should be decayed by exposure to various intervals of 400-Hz excitation and then examined carefully for physical and/or chemical changes. The work should be directed toward eliminating the decay and/or finding a means to eliminate its effects.

Although the principal emphasis should be given to ceramics, other ferroelectrics should be studied too. For example, KNO_3, YM_nO_3, and other materials not previously considered should be investigated for possible transcharger use.

Fabrication techniques for batch-fabricating ceramic ferroelectric transchargers require further study. Since doctor-blading is at present the most promising fabrication technique, this method should be studied further. Concentrating on the 50/50-14-2Nb material, firing schedules should be perfected so that flat wrinkle-free sheets of ceramic ferroelectric with good electrical properties can be produced.

For a practical display, electroluminescent cells with higher brightness and longer life are required. Emphasis should be given to techniques that promise to achieve these improvements without requiring substantial increases in the operating voltage. Work should also be done to find a better means of bonding electrical connectors to the back electrodes of the electroluminescent panels.

The general transcharger display circuit should be investigated in more detail. Although several specific circuits have been studied thoroughly, an exhaustive study of the entire family of possible circuits has not been made. The various circuit parameters should be varied systematically and the circuit behavior as a function of the parameters thus be determined. The objective of this work should be to optimize the circuit parameters for high-brightness and high-contrast operation with the lowest possible power and the least sensitivity to component tolerances. Particular emphasis should be given to finding a means to eliminate the diode from the circuit. Analytical and experimental verification should be made of the various design modifications that may be found. The use of ferroelectric control circuitry for other types of electroluminescent displays, such as bar graphs and alphanumeric indicators, should be studied further.

Further work should be done on panel fabrication techniques. Means to integrate the doctor-bladed ferroelectric with the electroluminescent cells should be studied. This work should include studies of various interconnection techniques including spring connectors and gang-soldering as well as evaporated and printed interconnections. The possibility of using a common substrate for both the ferroelectric and electroluminescent materials should be explored. Also, the use of laminated ferroelectric structures with electrodes and interconnections embedded wholly within a monolithic block of ferroelectric material should be studied.

Future work on scanning and driving circuitry should emphasize line-addressing. In particular, the problem of the horizontal storage register required in a line-addressed display with serial video input must be attacked in earnest. An all-semiconductor storage register should be developed and

efforts made to simplify it as much as possible in order to make integrated construction ultimately possible. Further work should also be done on means to provide the excitation signals for the electroluminescent cells. Techniques should be sought for generating the required signals with high efficiency and for distributing them without the need for transformers or other complex circuitry at each row of the display.

SECTION IV

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APPENDICES

APPENDIX I

ELECTRONICS FOR THE MAIN 120-ELEMENT MODEL

To exercise the main 120-element model display, electronic circuitry was required to provide the necessary row and column addressing signals, excitation signals for the electroluminescent cells, and a source of video input signals. Suitable transistor circuitry was designed and constructed to perform these functions. The circuitry includes a vidicon camera to provide input signals, thus permitting continuous real-time display of moving halftone images. Figure 85 shows the complete 120-element display system consisting

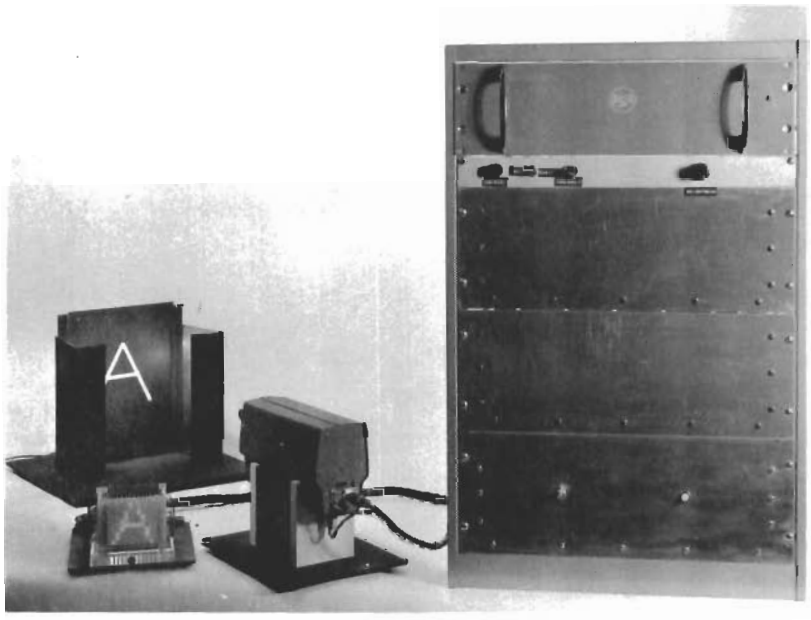

Figure 85. Complete 120-Element Display System.

of the display itself, the vidicon camera and the electronic system. Figures 86 and 87 are front and rear photographic views, respectively, of the complete electronic unit; the details of the circuitry are described in this Appendix.

Figure 88 is a block diagram of the electronic system for the 120-element model, and Figures 89 and 90 are timing diagrams for the electronics. The circled numbers identifying the waveforms in Figure 89 and 90 correspond to the similarly identified points in Figure 88. Also, note that the time scales are different in Figures 89 and 90.

If we refer to Figures 88, 89, and 90, the operation of the system is as follows: The 24-kHz clock provides the master timing signal and establishes the spot time T_S = 1/24 kHz = 41.6 μsec for the display. The 24-kHz buffer provides both positive and negative outputs. An output from the 24-kHz clock is fed to the three-stage divide-by-24 divider chain. The last stage of the divider chain which operates at 1 kHz, is the 1-kHz square wave source which establishes the line interval T_L' = 1/1 kHz = 1 msec for the display.

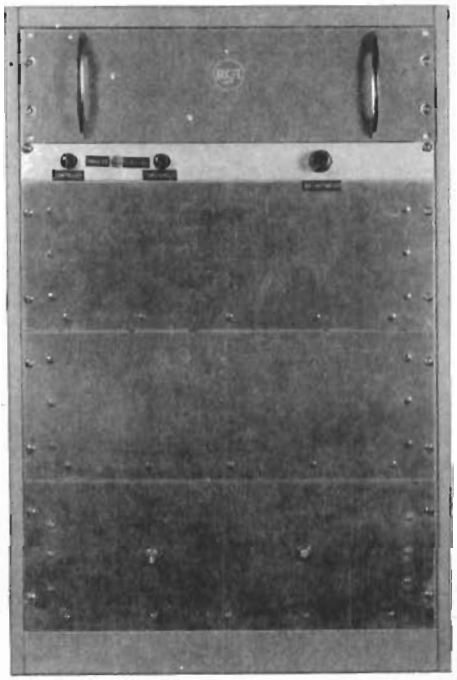

Figure 86.
Electronics for 120-Element
Display Model (front view).

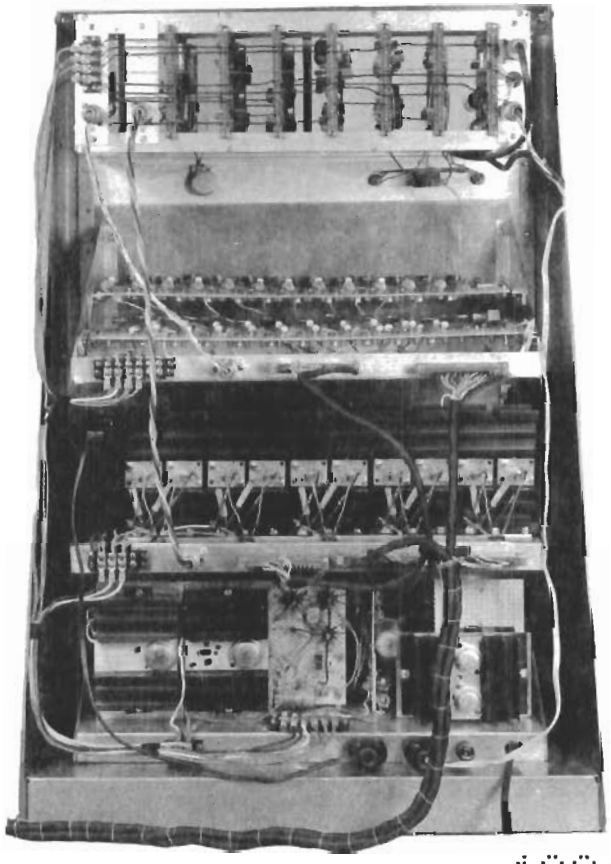

Figure 87.
Electronics for 120-Element
Display Model (rear view).

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(The line time $T_L = T_L'/2 = 500$ μsec since half of the interval T_L' is allowed for horizontal retrace and only one phase of the continuously gated excitation signal is provided.) Two outputs (phases A and B) of opposite polarity are provided from the 1-kHz square wave source. In addition, the 1-kHz trigger source provides 1-kHz trigger signals coincident with the leading and trailing edges of the phase A 1-kHz square wave. An output from phase A of the 1-kHz square wave source feeds the two-stage divide-by-12 divider chain. The last stage of this divider chain, which operates at 83.3 Hz, drives the 83.3-Hz trigger source and establishes the frame time $T_F = 1/83.3$ Hz = 12 msec for the display. The 83.3-Hz trigger source provides both positive and negative outputs. These various timing signals control the remaining circuitry of the electronics.

The excitation waveform generator consists of a 3-kHz square wave generator, a 1-kHz gate generator, a gate, and two preamplifiers. The 3-kHz square wave generator and the 1-kHz gate generator are synchronized by the 1-kHz trigger signals from the 1-kHz trigger source. Since the gate signal is approximately 420 μsec wide, the output of the gate consists of approximately 1-1/4 cycles of the 3-kHz square wave. This signal is amplified by the two excitation waveform preamplifiers which each drive 5 of the 10 push-pull class B excitation amplifiers associated with each of the 10 rows of the display.

Vertical scanning of the display is achieved by means of a 12-stage shift register whose operation is timed by signals from the 83.3-Hz trigger source and the 1-kHz trigger source. Since the display has only 10 lines, the first and last outputs from this vertical shift register are not used. This allows time for vertical retrace of the vidicon camera. The shift register output pulses have a duration of 1000 μsec. These pulses are applied to the row drivers in coincidence with the phase B 1-kHz square wave. The row driver outputs are thus 500-μsec pulses occurring during the interval that the excitation waveform is blanked. These row-select pulses are added to the excitation signals and fed to the 10 rows of the display.

Video signals for the display are obtained from a modified vidicon camera. The vertical deflection of the camera is synchronized by the 83.3-Hz trigger source. Horizontal blanking and deflection signals for the camera are obtained from a deflection generator synchronized by the phase A 1-kHz square wave. The video signal from the camera is amplified and synchronously clamped (by the phase B 1-kHz square wave) in two identical switch-selected amplifiers. For analog operation of the display, the amplified video is fed directly to the column drivers. For digital operation, a video digitizer is interposed in the video path. The video digitizer operates synchronously under control from the 24-kHz clock.

Horizontal scanning of the display is achieved by means of a 12-stage shift register whose operation is timed by signals from the 1-kHz trigger source and the 24-kHz clock. The outputs from the shift register are fed to the 12 column drivers. In addition to the shift register signals, the column drivers receive the video signal as an input. The resultant outputs from the column drivers are pulses whose time occurrence is determined by the signals from the shift register and whose amplitude is determined by the video signal.

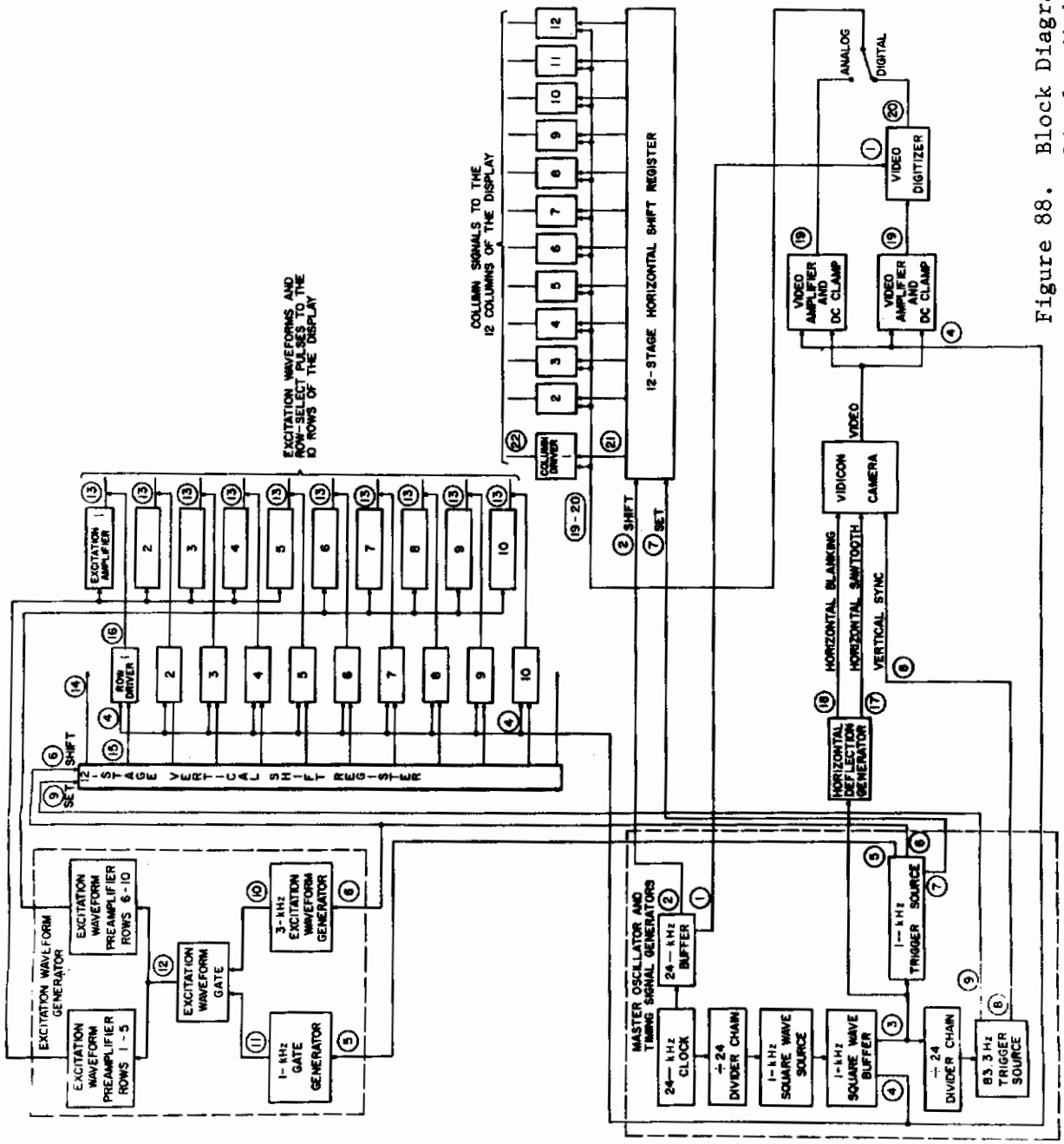


Figure 88. Block Diagram of 120-Element Display Model Electronics.

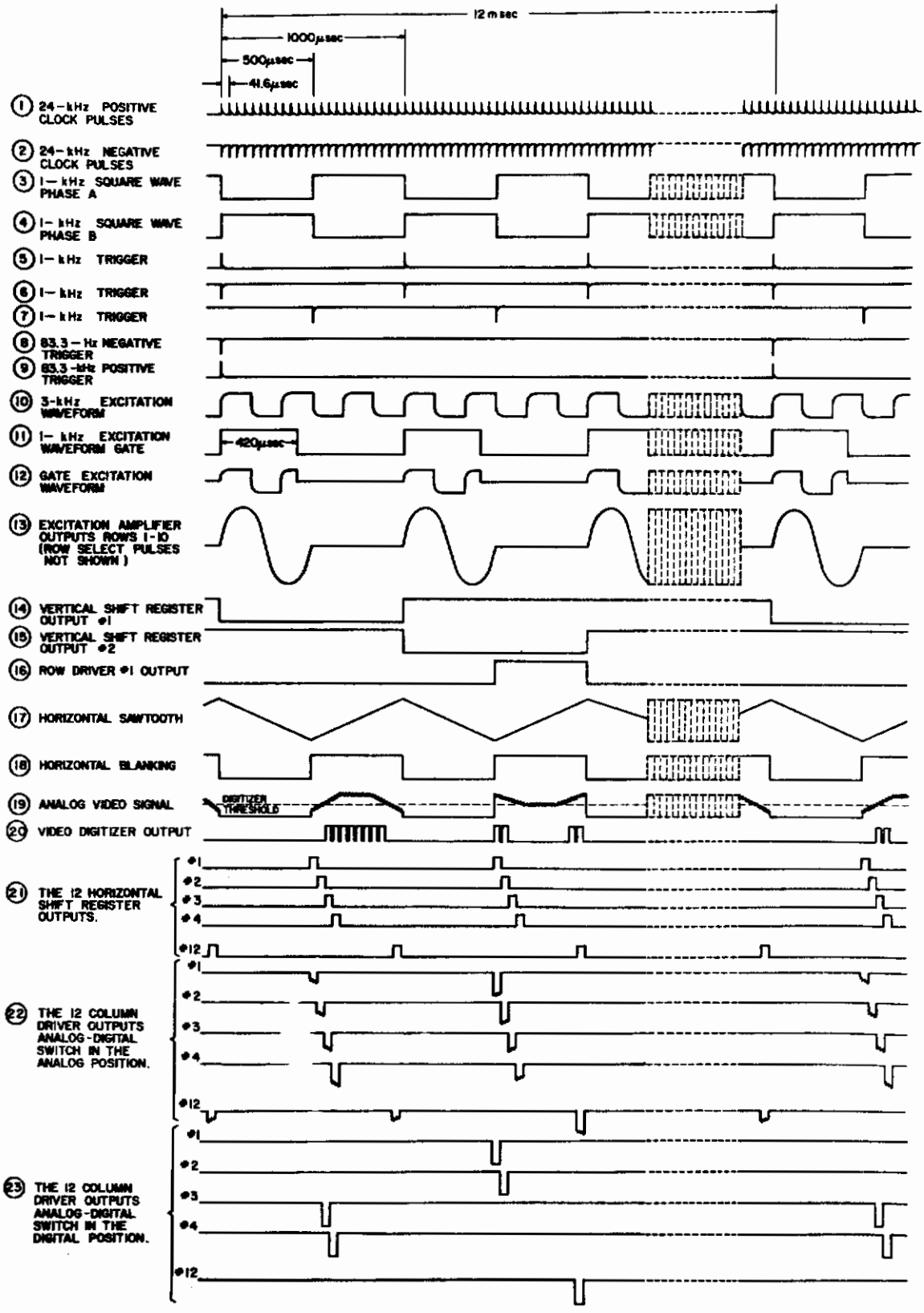


Figure 89. Timing Diagram for 120-Element Display Model, Part I.

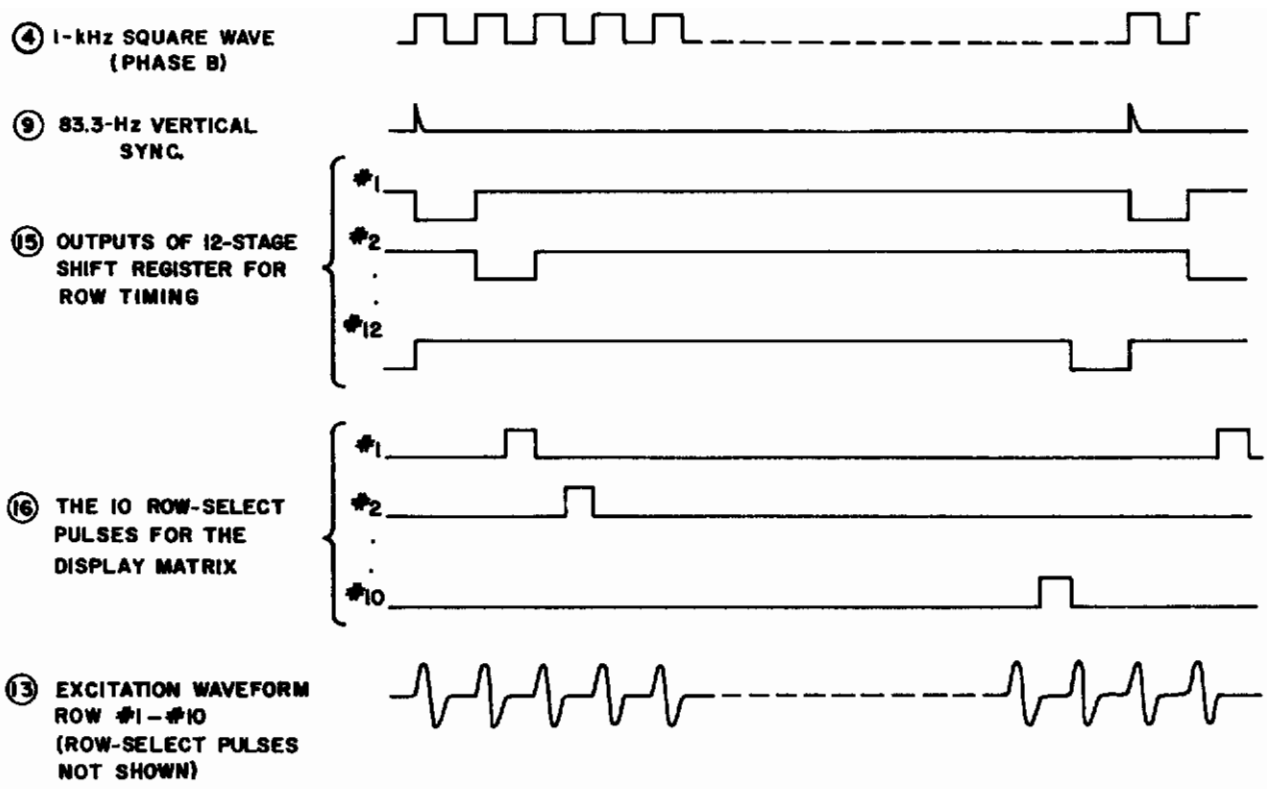


Figure 90. Timing Diagram for 120-Element Display Model, Part II.

As can be seen from the photographs of Figures 86 and 87, the display model electronics are built in a standard 30-inch table-top relay rack and consist of four separate chassis. The uppermost chassis in the rack contains the master oscillator and timing signal generators, the excitation waveform generator, the horizontal deflection generator, the video amplifier and clamps, and the video digitizer. The circuits are mounted on 7 plug-in boards. Operating controls for the electronics are mounted on a narrow panel directly beneath the top chassis in the rack. The second chassis from the top contains the vertical and horizontal shift registers and the row and column drivers. The third chassis from the top contains the ten excitation amplifiers, and the bottom chassis contains the power supplies for all of the circuitry. Following is a detailed description of all the circuitry in the display model electronics.

A. MASTER OSCILLATOR AND TIMING SIGNAL GENERATORS

The row and column addressing circuits of the display matrix are timed by waveforms of the following three distinct but synchronized frequencies:

> 24-kHz clock pulses from the master oscillator establish the size of one video element which corresponds to one cell in the display matrix.

One kHz is the row frequency of the display. A square wave and pulse signals of two different phases at that frequency are used to accomplish the necessary timing functions.

83.3-Hz pulses establish the frame rate of the matrix display.

The 1-kHz and 83.3-Hz signals are also used to synchronize the scanning waveforms of the TV camera as well as to generate the excitation waveform for the display.

Plug-in boards No. 4 and No. 5 in the uppermost chassis in the rack contain the circuits that generate the timing signals at the above-described frequencies. Each timing signal is made available in positive as well as negative phase from a source of low output impedance. Figure 91 is a wiring diagram for plug-in board No. 4, and Figure 93 the diagram for board No. 5. Figures 92 and 94 illustrate the waveforms at various points in these circuits.

In Figure 91, transistor T1 and its associated components form a blocking oscillator which produces the 24-kHz clock pulses. The RC timing network is in the emitter circuit of T1. The frequency of the oscillator may be adjusted over a limited range by potentiometer B. The collector of buffer stage 72 functions as a source of 24-kHz negative clock pulses, and its emitter as a source of positive pulses as illustrated by waveforms 5 and 6 in Figure 92. T3 is a blocking oscillator type frequency-divider circuit similar to T1. 24-kHz negative pulses are applied to the base of T3 to synchronize the oscillator waveform. Potentiometer C is adjusted to obtain frequency division by a factor of 6. Transistors T4 and T5 form a bistable circuit. Positive pulses from T3 are applied to the bases of both T4 and T5. Alternate pulses on the bases of T4 and T5 are effective in causing a change of state of the bistable circuit, and a square waveform results across the collector load of T4 or T5 as illustrated by waveform 3 in Figure 92. Consequently, frequency division by a factor of 2 is achieved by the circuit. The waveform on the collector of T4 is now differentiated, and the resulting pulses are applied to the bases of T6 and T7 which also form a bistable circuit. This stage then likewise performs division by a factor of 2. Since a bistable circuit is more sensitive to pulses trying to trigger a stage off rather then on, the differentiating networks must be such that the negative polarity pulses on the bases of T6 and T7 are insufficient in amplitude to cause a transition in the state of the circuit. Waveforms 1 through 4 in Figure 92 show the signals at various points of the circuits described thus far. Transistor T8 is biased so that the 1-kHz input waveform causes the stage to cut off during its peak positive excursion. The top of the resulting 1-kHz square wave output signal (designated the phase B signal) on the emitter of T8 is then truly flat as shown by waveform 8 in Figure 92. The emitter follower T9 provides a 1-kHz square wave output signal of opposite polarity (designated as the phase A signal) as illustrated by waveform 7 in Figure 92.

The 1-kHz waveform of phase A is applied to terminal No. 21 of plug-in board No. 5, which has the function of generating 1-kHz timing pulses as well as the 83.3-Hz synchronized timing signals. First, the 1-kHz square wave is applied to differentiator networks in the base circuits of transistors T4 and T5. Transistor T4 is normally biased off so that only negative pulses

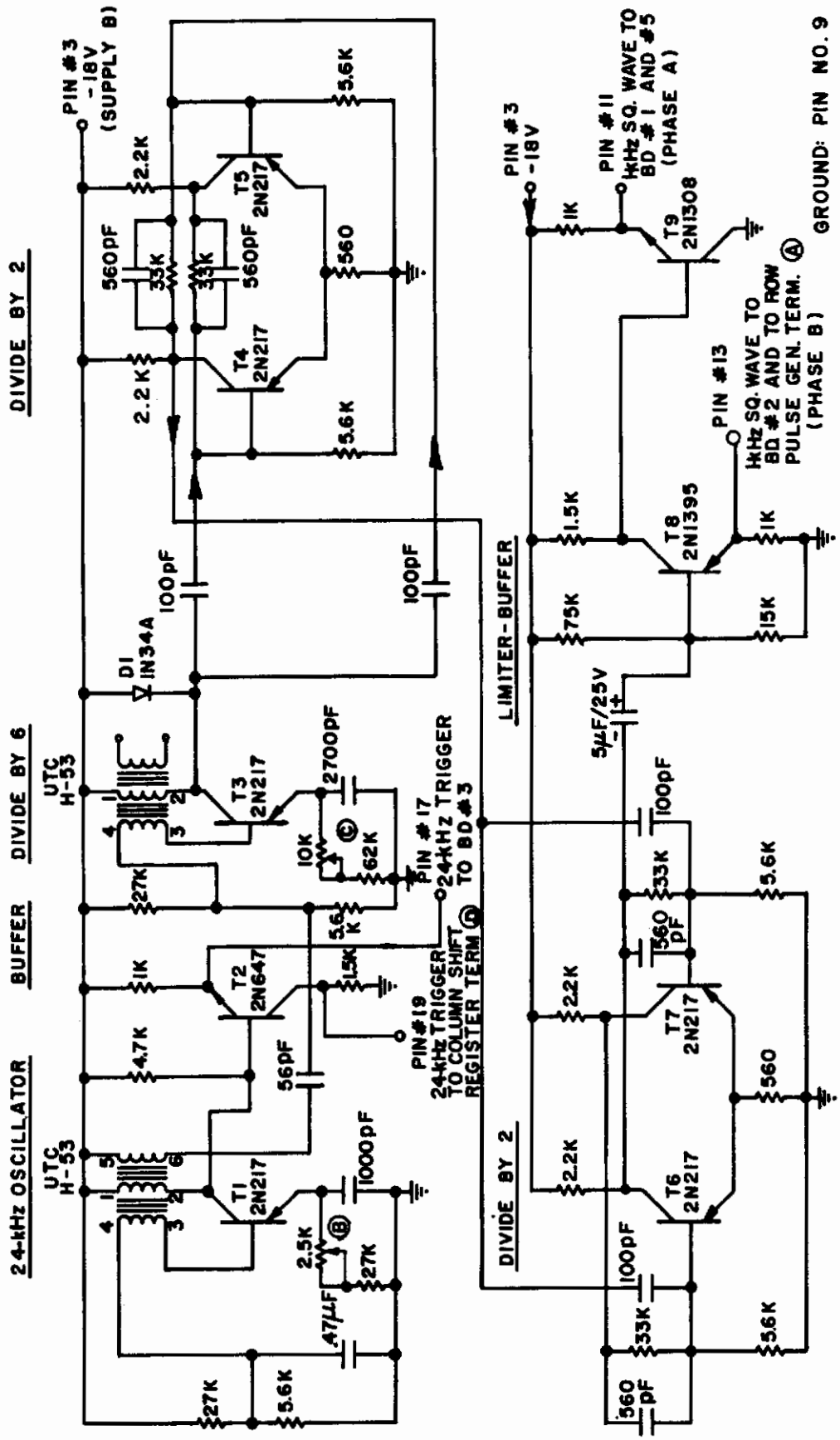
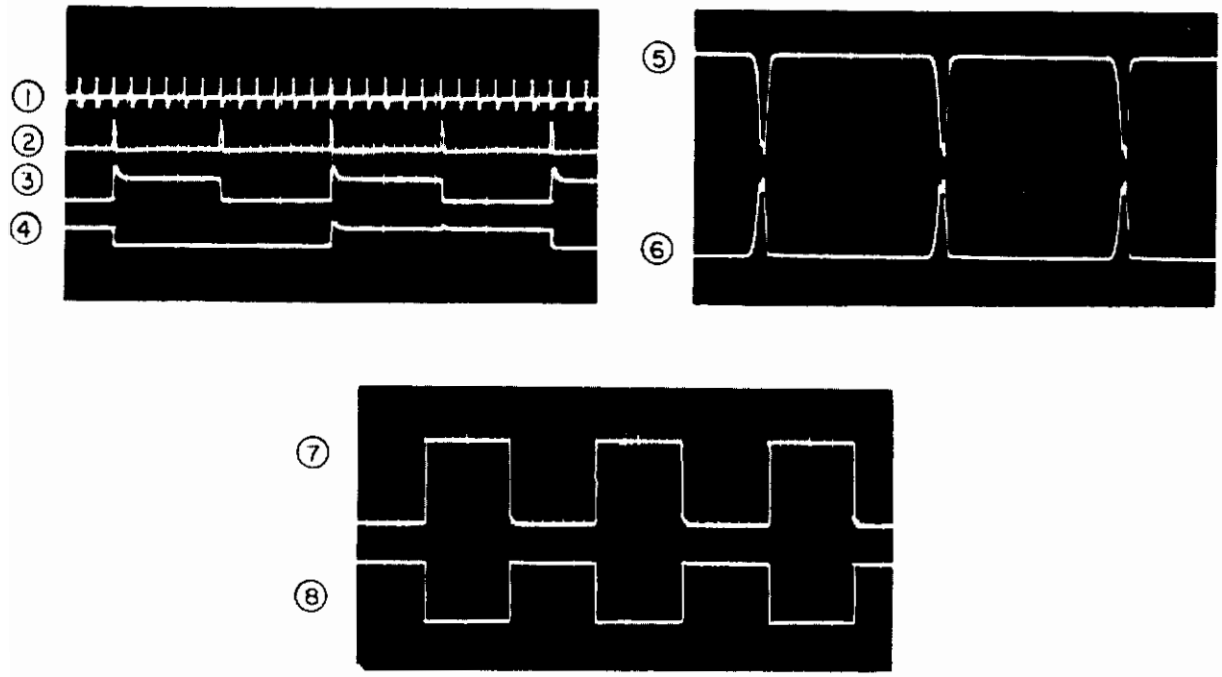


Figure 91. Master Oscillator and High-Frequency Dividers (Board #4).



	WAVEFORM	VERT. SCALE	HOR. SCALE
①	VOLTAGE ON COLLECTOR OF T1	20 V/div	100 μsec/div
②	VOLTAGE ON COLLECTOR OF T3	20 V/div	100 μsec/div
③	VOLTAGE ON COLLECTOR OF T4	20 V/div	100 μsec/div
④	VOLTAGE ON COLLECTOR OF T6	20 V/div	100 μsec/div
⑤	24-kHz CLOCK PULSES ON TERMINAL #19	5 V/div	10 μsec/div
⑥	24-kHz CLOCK PULSES ON TERMINAL #17	5 V/div	10 μsec/div
⑦	1-kHz SQUARE WAVE (PHASE A) ON TERMINAL #11	5 V/div	250 μsec/div
⑧	1-kHz SQUARE WAVE (PHASE B) ON TERMINAL #13	5 V/div	250 μsec/div

Figure 92. Waveforms for Timing Signal Generators on Plug-In Board #4.

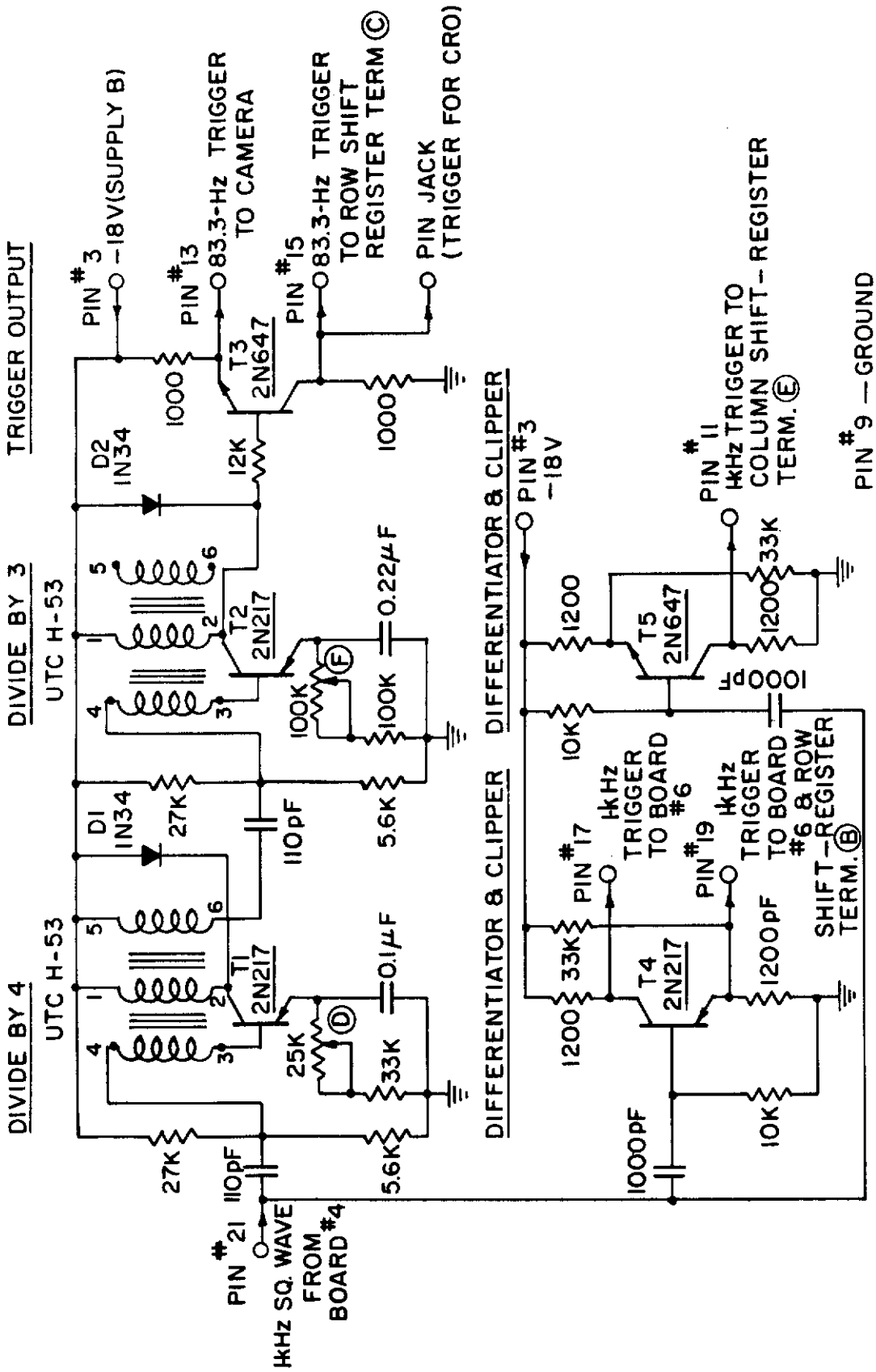
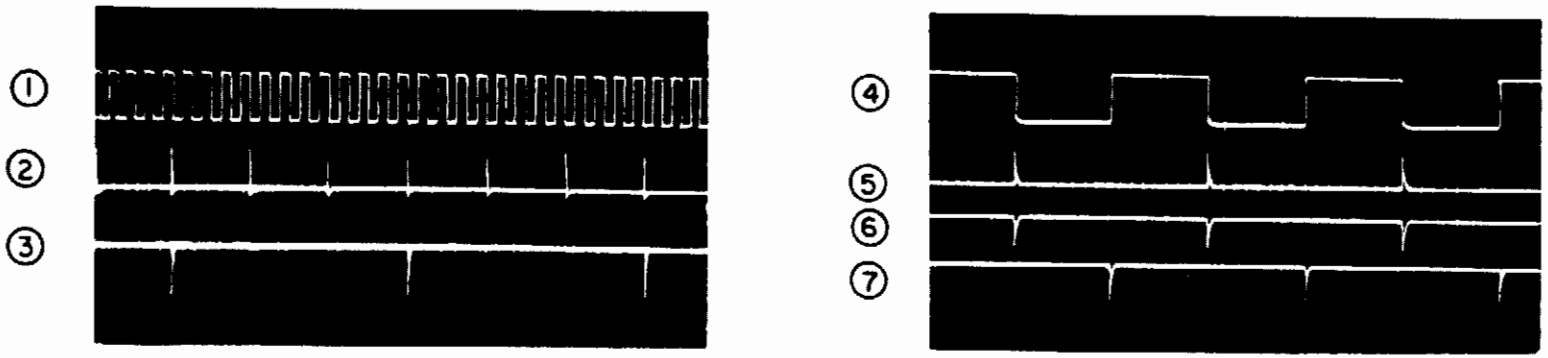


Figure 93. Low-Frequency Dividers and 1-kHz Trigger Generators (Board #5).



	WAVEFORM	VERT. SCALE	HOR. SCALE
①	1- kHz SQUARE WAVE INPUT (PHASE A) ON TERMINAL # 21	10 V/div	25 msec/div
②	VOLTAGE ON COLLECTOR OF T2	20 V/div	"
③	83.3-Hz PULSE ON COLLECTOR OF T3	10 V/div	"
④	1- kHz SQUARE WAVE INPUT (PHASE A) ON TERMINAL # 21	10 V/div	250 μsec/div
⑤	1- kHz TRIGGER PULSE ON OUTPUT TERMINAL # 17	10 V/div	"
⑥	1- kHz TRIGGER PULSE ON OUTPUT TERMINAL # 19	10 V/div	"
⑦	1- kHz TRIGGER PULSE ON OUTPUT TERMINAL # 11	10 V/div	"

Figure 94. Waveforms for Timing Signal Generators on Plug-In Board #5.

on its base will cause it to conduct. The collector and emitter circuits of T4 therefore furnish positive and negative 1-kHz timing pulses, respectively, which correspond in time to the negative-going edges of the phase A 1-kHz square wave. T5 is likewise normally biased off, but it in turn is able to conduct whenever positive pulses appear on its base. The negative 1-kHz timing pulses at the emitter terminal of T5 therefore correspond to the positive-going edges of the phase A 1-kHz square wave. All these signals are illustrated by waveforms 4 through 7 in Figure 94.

Transistor T1 is in the already familiar blocking-oscillator circuit. It is synchronized by the negative-polarity pulses generated by differentiating the 1-kHz waveform on terminal No. 21. By adjusting potentiometer D, the circuit is made to divide by a factor of 4 as illustrated by waveforms 1 and 2 of Figure 94. Negative output pulses from one of the windings of the transformer in the collector circuit of T1 synchronize still another blocking oscillator built around the transistor T2. The potentiometer F of that stage is adjusted to perform frequency division by a factor of 3. The positive 83.3-Hz pulses on the collector of T2 are applied to the buffer stage T3. The emitter of T3 is then a source of positive 83.3-Hz timing pulses, and the collector a source of negative pulses. The latter are illustrated by waveform 3 in Figure 94.

B. EXCITATION WAVEFORM GENERATOR AND DISTRIBUTION CIRCUITS

Plug-in board No. 6 in the uppermost chassis in the rack contains the circuitry for generating the signal for driving the amplifiers which provide the final excitation waveform for the elements of the display matrix. The circuit is shown in Figure 95 and the pertinent waveforms in Figure 96.

Transistors T2 and T3 are in a multivibrator circuit with a free-running frequency slightly lower than 3 kHz, adjustable by potentiometer G. The multivibrator is synchronized by 1-kHz negative pulses on terminal No. 15 through the buffer stage T1. The synchronizing pulses and the output of the multivibrator are shown by waveforms 1 and 2 in Figure 96.

One-kHz positive pulses are applied to terminal No. 17 to trigger a one-shot multivibrator consisting of transistors T4 and T5. The duration of the pulses produced by this circuit is adjusted by potentiometer C. The triggering pulses and the output waveform of the multivibrator are pictured by waveforms 3 and 4 in Figure 96. The negative excursion of waveform 4 drives the gating transistor T6 from cutoff into saturation. The output of the 3-kHz oscillator constitutes the collector supply voltage of T6 through the 18-kΩ resistor. While T6 is saturated, the collector voltage of T6 is approximately at zero volts, but when T6 is cut off, a fraction of waveform 2 will appear on the collector of T6. The function of the 5100-pF filter capacitor is to smooth the transitions of the excitation waveform to reduce undesirable high-frequency ringing in the output transformers of the power-amplifier circuits. The signal on the collector of the gate is similar to waveform 5 in Figure 96. This waveform is then amplified by transistor T7. The amplitude of this waveform is set by potentiometer E to a level such that the elements of the display receive the proper excitation with the "Brightness" control on the front panel turned to extreme clockwise position.

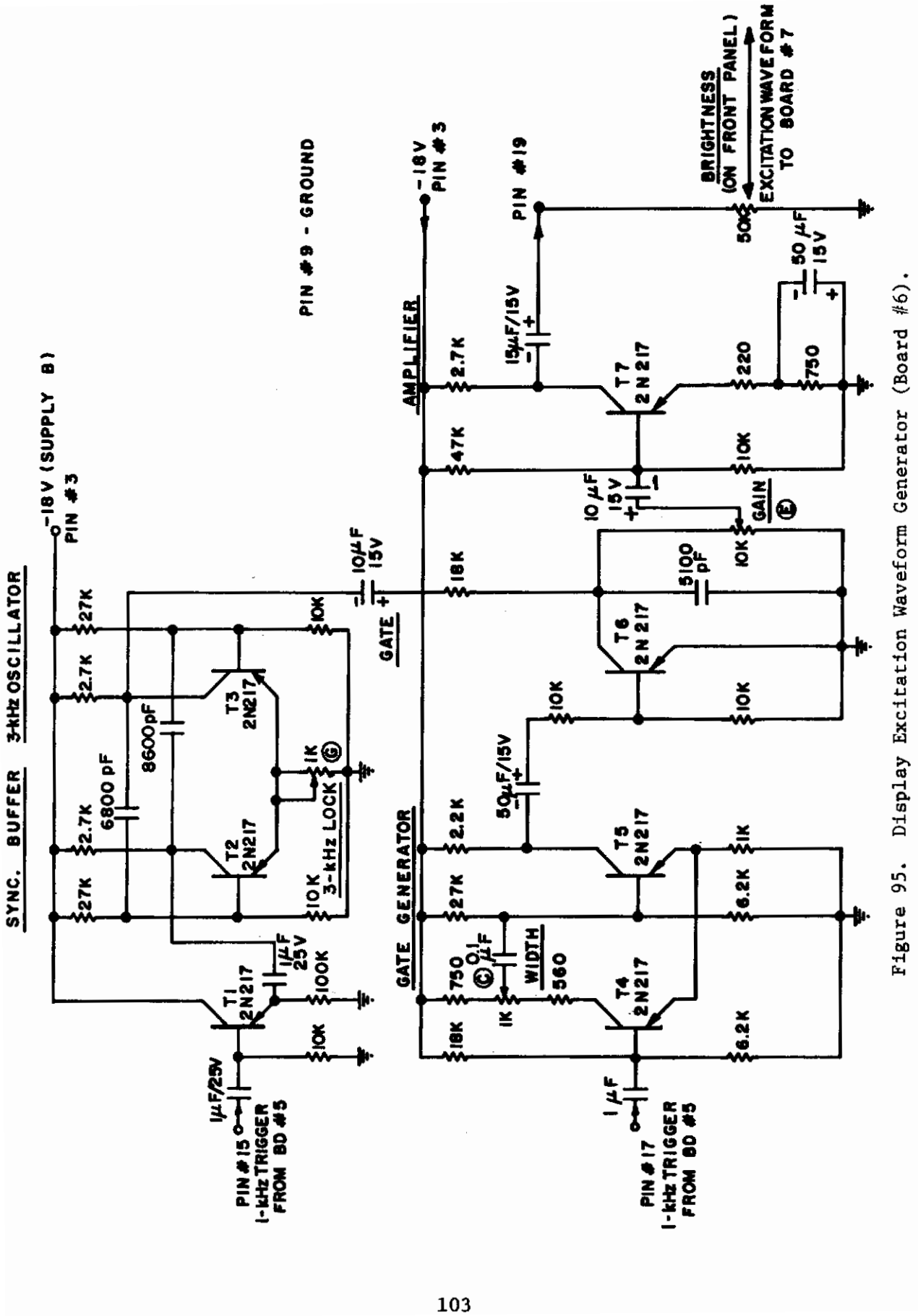
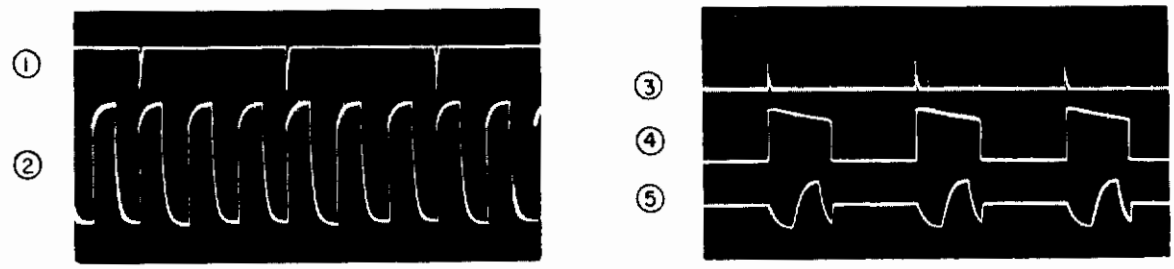


Figure 95. Display Excitation Waveform Generator (Board #6).



	WAVEFORM	VERT. SCALE	HOR. SCALE
①	1- kHz TRIGGER INPUT PULSE ON TERMINAL #15	5 V/div	250 μ sec/div
②	SYNCHRONIZED 3-kHz WAVEFORM OF COLLECTOR OF T3	5 V/div	"
③	1- kHz TRIGGER INPUT PULSE ON TERMINAL #17	10 V/div	"
④	1- kHz GATE WAVEFORM ON COLLECTOR OF T5	10 V/div	"
⑤	EXCITATION WAVEFORM ON TERMINAL #19	10 V/div	"

Figure 96. Waveforms for Excitation Waveform Generator on Plug-In Board #6.

The output waveform on terminal No. 19 of board No. 6 is applied via the potentiometer on the front panel, which has its control function labeled "Brightness," to terminal No. 21 of board No. 7. Waveform 1 in Figure 98 shows the signal at this terminal. The current preamplifier and distribution circuits for the excitation waveforms are on this plug-in board as shown in Figure 97. Transistor T1 is in a conventional phase-splitting circuit. Potentiometers A, B, D, and E in the collector and emitter circuits of T1 feed Darlington-pair type current amplifier circuits. The outputs of these amplifiers provide drive currents for power transistors in class B push-pull-type amplifier circuits. The Darlington pairs are therefore operated without DC bias such that they are conducting only during the negative excursions of the input waveforms. The transistor pairs T2-T3 and T6-T7 provide drive currents for amplifiers associated with rows 1 through 5, and the pairs T4-T5 and T8-T9 provide currents for amplifiers associated with rows 6 through 10. Potentiometers A, B, D, and E are used to make fine adjustments in drive waveforms to achieve a reasonably good balance between the negative and positive excursions of the excitation voltage applied to the elements of the display (waveforms 1 and 2 in Figure 99). The output signals of the circuits on plug-in board No. 7 are shown by waveforms 2 and 3 in Figure 98.

C. EXCITATION AMPLIFIERS

The circuit of one of the ten excitation amplifiers is shown in Figure 100. All ten excitation amplifiers are physically located on the third chassis from the top in the relay rack. The transistors T1 and T2 (Type 2N1905) and the output transformer (STANCOR P-6377) form a Class B push-pull amplifier which receives its input signals from plug-in board No. 7. The input signals are identical to waveforms 2 and 3 in Figure 98.

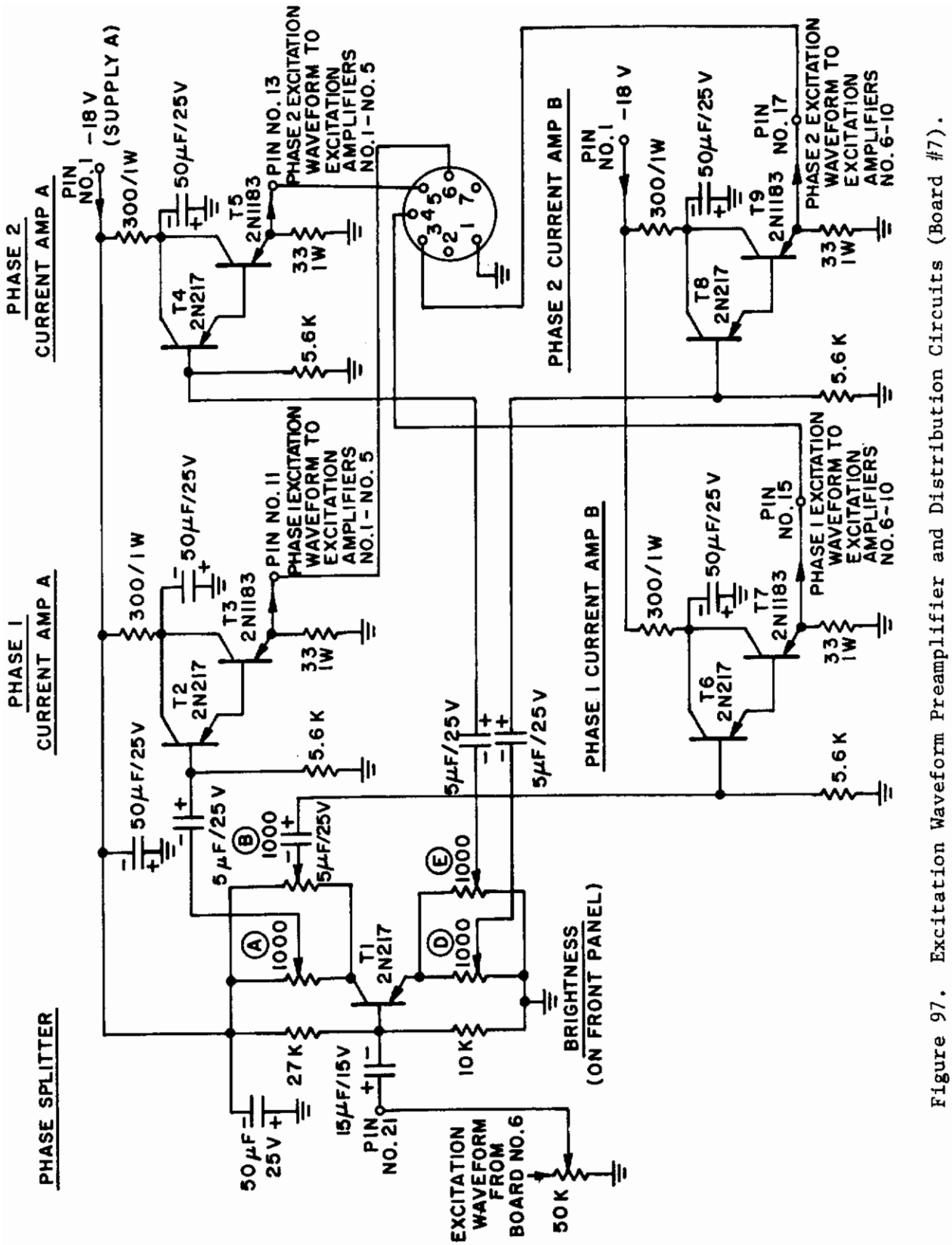
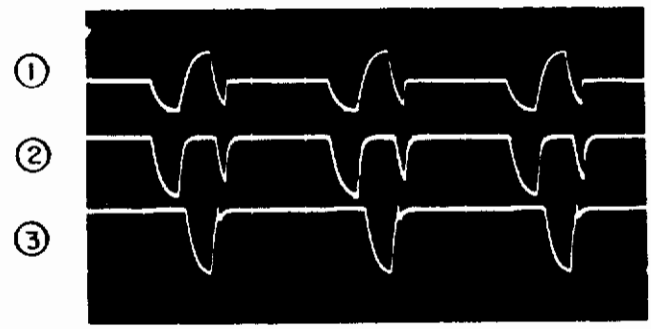
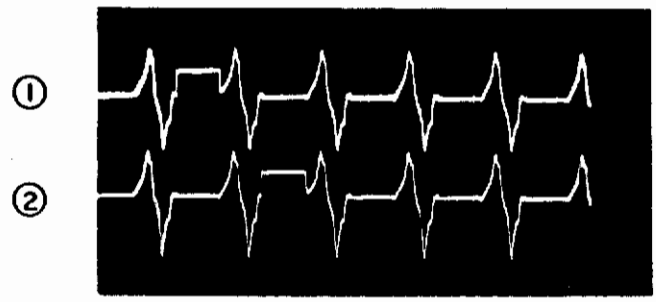


Figure 97. Excitation Waveform Preamplifier and Distribution Circuits (Board #7).



	WAVEFORM	VERT. SCALE	HOR. SCALE
①	EXCITATION WAVEFORM INPUT ON TERMINAL # 21	5 V/div	250 μsec/div
②	PHASE I EXCITATION SIGNAL OUTPUT ON TERMINAL #11 AND #15	2 V/div	"
③	PHASE 2 EXCITATION SIGNAL OUTPUT ON TERMINAL #13 AND #17	2 V/div	"

Figure 98. Waveforms for Excitation Signal Preamplifier and Distribution Circuits on Plug-In Board #7.



	WAVEFORM	VERT. SCALE	HOR. SCALE
①	EXCITATION WAVEFORM ON TERMINAL #1 OF TRANSFORMER DRIVING ROW #1	200V/div	500μsec/div
②	EXCITATION WAVEFORM ON TERMINAL #1 OF TRANSFORMER DRIVING ROW #2	"	"

Figure 99. Final Excitation Waveforms for Rows of the Display Matrix.

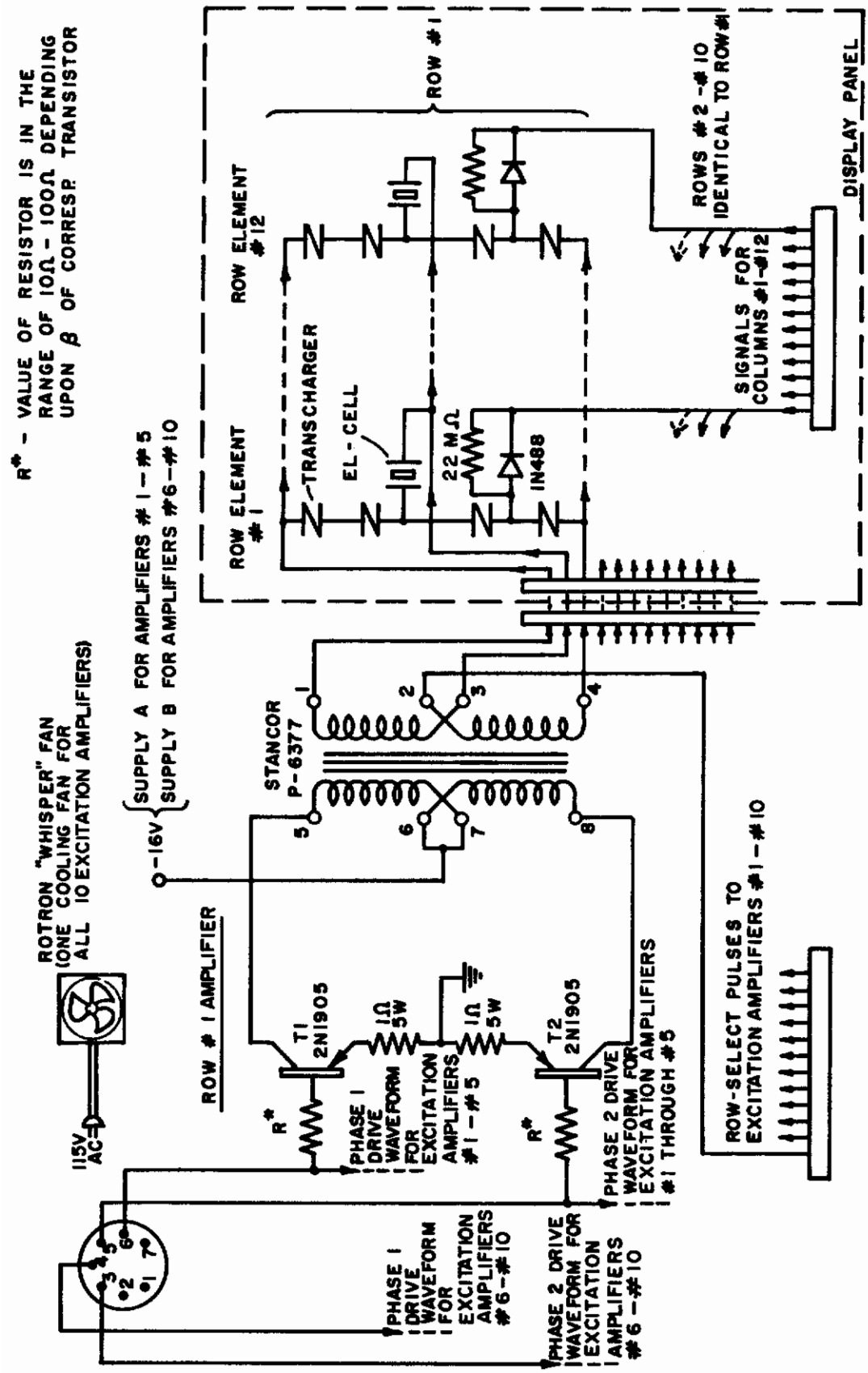


Figure 100. Excitation Amplifier and Display Panel Wiring.

Transistors T1 and T2 are driven from cutoff into saturation by the input waveforms to maintain an output of reasonably constant amplitude regardless of variations in loading. The output waveform has an amplitude of approximately 800 V peak-to-peak as shown in Figure 99, (row-select pulses are superimposed upon the excitation waveforms in this picture). The nonsimilarity between the input waveform shown in Figure 98 and the output waveform is a result of the nonlinear characteristic of the output transformer. Each cycle of the excitation waveform includes a 500-μsec interval during which all 12 elements of one row in the display are updated with the current video information. It is important to reduce and maintain the value of the excitation voltage reasonably close to zero volts during this interval to avoid any extraneous modulation components in the display. The drive currents in the base circuits of T1 and T2 must therefore be adjusted to achieve this condition. As may be observed in Figure 98, the waveforms of the currents in the base leads are not identical in shape. The small current spike in waveform 2 of Figure 98 preceding the row-addressing interval has the function of reducing the flux in the output transformer to zero very rapidly near the end of the interval allotted to the excitation signal. This allows the output voltage of the transformer to go to zero by the time the addressing interval commences. Since the period of the ungated 3-kHz excitation signal is 333 μsec, and the time interval actually assigned for the excitation waveform is 500 μsec (i.e., one-half cycle of 1 kHz), 167 μsec remain for reducing the flux in the output transformer to zero. The output of the excitation amplifier transformer is set for maximum flatness during the addressing interval by adjusting the width of the pulse which gates the 3-kHz waveform by potentiometer C on board No. 6. The width of the gate pulse determines the size of the smaller current spike in waveform 2, Figure 98. The resistor R* in the base of the transistors T1 and T2 are selected to compensate for differences in the amplification factors of these transistors to achieve symmetrical and equal amplitude output waveforms from all ten driver circuits.

Transistors T1 and T2 are mounted on a heat sink. All ten heat sinks are arranged on the chassis in such a maenner that they can be cooled by a single Rotron "Whisper" fan. Row selection pulses from the row drivers are fed to the center taps of the output windings of the appropriate excitation amplifier transformers.

D. ROW SELECTION CIRCUITS

As briefly described, the elements of a row in the display matrix are addressed sequentially, starting with the topmost row and finishing with the row on the bottom. It is, therefore, necessary to generate a sequence of pulses to activate the 10 rows of the display in the proper order. A 12-stage shift register and a set of 10 row drivers are provided for this purpose. These circuits are mounted on the second chassis from the top in the relay rack.

Figure 101 is a diagram of the circuits which accomplish the required task. On the bottom half of the figure, the first four stages of a 12-stage shift register are shown. Stage 1 is initially set by a negative 83.3-Hz trigger pulse. The stage is reset by the first pulse of the 1-kHz trigger

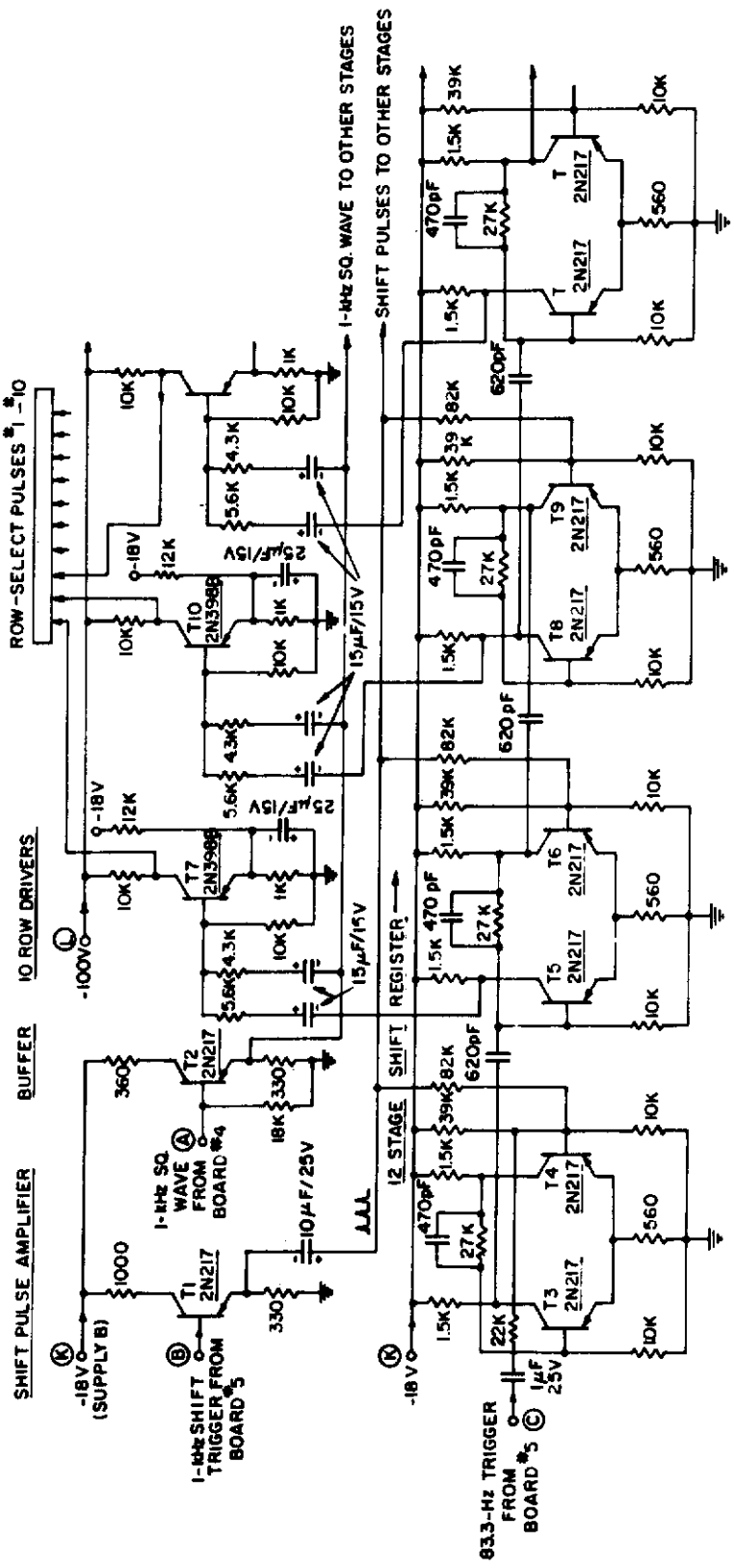
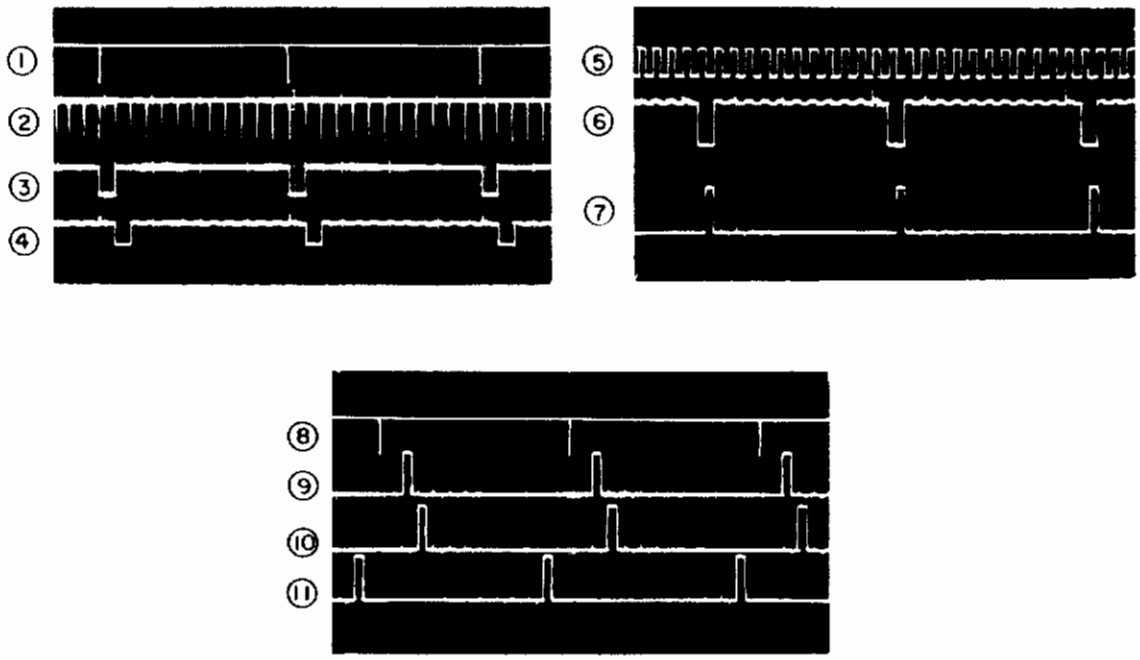


Figure 101. Row Shift Register and Row Drivers.

waveform which follows the set pulse. The edge of the voltage waveform generated when state 1 is reset is used to set stage 2, etc. The 1-kHz reset pulses are applied to all 12 stages of the shift register through the buffer transistor T1. The set pulses for the odd-numbered stages of the shift register are obtained and applied differently from those of the even-numbered stages to keep interfering pulse components from appearing in the setting pulse waveforms. Waveforms 1 and 2 in Figure 102 show the 83.3-Hz set pulses applied to the first stage of the shift register and the 1-kHz shift or reset pulses. Waveforms 3 and 4 illustrate the output waveforms of stages 1 and 2 of the shift register. Only ten of these 12 waveforms are used since there



WAVEFORM	VERT. SCALE	HOR. SCALE
① 83.3-Hz TRIGGER INPUT ON TERMINAL C	10V/div	2.5msec/div
② 1-kHz SHIFT PULSE INPUT ON TERMINAL B	5 V/div	"
③ VOLTAGE ON COLLECTOR OF T3 (1st STAGE OF SHIFT REGISTER)	20 V/div	"
④ VOLTAGE ON COLLECTOR OF T5 (2nd STAGE OF SHIFT REGISTER)	20 V/div	"
⑤ 1-kHz SQUARE WAVE (PHASE B) INPUT ON TERMINAL A	10 V/div	"
⑥ VOLTAGE ON COLLECTOR OF T5 (2nd STAGE OF SHIFT REGISTER)	10 V/div	"
⑦ VOLTAGE ON COLLECTOR OF T7 (ROW-SELECT PULSE FOR ROW #1)	100V/div	"
⑧ 83.3-Hz TRIGGER INPUT ON TERM. C (SAME AS ①)	10V/div	"
⑨ VOLTAGE ON COLLECTOR OF T7 (ROW-SELECT PULSE FOR ROW #1)	100 V/div	"
⑩ VOLTAGE ON COLLECTOR OF T10(ROW-SELECT PULSE FOR ROW #2)	100 V/div	"
⑪ ROW-SELECT PULSE FOR ROW #10	100V/div	"

Figure 102. Waveforms for Row Shift Register and Row Drivers.

are only ten rows in the display matrix. This is done to allow ample time for the vertical retrace in the TV camera where the video signal originates. Since the waveform on the collector of T3 is not used as an input to a row driver the corresponding waveform in Figure 102 differs slightly from the waveform on the collector of T5. The twelfth stage of the shift register is actually superfluous since its output waveform remains unused (by using the ten output waveforms of shift register stages 3 through 12 even more time could be made available for the vertical retrace).

The negative pulses from the shift register stages 2 through 11 are applied to the bases of the ten corresponding circuits where the final row-select pulses are formed. The circuits of the row drivers T7, T10, etc., are all identical. The collector supply voltage of these transistors is -100 V, and the transistors are ordinarily cut off by the negative bias applied to their emitter circuits. The negative pulses from a stage in the shift register are applied to the base of the corresponding row driver; but by themselves they are insufficient in amplitude to drive the transistor into conduction. However, a 1-kHz square wave of Phase B from the buffer T2 is added to the shift register pulse at the base of the row driver, and now the transistor is biased into conduction during the negative excursion of the 1-kHz square wave while the pulse from the shift register is also present. The collector circuit of the row driver actually saturates while the transistor conducts, and as a result, a positive 100-V pulse of 500-μsec duration, i.e., the period of a half cycle of the 1-kHz square wave, is produced across the collector load. The two input waveforms and the output waveform of one row driver are illustrated by waveforms 5, 6, and 7 in Figure 102. The ten consecutive row-select pulses in one frame are separated by 500-μsec intervals during which the excitation voltage is applied to the elements of the display. Waveforms 9, 10, and 11 in Figure 102 show the row-select pulses for rows 1, 2, and 10, respectively, as well as their relationship to the 83.3-Hz trigger pulse shown by waveform 8. The waveforms in Figure 100 illustrate the excitation waveform with superimposed row-select pulses for two consecutive rows.

E. TV CAMERA

The images which are displayed on the 10 x 12 display matrix are produced by a video signal which originates in a TV camera. A commercially available camera, Model TV-120, was appropriately modified to function as a signal source for the display. The optics consist of a 50-mm focal length, f/1.5 Cine-Raptar lens, made by Wollensak.

A schematic of the modified TV camera is shown in Figure 103. The high- and low-voltage power supplies shown on the lower part of the diagram, and the video amplification and processing circuits shown on the top section of the diagram did not require modification. The vertical deflection circuitry, shown in the middle section of the diagram and containing transistors T13 through T17, is also unmodified except for the synchronizing signal for the oscillator which is now an 83.3-Hz positive trigger pulse rather than the 60-Hz power line voltage used in the original circuit. Since the horizontal deflection frequency of 1000 Hz is appreciably different from the original

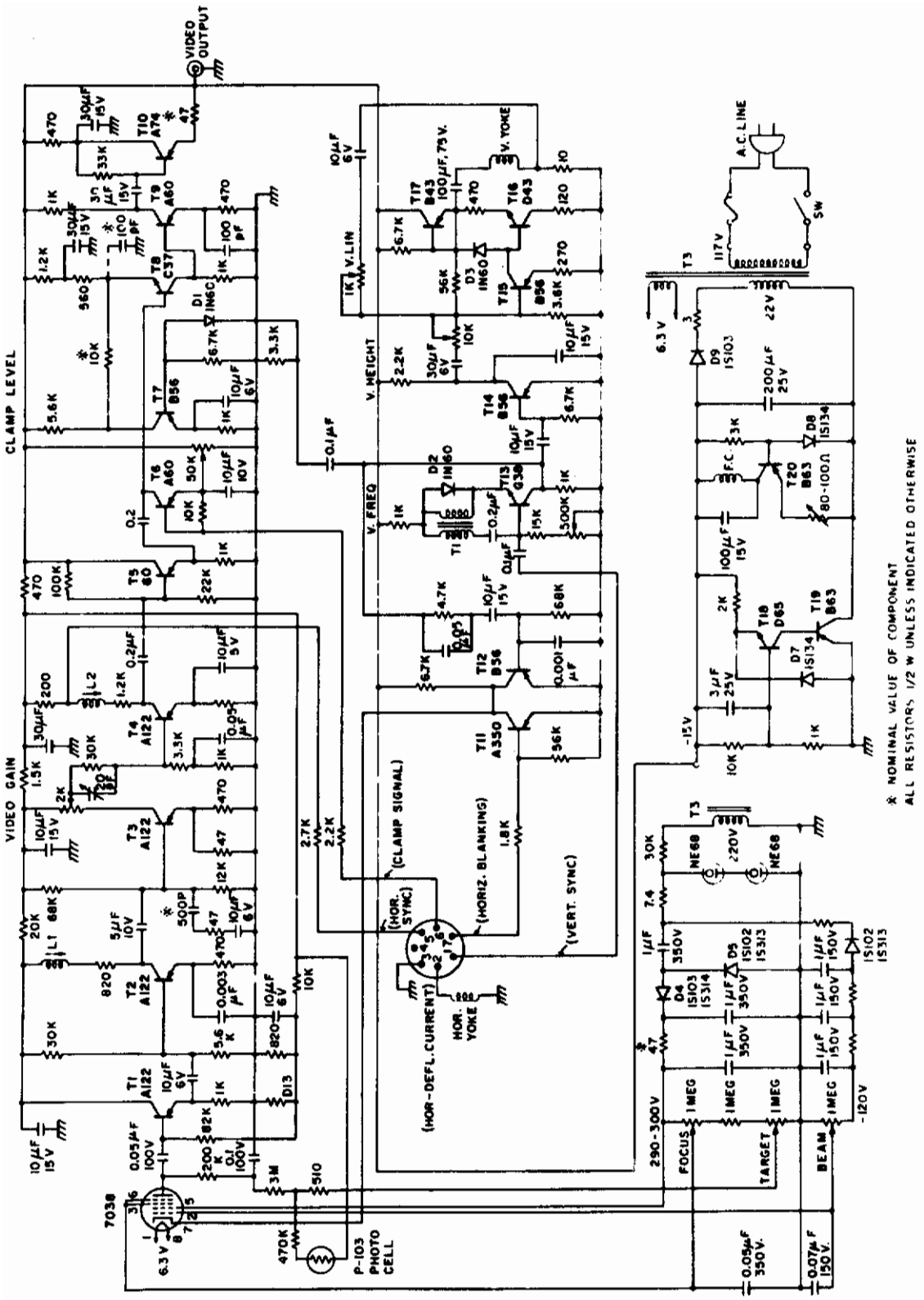


Figure 103. Circuit Diagram of TV Camera.

horizontal deflection frequency of 15.75 kHz of the TV camera, it was most practical to disable the horizontal deflection circuits altogether and generate the necessary waveforms externally.

Circuits on plug-in board #1 of the uppermost chassis in the relay rack, shown in Figure 104, generate the appropriate 1000-Hz waveforms for operating the TV camera. Transistors T1 and T2 are simply emitter followers which supply 1-kHz square wave signals from low output impedance sources. One output (terminal #11) feeds the horizontal blanking amplifier T11 in the camera. The vertical blanking waveform is added by T12 in the common collector load, and the resulting waveform is applied to the cathode of the vidicon to cut off the electron beam during retrace. The 1-kHz square wave on terminal #13 is added as a horizontal synchronizing signal to the video waveform in the collector circuit of T4 in the camera. The resulting signal is fed through T5 to a clamp circuit driven by T6, which has the purpose of adjusting the relative amplitude of the synchronizing component of the video waveform. The drive signal for the clamp circuit is obtained from terminal #15 of board #1.

The 15-kΩ resistor and 1-μF capacitor in the base circuit of T3 on board #1 constitute an integrator generating a sawtooth voltage waveform from a 1-kHz square wave input signal. The amplified sawtooth voltage from T3 drives the Class A current amplifier consisting of T4 and T5. The horizontal deflection yoke of the TV camera is connected in parallel with a choke in the collector circuit of T5 on board #1. The amplitude of the sawtooth current is adjusted by potentiometer B to about 150 mA peak-to-peak for full deflection. The 500-μF capacitor in series with the yoke prevents the direct current in the collector of T5 from flowing through the yoke. The pertinent waveforms at the output terminals of board #1 are shown in Figure 105.

The TV-120 camera is provided with a photocell for automatic light level compensation. The video output signal has a peak-to-peak amplitude of about 1 volt into a 75-Ω load under normal operating conditions. Since none of the coupling and bypass capacitors in the video amplifier were replaced by larger capacitors, while the horizontal scanning frequency was reduced from the original 15.75 kHz to 1000 Hz, it should be pointed out that the low-frequency response of the amplifier is now somewhat deficient.

F. VIDEO PROCESSING CIRCUITS

The circuits which supply the column drive signals for the display matrix require a video input signal such that -10 V corresponds to the black level and zero volts to the maximum brightness level of the video information. The video output signal from the TV camera therefore must be amplified by a factor of 10 and its sync level must be clamped to the appropriate DC voltage.

The circuitry on plug-in board #2 performs the functions just mentioned. A schematic is shown in Figure 106 and some relevant waveforms in Figure 107. T1 and T2 are low-gain voltage amplifiers with potentiometer B functioning as a gain control. The collector load of T2 is split to provide two video signal outputs individually controlled in amplitude by the two 2.5-kΩ potentiometers. The signal from the right-hand potentiometer, designated as the

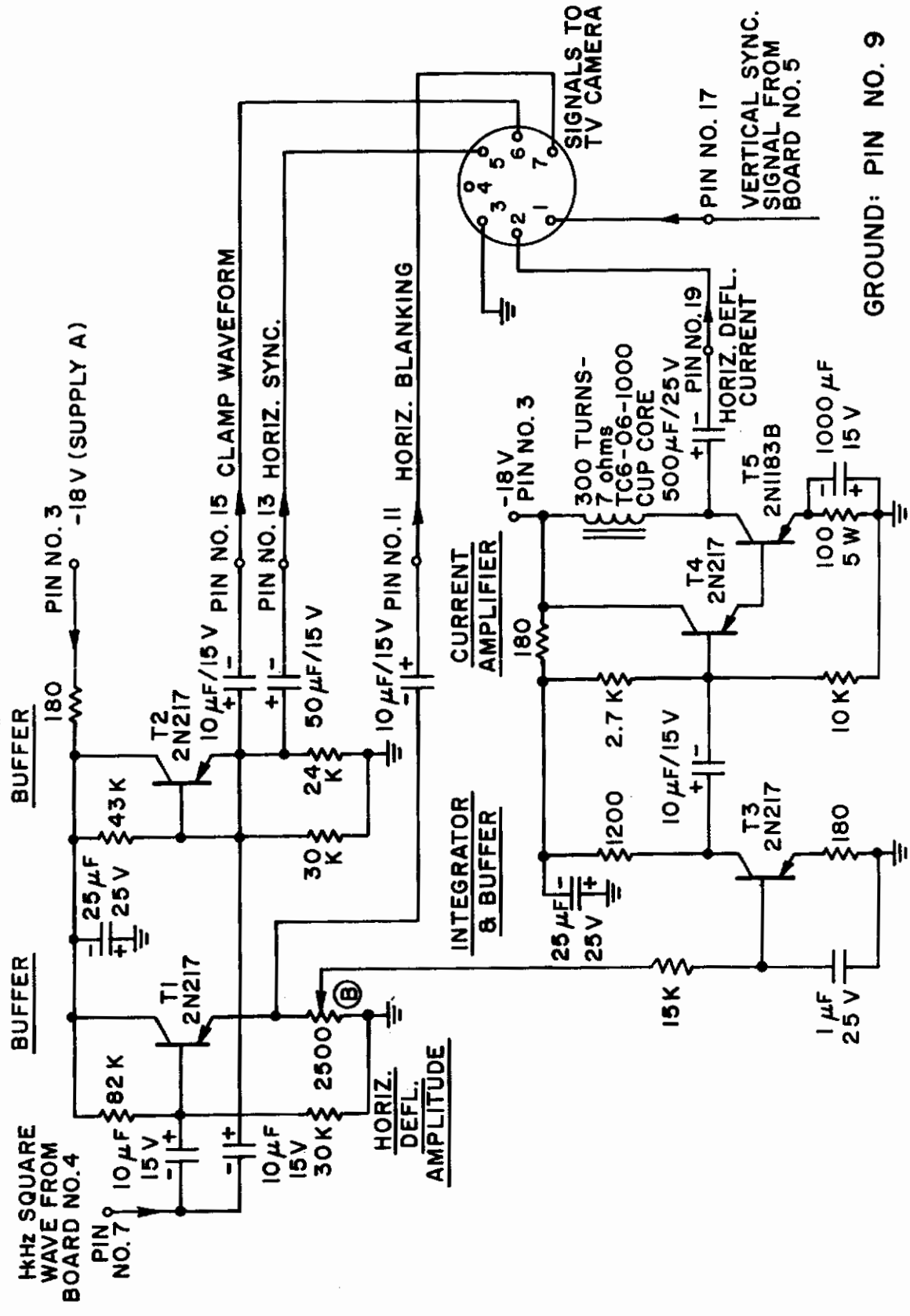
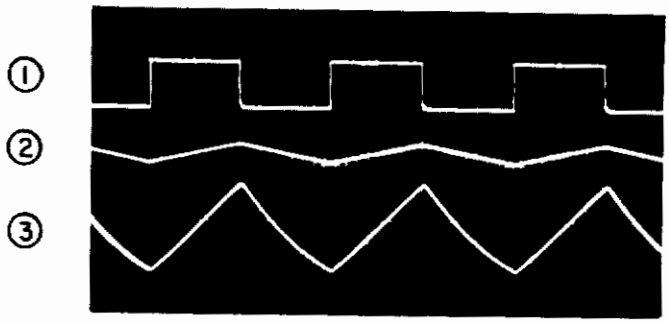


Figure 104. Camera Control Signal Generator (Board #1).



WAVEFORM			
①	1-kHz SQUARE WAVE (PHASE A) INPUT ON TERMINAL #7; ALSO OUTPUTS ON TERMINALS #11, #13 AND #15	10 V/div	250 μsec/div
②	1-kHz SAWTOOTH VOLTAGE ON BASE OF T3	0.2V/div	"
③	1-kHz HORIZONTAL DEFLECTION CURRENT THROUGH TERMINAL #19	100mA/div	"

Figure 105. Waveforms for Camera Control Signal Generator on Plug-In Board #1.

"Contrast" control, has its sync level clamped at the desired DC voltage determined by the setting of potentiometer D. It is then passed on through the emitter follower T8 to the video selector switch. The signal from the left-hand potentiometer, designated as the "Threshold" control, is clamped by T6 and is then fed through the emitter follower T7 to terminal #21. The signal is converted into a digitized video waveform by the circuits on board #3 which will be described shortly. The 1-kHz square wave applied to terminal #15 is amplified by T5 and is then used as the clamping signal to drive the bases of transistors T3 and T6. The sync level of the two video signals is set by these transistors to the DC voltages determined by the settings of potentiometers D and E.

Plug-in board #3 contains the video digitizer circuits shown in Figure 108. All of the important waveforms in these circuits are illustrated in Figure 109. The video signal from board #2 is applied to the base of transistor T7 which, together with T8, forms a Schmitt trigger circuit. This bistable circuit changes its state whenever the video signal passes through certain threshold voltage levels. Waveform 1 in Figure 109 shows a typical video input waveform, and waveform 2 the corresponding output voltage of the Schmitt trigger. Whenever T8 is on, its collector voltage is only a few volts negative such that when applied to the base of T9, a pulse train applied to the emitter of T9 causes T9 to conduct. A pulse waveform is then produced across the collector load of T9 as shown by waveform 3. The 24-kHz pulse train applied to the emitter of T9 is generated by the one-shot multivibrator T4-T5 which is triggered by a pulse from a delay multivibrator T2-T3.

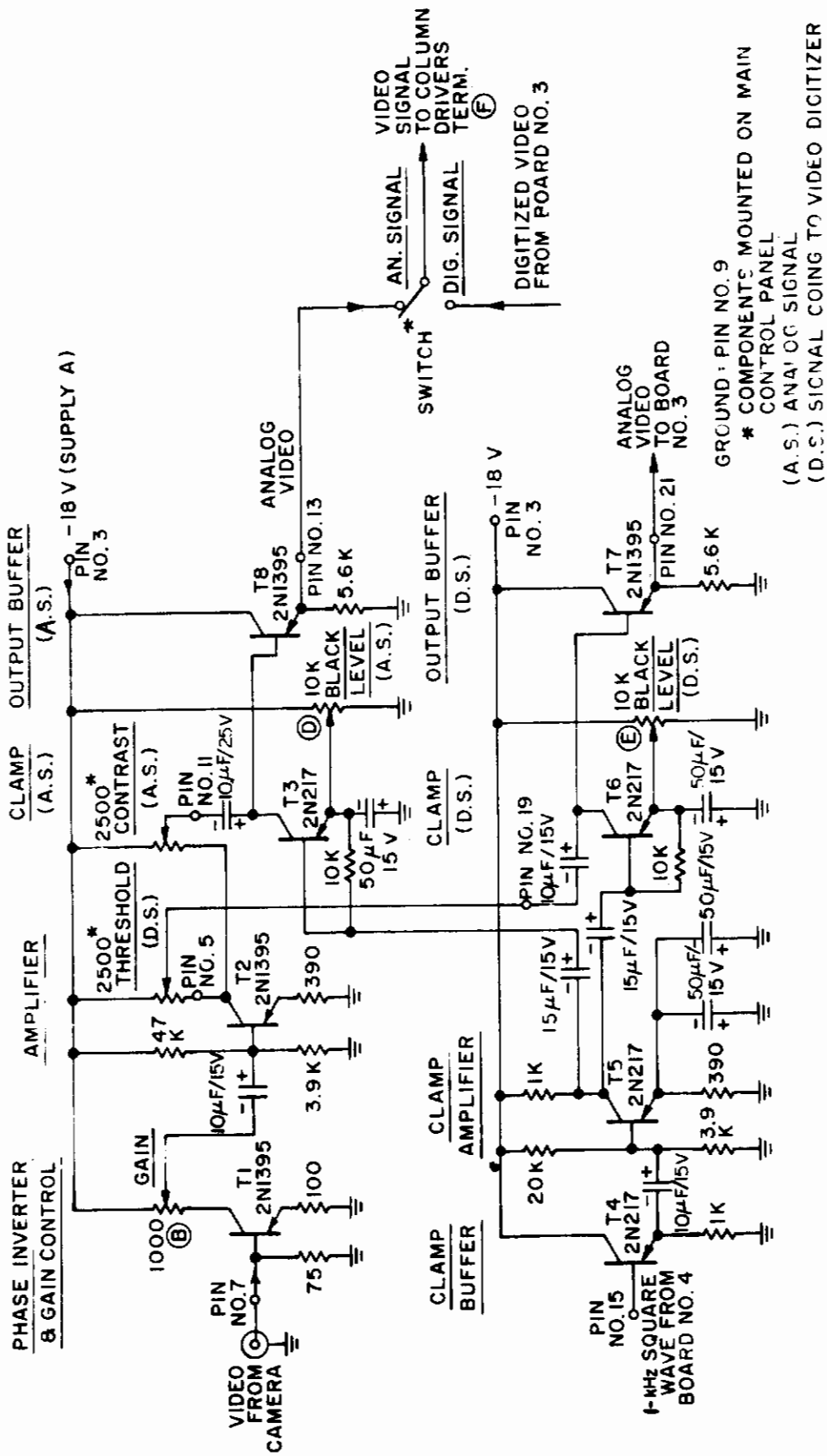


Figure 106. Analog Video Processor (Board #2).

	WAVEFORM	VERT. SCALE	HOR. SCALE
①	VIDEO OUTPUT SIGNAL ON TERMINAL # 13 (SIMILAR SIGNALS ALSO ON # 5,7,11,19, AND 21)	5 V/div	200 μ sec/div
②	1- kHz SQUARE WAVE INPUT (PHASE B) ON TERMINAL # 15	20 V/div	"
③	1- kHz CLAMP WAVEFORM ON COLLECTOR OF T5	20 V/div	"

Figure 107. Waveforms for Video Signal Processor on Plug-In Board #2.

This circuit in turn is triggered by 24-kHz clock pulses on terminal #17. The purpose of the time delay is to assure that the pulses in the final output waveform of the digitizer are properly aligned with the column-addressing pulses generated by the column shift register. Waveforms 5, 6, and 7 illustrate the operation of the multivibrator circuits.

The trailing edges of the pulses that appear on the collector terminal of gate T9 now set a bistable circuit T11-T12. Leading edges of the 24-kHz pulses on the collector of T4 will always reset the bistable circuit a certain number of microseconds after it has been set. The duration of the "set" interval of the bistable circuit is determined by the setting of potentiometer F. Since this potentiometer really controls the width of the pulses in the 24-kHz pulse train, it is obvious that the "set" time of the bistable circuit cannot exceed 40 μsec. The voltage on the collector of T9, waveform 4 in Figure 109, constitutes the digitized video signal. The level of the negative portion of the signal is now clamped to about -10 volts by diode D1. The signal is then applied through emitter followers T13 and T14 to the video switch on the control panel. This switch selects either the analog or the digitized video signal for application to the video signal bus of the column driver circuits.

G. COLUMN SIGNAL GENERATORS

The 12 elements in one row of the display matrix are addressed and simultaneously supplied with the appropriate video signal in sequential fashion under control of the column signal generator. Even though any one of the

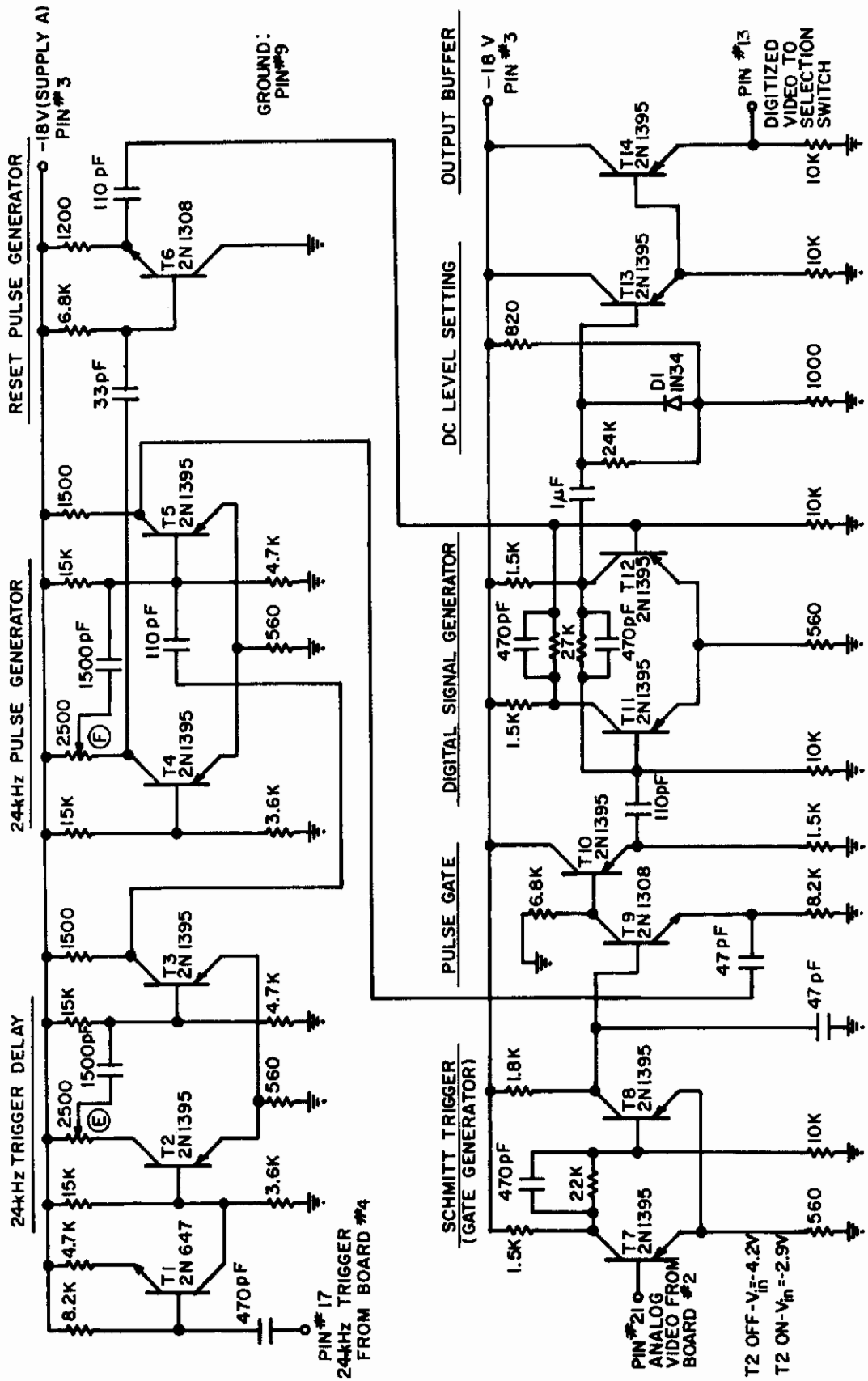
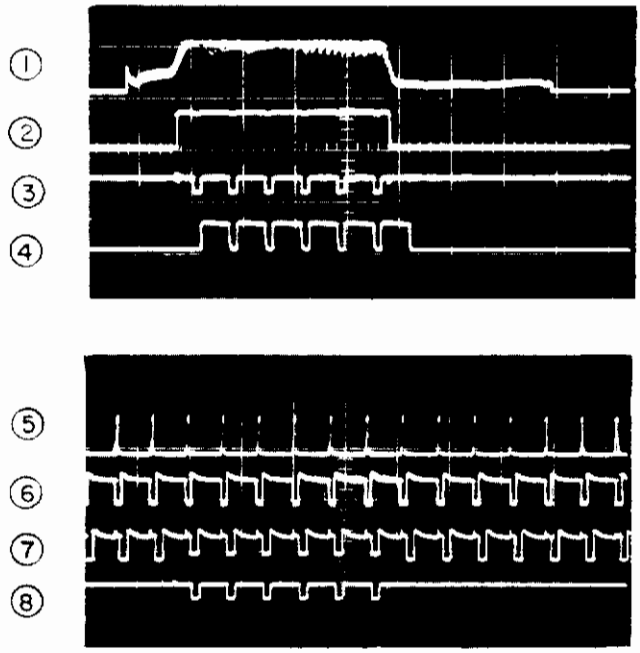


Figure 108. Video Digitizer (Board #3).



	WAVEFORM	VERT. SCALE	HOR. SCALE
①	VIDEO INPUT SIGNAL ON TERMINAL # 21	10 V/div	50 μsec/div
②	VOLTAGE ON COLLECTOR OF T8 (OUTPUT OF SCHMITT TRIGGER)	20 V/div	"
③	OUTPUT VOLTAGE ON COLLECTOR OF GATE T9	20 V/div	"
④	DIGITIZED VIDEO SIGNAL ON TERMINAL # 13 (SIMILAR WAVEFORMS ON COLLECTOR OF T12 AND BASE & EMITTER OF T13)	20 V/div	"
⑤	24 — kHz TRIGGER ON TERMINAL # 17	10 V/div	"
⑥	OUTPUT OF DELAY MULTIVIBRATOR, COLLECTOR OF T3	20 V/div	"
⑦	OUTPUT OF 24 — kHz PULSE GENERATOR, COLLECTOR OF T5	20 V/div	"
⑧	OUTPUT VOLTAGE ON COLLECTOR OF GATE T9 (SAME AS WAVEFORM ③)	20 V/div	"

Figure 109. Waveforms for Video Digitizer on Plug-In Board #3.

12 column signals is common to corresponding elements in all 10 rows of the display, the column signal is effective only for the row which is simultaneously activated by a row-select pulse from the row driver.

Figure 110 is a diagram of the circuits under discussion. These circuits are located on the second chassis from the top in the relay rack. On the lower half of Figure 110 the first three stages of the 12-stage horizontal shift register are shown. Each stage consists of two transistors in a bistable circuit configuration. T1 and T2 form the first stage, T4 and T5 the second stage, etc. Stage 1 of the shift register is set by a 1-kHz negative trigger pulse which is applied to the base of T1. 24-kHz negative pulses are simultaneously applied to the base of T2. These pulses will reset the bistable circuit whenever it is in the "set" state. Whenever pulses are simultaneously present on bases of both T1 and T2, the pulse on the base of T1 will set the circuit because it is much larger in amplitude than the pulses on the base of T2. The first stage in the shift register therefore produces a positive voltage pulse in the collector circuit of T1 with a duration equal to the time interval between successive 24-kHz clock pulses (about 42 μsec). Waveforms 1, 2, and 3 in Figure 111 illustrate the operation of this stage. The second stage of the shift register operates in the same manner, except that this stage is set by the negative-going edge of the waveform on the collector of T1 through a differentiating circuit. Stage 2 produces a waveform illustrated by waveform 4 in Figure 111. The remaining ten stages of the shift register will all produce similar output waveforms, each one delayed from the output of the preceding stage by 42 μsec. The output pulse produced by the last stage in the shift register is followed by a period of 500 μsec, i.e., the time interval occupied by 12 of the 24-kHz clock pulses, where outputs of all stages in the shift register are zero. This interval is utilized for applying the excitation waveform to all elements of the display matrix (as described in Section B) and for horizontal retrace in the camera. Following the 500-μsec "dead" interval, another 1-kHz negative pulse will set the first stage of the shift register, thus initiating a new cycle.

The positive pulses from the shift register stages are applied to the base circuits of the 12 corresponding column drivers. The circuits of the column drivers T3, T6, etc., are all identical. The collector supply voltage of these transistors is -100 V, and the transistors are ordinarily biased into collector saturation by the +3.9-V bias voltage applied to their emitter circuits. The collector voltages of these transistors are therefore approximately at zero, or actually a fraction of a volt positive. With zero voltage on the video signal bus, the positive pulse from a shift register will drive the corresponding column driver from saturation into cutoff, i.e., a 100-V negative pulse of 42-μsec duration is produced at the collector of the column driver. The video signal on the video bus may actually have any value between zero and -10 V, and a negative voltage on the video bus will counteract the effect of the positive pulses from the shift register applied to the bases of the column drivers. The output voltage of a column driver may therefore be a negative pulse of any amplitude from zero to -100 V, depending upon the voltage of the video signal on the video bus at the time that the positive pulse from the appropriate stage of the shift register is applied. To compensate for differences in the amplification factors of the column driver transistors, the gains of the ten drivers have been made adjustable by

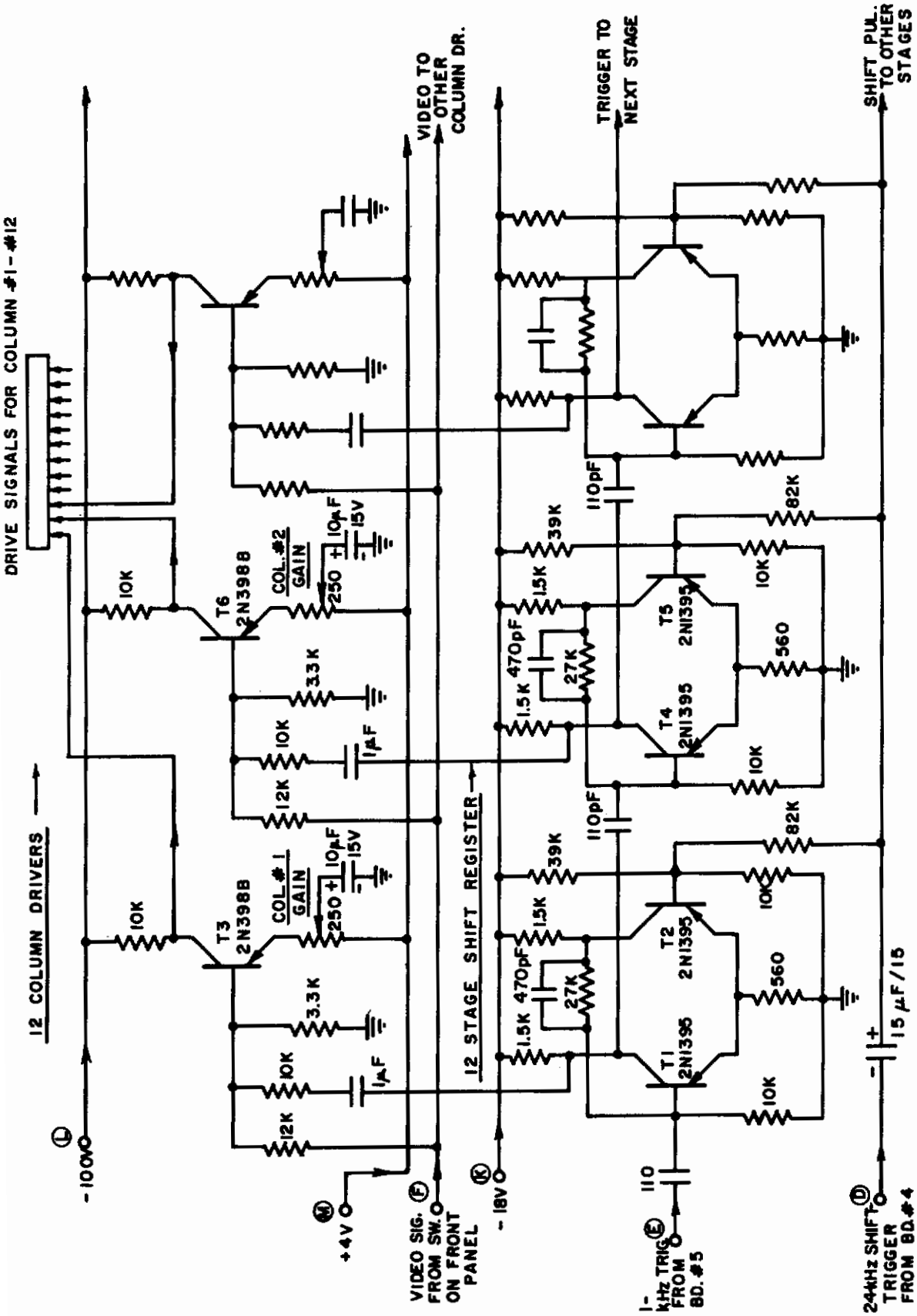
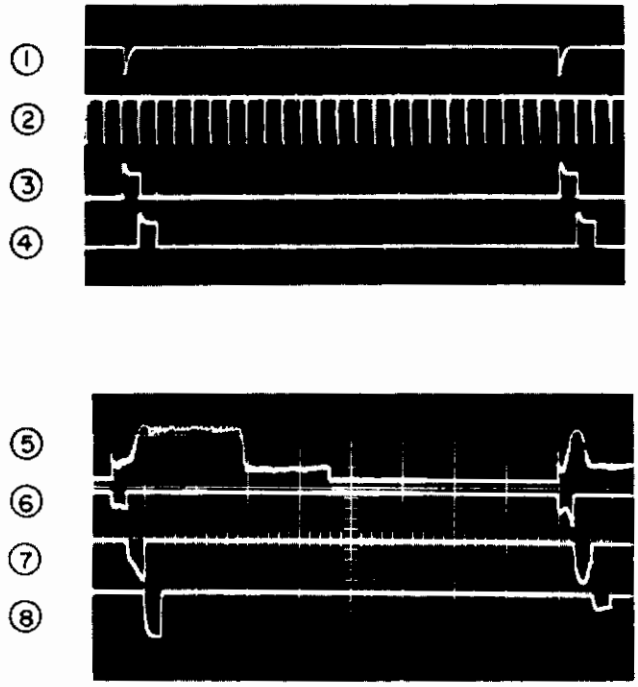


Figure 110. Column Shift Register and Column Drivers.



	WAVEFORM	VERT. SCALE	HOR. SCALE
①	1-kHz TRIGGER PULSE INPUT ON TERMINAL E	10 V/div	100 μsec/div
②	24-kHz SHIFT PULSE INPUT ON TERMINAL D	10 V/div	"
③	VOLTAGE ON COLLECTOR OF T1 (1st STAGE OF SHIFT REGISTER)	20 V/div	"
④	VOLTAGE ON COLLECTOR OF T4 (2nd STAGE OF SHIFT REGISTER)	20 V/div	"
⑤	ANALOG VIDEO SIGNAL INPUT ON TERMINAL F	10 V/div	"
⑥	COLUMN #1 DRIVE SIGNAL ON COLLECTOR OF T3	100V/div	"
⑦	COLUMN #2 DRIVE SIGNAL ON COLLECTOR OF T6	100V/div	"
⑧	COLUMN #3 DRIVE SIGNAL ON COLLECTOR OF T9	100 V/div	"

Figure 111. Waveforms for Column Shift Register and Column Drivers.

controlling the amount of emitter degeneration in each stage by the 250-Ω potentiometers. Even though the amplitudes of the column drive pulses can be equalized with these controls for any specific video signal level, the output signals unfortunately do not remain exactly equal at other video signal levels because the characteristics of the driver transistors are not accurately matched. A typical video signal and the outputs of column drivers #1, #2, and #3 (transistors T3, T6, T9) are illustrated by waveforms 5, 6, 7, and 8 in Figure 111.

H. POWER SUPPLIES

The lowermost chassis in the relay rack contains the power supplies for the display model. The circuits are shown in Figure 112. Six regulated supply voltages are provided by these circuits. There are two -16-V supplies, two -18-V supplies, one -100-V supply, all of which are series-regulated, and a +3.9-V bias supply which is shunt-regulated by a Zener diode. Reference voltages for the series-regulated supplies are also provided by Zener diodes.

The -100-V supply furnishes power for the collector circuits of the transistors providing row-select pulses, and the transistors providing the column drive signals for the display matrix. A bridge-type power rectifier is shared by the -100-V supply and the +3.9-V bias supply. The bias voltage is used to provide forward-bias for the transistors which drive the columns of the display matrix.

The two -18-V supplies also share a bridge-type power rectifier. The two identical regulator circuits are of standard design. Supply A furnishes power for the circuits which provide horizontal deflection and synchronization waveforms for the TV camera, the circuits which process the video output signal of the camera, and the preamplifier circuits for the excitation signals. Supply B furnishes power for the timing signal generators, the excitation generator, and the row and column shift registers.

The -16-V supplies again have identical circuits and are of large current capacity. Each has its own transformer and bridge-type rectifier. Turn-on transient protection is provided by a single 2-Ω resistor and time delay relay shared by the two supplies. The 2-Ω resistor is in the common return lead of the 3000-μF filter capacitors of these supplies. The 5-Ω surge-limiting resistor, 1N1764 diode, and 4-μF capacitor constitute a 150-V dc supply. When the power is turned on, the relay remains initially open. The 40-μF capacitor in parallel with the relay coil charges through the 1000-Ω resistor. When the capacitor has charged sufficiently, the relay is energized, and then receives sufficient current through the 1000-Ω resistor to remain energized. When the relay closes, in addition to shorting the 2-Ω surge-limiting resistor, the 40-μF capacitor is quickly discharged. This insures that the time delay circuit will recycle, should the power be only momentarily interrupted. The output voltages of the -16-V supplies are used to power the ten excitation waveform amplifiers for the ten rows of the display matrix. Supply A provides power for amplifiers #1 through #5, and Supply B for amplifiers #6 through #10.

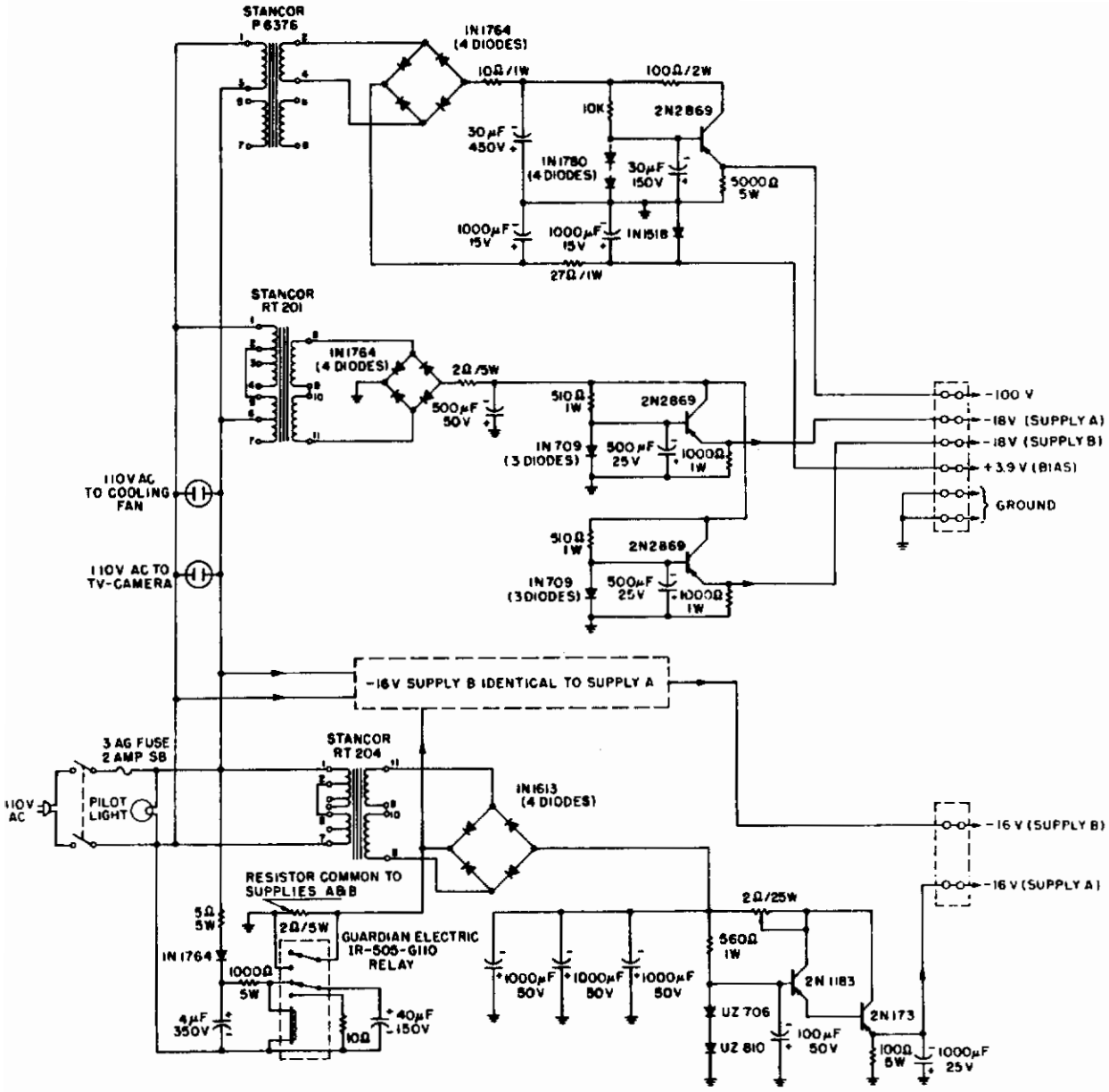


Figure 112. Power Supplies for Display Model Electronics.

The various connections from the power supply chassis to the other chassis in the relay rack are shown in Figure 113, which is the back-panel wiring diagram of display model electronics. All other interconnections between the chassis are also clearly indicated on this diagram. Figure 114 shows the back-panel wiring diagram of the chassis containing the plug-in boards #1 through #7.

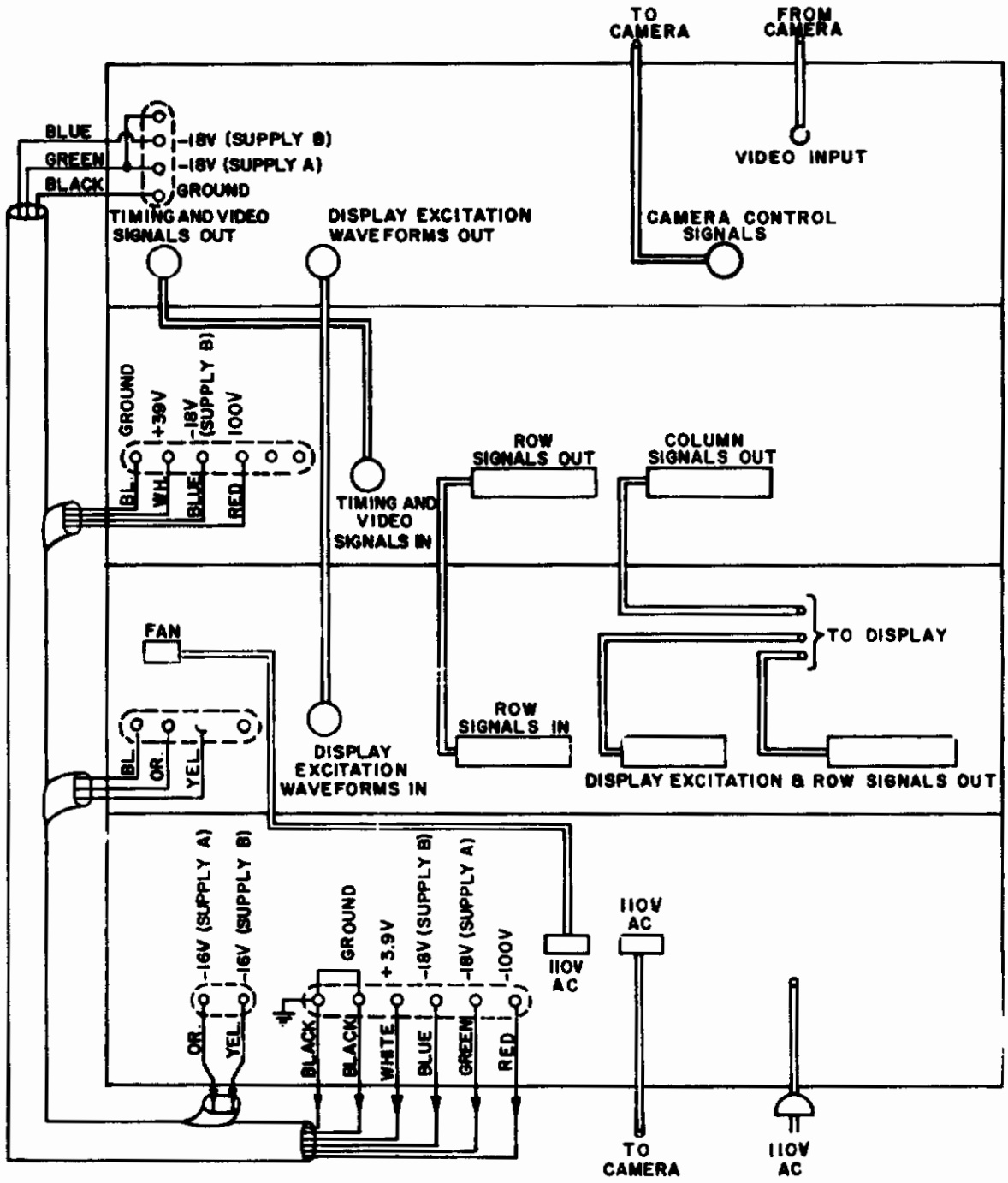


Figure 113. Back Panel Wiring for Display Model Electronics.

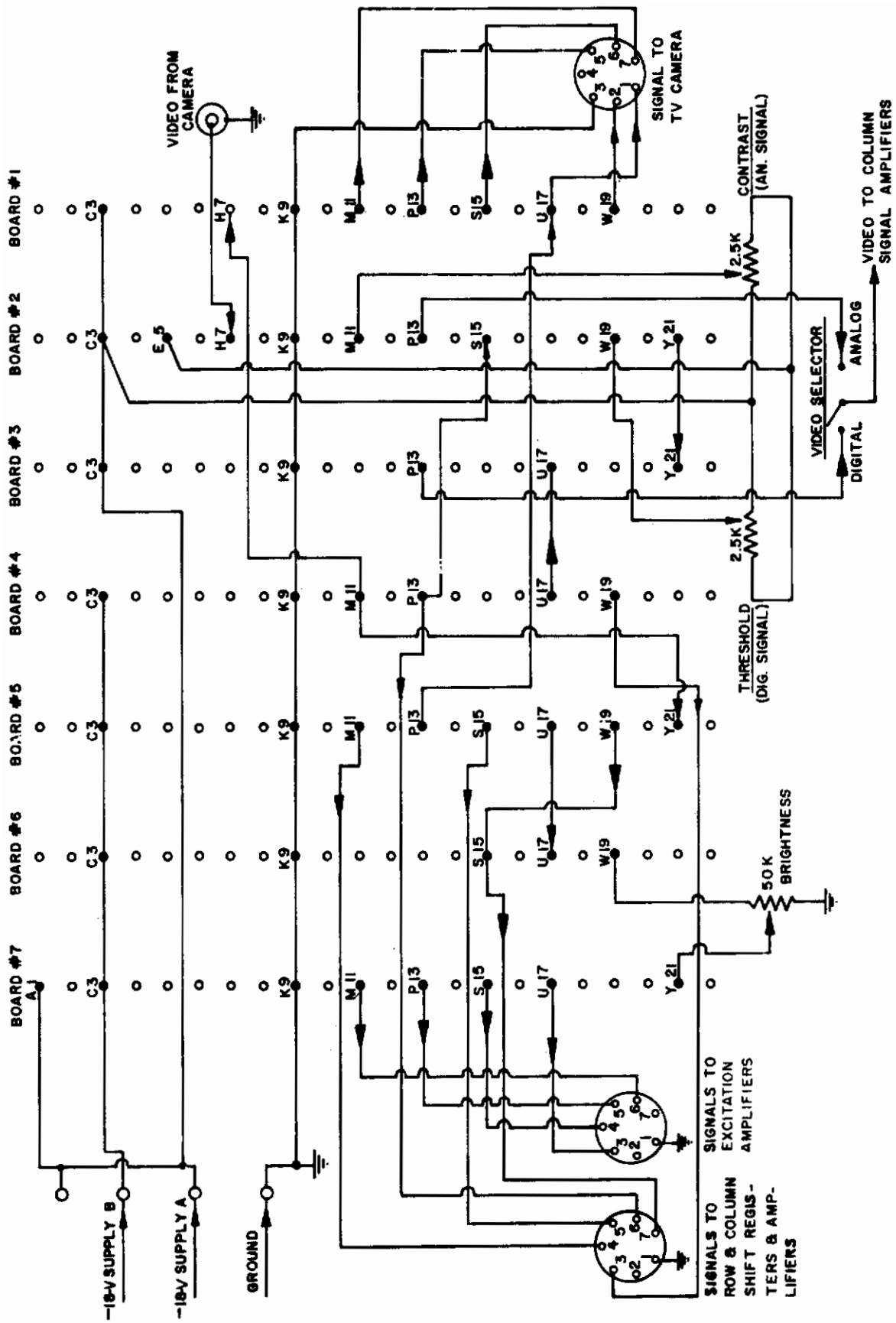


Figure 114. Front Panel Controls and Back Panel Wiring of Plug-In Boards.

APPENDIX II

ELECTRONICS FOR THE HIGH-BRIGHTNESS MODEL

In order to exercise the experimental model to show high brightness, electronic circuitry was required to provide the necessary excitation and addressing signals. Suitable transistor circuitry was designed and constructed to perform these functions. It includes a 2500-Hz power oscillator to provide the exciting signal for the electroluminescent cells, a -10-V regulated DC power supply for this oscillator, a -130-V DC power supply to provide bias and addressing signals, and the necessary circuitry for both analog and digital addressing of the display. The electronics are housed in a standard utility box as shown in Figure 115. The details of this circuitry are described in this Appendix.

Figure 115. Auxiliary Model to Show Brightness.

Figure 116 is a circuit diagram of the electronics for the auxiliary model to show high brightness. The portion of the circuit shown within the dotted area is mounted on the plug-in board. Only the odd-numbered pins are used on the board, and the socket is wired symmetrically so that the board may be plugged in either way. Transistors Q_1 and Q_2 and the Triad Type TY-82 toroidal transformer T_2 constitute a 2500-Hz square wave oscillator. One-ohm emitter resistors are used with Q_1 and Q_2 to improve stability, and bias is established for Q_1 and Q_2 by the resistive divider network R_1 and R_2. This bias is set at a point that is as close to cutoff as possible and yet allows reliable starting of the oscillator. The 0.005-μF capacitor across the output winding suppresses transients. Figure 117 shows the waveforms for this oscillator circuit. The output voltage from the oscillator is approximately 900 V peak-to-peak.

The oscillator is powered from a -10-V regulated DC power supply of conventional design. The supply utilizes the 6-V winding of transformer T_1, a full-wave voltage doubler, and a standard series regulator. Transistor Q_3 is the regulator transistor and the -10-V reference potential is established at its base by a 1N1523 Zener diode. The -130-V DC power supply for bias and addressing consists of half of the 250-V winding of T_1, a 4.7-Ω surge-limiting resistor, a 1N1764 diode, two 30-μF, 450-V filter capacitors, and a 1-kΩ filter resistor. A voltage divider consisting of a 27-kΩ resistor and a 25-kΩ potentiometer (a) provides adjustable negative bias for the model.

The -130-V supply is also utilized in the addressing circuitry to provide either analog or digital addressing signals to the display. In the analog mode, the 25-kΩ potentiometers (1) and (2) provide an adjustable DC signal to the two display elements. In the digital mode, the -130-V supply is connected to the bottom display element through <u>either</u> of the pushbutton switches (thus operating as an "OR" gate). In the digital mode the -130-V supply is also tied through a 15-kΩ resistor to the two 1N1764 "AND" gate diodes which are normally grounded. Only when <u>both</u> of the pushbutton switches have been depressed, thus "lifting" both 1N1764's from ground is the -130 V supplied as an addressing signal to the top display element (thus operating as an "AND" gate).

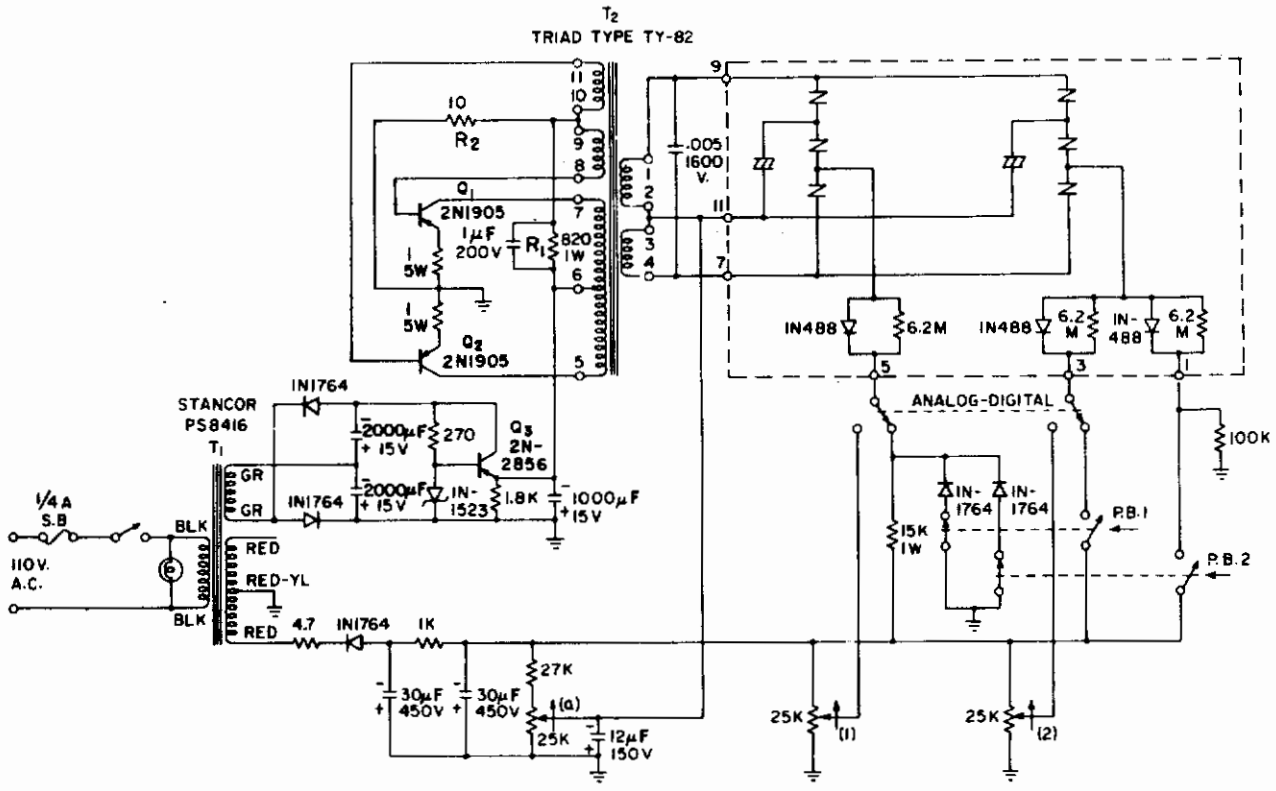
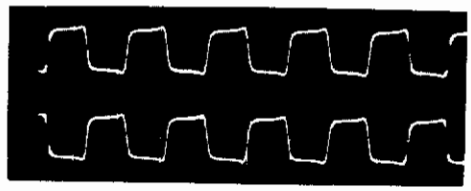


Figure 116. Electronics for High-Brightness Model.

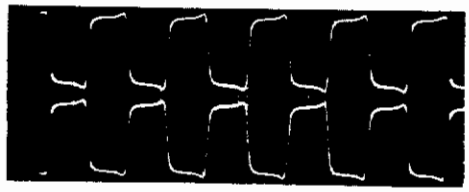
Hor. = 200 .sec/div. Vert. = 5 V/div.

(a) Base Voltage Waveforms
Top: Base of Transistor Q_1
Bottom: Base of Transistor Q_2



Hor. = 200 .sec/div. Vert. = 20 V/div.

(b) Collector Voltage Waveforms
Top: Collector of Transistor Q_1
Bottom: Collector of Transistor Q_2



Hor. 200 .sec/div. Vert. 250 V/div.

(c) Output Waveforms
Top: Transformer T_2 Pin 1
Bottom: Transformer T_2 Pin 4

Figure 117. Waveforms for the Electronics of the High-Brightness Model.

The setup procedure for the electronics is particularly simple, since only one adjustment need be made. This is the bias adjustment — potentiometer (a). To make the adjustment, the Analog-Digital Switch should be in the Analog position and both analog potentiometers (1) and (2) should be set to minimum. The bias potentiometer (a) should be advanced slowly until the electroluminescent cells are just extinguished. This completes the setup procedure.

APPENDIX III

ELECTRONICS FOR THE HIGH-RESOLUTION MODEL

Since the auxiliary model to show high resolution is electrically identical to the experimental model display constructed under Contract No. AF33(615)1193, the electronics designed and constructed for that model were used to exercise the high-resolution model. The electronics consists of suitable transistor circuitry designed and constructed to provide the necessary addressing and excitation signals. It includes a video matrix and a mechanically operated stepping switch to provide the necessary column-addressing signals to produce a moving halftone image on the face of the display. Figures 118 and 119 are front and rear views, respectively, of the complete electronic unit. The details of the circuitry are described briefly below and in detail in Reference 3.

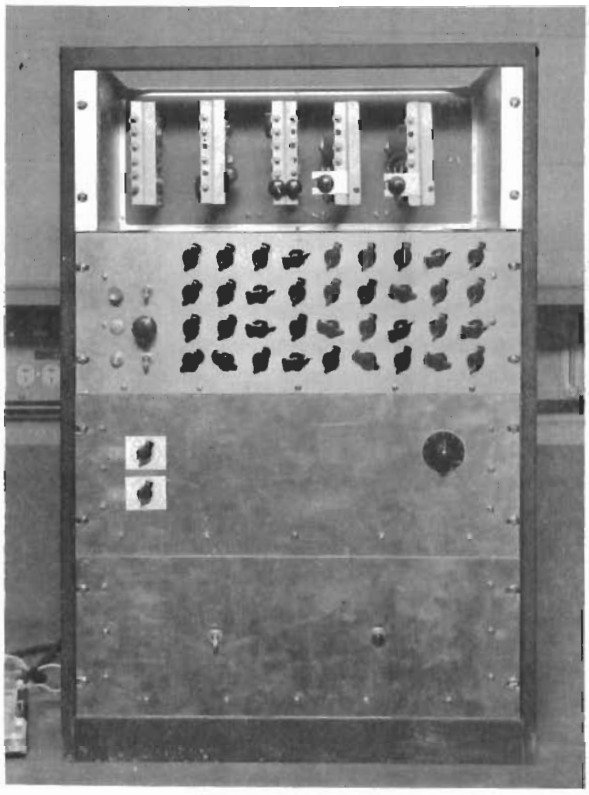


Figure 118. Electronics for High-Resolution Model (front view).

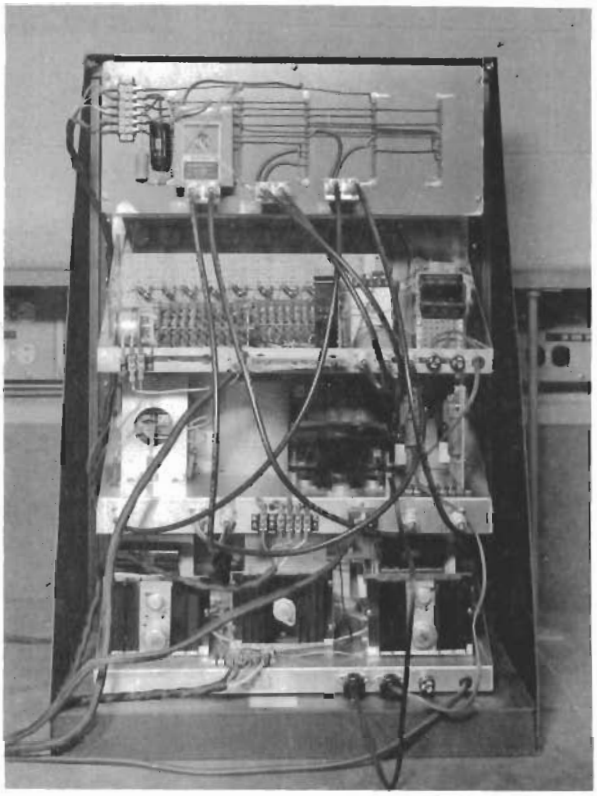


Figure 119. Electronics for High-Resolution Model (rear view).

Figure 120 is a block diagram of the display model electronic system, complete except for the column signal processing circuitry, and Figure 121 is a timing diagram for the electronics. The circuit operation is as follows:

The master timing signal is provided by the 900-Hz sine-wave generator. An output from the 900-Hz sine-wave generator is fed to a three-stage synchronized multivibrator divider chain which divides the frequency by 30. The last stage of this divider which operates at 30 Hz is the 30-Hz clock that establishes the frame rate of 30 per second for the display model. Four outputs (waveform 1 in Figure 121) are taken from the 30-Hz clock; these are fed to the disturb pulse gate, the sine-wave gate delay circuit, and the row 1 and row 2 delay circuits. When the 30-Hz clock operates, the disturb pulse gate produces a 300-μsec pulse (waveform 2 in Figure 121) to disable the disturb pulse generator for this interval. Except when disabled, the disturb pulse generator, a free-running multivibrator, produces 30-μsec disturb pulses at a rate of approximately 12.5 kHz (waveform 13 in Figure 121). These pulses are amplified to the necessary 60-V level by the disturb pulse amplifier. Another output from the 30-Hz clock is fed to the sine-wave gate delay circuit, which provides a 20-μsec delay. Its output triggers the sine-wave gate generator, which generates a 250-μsec gate pulse (waveform 3 in Figure 121). This pulse is fed to the sine-wave gate to clamp the 900-Hz sine wave to zero for the pulse duration. The resulting gated sine wave (waveform 4 in Figure 121) is amplified by the preamplifiers and the row 1 and row 2 sine-wave amplifiers. Front-panel gain controls are provided for each of these amplifiers and serve as brightness controls for rows 1 and 2 of the display model.

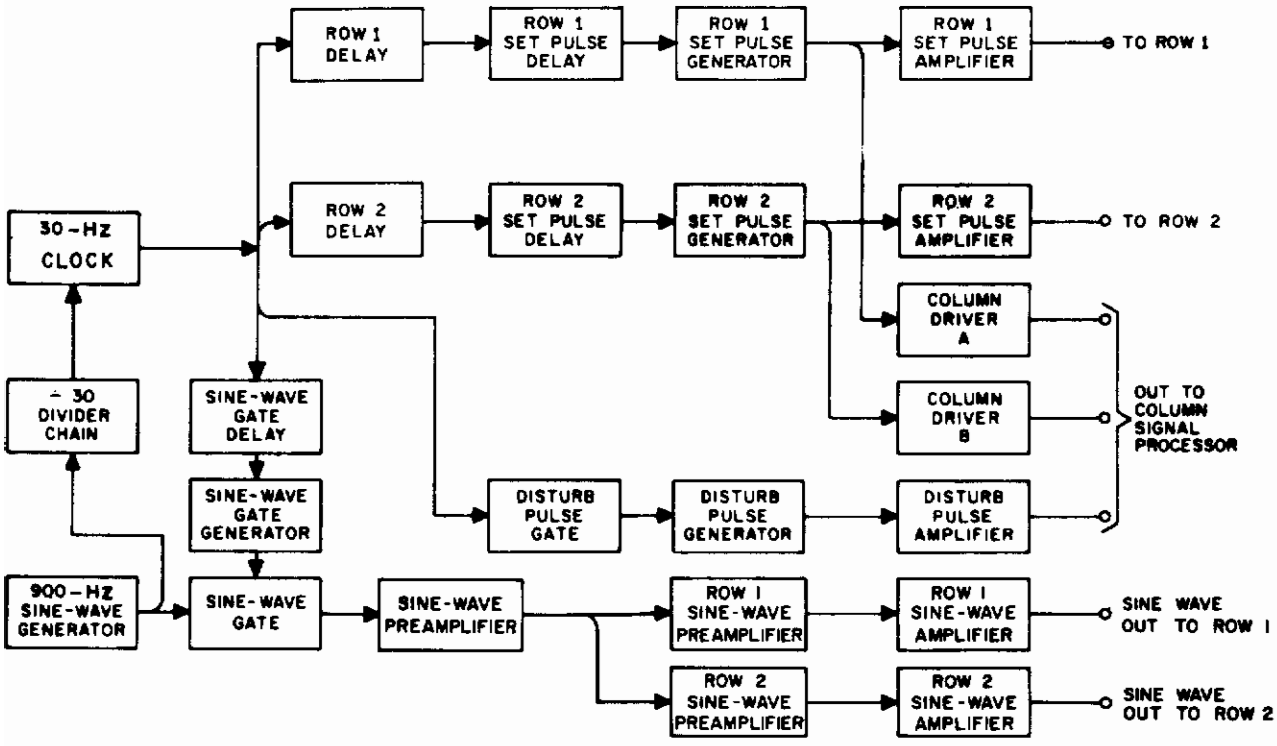


Figure 120. Block Diagram of Display Model Electronics.

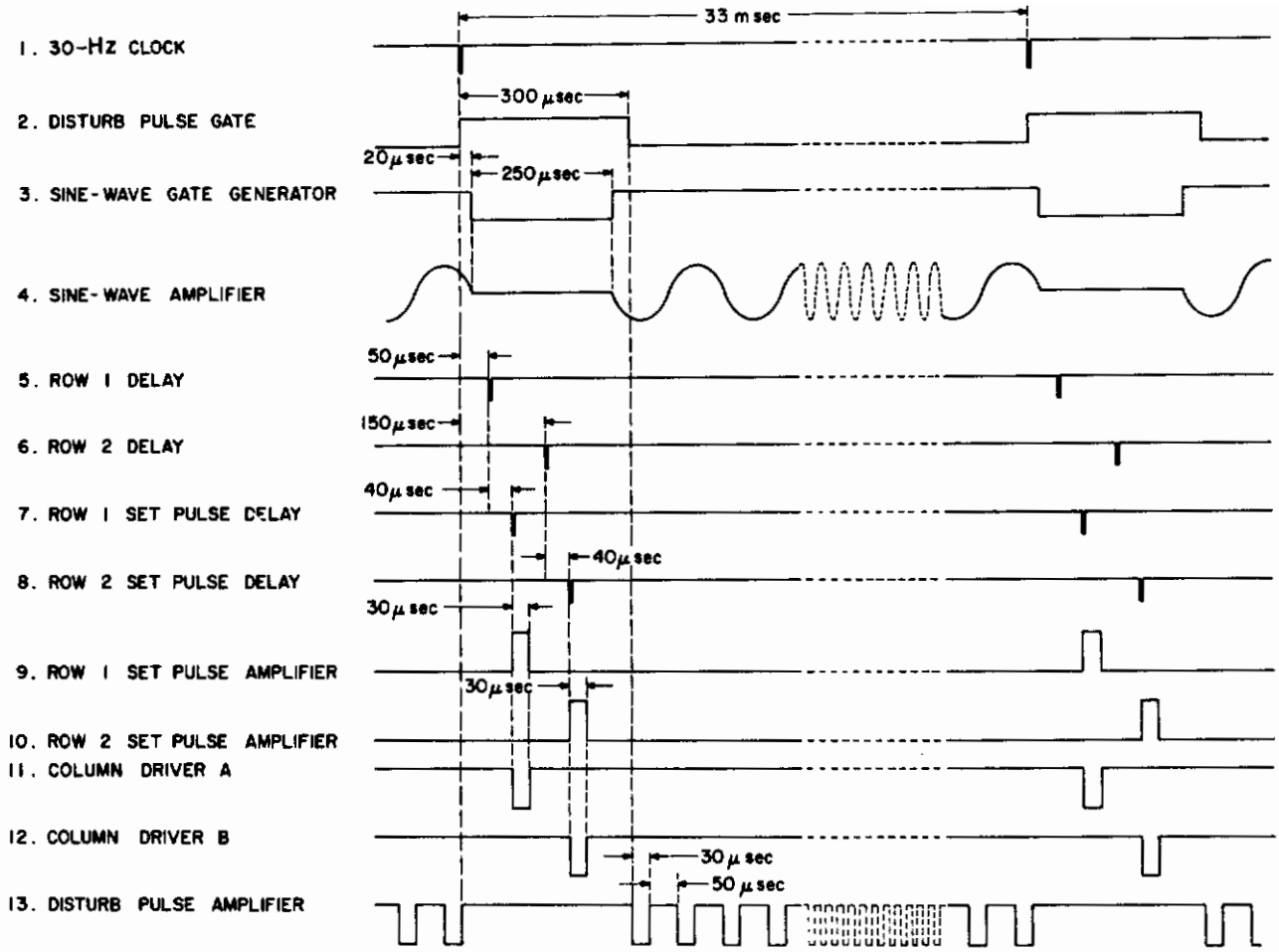


Figure 121. Timing Diagram for Display Model Electronics.

The remaining outputs from the 30-Hz clock are fed to the row 1 and row 2 delay circuits, which provide delays of 50 μsec and 150 μsec, respectively (waveforms 5 and 6 in Figure 121). The outputs of the row delay circuits feed the row 1 and row 2 set pulse delay circuits, which each provide a 40-μsec delay. The output from the row 1 set pulse delay circuit thus occurs 90 μsec (50 + 40) after the pulse from the clock, and the output from the row 2 set pulse delay circuit occurs 190 μsec (150 + 40) after the pulse from the clock. (waveforms 7 and 8, respectively, in Figure 121). The outputs from the row 1 and row 2 set pulse delay generators trigger the row 1 and row 2 set pulse generators, respectively, which in turn produce 30-μsec pulses that are amplified by the set pulse amplifiers and by the column drivers. The set pulse amplifier outputs are positive-going 30-μsec pulses (waveforms 9 and 10 in Figure 121). The column drivers provide negative-going 30-μsec pulses coincident with the output pulses from the set pulse amplifiers (waveforms 11 and 12 in Figure 121). The outputs from the set pulse amplifiers are combined with the outputs from the sine-wave amplifiers and fed to the row bus connections of the model. The outputs from column drivers A and B and from the disturb pulse amplifier are matrixed and switched in the column signal processor and then fed to the column busses of the display model.

Figure 122 is a schematic diagram of the column signal processor, video matrix, and column driving circuitry; and Figure 123 shows the waveforms for this circuitry. In Figure 122, the input signals from column drivers A and B each feed a bank of 18 potentiometers (for clarity only three are shown); 18 groups of three emitter followers each (again only three are shown) derive signals from these potentiometers and from the input from the disturb pulse amplifier. The signals at the bases of the 2N398B output emitter followers (points e, f, g, etc.) will thus be: a pulse when column driver A operates, a pulse when column driver B operates, and then a chain of disturb pulses at a 12.5 kHz rate. The amplitudes of the pulses that occur when the column drivers operate will depend on the settings of the 36 potentiometers; the panel-mounted potentiometers are thus used to establish a video halftone pattern for the display.

As shown in Figure 123(a) the input signals are all nominally 60-V negative-going pulses. Except when these negative input pulses are present, the 2N398 emitter-follower transistors are held cutoff. Since transistor dissipation is limited, it is essential that the input pulses from the disturb pulse amplifier be of sufficient amplitude to drive the emitter-follower transistors T_{11}, T_{21}, T_{31}, etc., into saturation; otherwise their dissipation ratings will be exceeded. Since their duty cycle is much lower, the column driver signals need not drive the transistors to saturation. The 2N398B

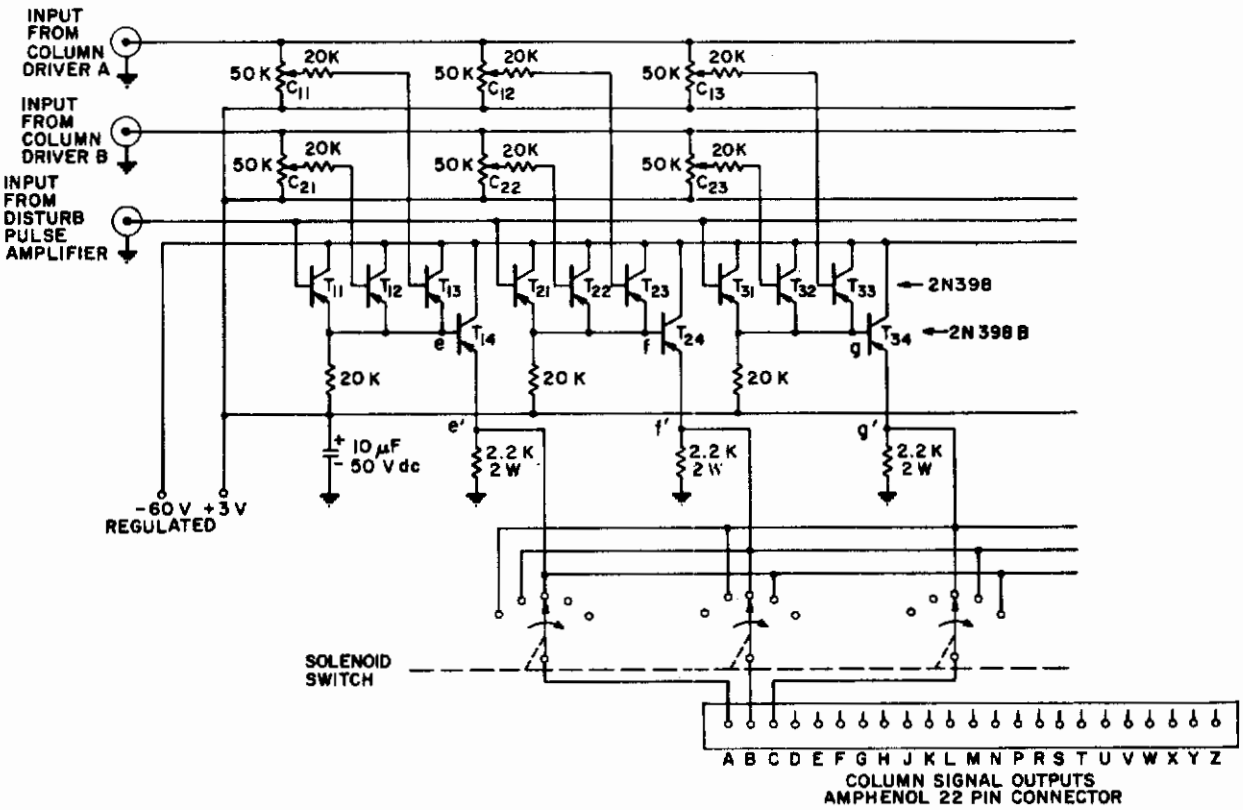
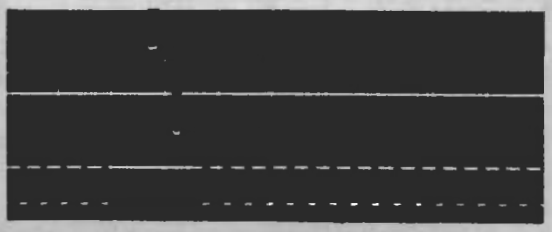


Figure 122. Column Signal Processor, Video Matrix, and Column Driving Circuitry.



Hor. = 200 μsec/div Vert. = 100 V/div

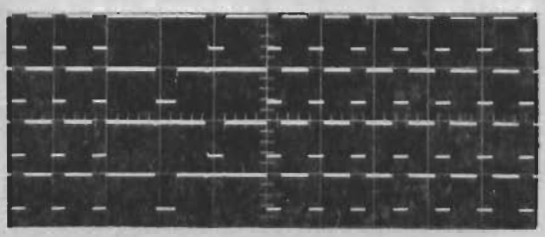
(a) Column processor input waveforms

Top: Input from column driver A
Middle: Input from column driver B
Bottom: Input from disturb pulse amplifier

Hor. = 100 μsec/div Vert. = 100 V/div

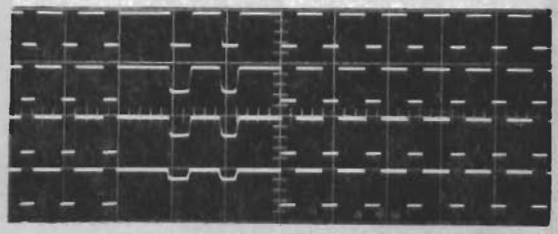
(b) Column signal output waveforms with video matrix set to produce a checkerboard pattern (solenoid switch in home position).
From top to bottom:

Terminal A	Column 1
Terminal B	Column 2
Terminal C	Column 3
Terminal D	Column 4



Hor. = 100 μsec/div Vert. = 100 V/div

(c) Same as in (b) but with the stepping switch advanced one position



Hor. = 100 μsec/div Vert. = 100 V/div

(d) Column signal output waveforms with video matrix set to produce a shading bar (solenoid switch in home position).
From top to bottom:

Terminal A	Column 1
Terminal B	Column 2
Terminal C	Column 3
Terminal D	Column 4

Figure 123. Waveforms for the Column Signal Processor, Video Matrix, and Column Driving Circuitry (Figure 122).

emitter-follower transistors T_{14}, T_{24}, T_{34}, etc., provide the necessary current gain to drive the column busses of the display model. By emitter follower action the signals at points e', f', and g' are replicas of the signals at points e, f, and g, respectively. The load resistance for each 2N398B emitter follower is 1.1 kΩ, consisting of the parallel combination of a 2.2-kΩ resistor mounted on the column processor chassis and another 2.2-kΩ resistor mounted on the display model chassis at the other end of the interconnecting cable.

The outputs from the 2N398B emitter followers (e', f', g', etc.) are connected to an 18-gang, 18-position solenoid-driven rotary switch (only three gangs and five positions are shown). Rotation of the switch causes the output terminals A, B, C, D, etc., to be progressively connected to the emitter-follower outputs e', f', g', etc. With the switch in its home position e' is connected to A, f' to B, g' to C, etc. One switch position clockwise, e' is connected to B, f' to C, g' to D, etc. Figure 123(b) shows the output waveforms at terminals A, B, C, and D for a checkerboard pattern with the solenoid switch in its home position. To produce the checkerboard pattern potentiometer C_{11} has been set to maximum, C_{21} and C_{12} to minimum, C_{22} and C_{13} to maximum, C_{23} to minimum, etc. Figure 123(c) shows the same output waveforms for the same video pattern but with the solenoid switch advanced one position. Figure 123(d) shows the output waveforms at A, B, C, and D for a halftone shading bar. In this case the solenoid switch is in its home position, potentiometers C_{11} and C_{21} have been set to maximum, C_{12} and C_{22} to three-quarters, C_{13} and C_{23} to half and C_{14} and C_{24} to one-quarter. It is thus possible, by appropriately setting the 36 potentiometers, to establish any desired halftone pattern on the face of the display and then, by operating the solenoid-driven rotary switch, to move this pattern from left to right across the face of the display.

The solenoid switch may be operated manually with a front-panel push-button or automatically with built-in stepping circuitry. When operated automatically, a front-panel control permits continuous adjustment of the stepping rate from several seconds per step to several steps per second.

As can be seen from the photographs of Figures 118 and 119, the display model electronics are built in a standard 30-inch table-top relay rack and consist of four separate chassis. The uppermost chassis in the rack contains all of the circuitry shown in the block diagram of Figure 120, except the disturb pulse amplifier and the row 1 and row 2 sine-wave preamplifiers and amplifiers. The circuits are mounted on five plug-in boards. The second chassis from the top contains the column signal processor (including the video matrix and the solenoid-driven rotary switches) and the power supply for the video matrixing circuitry. The third chassis from the top contains the disturb pulse amplifier and the row 1 and row 2 sine-wave preamplifiers and amplifiers, and the bottom chassis contains the power supplies for all circuits except the video matrixing circuitry.

For a complete description of the electronics, including detailed schematic diagrams, waveform photographs, and adjustment procedures, the reader is referred to Reference 3.

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DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) Radio Corporation of America RCA Laboratories Princeton, New Jersey	2a. REPORT SECURITY CLASSIFICATION Unclassified 2b. GROUP N/A

3. REPORT TITLE

PRELIMINARY DEVELOPMENT OF A SOLID-STATE MATRIX DISPLAY

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Final Report — April 1, 1964 to April 30, 1965

5. AUTHOR(S) (Last name, first name, initial)

Lechner, Bernard J.

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
January 1967	146	6

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
AF33(615)1493 b. PROJECT NO. 6190 c. Task No. 619009 d.	AFFDL-TR-66-5 9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)

10. AVAILABILITY/LIMITATION NOTICES

Distribution of this document is unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
Final Report	Air Force Flight Dynamics Laboratory Research and Technology Division, AFSC Wright-Patterson Air Force Base, Ohio

13. ABSTRACT

The use of ferroelectric transchargers as storage and control elements in an electroluminescent matrix display is reported. Research on display panel circuitry led to control circuits useful for solid-state matrix display. In these circuits, ferroelectric elements provide analog storage and control energization of electroluminescent cells in accordance with stored analog signals. The ferroelectric, in conjunction with a diode, provides a selection threshold which permits the element to be addressed in a matrix by voltage coincidence. The new circuits give greatly improved brightness and contrast compared with previous ferroelectric control circuits. Transcharger circuits with logic capability have also been developed; such circuits are especially useful for bar graph, moving pointer, and similar displays. Three experimental model displays demonstrated brightness as high as 48 ft-L; contrast ratio in excess of 100:1; geometric resolution as great as 10-elements per in.; capability for producing a gray scale; and a frame rate which allows continuity of motion without blurring or flicker. The performance of these models demonstrates the potential of using ferroelectric control circuits and electroluminescent elements for high-brightness, high-resolution, all solid-state matrix displays.

DD FORM 1 JAN 64 1473

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Solid-State Matrix Display Ferroelectric Elements Ferroelectric Transchargers Electroluminescent Elements Display Systems						

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