

**PULSE DURATION MODULATION
MULTIPLEXER**

JOHN G. HOWELL

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FOREWORD

This research was conducted by Space Craft, Inc., 8620 South Memorial Parkway, Huntsville, Alabama, on Air Force contract AF 33(615)-5076 and in support of Project 7222, "Biophysics of Flight." This contract was monitored by A. R. Marko, Medical Electronics Branch, Environmental Medicine Division, Biomedical Laboratory, Aerospace Medical Research Laboratories, Wright-Patterson Air Force Base, Ohio 45433.

The work presented began in June 1966, was concluded in September 1966, and represents the efforts of the Telemetry Systems Group of Space Craft, Inc. The engineers who participated in the project were John G. Howell and O. Leon Pierce.

This technical report has been reviewed and is approved.

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Technical Director
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ABSTRACT

This report describes the Research and Development Study of a Pulse Duration Modulation Multiplexer for use in personal telemetry systems. The objective of the program was to develop a low power, accurate pulse duration modulation multiplexer which has the potential of small physical size and low weight. The technical approach includes the design of low power logic, the use of the most advanced multiplexer switch, and the development of a unique amplification and comparison technique. All the system general requirements and specific requirements are satisfied by the design. The system performance is demonstrated by a laboratory breadboard model. Results of the tests performed on the model verify the feasibility of the engineering design.

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SECTION I

INTRODUCTION

This document relates Space Craft's approach to the design and development of an advanced seven channel multiplexer with pulse duration modulation output. The design described is considered to offer a system which best meets the requirements for low power, high accuracy and potentially small size system. To design a personal telemetry system which has the potential for exceeding these requirements, a unique, yet simple, design approach was required. The following characteristics were considered in the design:

- A. Low power consumption
- B. High temperature stability
- C. High resolution (accuracy)
- D. Potential for small size and low weight

An advanced low level multiplexer utilizes Metal Oxide Semiconductor Field Effect Transistors (MOS-FET) for switches. These devices are relatively new and offer the advantages of small size, simplicity of selection and drive circuitry and excellent temperature stability. Also, MOS switches are available in multiple switch arrays in a flat pack.

A single amplifier is used to provide high input impedance, amplify the 0-20 mv sample to high level (0-4 volts), and compare the amplified level to an accurate ramp (reference) voltage to produce the required PDM output.

The multiplexer switches are selected and driven by use of a unique low power logic circuit connected in an eight stage ring counter configuration. Each stage consists of complementary transistor (NPN-PNP) pairs which are turned on sequentially and dissipate power only in the ON condition. These stages also act as drivers for the MOS switch, since the transistor has extremely high input impedance (10^{15} ohms) at the gate.

The system clock is a low power (complementary) multivibrator circuit, which furnishes the basic timing for selection and control.

Integrated circuits have been considered in all areas of the design, but are ruled out due, in general, to high power consumption. The design concepts described are based on maximum simplicity to minimize power required, yet offer a potential size, weight, and cost advantage. The potential size using various techniques will be demonstrated in this report.

SECTION II

TECHNICAL DESCRIPTION

System

The overall system block diagram is shown in figure 1, and the system timing is shown in figure 2. The basic system concept is as follows. Very low power logic circuits are used for timing and control. The logic circuits drive the MOS switch elements to produce a single time shared wavetrain to the input of a low power relatively high speed amplifier. This single amplifier operates in both a sample and compare mode to produce the Pulse Duration Modulation Output. For discussion purposes the system is divided into two main blocks; i. e., the basic multiplexer and logic and the analog circuitry.

Multiplexer and Logic

The basic multiplexer switches are mechanized using seven MOS transistors. The MOS transistor offers extremely low power, potentially small size and simplicity for low level switching. Leakage currents from the switch into the source are less than 1 nanoampere at ambient temperature causing a negligible error at the specified source impedance. No offset is introduced by the switch, since no junction is in the signal path. The comparatively high ON resistance (300 ohms) of this type of device is compensated by the high input impedance to the low level amplifier (> 10 megohms); thus, the effect on overall system accuracy is negligible. The power required for this part of the system operation is less than 1 milliwatt.

One problem was encountered in the use of the MOS during the design phase. Switch turn-on voltage, originally -7.5 volts, had to be increased to achieve proper series ON resistance. This was accomplished without increasing the primary system power supply voltages, using the voltage doubler circuit shown in figure 3. As the switch drive voltage swings between +7.5 and -7.5 volts the switch gate swings between ground and -15 volts since the gate is clamped at ground and the drive point goes from +7.5 volts to -7.5 volts when the switch is to be turned ON.

The system logic is composed of an eight bit ring counter driven by a low power four transistor clock. The clock circuit (figure 4) is designed for 3 milliwatt operation and is compensated for stable operation (0.1%) over the required temperature range. The clock circuit represents a basic low power circuit technique with the two PNP transistors serving as ideal loads for the two NPN transistors; i. e. Q2 offers a high impedance when Q1 is

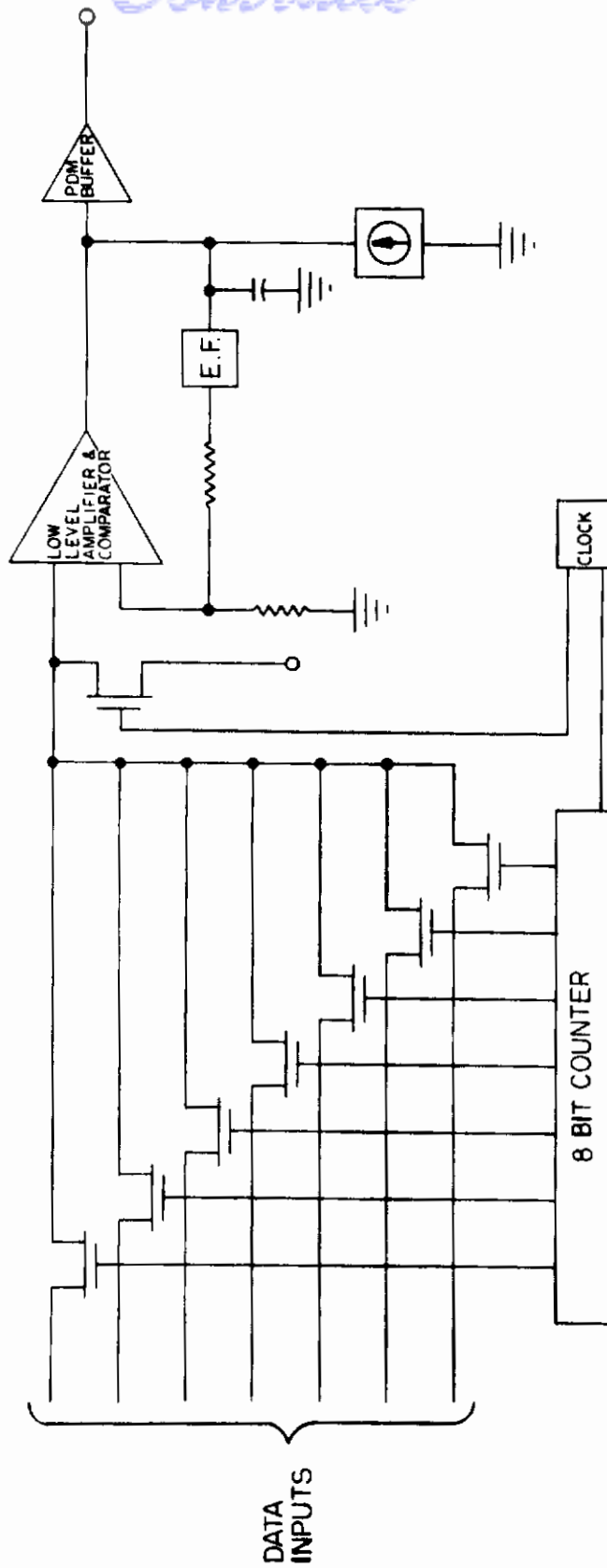


FIGURE 1
SYSTEM BLOCK DIAGRAM

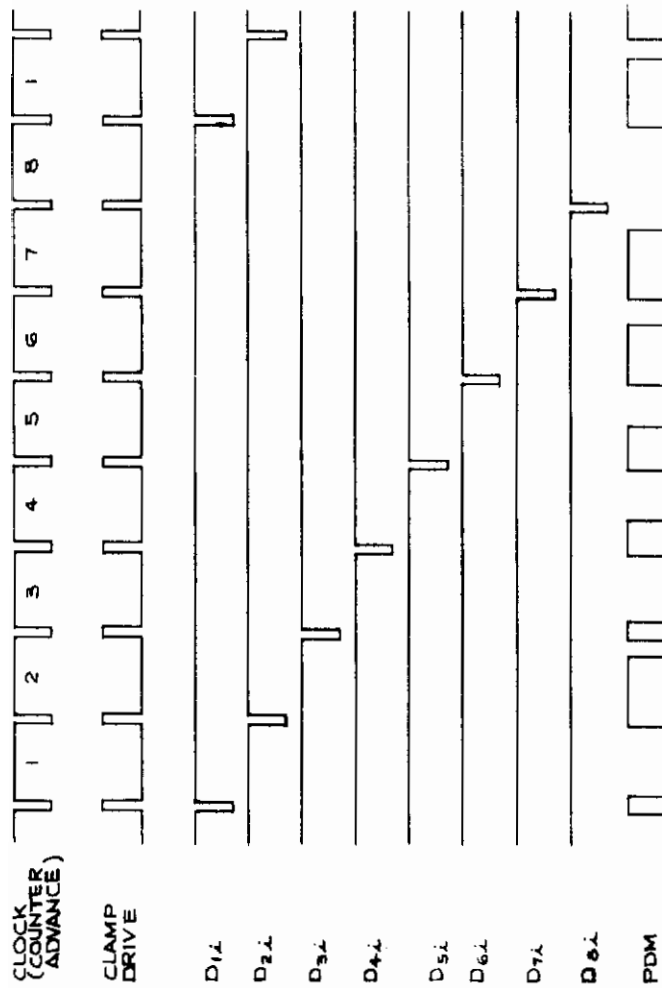


FIGURE 2
SYSTEM TIMING DIAGRAM

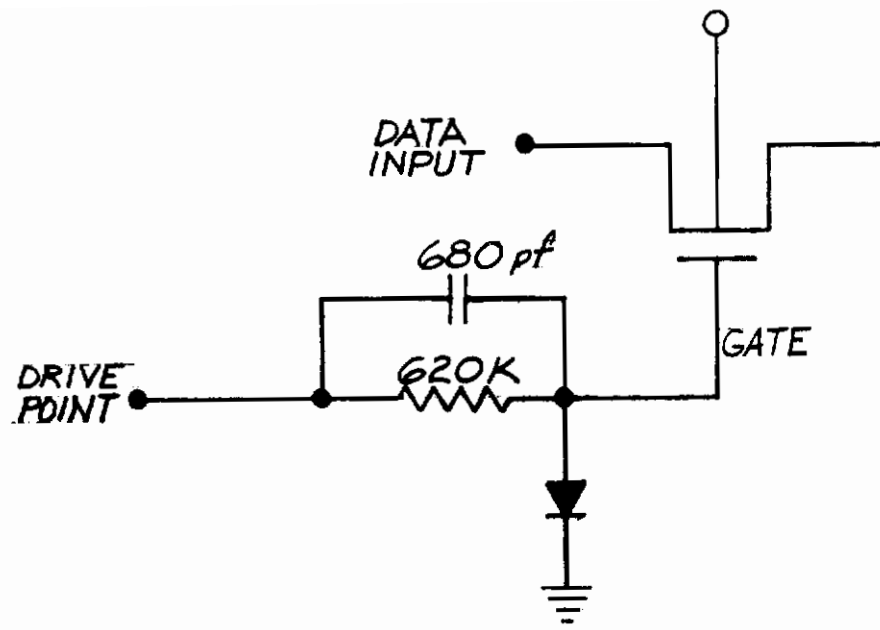


FIGURE 3
VOLTAGE DOUBLER CIRCUIT

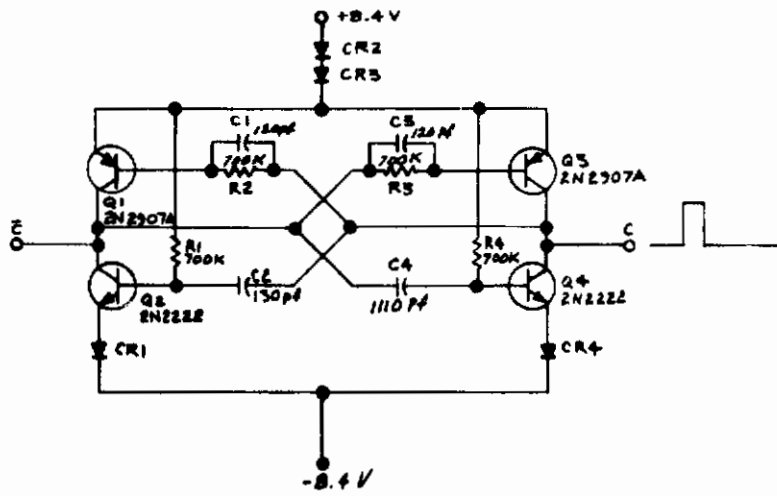


FIGURE 4
CLOCK

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conducting and a low impedance when Q1 is OFF. The circuit also operates extremely well at 90% duty cycle and exhibits excellent drive characteristics.

The clock drives the eight bit ring counter logic shown in figure 5 (schematic shown in 6). The counter is mechanized using low power two-transistor flip flops which draw power only when they are a logic ONE. In the ring counter configuration, only one stage is a logic ONE at any one time resulting in a total power consumption of 5 milliwatts for the complete selection and drive circuit. To insure that no more than one logic ONE is circulated in the counter, a seven input gate examines the state of D1 through D7 and inhibits the clock input to D1 when one or more of these stages is at a logic ONE. Thus, the counter will always count to a valid state if an error is introduced due to noise or when power is originally applied. The electrical schematic of the counter is shown in figure 6. The counter outputs D1i through D7i drive the multiplexer switch drive points directly; thus, eliminating the requirement for separate switch drivers. Counter stage D8 is used to inhibit the PDM output during the synchronization period.

Analog Circuits

The analog circuitry, figure 7, takes the output from the multiplexer switches and generates the pulse duration modulation output. This section is composed of the low level amplifier and comparator, constant current generator and the PDM output driver.

The incoming data is sampled for 10% of one word time. The amplitude of the data sample is stored in capacitor C_7 . At the end of the sample period the multiplexer switches open and MOS transistor Q_{16} clamps the amplifier input to a small negative voltage causing amplifier output to swing negative. Diode CR5 becomes back biased effectively disconnecting the amplifier output from the sample capacitor. Constant current generator, Q_{14} , Q_{15} , begins discharging C_1 at a linear rate. The voltage on the sample capacitor is sensed continuously by the high current gain buffer, Q_9 and Q_{10} , and fed back to the amplifier input (base of Q_6). When the ramp voltage equals the clamped input voltage the amplifier output switches positive. This defines the end of the PDM pulse time. The start of the PDM pulse is caused by the clock forcing the PDM output driver positive, through Diode CR6, at the beginning of the sample time. When the amplifier input is clamped at the end of the sample period the amplifier output goes negative. This point is applied to the base of Q_{12} and holds the PDM output positive until the amplifier switches at the end of the pulse period. Since the sampling capacitor discharges at a constant linear rate the time required for the ramp to discharge to the point where the feedback voltage is equal to the input voltage is determined by the starting point of the ramp. The starting point of the ramp is determined by the level of the input signal; thus, the output pulse duration is proportional to the input signal level.

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The amplifier input is clamped to a slightly negative voltage so that if the input voltage is zero the output PDM will equal 20% of the word time.

The amplifier proper is composed of two differential stages, Q_2 , Q_5 and Q_3 , Q_4 . The collector of Q_3 is referenced to ground rather than the conventional collector load to improve the common mode characteristics. A buffer stage, Q_7 and Q_8 , is added in front of each differential input to reduce amplifier input current and improve the loop gain. Amplifier gain is further improved by the addition of a "single-ended" voltage gain stage Q_7 . The output of Q_9 drives a current gain stage Q_8 to obtain the final amplifier output. Diode, CR5, acts as a switch; i. e., it is back biased during the compare mode and forward biased during sample mode. Amplifier response is further tailored by R16 and R18 which control the rate of charge of the sample capacitor.

Switching spikes on the amplifier input occurred as the result of coupling from the input clamp drive signal. These spikes were reduced to a tolerable level (0.1%) by the addition of a 75pf capacitor to ground and a 2k resistor in series with a 2pf capacitor connected to the logic complement of the clamp drive. The energy coupled into the amplifier input cancels the coupled energy from the clamp switch.

Transistor Q_{13} is referenced to the constant current generator Q_{14} and Q_{15} to establish a negative input clamp voltage which is not dependent on power supply variations. Resistors R_{31} and R_{32} are adjusted to establish 20% modulation with zero input voltage.

Over voltage clamping is established by transistor Q_{11} which conducts when the input rises above 20 millivolts. The bias point for Q_{11} is zener regulated to provide stability with power supply variations.

Full scale modulation is set to 80% by adjusting R_{34} in the constant current generator or adjusting the value of the sample capacitor (C7).

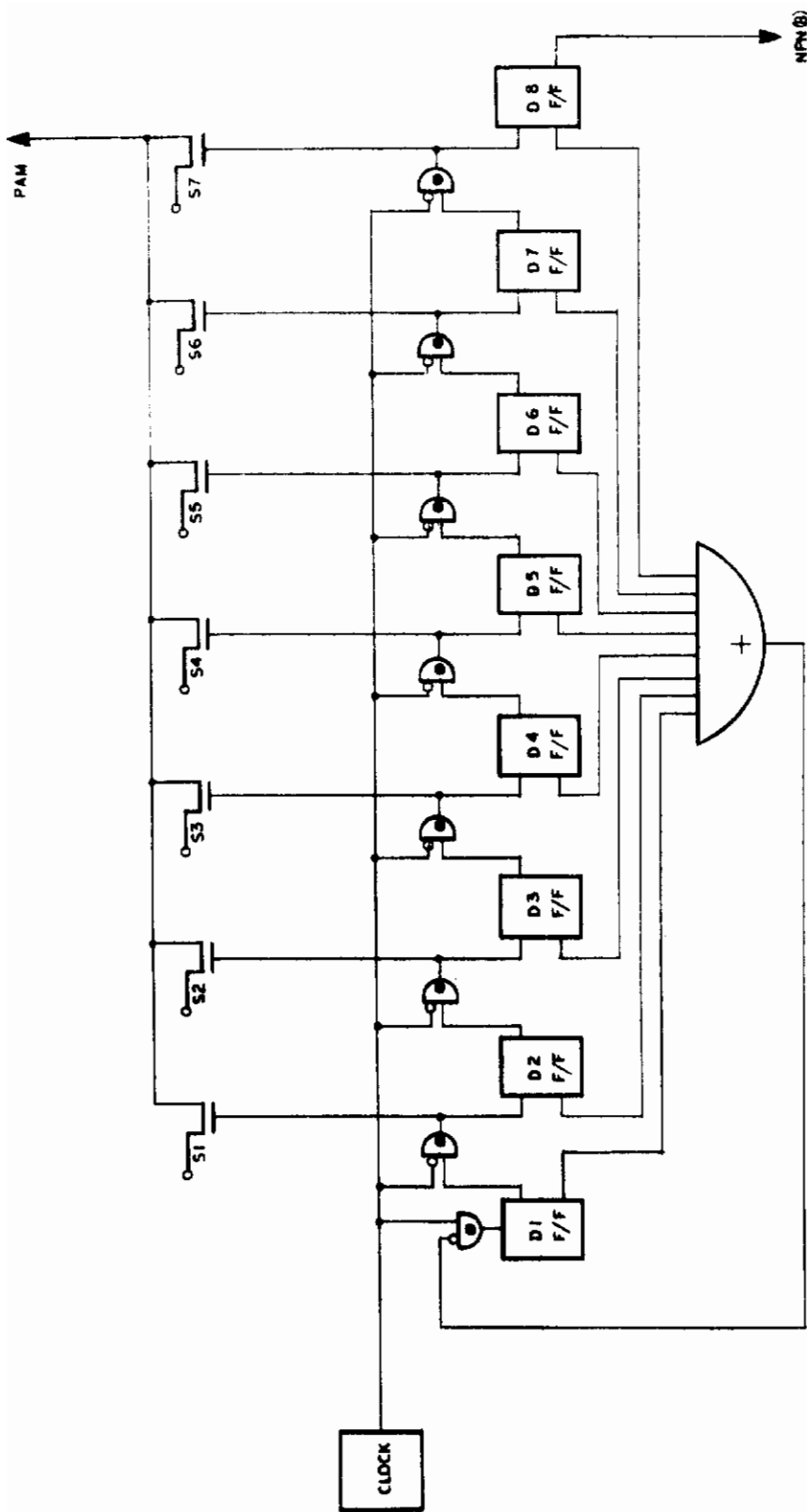


FIGURE 5
EIGHT BIT RING COUNTER LOGIC DIAGRAM

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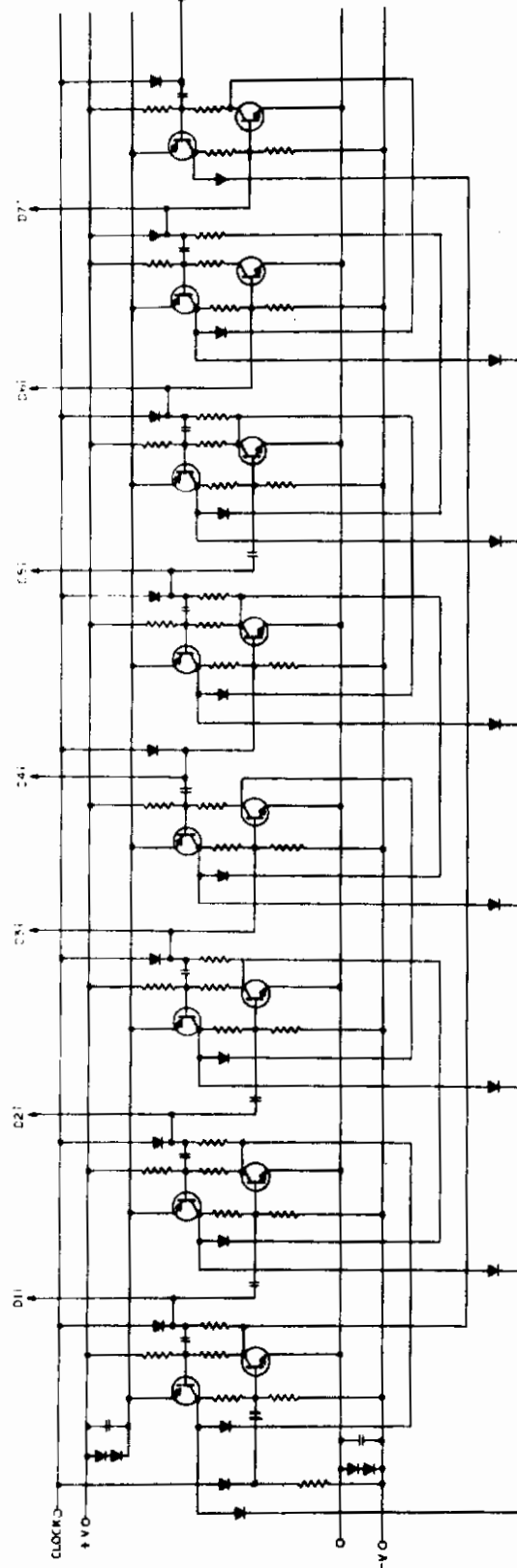


FIGURE 6
EIGHT BIT RING COUNTER SCHEMATIC

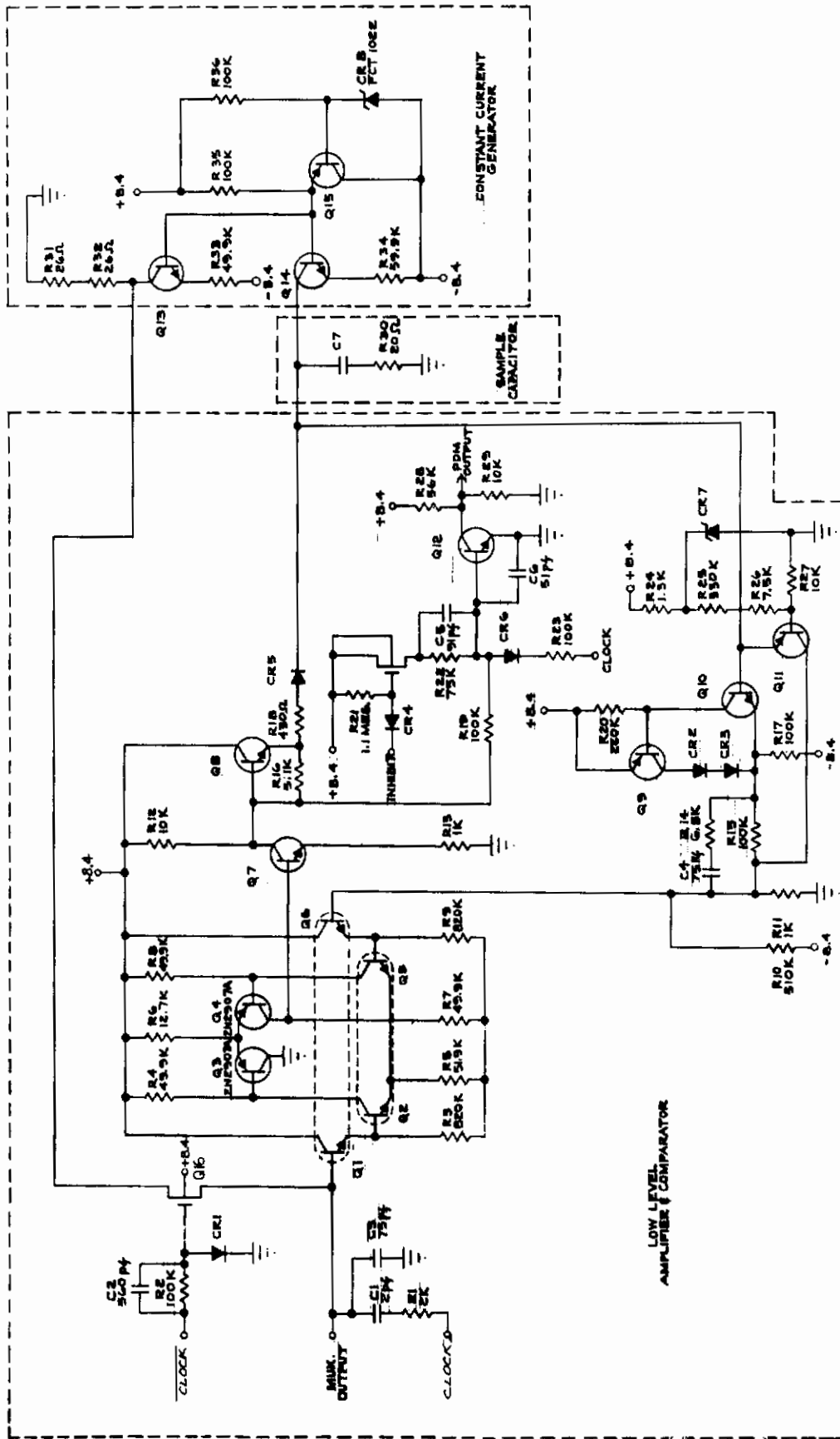


FIGURE 7
ANALOG CIRCUITS

SECTION III

PROPOSED PACKAGING

General Packaging Approach

A preliminary system package design is submitted to illustrate the potential small size and low weight of the design.

The electronic packaging concept proposed for the PDM system is one that Space Craft, Inc. has used successfully in many applications. In general, electronic components such as resistors, capacitors, diodes, transistors, and microcircuits are assembled into a cordwood welded wire module. These assemblies are encapsulated in an epoxy compound or urethane foam. The encapsulated component assembly is placed on a printed circuit board. The leads from the module pass through holes in the board and solder to printed pads. Printed circuit wires interconnect the soldered pads. The clad side of the interconnect board is covered with a polyurethane coating.

The system package concept is illustrated by figure 8. The total volume is 29.5 cubic centimeter at a weight of 42.6 grams.

Detailed Packaging

Two welded module layouts and a sample module are submitted to demonstrate the package concept. The module layouts are drawn on a five to one scale. Figure 9 is the module layout of a counter stage using conventional discrete components. This approach represents small size at a reasonable cost.

Figure 10 illustrates the same circuit packaged with microminiature discrete components. This represents a considerable size reduction with a material price increase of about \$6 per module.

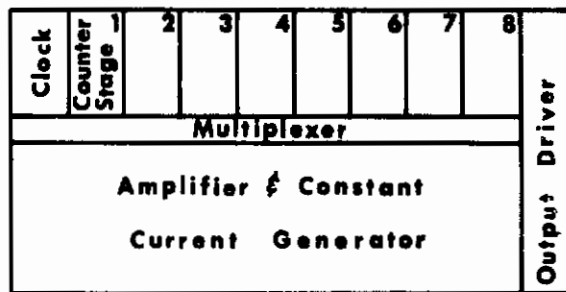
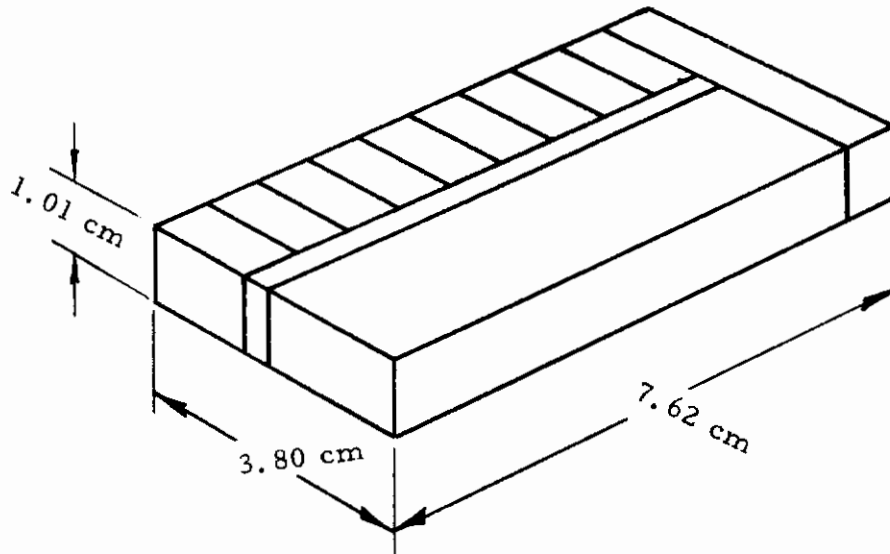
Another approach was pursued for the counter stage packaging. Quotes were obtained for the microminiature hybrid circuit in "chip form" in a 1/4 x 3/8 inch flat pack. The cost of this approach is considered prohibitive especially in small quantities; i. e., one to one hundred quantity price is \$64.

The sample module presented is built from the layout of figure 9 (Conventional Discrete Components). The black area around the outside of the module film indicates the required potting thickness with the outside edge being the finished module size.

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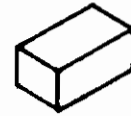
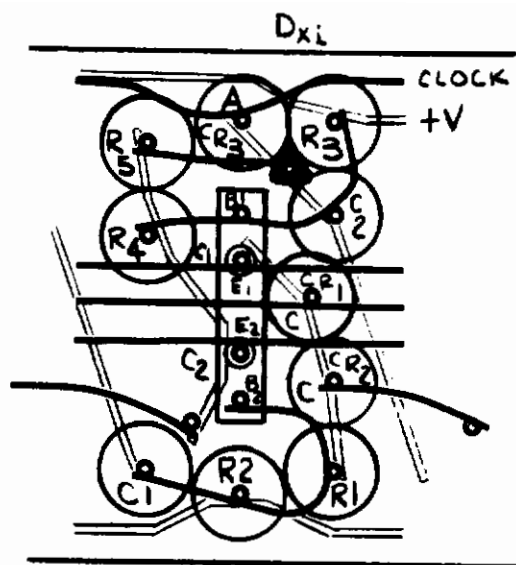
Since much of the system volume is required for the multiplexer counter stages an additional approach was investigated for counter mechanization. It is possible to implement the eight counter stages using a MOS logic array in one flat pack and the switches with multiple MOS switch elements in one flat pack. This technique would reduce the overall system size by at least 50% but would increase the system power by 100% and the overall price by at least 50%.

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29.5 cu. cm.

FIGURE 8
SYSTEM PACKAGE DESIGN

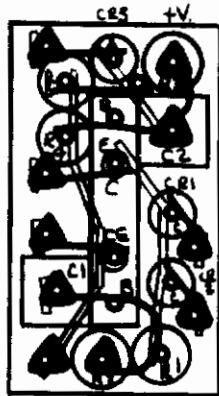


ACTUAL SIZE

1.39 cm. x .762 cm. x .762 cm. High

SCALE 5/1

FIGURE 9
MODULE LAYOUT WITH CONVENTIONAL DISCRETE COMPONENTS



1.02 cm. x .572 cm. x .508 cm. High

SCALE 5/1

FIGURE 10
MODULE LAYOUT WITH MICROMINIATURE DISCRETE COMPONENTS

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INPUT VOLTAGE	OUTPUT IN MICROSECONDS							CALCU- LATED
	CH1	CH2	CH3	CH4	CH5	CH6	CH7	
100 MV	535.8	535.5	535.5	535.6	535.2	535.7	535.8	
0	124.6	124.7	125.0	124.8	124.7	124.9	124.7	125.0
2	163.6	163.5	163.7	163.7	163.7	163.8	163.4	162.5
4	201.0	201.9	202.1	202.2	201.8	201.9	201.8	200.0
6	238.9	239.2	238.9	239.2	239.1	238.9	239.1	237.5
8	276.5	276.7	276.5	276.8	276.9	276.6	276.5	275.0
10	313.6	313.5	313.5	313.7	313.7	313.6	313.7	312.5
12	350.9	351.0	350.9	351.0	350.8	350.9	351.0	350.0
14	388.0	387.9	387.9	388.0	388.1	388.0	388.1	387.5
16	425.5	425.7	425.5	425.0	425.5	425.6	425.6	425.0
18	462.7	462.9	462.8	463.0	463.1	462.8	463.1	462.5
20	499.5	499.4	499.5	499.5	499.6	499.5	499.3	500.0

TABLE I
AMBIENT TEMPERATURE SYSTEM PERFORMANCE

INPUT VOLTAGE	OUTPUT IN MICROSECONDS							CALCU- LATED
	CH1	CH2	CH3	CH4	CH5	CH6	CH7	
100 MV	535.5	536.4	537.6	537.7	537.6	537.4	537.0	
0	125.3	125.1	125.4	125.7	125.5	125.4	125.5	125.0
2	164.1	164.5	164.5	164.5	164.4	164.6	164.7	162.5
4	202.3	202.4	202.3	202.7	202.6	202.4	202.5	200.0
6	239.6	239.7	239.6	239.4	239.2	240.0	239.5	237.5
8	276.8	277.1	277.1	276.2	277.4	277.5	277.2	275.0
10	314.5	314.6	314.7	314.9	315.0	314.8	314.7	312.5
12	351.6	351.7	351.6	351.8	351.8	351.8	351.5	350.0
14	388.7	388.7	388.5	388.9	388.8	389.1	388.9	387.5
16	425.8	425.7	425.6	425.8	425.7	426.2	425.8	425.0
18	463.2	463.2	463.3	464.4	463.8	463.5	463.4	462.5
20	500.1	499.8	499.9	500.0	499.9	500.0	500.3	500.0

TABLE 2
SYSTEM PERFORMANCE AT 0 CENTIGRADE

INPUT VOLTAGE	OUTPUT IN MICROSECONDS							CALCU- LATED
	CH1	CH2	CH3	CH4	CH5	CH6	CH7	
100 MV	536.8	586.4	536.8	536.7	536.5	536.7	536.6	
0	124.8	124.7	124.7	124.8	124.9	124.4	124.6	125.0
2	164.4	164.3	164.3	164.4	164.3	164.4	164.2	162.5
4	201.5	202.7	201.8	202.9	201.8	201.8	201.6	200.0
6	239.2	239.3	239.3	239.4	239.1	239.2	238.8	237.5
8	278.2	278.4	278.3	278.4	278.4	277.5	277.8	275.0
10	313.9	314.2	314.1	314.2	314.1	314.2	314.6	312.5
12	351.3	351.2	351.3	351.2	351.4	351.3	351.2	350.0
14	388.2	388.2	388.3	388.4	388.4	388.3	388.2	387.5
16	425.4	425.4	425.3	425.5	425.5	425.8	425.3	425.0
18	462.3	462.4	462.3	462.3	462.4	462.3	462.5	462.5
20	499.1	499.3	499.0	499.3	499.5	499.2	499.3	500.0

TABLE 3
SYSTEM PERFORMANCE AT 38 CENTIGRADE

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(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

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11. SUPPLEMENTARY NOTES		12. SPONSORING MILITARY ACTIVITY Aerospace Medical Research Laboratories Aerospace Medical Div., Air Force Systems Command, Wright-Patterson AFB, O. 45433	
13. ABSTRACT This report describes the research and development study of a pulse duration modulation multiplexer for use in personal telemetry systems. The objective of the program was to develop a low power, accurate pulse duration modulation multiplexer which has the potential of small physical size and low weight. The technical approach includes the design of low power logic, the use of the most advanced multiplexer switch, and the development of a unique amplification and comparison technique. All the system general requirements and specific requirements are satisfied by the design. The system performance is demonstrated by a laboratory breadboard model. Results of the tests performed on the model verify the feasibility of the engineering design.			

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Security Classification

Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Multiplexer Pulse duration modulation Mimiature telemetry systems Low level multiplexing Advanced personal telemetry systems Medical electronics						

Security Classification