FOREWORD

This is the final report for the Solid State Matrix Program, which was conducted from 1 April 1962 to 12 July 1963 under Contract Nr. AF33(657) - 8688 , Project Nr. 8128, and Task Nr. 812806 for the Aeronautical Systems Division, Air Force Systems Command, United States Air Force. It was under the direction of the AF Aero-Propulsion Laboratory with Mr. Lester E. Schott as RTD project engineer.

The program was conducted at the Alexandria Laboratories of the Research and Development Division of AMF. It was assigned to the Systems Engineering Department under Mr. Saul H. Silver. It was directed by Mr. R. N. Stock as AMF project engineer and was performed by Mr. R. N. Stock and Mr. R. W. Powell. Mr. S. Rubin of the Alexandria Laboratories and Mr. R. W. Townsend of the Springdale Laboratories acted as technical consultants in establishing the logic design. Mr. L. Mittelman, senior electronic engineer, Alexandria Laboratories, contributed many helpful suggestions to the circuit design effort. This report has been written by Mr. R. N. Stock and Mr. R. W. Powell.

In the event of a conflict between data presented in this report and data presented in any earlier report issued under this program, the data of this report shall prevail.

ABSTRACT

This report describes an engineering study and development effort to produce efficient and practical solid state transmission links (i.e., electrical power control and distribution systems). They were to be suitable for advanced aerospace vechicles and to have higher reliability than the conventional electromechanical transmission links used in present-day aircraft.

Two transmission links of the F-106B were re-designed as solid state systems to demonstrate the feasibility of solid state transmission links. Components were not replaced on a one-for-one basis. Instead, an overall functional analysis was made and then the logic system was designed so that solid state devices would be employed most efficiently. In particular, control and protection functions were performed by a single power switch. Also, all logic was performed at a low level. However, the operational functions of the original systems were retained.

The solid state systems used controlled rectifiers and power transistors as power handling devices. Control circuits were implemented with T.I. Solid Circuits, the G.E. silicon controlled switch (3N60), the unijunction transistor (2N491B), a compound transistor (2N2223), and a complementary pair of transistors (2N718/2N722). An interesting aspect of the systems was that relatively few types of devices were needed to implement a variety of functions. These functions included 4 areas: (1) power switches; (2) control circuits; (3) power supplies; and (4) circuit breakers.

The solid state systems were tested over the temperature range of -55°C to +80°C. Results were good; however, some alternate circuits were designed after the satisfactory completion of system tests. This was done because it became apparent that significant improvements could be made with relatively little effort. For example, the original dc overload circuit contained 42 parts and exhibited a trip current variation of 20% over the temperature range of -55°C to +80°C; the alternate dc overload circuit contained 23 parts and exhibited a trip current variation of only 1% over the same temperature range.

It was concluded that definite advantages can be provided by the application of solid state techniques to transmission links for advanced aerospace vehicles. However, 2 key problems are voltage transients and power switch cooling. By virtue of the techniques developed, applied, and then clearly presented in the design manual, this program furnished a sound

basis for the future development of operational solid state transmission links for advanced aerospace vehicles.

This technical documentary report has been reviewed and is approved:

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

INTRODUCTION

An electrical power system can be regarded as consisting of an energy source, utilization devices, and the transmission link that connects them. Components in the transmission link must often serve a dual purpose in that they not only control electrical energy flow but also provide protection against overloads. Present-day transmission links in aircraft consist of switches, contractors, relays, and circuit breakers, all of which utilize mechanical motion. Thus, they exhibit failures due to pitting, misaligned contacts, and other causes common to electromechanical devices.

The advent of space vehicles has placed increased emphasis on reliability and long life, and therefore, transmission links of increased reliability and longer life are required. Thus, the goal of this program was to develop a highly reliable, efficient, and practical solid state transmission link having positive advantages over conventional electromechanical transmission links. Primary emphasis was on higher reliability and longer life, but improved performance and reduced size and weight were considered highly desirable.

The basic approach for achieving the optimum solid state system was to subject the entire transmission link to an overall functional analysis, and then redesign the logic system to make the most efficient use of solid state devices. Also, dual functions such as control and protection were combined into a single power handling device wherever possible. The equivalent solid state circuit contained all the original circuit operational functions plus the improved functions or characteristics made possible by solid state technology.

This program was divided into 2 phases. During the first phase, which was completed in October, 1962, 2 transmission links of the F-106B were redesigned as solid state systems. They had been selected only as representative examples of the functions and loads that transmission links must support in an advanced aerospace vehicle.

During the second phase, which was completed in July, 1963, the designed systems were tested and a design manual was prepared. The following paragraphs discuss the 8 separate tasks that were performed during the program. The first 5 comprised the first phase and the last 3 comprised the second phase.

The first task was to analyze the operating sequence and functions of the 2 transmission links of the F-106B that were under consideration. These were the following:

Manuscript released by the authors 30 July 1963 for publication as an ASD Technical Documentary Report.

(1) Schematic Diagram - Master Electrical, Surface & Engine Anti-Ice, nr. 8-69741, Rev. G, sheet 3 (presented in T. O. 1F-106A-2-10 as Figure 12-51, Surface and Engine Air Anti-Ice Schematic);

(2) Schematic Diagram - Master Electrical, DC Power, nr. 8-69770, Rev. B, sheet 5 (presented in T. O. 1F-106A-2-10 as Figure 12-90, DC Power Schematic, sheet 2 of 3).

The analysis had to provide sufficient data to make possible the logic and circuit design of solid state systems that would provide all the functions provided by the original electromechanical systems. The analysis of the schematics was divided into 3 parts: (1) description of operation; (2) definition of system bounds; and (3) system loads.

The second task was to evaluate the suitability of semiconductor devices for the anticipated logic and circuit requirements of the systems. The devices needed were divided into power switching devices and control circuit devices. Controlled rectifiers, power transistors, and conventional rectifiers were evaluated as power switching devices. Discrete devices and functional devices were evaluated as control circuit devices.

The third task was to determine the most reasonable temperature range for which to design the circuitry. The anticipated thermal environment was reviewed and the temperature ranges of present devices and circuitry was considered. It was decided to design for an operating temperature range of -55° C to +80° C and for a storage temperature range of -55° C to +125°C.

The fourth task was to provide the logic design and circuit design. It was based on the overall functional analysis made initially and was devised to make the most efficient use of solid state devices. For example, the dual functions of control and protection were combined into a single power switching device. The solid state systems provided all the functions of the original electromechanical systems plus the improved characteristics made possible by solid state techniques.

The fifth task was to prepare a general specification for the solid state system that had been designed. This consisted basically of 2 sections; (1) the requirements; and (2) the experimental evaluation procedure. Also a preliminary evaluation was made of the extent of advantage of the solid state systems over conventional electromechanical systems.

The sixth task was to test the solid state systems. The systems were divided into 3 sections and the tests were conducted separately for each section. The results of these tests were good. All circuitry operated properly under the specified conditions.

The seventh task was to design and test alternate circuits. The evaluation of the designed systems revealed that certain simple design modifications could be effected that would considerably improve the solid state systems. Therefore, alternate circuits were designed to achieve these improvements.

The eighth task was to prepare a design manual that set forth the design criteria, problem areas, and installation considerations necessary to apply solid state transmission links in aerospace vehicles. This design manual is presented in Appendix I.

1. ANALYSIS OF SCHEMATICS

The first task was to analyze the operating sequence and functions of the two electrical schematics referenced by the contract. The analysis had to provide sufficient data to make possible the logic and circuit design of a solid state system that would provide all the functions provided by the present electromechanical systems. The analysis of the schematics was divided into three parts: (1) description of operation; (2) definition of system bounds; and (3) system loads. The description of operation was prepared from data provided in the applicable technical manuals as well as by study of the schematics themselves. It was necessary to prepare this so as to insure that the solid state systems would provide all functions provided by the electromechanical systems.

The definition of system bounds was necessary to precisely define the boundaries of the systems to be made solid state and to enumerate the inputs and outputs. For example, a switch operated by the pilot and shown on the schematic was defined as an input to the system. Also, a heating element shown on the schematic was defined to be a load on the system and the current to it an output of the system.

System loads had to be established so as to provide power handling devices of appropriate ratings, and also for proper solid state fusing. Thereby, a direct comparison between the size and weight of the new solid state system and that of the electromechanical system is possible.

1.1 DC Power System

As a first step, it seemed desirable to modify the original schematic for better format. Thus, the original dc power schematic presented in Figure 1 contains the following minor changes:

(1) a few bits of data which were added to the schematic when it was inserted into the T. O. (e. g., T. O. page nr.) have been deleted;

(2) the manufacturer's title block has been deleted;

(3) the circuit symbol for the dc external interlock relay has been changed from R12 to K12;

(4) the circuit symbol for the aft nonessential bus tie relay has been changed from K35 to K36;

(5) the circuit symbol for the LH fwd sub-console master electrical power switch has been changed from S46/S36 to S45/S35;

(6) the circuit symbols for the emergency dc power fuses have been changed from F15 (for all three) to F17, F18, and F19;

(7) the circuit symbols R1, CR1, CR2-CR7, S1, and S2 have been added;

(8) terminal symbols B1 and B2 have been added to K35 and K36;

(9) the section of the schematic shown in block diagram form and marked ⚠1 was added with note ⚠1 explaining it;

(10) notes have been added that apply to the schematic but which were orignially presented elsewhere.

1.1.1 Description of Operation

There are four sources of main dc power in the F-106B.

(1) The primary dc generator provides 100 amperes at 30 volts. This unit consists of a brushless ac generator with internal silicon rectifiers to provide a dc output; an internal permanent magnet generator provided field excitation current.

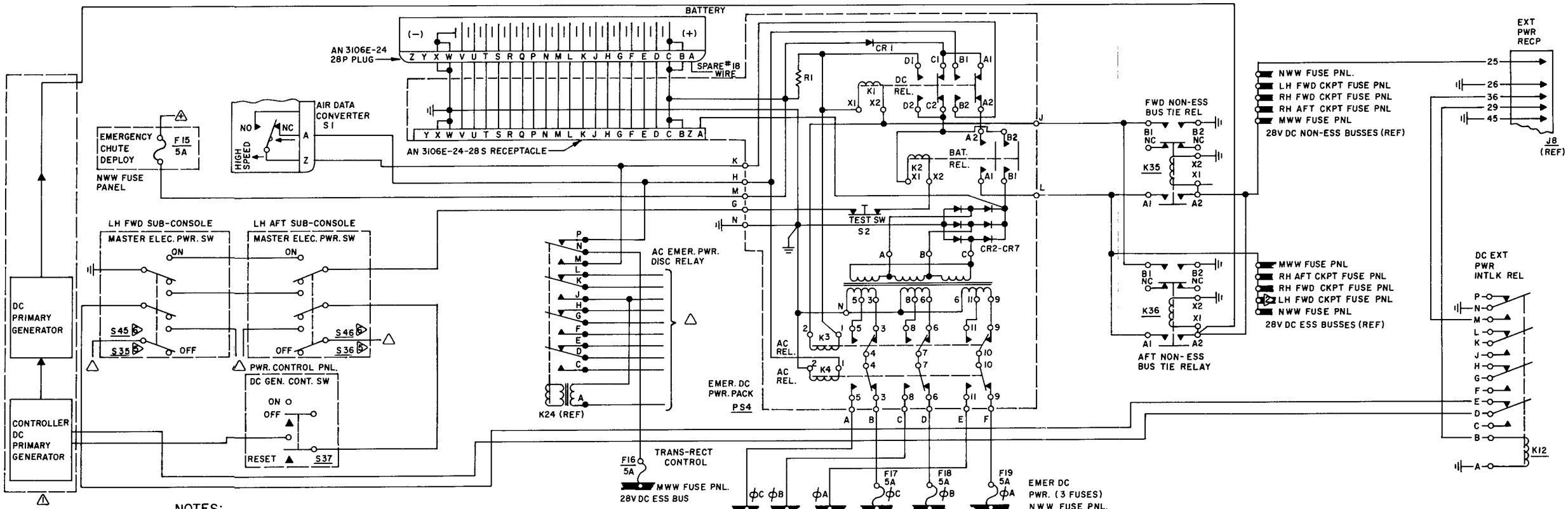
(2) The 18-cell emergency battery, which is part of the emergency dc power pack, provides 33.5 volts when fully charged and has a capacity of 15 ampere hours.

(3) The emergency power pack's transformer-rectifier converts three-phase ac into 36 vdc or 28 vdc, depending on whether in normal or emergency operation.

(4) DC power may be provided from an external source through the external power receptable.

Primary power is supplied to the F-106B on four sets of buses; ac essential, ac nonessential, dc essential, and dc nonessential. The dc power control system will keep the essential dc buses supplied with voltage under various failure conditions. The emergency dc power package supplies emergency power to dc essential buses if the primary dc generator fails. The power package contains a storage battery and transformer-rectifier. The transformer-rectifier draws power from three-phase ac buses to charge the battery or to assist the battery to power dc essential buses in emergencies.

A summary of operating conditions for the system is given in Table 1. A detailed description of operation is given in the following sections.



NOTES:

△ SEE AC POWER CIRCUIT

△ SEE SPEED BRAKE AND DRAG CHUTE CIRCUIT

△, △, △ VARIOUS AIRCRAFT APPLICABILITY NOTES

△ THIS SECTION FORMERLY INDICATED SO: FOR CONTINUATION SEE 8-69770, SHT 4,

Figure 1. Original DC Power Schematic

TABLE 1.

Summary of DC Power System

Condition		State Description
1. Normal	(1)	Primary dc power supply to dc essential and nonessential buses
	(2)	Emergency dc power pack to ac nonessential bus
	(3)	Three-phase rectifier to 36 vdc output
	(4)	Battery to three-phase rectifier through current-limiting resistor
	(5)	Emergency dc power pack off dc essential buses
2. Primary DC Supply Failure	(1)	DC nonessential buses inactive
	(2)	Emergency dc power pack to ac nonessential bus
	(3)	Power pack's transformer-rectifier to 28 vdc output
	(4)	Battery (through rectifier) in parallel with T-R feeds dc essential buses
3. Primary AC Supply Failure		AC nonessential bus inactive; battery charge cut off
4. Both DC and AC Primary Supplies Failed		
a. Airspeed above 280 knots	(1)	DC nonessential buses inactive
	(2)	Emergency dc power pack fed by ac essential bus
	(3)	Power pack's T-R has 28 vdc output
	(4)	Battery (through rectifier) in parallel with T-R feeds dc essential
b. Airspeed below 280 knots	(1)	DC nonessential buses inactive
	(2)	Power Pack connected to inactive ac nonessential bus so T-R has no output
	(3)	Battery alone feeds dc essential buses

Table 1. (Continued)

Condition	State Description
5. Engine Failed	
a. Windmilling above 280 knots	Same as 4a.
b. Windmilling below 280 knots	Same as 4b.
c. Stalled	Same as 4b. except no ac essential bus power in aircraft.
6. External Power	Primary dc generator cut off; external source supplies power as in 1

Throughout this description, reference is made to Figure 1, the original dc power schematic.

1.1.1.1 Normal Power-On Sequence

(1) Closing both master electrical power switches puts ground on terminal G of the emergency dc power pack. The battery relay (K2) is then actuated through terminals C2 and C1 of the dc relay (K1) and the diode tied to the positive terminal of the battery. Actuation of K2 applies battery voltage to the 28 vdc essential bus through terminal L of the emergency dc power pack.

(2) Turning on the dc generator control switch (S37) completes a circuit through terminals D and E of the dc external power interlock relay (K12) and the Master Electric Power Switches (S45 and S46) to energize the primary dc generator.

(3) The main dc power supply is connected directly to the 28 vdc nonessential buses and to terminals A2 and X1 of the nonessential bus tie relays (K35 and K36). When the main dc power supply comes up to the voltage, the 28 vdc nonessential buses are energized directly and the nonessential bus tie relays (K35 and K36) actuate connecting the main dc power supply to the 28 vdc essential bus. The closure of the nonessential bus tie relays also grounds terminal J of the emergency dc power pack.

(4) Ground on terminal J of the emergency dc power pack actuates the dc relay (K1) and the ac relay (K3). The dc relay (K1) removes the battery

from terminal L by breaking the circuit through relay terminals A1 and A2, and connects the battery through a resistor (R1) and relay terminals D1 and D2 to the output of the rectifier (CR2 - CR7). The ac relay (K3) connects the transformer primary taps to provide 36 vdc from the three-phase rectifier. Thus, the battery is charged from the ac nonessential bus through the transformer, rectifier, and current-limiting resistor (R1).

(5) The ac relay (K4) is actuated by the 28 vdc essential bus through terminals N and P of the ac emergency power disconnect relay (K24). The ac relay (K4) connects the transformer to the ac nonessential bus during normal operation.

1.1.1.2 Emergency Operation

There are four emergency conditions that must be provided for by the dc power system: (1) failure of the primary dc power supply; (2) failure of the primary ac generator; (3) failure of both the primary dc and primary ac generators; and (4) engine failure.

Primary DC Power Supply Failure

If the primary dc generator fails, voltage is removed from the 28 vdc nonessential buses and the nonessential bus tie relays (K35 and K36) open. Ground is removed from terminal J of the emergency dc power pack and relays K1 and K3 drop out. Dropping of K3 connects the transformer primary to give an output of about 28 vdc from the output of the three-phase rectifier. Dropping of K1 connects the battery to the 28 vdc essential buses through the rectifier (CR1) terminals A1 and A2 of K1, terminals A1 and A2 of K2, and terminal L of the emergency dc power pack. At the same time the output of the three-phase rectifier is connected in parallel with the output of the battery through terminals C1 and C2 of K1, and terminals B1 and B2 of K2.

Failure of the AC Generator

The ac emergency power disconnect relay (K24) is part of the ac power supply system. Terminals M, N, and P of the ac emergency power disconnect relay (K24) are used in the dc power supply system. The ac emergency power disconnect relay (K24) operates when the ac emergency generator operates and certain other conditions in the ac power supply system are fulfilled. The effect of the operation of this relay is to switch the voltage from the 28 vdc essential bus from terminal H to terminal K of the emergency dc power pack. If the primary dc generator is working and the dc relay (K1) is actuated, terminals H and K of the emergency dc power pack are connected through terminals B1 and B2 of the dc relay (K1). Thus, failure of the primary ac generator alone will not cause ac relay (K4) to drop out, and the emergency dc power pack will

continue to be connected to the ac nonessential bus. However, failure of the primary ac generator causes the ac nonessential bus to become inactive, and so failure will stop the battery from being charged by the transformer-rectifier.

Failure of Both Primary DC and AC Power Supplies

As described above, failure of the primary ac generator causes 28vdc power to be switched from terminal H to terminal K of the emergency dc power pack. Failure of the primary dc power supply, however, causes the dc relay (K1) to drop out and the battery and rectifier to be connected in parallel with the 28vdc essential buses. The dropping of the dc relay (K1) breaks the connection between terminals K and H of the emergency dc power pack and causes the ac relay (K4) to drop out. The dropping of the ac relay (K4) switches the primary of the emergency dc power pack's transformer from the ac nonessential bus to the ac essential bus. The ac essential bus is powered by the ac emergency generator during failure of the ac primary generator. Thus, when both dc and ac primary power supplies fail, the dc essential bus is supplied both by the battery and the emergency dc power pack's transformer-rectifier. However, if airspeed decreases below 280 knots, the contacts of the airspeed data converter close and re-energize K4 to reconnect the transformer-rectifier to the nonessential bus. Thus, that load is removed from the ac emergency generator.

Engine Failure

The hydraulic system which operates the generators obtains its pressure from an engine power take-off. If the engine fails in flight, but is free to windmill, sufficient hydraulic power will be developed to operate the ac emergency generator until the airspeed drops below 280 knots. Thus, under engine failure and windmilling conditions above 280 knots, emergency power on both the ac and dc systems can be supplied as described in the preceding paragraph. When airspeed drops below 280 knots, it is desirable to operate the dc essential buses from the battery alone without taxing the ac emergency generator. With both primary power systems failed, the air data converter operates below 280 knots to connect terminals K and H of the emergency dc power pack. This connection operates the ac relay (K4) from the 28 vdc essential bus through terminals M and N of the ac emergency power disconnect relay and terminals A and Z of the air data converter. Operation of the ac relay (K4) switches the input to the emergency dc power pack from the ac essential bus to the ac nonessential bus. However, the ac nonessential bus is inactive under these failure conditions, and the transformer-rectifier will no longer supply current to the dc essential buses. Thus, the full dc essential bus load is assumed by the battery. If the engine fails, but does not windmill, hydraulic power will be lost, and the only source of electric power available will be from the battery, which will supply the 28 vdc essential buses until it is discharged.

1.1.1.3 External Power

Both dc and ac power can be supplied from an external source through the external power receptacle (J8). Inserting an energized power plug in this receptacle will supply power to the 28 vdc buses in lieu of the primary dc generator. This is done in two steps. First, the dc external power interlock relay is energized. Operation of this relay opens the permanent magnet generator field control circuit through the master electrical power switches and the dc generator control switch so that when external power is supplied, the primary dc power supply is turned off. In addition, operation of this relay provides a ground for pin 36 of the external power receptacle. Thereupon, dc power is furnished from pin 25 of the external power receptacle to the dc buses precisely as it would be furnished by the primary dc generator.

1.1.2 Definition of System Bounds

It was necessary to define carefully that portion of the total F-106B electrical system which would be constructed out of solid state components during this program. In the subsystem already described, only certain portions can be considered as wholly part of the pertinent subsystem. The principles of inclusion and exclusion were laid down and then these principles were applied to a definition of the two subsystems under study.

1.1.2.1 Boundary Criteria

Because it is very convenient to do so, these criteria are written to include the anti-ice system. Rules for including or excluding an element in the subsystem are as follows:

(1) The element must appear in Figure 12-51 or Figure 12-90 of T. O. IF-106A-2-10. This rule defines the area of interest in accordance with the contract.

(2) Elements which operate mechanically or manually will be excluded from the subsystem proper although

(a) electrical connections to or from such elements will constitute outputs and inputs of the subsystem, and

(b) requirements of the subsystem may possibly dictate such modifications to these elements as a change in the number of required connections. This rule, in effect, recognizes that there can be no solid state substitute for the man who throws a switch nor is it a part of this program to find solid state transducers for such environmental conditions as airspeed, ice formation, or heat generation.

(3) Relays whose coils are controlled solely by aircraft sources external to the pertinent pages other than power buses will be considered part of

the environment, not the subsystem; however, contacts on these relays may be inputs to the subsystem. This rule provides that inputs to the subsystem will be generally in the form of dry contact closures rather than voltage levels except for power buses, and also isolates the subsystem from conditions established in other systems appearing on non-pertinent drawings. However, it does not exclude any relay whose coil is controlled by an external source. Thus, the dc external interlock relay is not excluded.

(4) Power buses will be considered as inputs or outputs of the subsystem but not as parts of the subsystem. These buses are shared by many systems, and this rule therefore, serves as a convenient way of isolating the pertinent subsystems from the others.

1.1.2.2 Solid State System Boundaries

Using the above defined criteria for system boundaries, the inputs and outputs of the solid state portion of the dc power system can be determined. The components that will be replaced by solid state devices are the following:

(1) K1, dc relay
(2) K2, battery relay
(3) K3, ac voltage relay
(4) K4, ac bus relay
(5) K12, dc external power interlock relay
(6) K35, forward nonessential bus tie relay
(7) K36, aft nonessential bus tie relay
(8) F15 and F16, T-R control and emergency chute fuses (28v, 5a)
(9) F17, F18, and F19, ac essential bus fuses (115v, 5a)

Inputs to the solid state portion of the system are as follows:

(1) S45 and S46, master electrical power switches
(2) S37, dc generator control switch
(3) Pins M, N, and P of K24, ac emergency power disconnect relay
(4) 100 a, 28 vdc main power supply
(5) External power source
(6) Battery output current
(7) Test switch, S2
(8) Air data converter switch, S1

Outputs from the solid state portion of the system are as follows:

(1) 28 vdc essential and nonessential buses
(2) Emergency chute deploy
(3) External Power interlock
(4) Battery charging current

After the definition of system bounds was completed, the original dc power schematic was simplified to make clearer the items of interest. The simplified dc power schematic is shown in Figure 2.

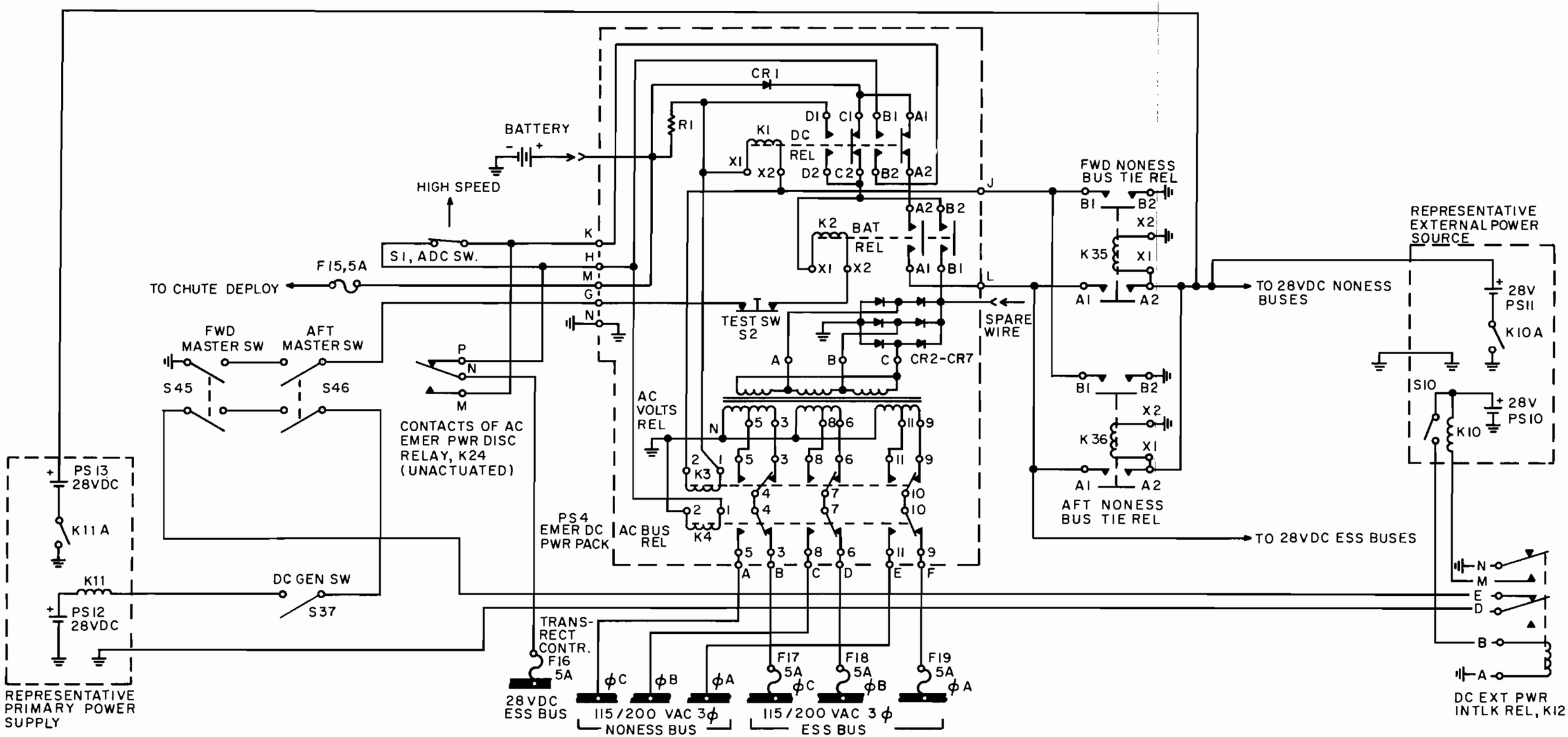


Figure 2. Simplified DC Power Schematic

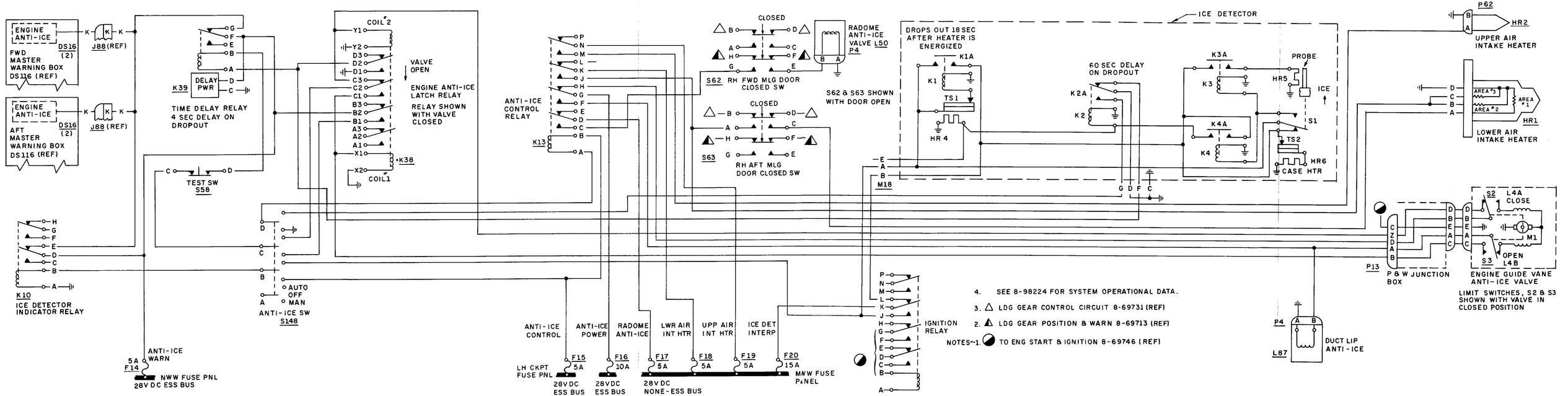


Figure 3. Original Anti-Ice Schematic

1.1.3 System Loads

The following data was provided by the San Antonio Air Material Area:

(1) The maximum current drawn by the dc essential bus is 42.9 amperes for 5 seconds average, 32.5 amperes for 1 minute average, and 27.9 amperes for 15 minutes average;

(2) the maximum rating of the transformer-rectifier is 0.82 KVA;

(3) the D-E contacts of the dc external power interlock relay carry 0.2 amperes and the M-N contacts carry 0.4 amperes.

(4) the maximum current per phase of the ac input to the transformer is 2.17 amperes.

Examination of this data revealed some interesting facts. First, the power switches between the battery and the essential bus should have a 43 ampere capability. Second, the transformer-rectifier rating was based on the 15 minute average load, but the output current capability based on the 5 second average load should be 43 amperes. Third, the ratings for the dc external power interlock relay were acceptable as presented. Fourth, the maximum current per phase of the ac input as given was based on the 15 minute average load; it was then calculated as 3.36 amperes rms per input line on the basis of a 43 ampere T-R output.

1.2 Anti-Ice System

The original anti-ice schematic is presented as Figure 3. For greater clarity, the following changes have been made:

(1) a few bits of data which were added to the schematic when it was inserted into the T.O. (e.g., T.O. page nr.) have been deleted;

(2) the manufacturer's title block has been deleted;

(3) the circuit symbol for the ignition relay has been deleted;

(4) the circuit symbol of RH aft MLG switch has been changed from S62 to S63;

(5) circuit symbols TS1, TS2, S1, HR4, HR5, HR6, K1, K1A, K2, K2A, K3, K3A, K4, K4A, S2, S3, and M1 have been added;

(6) circuit symbols for 5A fuses have been changed from F15 (for all) to F14, F15, F17, F18, and F19;

(7) circuit symbol for ice detector interpreter fuse has been changed from F17 to F20;

(8) circuit symbol L4 has been separated into L4A and L4B;

(9) pressure switch (S1) has been changed from ice position to no-ice position;

(10) note on engine valve position has been modified and relocated;

(11) probe identification has been added;
(12) the call-out "ice detector interpreter" has been changed to "ice detector" and relocated;
(13) K1 drop-out note's "14-19" has been changed to "18";
(14) K39 drop-out note has been changed from 3 sec. to 4 sec.;
(15) relay position note has been added for K38;
(16) pole identification symbols have been added for S148;
(17) a switch condition note has been added for S62 and S63.

With the above changes completed, it was possible to proceed to the description of operation.

1.2.1 Description of Operation

1.2.1.1 General Description

This anti-ice system is properly titled the surface and engine air anti-ice system. It is an automatic anti-ice detection and control system that can also be operated manually. Four individual anti-ice systems are involved: the engine anti-ice system; the engine inlet duct lip and anti-ice system; the radome anti-ice system; and the artificial feel air intake anti-ice system. Henceforth, these systems will be referred to with abbreviated names, and anti-ice generally will be abbreviated to a-i. The engine a-i system and the duct lip a-i system use hot engine bleed air. The radome a-i system uses stored a-i fluid, and the air intake a-i system uses electrical current. The s & e a-i system also consists (in addition to the 4 individual systems listed above) of an a-i switch, an a-i control relay, a latch relay, an ice detector, a warning system, and a test switch.

The a-i switch has 3 positions: off, manual, and automatic. When the a-i switch is in the off position, no anti-icing operation can occur, and the warning lights are illuminated. When the a-i switch is in the manual position, the a-i control relay is energized via the a-i switch directly. As a result, the 4 controlled a-i systems are energized continuously via the a-i control relay until the a-i switch is transferred to the off position. When the a-i switch is in the auto position, the a-i control relay is automatically energized via the ice detector when ice is detected and is de-energized by a timing mechanism 60 (±10) seconds after the detector probe has been de-iced.

K13, the a-i control relay provides power distribution when actuated as follows: (1) from fuse F17 via pole D to the radome a-i valve; (2) from fuse F16 via pole G to the open coil L4B of the engine a-i valve; (3) from fuse F18 via pole K to the lower air intake heater; (4) from fuse F19 via pole N to the upper air intake heater. K13 when unactuated provides power only from fuse F16 via pole G to the close coil L4A of the engine a-i valve. In certain cases, power is not applied directly from the relay to the load. These cases are now

listed. First, the radome a-i power must pass through S62. Second, the lower air intake heater area #1 power must pass through S63. Third, power to the open or close coils of the engine a-i valve must pass through their respective limit switches and therefore, this power is removed after the proper valve position is reached.

When the engine a-i valve opens, the power which opened it is switched by S3 to coil #1 of K38 and it latches K38 in the valve open position. Power is furnished from fuse F14 via K38/B2, S148, and S58 to K39 coil, pin B. Ground is furnished from K38/D2 and thus K39 actuates to remove power from K39/G. Since S148 in the manual position has already actuated K10, both possible sources of power to the warning lights have been disconnected.

The ice detector consists of a detector probe and an interpreter assembly. The interpreter assembly incorporates a timing mechanism that will de-energize the a-i control relay and shut off the 4 controlled systems 60 (± 10) seconds after the detector probe has been de-iced. However, the system will cycle on and off as long as icing conditions exist. The a-i warning light in the cockpit illuminates if the a-i switch is in the off position, or if the control system malfunctions.

During engine start, the probe heater and 3 of the 4 a-i systems are energized automatically to melt any accumulated ice if S148 is in the "auto" position. Depressing the ignition button energizes the ignition relay momentarily and initiates an automatic anti-icing period. This is necessary because the pressure switch will always be in the ice position prior to engine start. Thus, it would not be possible to initiate an automatic anti-icing cycle if this did not occur. Airflow through the engine, after engine start, will de-energize the system if the probe is clear of ice.

Power for the automatic control system is supplied from the 28vdc essential bus through the a-i control fuse F15 and from the 28vdc nonessential bus through the ice detector fuse F20. The engine a-i and duct lip a-i systems are connected to power through the a-i power fuse F16. The radome and air intake a-i systems receive power through 3 separate fuses, F17, F18, and F19. The warning system receives power from the 28vdc essential bus through fuse F14.

1.2.1.2 Anti-Ice Warning System

A warning light system affords the pilot visual indication of a malfunction in the s & e a-i system. On the ground or in the air, the warning light will illuminate if the airplane electrical system is energized and the a-i switch is in the off position. In flight, warning light illumination occurs if the a-i switch is in the auto position and the system is inoperative, or when the detector probe ices over and cannot be cleared by the probe heater within 18 (+2, -3) seconds. A malfunction of the detector that allows K1A to open while

S1 is in the ice position will de-energize K10 and complete the circuit to the warning light, thus illuminating it.

Relay K39 has a 4 (±1) second delay on dropout. Thus, it prevents warning light illumination while the engine a-i valve completes its cycle. During automatic operation, when the engine a-i valve is completely closed, coil nr. 2 (Y1 and Y2) of the K38 latch relay is energized. This closes contacts C3 and C2 and power is transmitted via C2 and S148/C to K39 coil. Ground for K39 coil is provided by K2A. When icing conditions exist, the engine a-i valve moves to the open position and completes a circuit to coil nr. 1 (X1 and X2) in the latch relay. This closes contacts C1 and C2 in the latch relay and energizes the K39 coil via C2 and S148/C. Ground for K39 coil is provided by K38/D2 via D1.

A press-to-test switch on the pilot's right-hand console is provided to check operation of the 4 second delay relay. Holding the test button down for more than 4 (±1) seconds will illuminate the warning light if the relay is operating properly. This test button is installed in the forward cockpit only.

1.2.1.2 Details of Warning System Operation

The following discussion applies when the a-i switch is in the auto position. The A-B coil of K39 is energized when the engine a-i valve is closed, K38 is in the proper position for valve closed, and K2 is not energized. The significance of K2 not being energized is that the automatic ice detector is not requesting an anti-icing cycle. Thus, it is appropriate that the engine a-i valve be closed, and of course, that K38 have the proper position for a-i valve closed. This first set of conditions represents a normal inactive period. Now, there is a second set of conditions for which the A-B coil is energized. This second set consists of a normal anti-icing period and consists of the engine valve open, K38 in the proper position for valve open, and K13 actuated. The fact that K13 is actuated indicates that K2 is energized, and thus, that the automatic ice detector is requesting an anti-icing period. With an anti-icing period being requested, it is appropriate that the engine valve be open and the K13 be actuated.

The purpose of energizing the K39 coil is to prevent the a-i warning lights from being illuminated. This purpose is achieved whenever a normal inactive period exists or whenever a normal anti-icing period exists. However, there is an interval when no malfunction exists when the lights would be briefly illuminated. This interval occurs when changing from the one set of conditions to the other. As a consequence, it is desirable that pole F of K39 not return to the unactuated position instantly upon loss of power to the A-B coil, but that a few seconds delay occur. This is the purpose of the delay power block beneath the A-B coil.

The delay power block contains a relay coil, 2 relay contacts, a resistor, and a capacitor. The relay coil, resistor, and capacitor are connected as a time delay relay on dropout. When coil A-B energizes, it actuates pole F and the 2 poles of the delay power block. These 2 poles are now closed and permit the delay coil to energize, and of course, the capacitor charges. When the A-B coil is de-energized, the 2 poles open. However, the delay coil stays energized and keeps pole F in the actuated position until the delay coil is no longer energized sufficiently by the discharging capacitor. The delay achieved in the return of pole F to the unactuated position is 4 (±1) seconds. This is longer than the time of transition between a normal inactive period and an anti-icing period. Thus, no false indication of malfunction is given during such a transition.

1.2.1.4 Engine A-I System

When the engine a-i valve is open, heated engine air flows into the inlet guide vane manifold and then into the engine. Heating is sufficient to prevent the formation of ice. The valve controls duct air flow and is actuated by a 28 vdc reversible electric motor. The motor is controlled by the s & e a-i system. It positions the valve to the full open position during an anti-icing period or the full closed position during an inactive period. Limit switches in the motor circuit prevent intermediate valve positions.

A failure warning system provides the pilot with an indication of a defective valve. The system can be checked by positioning the a-i switch to "manual". The a-i warning light should illuminate, valve actuation should be complete within 4 (±1) seconds, and the warning light should then extinguish. If the valve does not actuate, then the a-i warning light will remain illuminated, indicating valve failure. The engine a-i warning system is controlled by a latching relay and a 4 second delay relay. Both relays are energized through the valve limit switches.

1.2.1.5 Duct Lip A-I System

The duct lip a-i system is solenoid-controlled via the s & e a-i system. The duct lip a-i valve is a solenoid-controlled, pneumatically actuated valve. When its control solenoid is energized, the valve opens (if the engine is running to provide pressure). The solenoid is energized when K13 is actuated.

1.2.1.6 Radome A-I System

The operation of the radome a-i system is controlled by the s & e a-i system. The a-i fluid control valve is solenoid-actuated and it will be open when the solenoid is energized. Power is furnished when K13 is actuated. However, the system is always de-energized when the main landing gear doors are open because power is furnished via the forward main landing gear door-

closed switch.

1.2.1.7 Air Intake A-I System

The upper and lower air intakes are anti-iced by means of electrical heating elements controlled by the s & e a-i system. The lower intake heater has 3 elements and the upper intake heater has one element. The heater elements operate to anti-ice the intakes when K13 actuates to energize them. The area #1 element of the lower intake heater is de-energized while the airplane is on the ground by connection to the right main landing gear aft door-closed switch.

1.2.1.8 Ice Detector

The ice detector assembly is mounted on the right outboard surface of the engine inlet duct. It consists of a detector probe, an interpreter assembly and a case heater. The detector probe extends through a hole in the duct into the airstream inside the duct when it can detect ice formation. The interpreter is contained in the detector case and responds to indications from the probe. The probe and interpreter automatically control the s & e a-i system when the a-i switch is in the "auto" position. When the electrical system is energized, the case heater operates to prevent moisture accumulation within the case. A thermoswitch cycles the case heater to prevent overheating. The detector probe consists of a probe heater and a pressure switch. Under non-icing conditions with the engine running, the probe develops a differential air pressure that is applied to the pressure switch to cause its bellows to expand. However, if ice accumulates on the probe, then the pressure differential decreases and the bellows contracts to actuate the pressure switch.

The interpreter assembly consists of an 18 second timer and 3 relays. If the pressure switch is actuated by probe icing, then K2, K3, and K4 operate to actuate the probe heater, the a-i control relay, and the 18 second timer. The control relay supplies power to actuate the 4 anti-ice systems. If the probe is cleared of ice by the probe heater in less than 18 (+2, -3) seconds, then differential pressure is restored and the pressure switch de-energizes the probe heater. Power to the control relay continues for 60 (±10) seconds after differential pressure is restored because K2 has a 60(±10) second delay on dropout. This insures complete surface de-icing. Within 4 (±1) seconds after de-icing is completed, all relays and valves in the system will be re-cocked for another cycle.

Consider what happens if differential pressure is not restored within 18 (+2, -3) seconds. This effect could be produced by a clogging of the probe pressure ports by foreign matter, by abnormally heavy icing conditions, by an inoperative probe heater, and so forth. After HR4 has been energized for

18 (+2, -3) seconds, TS1 will open and de-energize K1. Thereby, S1 can no longer furnish power to K3, K4, or K2 and this actuates the warning system. Surface de-icing continues for the normal 60 (± 10) seconds, and then the entire system will cut off. With the probe still iced over, the automatic system cannot re-cycle, and manual control by the pilot is required. Illumination of the warning lights so informs the pilot.

1.2.1.9 Details of Interpreter Assembly Operation

Power normally enters the ice detector on pin B, and is transmitted via the pressure switch (no ice) to K1 coil via TS1, so that K1 contacts close to latch K1 via TS1. At this time, the K1 coil is energized via its own contacts and the pressure switch in parallel. When the probe ices, power is applied to K3 and K4 coils via the pressure switch and K1A so that K3A and K3B close. When K3A closes, power is applied to K2 coil and to HR4. K2A actuates and grounds the coil of K13, a-i control relay which actuates. When K3B closes, power is applied to the probe heater.

If the probe is not de-iced within 18 (+2, -3) seconds, then TS1 will open and de-actuate K1A. Thereupon, power is removed from K3 and K4 and cannot be reapplied. However, under normal conditions, the probe is de-iced within 18 (+2, -3) seconds so that S1 returns to the no-ice position and removes power from HR4 so that TS1 does not open. When the probe ices again, the cycle will repeat as before.

The method by which K2 achieves a 60 second delay on dropout is not shown but is accepted as a stated fact.

1.2.2 Definition of System Bounds

Using the previously defined criteria for system boundaries, the inputs and outputs of the solid-state portion of the anti-ice system can be determined. The components that will be replaced by solid-state devices are the following:

(1) K1, TS1, and HR4 (18 second delay system)
(2) K2, 60 second delay relay
(3) K3, probe heater relay
(4) K4, de-ice relay
(5) TS2, case heater thermoswitch
(6) K10, ice detector indicator relay
(7) K13, anti-ice control relay
(8) K38, engine anti-ice latch relay
(9) K39, 4 second delay relay
(10) F14 through F20, fuses (all 28v, 5a, except F16 - 28v, 10a and F20 - 28v, 15a)

Inputs to the solid-state portion of the anti-ice system are as follows:

(1) Pins J, K, and L of the ignition relay
(2) S1, ice detector pressure switch
(3) S3/C, valve open limit switch
(4) S2/D, valve close limit switch
(5) S148, anti-ice switch
(6) S58, test switch
(7) 28 vdc essential and non essential buses

Outputs from the solid-state portion of the anti-ice system are as follows:

(1) Power to engine anti-ice warning lights
(2) Power to S3/A, valve open limit switch
(3) Power to S2/B, valve close limit switch
(4) Power to radome anti-ice valve via fwd MLG switch
(5) Power to area 1 of HR1 via aft MLG switch and to areas 2 and 3 directly.
(6) Power to upper air intake heater (HR2)
(7) Power to duct lip anti-ice valve
(8) Power to HR5, probe heater
(9) Power to HR6, case heater

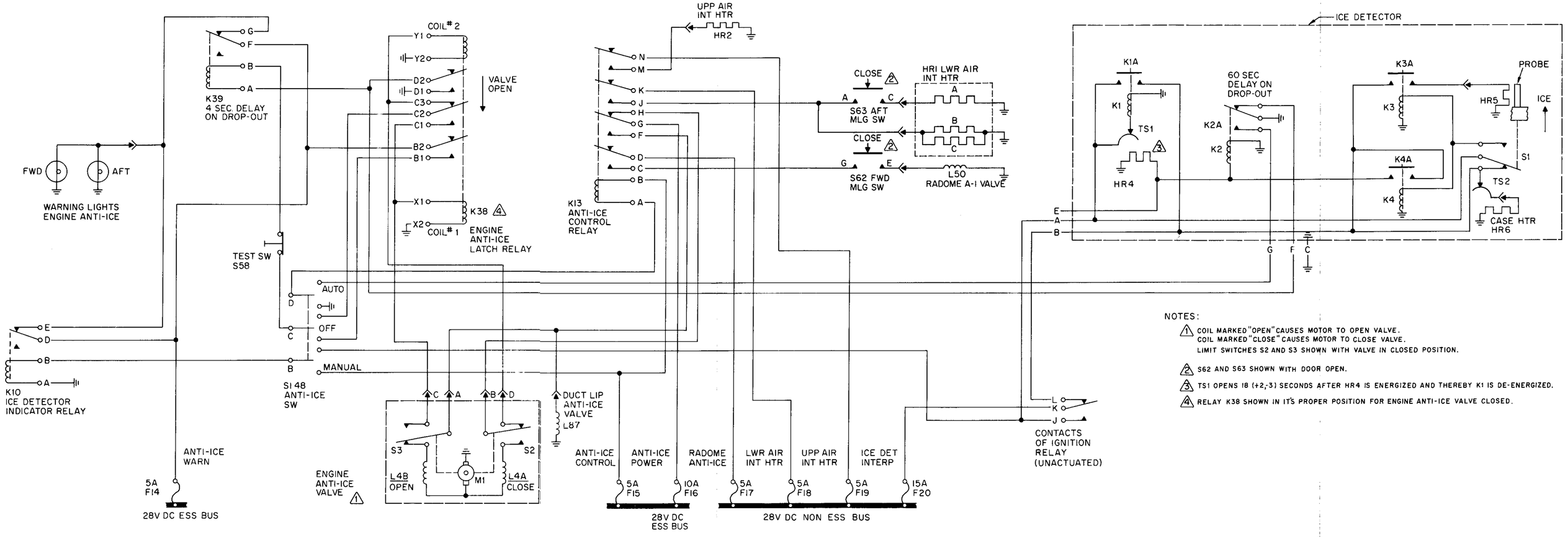
After the definition of system bounds was completed, the original anti-ice schematic was simplified to make clearer the items of interest. The simplified anti-ice schematic is shown in Figure 4.

1.2.3 System Loads

The following data was provided by the San Antonio Air Material Area:

(1) the resistance of the forward and aft engine anti-ice warning indicators consists of 2 each Mayda Nr. 327 lamps connected in parallel;
(2) the radome anti-ice valve has a solenoid resistance of 65 ± 5 ohms and an inductance of 85 millihenries;
(3) the case heater is 25 ohms;
(4) the probe heater is 6 ohms;
(5) the duct lip anti-ice valve has a solenoid resistance of 84 ohms and inductance of 69 millihenries;
(6) the "close" and"open" coils of the engine anti-ice valve each have a resistance of 7 ohms and an inductance of 11 millihenries.
(7) the case heater thermostat closes at 55 ±5° F and opens at 75° F maximum.

All resistances were given for +25° C. Examination of the above data and T.O. 15A12-2-3-3, Ice Detector Assembly, indicated a slight conflict. The T.O. presented the probe heater resistance as 4.1 ± 10% ohms at ± 25°C. Also, the T.O. presented the case heater thermostat as closing at +52 ±5°F. and opening at 67 ± 8°F. The values presented by the T.O. were accepted.



NOTES:

1. COIL MARKED "OPEN" CAUSES MOTOR TO OPEN VALVE.
   COIL MARKED "CLOSE" CAUSES MOTOR TO CLOSE VALVE.
   LIMIT SWITCHES S2 AND S3 SHOWN WITH VALVE IN CLOSED POSITION.
2. S62 AND S63 SHOWN WITH DOOR OPEN.
3. TS1 OPENS 18 (+2,-3) SECONDS AFTER HR4 IS ENERGIZED AND THEREBY K1 IS DE-ENERGIZED.
4. RELAY K38 SHOWN IN IT'S PROPER POSITION FOR ENGINE ANTI-ICE VALVE CLOSED.

Figure 4. Simplified Anti-Ice Schematic

2. EVALUATION OF SEMICONDUCTOR DEVICES

The goal of this program was to develop a highly reliable, efficient, and practical solid state transmission link. It was not intended to provide solid state equivalents for individual relays. Thus, a proper evaluation of semiconductor devices had to be in terms of suitability for implementing the overall solid state system.

Relays are available that range in size from the Branson type JR (that measures only 0.2 x 0.4 x 0.5 inches, weighs 5 grams, has an operating temperature range of -65° C to +125° C, and can handle 1 ampere at 28 vdc), to huge contactors that can interrupt thousands of amperes. The largest size applicable to the control circuitry under consideration was similar to the Potter & Brumfield MB contactor that can handle 60 amperes at 28 vdc. It is about 1-1/2 x 1-3/4 x 3/4 inches. Relays, generally speaking, are available for operation in the temperature range of -55° C to +85° C and -65° C to +125°C. On special order they are available for operating temperatures in excess of +200° C.

Data from field reports, laboratory evaluations, and engineering estimates have shown that 75% of relay failures can be attributed directly to contact failure. Contacts fail either when the closed resistance is too high or the open resistance is too low. Basic causes of unsatisfactory contact performance include contact contamination, constriction of the effective contact surface, melting, arcing, and mechanical wear. These difficulties can all be eliminated by replacement of mechanical switching devices with electronic switching devices.

Basically, solid state switching systems have the advantage of no mechanical motion with a resulting insensitivity to shock and vibration, and an absence of the failure modes common to electromechanical systems. However, they have the disadvantage of greater temperature sensitivity and overload damage susceptibility.

An evaluation of semiconductor devices suitable for application to the present program began with a consideration of the material that should be used. Among semiconductor materials the outstanding competitor of silicon and germanium is gallium arsenide, a III-V compound. Its maximum allowable temperature of +400° C makes it quite attractive. Unfortunately, very few semiconductor devices are available that use this material. Germanium devices have extensive availability but are restricted to a maximum allowable junction temperature of about +100° C. However, silicon devices can operate with junction temperatures as high as +200° C. Thus, it was decided to use silicon devices exclusively because germanium devices have a much lower maximum allowable junction temperature, and gallium arsenide devices have very limited

availability.

The devices that were needed for this program can be divided into 2 categories, power handling devices and control circuit devices. Each category will be discussed separately in the following sections.

2.1 Power Handling Devices

The active devices that are suitable as power handling devices are controlled rectifiers and power transistors. Also, ordinary rectifiers are applied as passive elements. These devices will be discussed in the following sections.

2.1.1 Controlled Rectifiers

The very high current and voltage ratings available in controlled rectifiers exceed any requirement of the systems under consideration. Several types which are representative of the current capacities available will be discussed in the following paragraphs.

The C5 series of controlled rectifiers have a maximum allowable average current of 1.6 adc and a peak one cycle surge current of 18 amperes. Units are available with PRV ratings from 25 volts to 400 volts. The forward voltage drop varies significantly with current but only slightly with temperature. This is true for all controlled rectifiers. At +25° C, it is 1.5 volts at 1 milliampere, 1.0 volt from 2 to 200 milliamperes, 1.3 volts at 1.6 amperes, and 2.5 volts at 6.4 amperes. Thus, the power dissipation at 1.6 adc is about 2 watts. The firing requirements for the gate never exceed 350 microamperes at 1.0 volt. The operating temperature range is -65° C to +125° C and the storage temperature range is -65° C to +150° C. The maximum allowable case temperature is given as +87° C at 1.6 adc. This indicates a thermal resistance of 20° C/W. The C5 series is in a TO-5 package.

The C10 series of controlled rectifiers have a maximum allowable average current of 7 adc and a peak one cycle surge current of 60 amperes. Units are available with PRV ratings from 25 to 400 volts. At +25° C, the forward voltage drop is 1.2 volts at 18 milliamperes, 1.1 volts from 30 to 400 milliamperes, 1.6 volts at 7 amperes, and 2.4 volts at 28 amperes. Thus, the power dissipation at 7 adc is about 11 watts. The firing requirements for the gate never exceed 30 milliamperes at 2.0 volts. The operating and storage temperature range is -65°C to +150° C. The maximum thermal resistance is given as 3.1° C/S. Thus, the maximum allowable case temperature is +115°C at 7 adc. The C10 series is in a stud-mounted package 1.2 inches long and 0.4 inches in diameter.

The C35 series of controlled rectifiers have a maximum allowable average current of 25 adc and a peak one cycle surge current of 150 amperes. Units are available with PRV ratings from 25 to 800 volts. At 25° C, the forward voltage drop is a maximum of 1.4 volts at 50 milliamperes, 1.2 volts from 90 to 900 milliamperes, 1.7 volts at 25 amperes, and 2.4 volts at 100 amperes. Thus, the power dissipation at 25 adc will not exceed 42 watts. The firing requirement for the gate never exceeds 80 milliamperes at 3.0 volts. The operating temperature is -65° C to +125° C and the storage temperature range is -65° C to +150° C. The maximum thermal resistance is 2° C/W. Thus, the maximum allowable case temperature is +41° C at 25 adc. (The manufacturer gives a higher allowable case temperature of +58° C for this current but that calculation is based on typical rather than maximum characteristics.) The C35 series is in a stud-mounted package 1.6 inches long and 0.6 inches in diameter.

The C60 (2N2023-29) series of controlled rectifiers have a maximum allowable average current of 110 adc, and a peak one cycle surge current of 1000 amperes. Units are available with PRV ratings from 25 to 400 volts. At +25° C, the maximum forward voltage drop is 1.1 volts at 30 milliamperes, 1.0 volts at 0.1 to 10 amperes, 1.7 volts at 110 amperes, and 2.5 volts at 440 amperes. Thus, the power dissipation at 110 adc will not exceed 187 watts. The firing requirement for the gate never exceeds 130 milliamperes at 3.0 volts. The operating and storage temperature range is -65° C to +150° C. The maximum thermal resistance is 0.4° C/W. Thus, the maximum allowable case temperature is +75° C at 110 adc. This series is in a stud-mounted package 2.6 inches long and 1.1 inches in diameter.

The largest capacity series known is the C80 series with 235 adc maximum allowable average forward current and 100 to 800 volt ratings. It has a thermal resistance of 0.17° C/W maximum but an operating temperature range of only -40° C to +125°C, and a storage temperature range of only -40°C to +150° C.

An interesting new development is the TI-X120AO series PNPN gate controlled switch offered by T.I. that can be both turned on and turned off by the gate. Turn-off gate control was restricted previously to devices having a maximum anode current of 200 milliamperes or less. This device has a maximum average dc forward of 5 amperes and an operating temperature range of -55° C to +125° C. Storage temperature range is not specified. Turn-on current gain is about 100 but turn-off current gain is about 14 at 5 amperes anode current. It has voltage ratings of 50, 100, and 200 volts.

2.1.2 Power Transistors

An attempt to use triode transistors as power handling elements requires

circuitry to maintain them in either saturation or cutoff. By this means it is possible to minimize the power which the transistor must dissipate, and thereby alleviate the cooling problem.

The 2N2016 is an NPN silicon power transistor with a rated dissipation of 150 watts at +25° C case temperature. The maximum collector current is 10 amperes, the maximum collector-to-emitter voltage is 130 volts, and the maximum saturation resistance at 5 amperes collector current is 0.25 ohms. DC beta is 15 to 50 at 5 amperes collector current. It has an operating temperature range of -65° C to +200° C and a maximum thermal resistance of 1.17° C/W. It is in a JEDEC TO-36 package.

The 2N2226 is a NPN silicon power transistor with a rated dissipation of 150 watts at +75° C case temperature. The maximum collector current is 10 amperes, the maximum collector-to-emitter voltage is 50 volts, and the maximum saturation resistance at 10 amperes collector current is 0.35 ohms. DC beta is 100 minimum at 10 amperes collector current. It has an operating and storage temperature range of -65° C to +150° C and a maximum thermal resistance of 0.5° C/W. Its case is 1.3 inches in diameter and 1.1 inches in height overall. This transistor is one of a series of high gain units offered by Westinghouse that exhibit gains as high as 400 at 10 amperes and voltage ratings as high as 200 volts.

The 2N1823 is one of a family of Westinghouse NPN silicon power transistors with 30 ampere and 50 volt to 300 volt ratings. The rated dissipation is 250 watts and the maximum saturation resistance is 0.075 ohms at 20 amperes. DC beta is 10 minimum at 20 amperes collector current. It has an operating and storage temperature range of -65° C to +175° C, and a maximum thermal resistance of 0.45° C/W. Its case is 2.5 inches long and 1.1 inches in diameter overall.

The highest current rating known is given by a power transistor recently introduced by Silicon Transistor Corporation. It is rated at 50 amperes, 150 volts, and 300 watts. The forward current gain is 10 minimum at 50 amperes. The saturation resistance is 0.04 ohms maximum at 50 amperes. It is housed in a 1.1 inch diameter, double-ended, stud-mounted package with flag-type collector terminals.

The highest voltage rating known is given by the Delco 2N2583. It is an NPN silicon power transistor with a voltage rating of 500 volts, a maximum collector current of 10 amperes, and a maximum saturation resistance of 0.10 ohms at 10 amperes collector current. DC beta is 10 minimum at 10 amperes collector current. It has an operating temperature range of -65° C to +150° C, a storage temperature range of -65° C to +200° C, and a maximum thermal resistance of 0.7° C/W. It is in a JEDEC TO-36 package.

A recent development is the high power PNP silicon transistor. The STC5555 is one of a family of PNP silicon power transistors that are offered by the Silicon Transistor Corporation. It has a rated dissipation of 85 watts. The maximum collector current is 5 amperes, the maximum collector-to-emitter voltage is 80 volts, and the maximum saturation resistance is 0.5 ohms at 2 amperes collector current. DC beta is 10 to 30 at 2 amperes collector current. It has an operating and storage temperature range of -65° C to +200° C, and a maximum thermal resistance of 2.3° C/W. Its case is 0.69 inches in diameter and 1.3 inches in length overall.

2.1.3 Rectifiers

Silicon rectifiers are available that range from 75 milliamperes and 50 volts (Transitron TMD41) to 250 amperes and 1000 volts (G.E. type 1N3742). A new development in power rectifiers is the G.E. controlled avalanche rectifier. This rectifier exhibits extremely high surface dielectric stability and a non-destructive internal avalanche breakdown which is designed to occur below the maximum voltage of surface dielectric stability. In effect, this rectifier has its own built-in zener diode type protection against transients. This rectifier is available in a 500 milliampere series (A7) and a 12 ampere series (A27). The 12 ampere series is available in 6 ratings of working PRV from 200 to 1200 volts. It has a peak 1 cycle surge current rating of 200 amperes. The operating and storage temperature range for this device is -65° C to +175° C, and the maximum thermal resistance is 2.0° C/W.

2.2 Control Circuit Devices

Today's literature generally classifies the 3 practical techniques of microelectronics as microcomponents, thin film circuits, and molecular electronics, However, the circuit designer views electronic devices in terms of their circuit capability rather than the technique or process by which they are manufactured. Thus, all commercially available devices can be classified in 2 broad groups. The first group consists of devices which are discrete passive and active elements. These, when properly interconnected, will perform a circuit function such as gating, pulse generation, and so forth. The second group consists of devices or packaged units which in themselves are capable of performing a circuit function. The first group will be referred to as discrete elements and the second group will be referred to as functional devices. Thus, not only devices classified under microelectronics but all other circuit devices as well will be discussed as either discrete elements or functional devices.

2.2.1 Discrete Devices

Discrete devices will be divided into conventional, special, and micro-

components. Conventional devices refer to triode transistors and various diode types that are available in common case sizes. Special devices refer to such devices as the binistor and silicon controlled switch that are suited to switching applications. Microcomponents refer to transistors and diodes available in ultra-small cases.

2.2.1.1 Conventional Devices

Transitron offers a line of military type silicon diodes which are designed to deliver the maximum in quality assurance under severe electrical, mechanical, and environmental operating conditions as specified in MIL-S-19500B and MIL-E-1. These diodes perform reliably at up to +200° C with almost negligible leakage currents. The general purpose alloy type offers an optimum balance of speed, voltage, and conductance for computer or low level rectification applications. An example of this type is the JAN 1N457. It has maximum ratings of 75 milliamperes average forward current, one ampere maximum pulse current, and a PIV rating of 60 volts. The maximum allowable average power dissipation is 250 milliwatts at 25° C. The operating and storage temperature range is -65° C to +200° C. It is in a case 0.14 inches in diameter and 0.3 inches long.

Transitron's subminiature glass diffused silicon regulators are constant voltage elements for control and similar circuitry. They are available in 14 voltage ranges between 3.3 and 12.0 volts and have a maximum power dissipation of 400 milliwatts at 25° C. The operating and storage temperature range is -65° C to +175° C. The case is 0.125 inches in diameter and 0.3 inches long. It is an all glass hermetically sealed case to insure complete environmental protection. Similar regulators are available in power ratings up to 10 watts.

2.2.1.2 Special Devices

The binistor is a 4-layer, 4-terminal NPN silicon device with a negative resistance characteristic. This characteristic is determined for the binistor by the external circuitry instead of by internal parameters as is the case for conventional 4-layer devices. This results in a significant reduction in peripheral circuitry and stable operation over a wide temperature range.

The higher temperature type of binistor has an operating and storage temperature range of -65° C to +150° C. It is in a JEDEC TO-33 case (0.33 inches in diameter and 0.26 inches long). It has a typical turn-off current gain of 20 at 15 milliamperes collector current. The operating collector current range is 0.5 to 30 milliamperes.

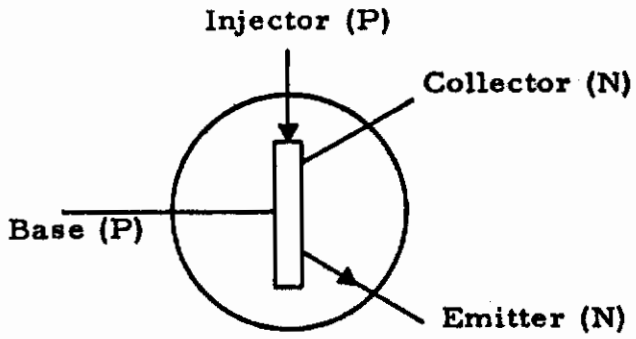
Binistor action can best be understood by referring to the 2-transistor equivalent circuit which is shown connected in a typical bistable configuration in Figure 5. The insertion of base current causes a regenerative action as soon as the collector voltage falls below the injector clamp voltage. The binistor then turns on and no further base current is required to maintain the on state. A typical collector current in the on state would be 10 milliamperes and a typical injector current would be one milliampere. By diverting the injector current, the binistor can be switched off. Typical applications include ring counters, binary counters, shift register, and general purpose switching circuits.

A general comparison of the binistor flip-flop with a triode transistor flip-flop may be instructive. A medium speed, wide temperature range triode transistor flip-flop requires at least 2 transistors, 7 resistors, 2 capacitors, and 2 diodes. This would require a total of 28 solder connections. Also, well designed high-speed flip-flops usually require far more components. In contrast, a binistor flip-flop of comparable performance requires only one binistor and 3 resistors (this assumes a common clamping diode for several flip-flop stages). This would require a total of 10 solder connections. This simplicity reduces size and weight while enhancing reliability.

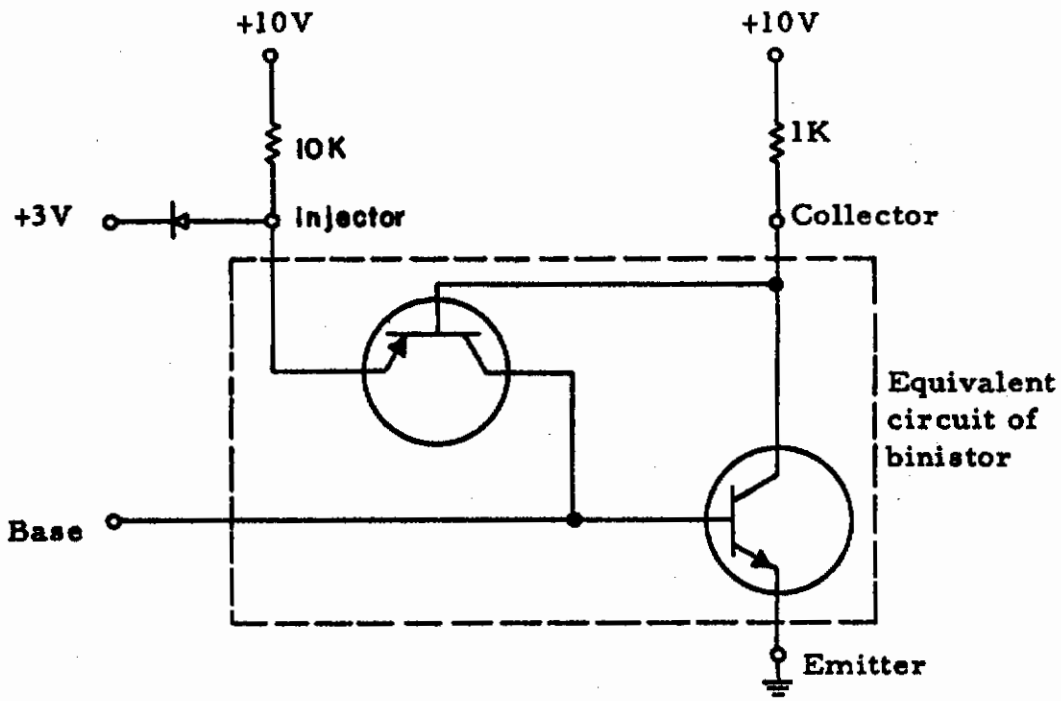
The transwitch is a 4-layer, 3-terminal PNPN bistable silicon device that can be switched both on and off by a gate signal. It is available in 4 voltage ratings from 30 to 200 volts and with either a 50 or 100 milliampere current range. The saturation voltage is 2 volts maximum at full rated current. The turn-on current gain is greater than 100 but the turn-off current gain can be as low as 5. The operating temperature range is -55° C to +125° C and the storage temperature range is -65° C to +150° C. It is available in a TO-18 case (0.18 inches in diameter and 0.20 inches high).

Solid State Products, Inc. produces a variety of small silicon controlled rectifiers, silicon controlled switches and silicon trigistors. The controlled rectifiers are available in one ampere and 200 milliampere types, with voltage ratings from 30 to 200 volts. The maximum gate current needed to fire most types is 2 milliamperes. The one ampere unit is in a TO-9 case and the 200 milliampere unit is in a TO-18 case. The operating and storage temperature range for both types is -65° C to +150° C.

The controlled switches are available in one ampere, 200 milliamperes, fast recovery, and military types. The maximum gate current needed to fire is as low as 20 microamperes for anode currents as high as one ampere. The operating and storage temperature range for all types is -65° C to +150° C. The units are packaged in TO-9 cases except for the 200 milliampere type which is in a TO-18 case.



(a) Circuit symbol with terminals and material indicated.



(b) Binistor Bisable Multivibrator Circuit.

Figure 5. The Binistor

The trigistor is available in 8 milliampere and 200 milliampere types, and has voltage ratings up to 200 volts. It needs a maximum gate current to fire of 50 microamperes for the low current units and 10 milliamperes for the high current units. However, it exhibits a turn-off current gain as low as 2. The operating and storage temperature range for both types is -65° C to +125° C. They are available in TO-9 and TO-18 cases.

The Shockley 4-layer diode is a 2-terminal silicon switch with 2 stable states, namely, off and on. To turn the device on, the voltage applied across the terminals must exceed the switching voltage. To turn the device off, the current flowing through the device must be reduced below the holding current. Type E of the MIL-Line series has the widest temperature range of any type. It can operate in the ambient temperature range of -60° C to +125° C, but the storage temperature range of the device is not specified. It is available in 6 voltage ratings from 20 to 200 volts with a maximum forward dc current of 150 milliamperes, a maximum peak current of 10 amperes, and a holding current of 1 to 45 milliamperes. The maximum power rating is 150 milliwatts with a derating of 1.5 milliwatts per °C above 50° C. The reverse breakover voltage is greater than 50% of the nominal switching voltage.

Other types of the MIL-Line series are available with maximum forward dc currents of 5 amperes and voltage ratings of 50, 100, and 200 volts. However, they are available for only the lesser temperature range of -60° C to +105° C. Although the use of this device can lead to considerable simplification of circuits, it is subject to as much as a 40% variation in switching voltage as the temperature varies from -60°C to +125° C. Also, only a few voltage ratings are offered, which is restrictive in the application of this device.

General Electric offers the unijunction transistor, which is a 3-terminal device having a stable "N" type negative resistance characteristic over a wide temperature range. A stable peak point and a high peak current rating make this device useful in timing circuits, trigger circuits, and bistable circuits, where it can replace 2 conventional silicon transistors. It is widely used in firing circuitry for controlled rectifiers. Type 2N2417 has a maximum power dissipation of 390 milliwatts, a maximum RMS emitter current of 70 milliamperes, and a maximum emitter reverse voltage of 60 volts. The operating temperature range is -65° C to +140° C and the storage temperature range is -65° C to +175° C. The case is 0.23 inches in diameter and 0.20 inches high.

General Electric also offers a series of silicon controlled switches such as the 3N60. This is a 4-layer device that also has 4 terminals so as to make all layers accessible. It is suitable for applications including bistable memory elements, binary counters, ring counters, time delay generators, and pulse generators. It has a maximum anode blocking voltage of 40 volts, a maximum allowable average forward current of 100 milliamperes, and a maximum power dissipation of 300 milliwatts. The operating temperature range is -65° C to

+150°C, and the storage temperature range is -65°C to +200°C. The case is 0.33 inches in diameter and 0.26 inches high.

It should be noted that the term "silicon controlled switch" has been used (and still is) to designate a device which is only an ultra-sensitive controlled rectifier. However, the device just discussed is not only able to function as an ultra-sensitive controlled rectifier (PNPN configuration), but also in many other ways. Among the other functions which it can perform are these: (1) NPNP controlled switch (SCR complement); (2) NPN or PNP transistor; (3) Trigistor or Transwitch (gate control of turn-on and turn-off); (4) S type negative resistance (Binistor); (5) 4-layer diode (Shockley diode); and (6) zener diode.

2.2.1.3 Microcomponents

Transitron's high conductance diffused silicon microdiodes provide the same high performance forward and inverse characteristics of conventional types. The minute rugged microdiode design permits major space savings. A true hermetic glass seal and sturdy construction insure a unit capable of providing long term reliability under wide environmental conditions. The TMD45 has a PIV rating of 200 volts, a maximum forward current of 75 milliamperes, a maximum surge current of 400 milliamperes, and a maximum forward voltage drop of 1.0 volts at 100 milliamperes, and a maximum average power dissipation at +25°C of 100 milliwatts. It has an operating and storage temperature range of -55°C to +150°C. The case is 0.08 inches in diameter and 0.05 inches long.

The diffused silicon microdiode line includes microminiature stabistors. They are useful in temperature compensating transistor and zener diode circuits, and in providing bias voltages for transistor circuits. The TMD-20 has a maximum average forward current of 25 milliamperes and a maximum inverse working voltage of 10 volts. The operating and storage temperature range is -55°C to +150°C, with a required derating of 1.25 milliamperes for each 5°C rise above +25°C. The case is 0.08 inches in diameter and 0.05 inches long.

The diffused silicon microdiode line includes microregulators. They are available in 10 voltage ranges between 5.1 and 12.0 volts, and have a maximum power dissipation of 100 milliwatts at +25°C. Power derating above +25°C is 0.8 milliwatts per °C. The operating and storage range is -55°C to +150°C. The unit is packaged in a true hermetic glass seal with a body 0.08 inches by 0.05 inches.

Transitron's microtransistors are NPN silicon transistors designed for small signal amplifying and switching applications. They have a maximum power dissipation of 150 milliwatts at +25°C and a voltage rating of 45 volts. The storage and operating temperature range is -55°C to +175°C. The case is hermetically sealed glass that is 0.16 inches in diameter and 0.06 inches thick.

Pacific Semiconductors, Incorporated offers off-the-shelf microdiodes and microtransistors which are packaged in sizes one to two orders or magnitude smaller than conventional counterparts. The product line includes micro-

transistors, pico-transistors, micro-diodes, micro-rectifiers, and micro-regulators. PSI uses surface passivation to provide environmental protection for its microcomponents, and by application of this chemical treatment a good hermetic seal is provided. These micro-components meet the requirements of MIL-S-19500. They have passed severe environmental tests of salt spray, centrifuge (20, 000G); vibration, shock (1000 G), thermal shock, moisture resistance, and hydrostatic bomb. The operating and storage temperature range is -65° C to $+150^{\circ}$ C or $+175^{\circ}$ C.

2.2.2 Functional Devices

The term "functional devices" can be used as an inclusive term for all packaged circuits and circuit modules that are intended to perform a single, specific circuit function. However, it is often restricted to micro-electronic devices such as the T. I. solid circuit or the Fairchild micrologic. This restriction applies here because the devices to be discussed here are all in the category of microelectronic functional devices (henceforth referred to as MFD); they are all commercially available.

MFD can be classified as 3 types, depending on the basic process employed in fabrication. These types are integrated circuits, thin-film circuits, and modular circuits. The integrated circuit is constructed on a silicon or other active substrate where both active and passive circuit elements are integrated with, and inseparable from the substrate. The thin-film circuit is constructed on an inactive substrate where the passive elements (R, C, L) are produced by vapor deposition or other electrochemical process and the active elements are discrete. The modular circuit is constructed of discrete ultra-small components interconnected by any of a number of methods (wires, thin films, conductive cement, etc.) and packaged in extremely small modules or in transistor packages.

The molecular circuit might be considered a fourth type but really is an extension of the integrated circuit concept. Such circuits are formed within solid blocks of doped silicon or other suitable solid state materials and identifiable only by functions performed not as individual circuit components. The molecular circuits are not yet available for specification by circuit designers.

A first decision was whether integrated, thin-film, or modular MFD would be used. It was noted that only integrated circuits are available as stock items. The possibility of T. I. providing to us a thin-film equivalent of the Solid Circuit was investigated. T. I. 's replies were discouraging and conveyed the idea that T. I. is definitely not interested in making a thin-film availability commitment.

Investigation has indicated that integrated circuits are the best choice if features are ranked in the following order: (1) reliability; (2) cost; and (3) performance. Thin films have an advantage in speed only. It is likely that standard practice will jump from miniaturized printed circuit boards directly to integrated circuits. It is doubtful if the Signal Corps micromodule approach will become popular because the specialized assembly machinery that is needed to bring costs down just hasn't emerged. The dot or pellet approach does not have any considerable advantage over the existing microminiature approaches with discrete components. As a result of these considerations, it was decided to restrict further consideration to integrated MFD.

Items of interest in evaluating integrated MFD may be listed as follows:

- Reliability
- Power Dissipation
- Power Supply Requirements
- Fan-In and Fan-Out
- Input and Output Criteria
- Temperature Range
- Speed
- Propagation Delay
- Voltage Rating
- Circuit Description
- Logic Equations
- Gain and Bandwidth
- Environmental Test Specs
- External Connections
- Package Geometry and Size
- Adequacy of Specification and Application Data

Not only the device specifications, but also certain facts regarding the manufacturer must be scrutinized. Among these are the following: (1) general reputation; (2) solid state technological capability; (3) technique of specifying and measuring; and (4) stability. Integrated MFD offered by several manufacturers will be discussed in the following sections.

2.2.2.1 Texas Instruments

T. I. offers various MFD as off-the-shelf items. The SN510 and SN511 are flip-flops. The SN512 and SN513 are NOR or NAND gates. The SN514 is a dual NOR or NAND gate. The SN515 is an EXCLUSIVE OR network. The maximum supply and input voltages are 8 volts and typical MFD dissipation is 7 milliwatts. The operating and storage temperature range is -55° C to +125° C. T. I. Solid Circuits are mounted in a glass-to-metal hermetically sealed package with leads of gold-plated nickel-flashed Kovar. The weight is 0. 1 grams and the size is 1/4 x 1/8 x 1/32 inches. T. I. has the distinction of being the only manufacturer to provide detailed reliability data for its MFD. The size and equivalent circuit of a solid network is shown in Figure 6.

2.2.2.2 Fairchild

Fairchild Semiconductor manufactures MFD known as Micrologic elements. They are off-the-shelf items primarily intended for building the logic section of a digital computer. Available functional devices which comprise the Micrologic family are a flip-flop, half-shift register, gate buffer, half adder, and counter adapter. They dissipate an average power of 30 milliwatts and have an operating temperature range of -55° C to +125° C. The MFD is packaged in a TO-5 case. The flip-flop requires accessory gates to function as a clocked flip-flop and even then requires a 2-phase clock, whereas a single-phase clock system is preferred in this application. The speed is of the same order as the T. I. device, but the power dissipation is much greater.

2.2.2.3 General Instrument

General Instrument Corporation manufactures MFD known as Nanocircuits. They are off-the-shelf items available as a flip-flop, flip-flop steering gate, NOR gate, NAND gate, and buffer amplifier. The operating temperature range is -55° C to +125° C. The device is packaged in a TO-5 case. It is not a true integrated circuit but has been described as a multiple integrated circuit because of an unusual construction technique.

The General Instrument approach is to mount the individual elements, such as the transistors, diodes, resistors, capacitors, and inductances, on their own support substrates. Each individual substrate is then appropriately bonded to one master substrate. This approach is represented as having several advantages:

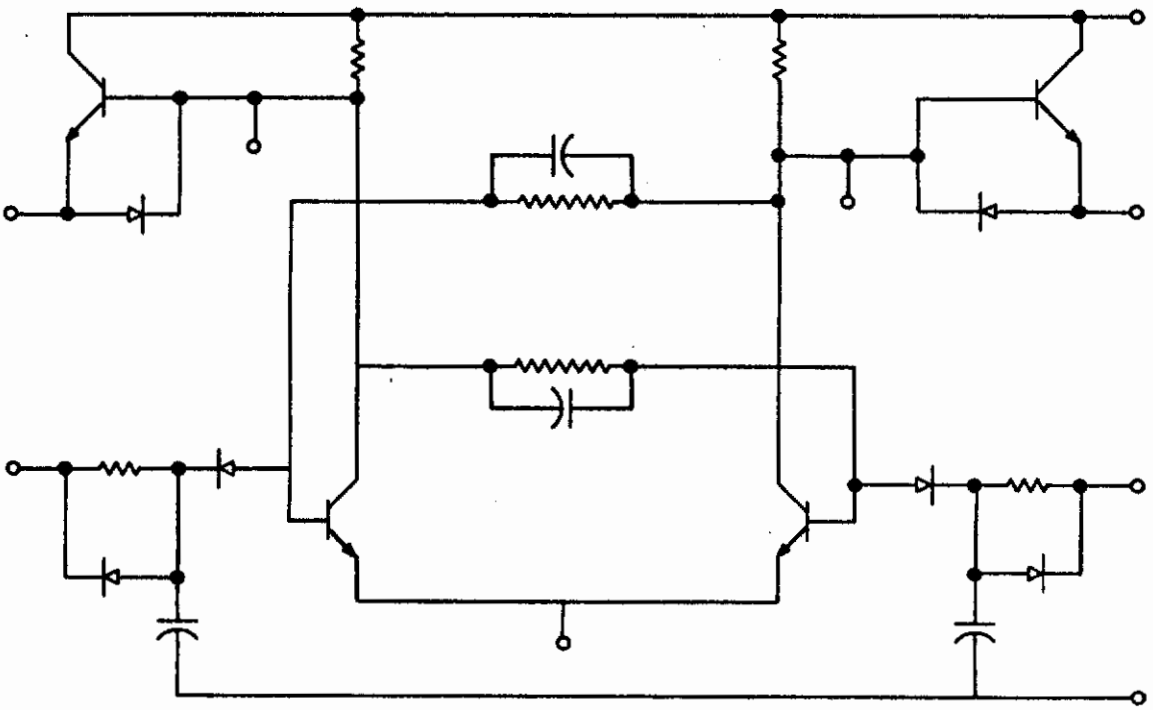
(1) The individual sub-elements are mass-produced and tested using techniques and procedures dictated by the inherent properties of the particular element. These procedures and techniques are optimized without regard to the problems of compatibility with other sub-elements.

(2) All the sub-elements are thoroughly pretested prior to the bonding to the master substrate. This assures the final acceptance of the completed assembly. In other techniques, a malfunction of any one sub-element results in the rejection of an entire circuit.

(3) This program allows variations in final assembly which might be costly or impossible in other approaches.

Epitaxial planar transistors and diodes are incorporated in Nanocircuits using either ceramic or metal master substrates. Film-deposited resistors and silicon-oxide capacitors are also used. As many as nine diodes and two transistors can be mounted in a single standard TO-5 transistor package. The sub-elements used are prepared specifically for Nanocircuit end-use, and the techniques developed for producing these elements minimize problems of surface

(a) Actual Size 



(b) Equivalent Circuit

Figure 6. Example of a Commercially Available Solid Network.

protection and internal connections.

The primary advantage of Nanocircuits is a 20 mc repetition rate. Disadvantages are the same as those given for the Fairchild MFD.

2.2.2.4 Other Manufacturers

Other integrated MFD are available as standard catalog items from TRW Electronics, Motorola, General Electric, Signetics, and a few others. Signetics employs a logic system similar to T. I. but offers somewhat higher speed. General Electric offers Emitter-Coupled Transistor Logic, but the standard packages are regarded as less desirable than the T. I. MFD. However, the custom service offered permits incorporation of 66 resistors and 18 transistors in a TO-5 case. It has 2 primary disadvantages. First, only the custom service appears interesting. Second, it has only recently been made available and lacks the reliability data of the T. I. MFD.

3. TEMPERATURE RANGE

The contract does not specify the temperature range for which to design the circuitry. However, in the design of solid state circuitry, the temperature range in which it is to be used is a matter of great importance. This is because solid state circuit configurations that function efficiently and well in a moderate temperature range can fail completely in a more severe temperature range. Not only can they fail, but in many cases, it will be extremely difficult to adapt the circuitry to the more extensive temperature range. Thus, it is necessary to determine the most reasonable temperature range for which to design the circuitry.

It is desirable to restrict the temperature range insofar as possible because thereby circuit design is simplified and reliability is improved. However, it is a basic premise of HIAD that equipment should be as compatible as possible with the anticipated environment, both natural and induced, so as to minimize the need for artificial environmental systems.

It should be remembered that reduction in size and weight of electronic equipment is not always indicative of penalty reduction to vehicle performance. In certain cases, the savings in size and weight achieved by miniaturization can be shown to be a delusion if lower temperature levels have to be maintained. Thus, the temperature range of the electronic equipment should allow it to function reliably with minimum penalty to the overall vehicle in the form of the required shielding and insulation from the extremes of the environment. Therefore, the circuitry should be capable of operating in the anticipated thermal environment insofar as this is possible with present devices.

3.1 Anticipated Thermal Environment

The first consideration is the possible thermal environment of the space vehicle in which the circuitry will be used. This environment can be considered separately for the earth, space, the planets, and re-entry.

3.1.1 Earth

As regards the earth's environment, MIL-STD-210 and specification MIL-W-9411 give the following ground level ambient temperature ranges for equipment:

(1) for storage,	-62.2° C to +52° C plus 360 BTU per square foot per hour for 4 hours, or +71.1° C;
(2) for operation,	-54.4° C to +52° C plus 360 BTU per square foot per hour for 4 hours, or +71.1°C.

Also indicative of the earth's ambient temperatures are the requirements given in HIAD for equipment used in conventional aircraft. The operating and storage temperature ranges correspond to those given above. It is also mentioned that it is necessary to design for the highest rate of change of temperature (temperature shock) that can be produced by the vehicle. The lowest temperature of the range is -54° C and the highest is the highest induced by the vehicle.

3.1.2 Space

In space where there is no significant gaseous atmosphere, heating and cooling take place solely by radiation. Assume that a vehicle is operating in the vicinity of the earth and that the moon's influence is negligible. Then, the energy input consists of solar energy received directly, solar energy reflected by the earth, and thermal energy radiated from the earth. At the same time, internal heat will be generated and the vehicle will radiate thermal energy. Thereby, the vehicle will achieve a heat balance.

As a vehicle moves farther into space, the energy received from any planet becomes small compared to solar energy input. Considering solar energy input only, the temperature of a vehicle will be inversely proportional to the square of its distance from the sun. The equilibrium temperatures due to solar radiation for a rapidly rotating small solid black body in space are given in Table 2.

TABLE 2

Equilibrium Temperatures Due to Solar Radiation

Position	Temperature
0.4 A. U. (Mercury)	+ 170° C
0.7 A. U. (Venus)	+ 54° C
1.0 A. U. (Earth)	+ 10° C
1.5 A. U. (Mars)	- 46° C

3.1.3 Planets

Temperatures on the moon average about +100° C for surface facing the sun and the hottest areas have temperatures up to +132° C. At night, these temperatures drop to -152° C, or less. These temperatures affect surrounding objects through transfer of heat by radiation, and in some cases by conduction. Convection, so important in the presence of an atmosphere, is totally absent.

The surface temperature of Mars is not precisely known, largely because of the uncertainties of various constants used in the theoretical calculations and in measuring the reflected radiation. However, it is calculated that the surface temperature can vary in the polar regions from a winter average of -100°C to a summer average of -1° C. In the equatorial regions, it varies from +30°C at noon to -85°C at night.[1] A surface temperature of +15° C on the surface decreases to -18° C at 5 miles altitude, -46° C at 10 miles, and -96° C at 20 miles. Thus, the vertical lapse rate is about 5.6° C per mile.

The surface temperature of Venus is unknown, but is generally assumed to be very warm by earth standards. This is assumed because of the insulating effects of carbon dioxide, which exists in abundance in the atmosphere. The surface temperatures have been estimated to range from a low of -25° C to a high of +800° C. The upper atmosphere has a temperature of about -40° C.

3.1.4 Re-Entry

Thermal control of aerospace vehicles is always a problem of critical importance. However, an extreme thermal problem exists in the case of vehicles re-entering the earth's atmosphere. The temperatures developed are so high as to affect the mechanical integrity of the vehicle itself.

3.1.5 Typical Requirements

Some temperature ranges that have been specified for equipment in aerospace vehicles are the following:

(1) Missile (SM-62), reference NA1-54-460 of 10/8/57; -62° C to +85°C in flight and -54° C to +46° C with solar heating to+60° C in transportation.

(2) Ballistic Missile (WS-107A), reference RAD-T128F of 9/4/59: -54° C to +63° C in transportation, and a lesser range in flight.

(3) Ballistic Missile (POLARIS), reference BuWeps Code Ident 10001 OD14181: -54° C to +71° C for flight and transportation (and 2 minutes at +93° C).

(4) Missile Satellite (WS-417L), reference LMSD-6117A of 6/24/59, has a skin temperature of -46° C to+77° C in orbit, and in transportation must withstand -54° C to +52° C plus solar radiation heating to +71° C.

(5) The electronic equipment of the Mariner B Mars Probe scheduled for 1964 must withstand sterilization at +135° C for 26 hours and -20° C to +20° C

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[1] Criteria for Environmental Analysis of Weapon Systems by C. J. Eiwen and D. E. Winer, WADD Tech Report 60-627, August 1960.

in transit.

(6) On the surveyor project, scheduled for 1963, a solid state electronic system was developed to survive at -152° C, which is moon temperature at night. This system utilized components usually restricted to -65° C storage. The sterilization temperature was +140° C. No attempt was made to operate components at temperatures higher than manufacturers' specifications. The high temperature rating is believed to be much more critical than the low temperature rating.

3.1.6 Temperature Limits

It can be concluded that a spacecraft suitable for the moon, Mars, or Venus would be exposed to temperatures as low as -152° C during the lunar night and as high as +800° C on Venus. Re-entry temperatures would exceed that upper limit.

3.2 Temperature Range of Present Devices

A previous discussion of the temperature range and availability of present semiconductor devices indicated that only silicon devices can be considered at this time, Silicon controlled rectifiers generally have an operating temperature range of -65° C to +125° C or +150° C and a storage temperature range of -65° C to +150° C. Silicon power transistors generally have an operating and storage temperature range of -65° C to +150° C, or +175° C, or +200° C. Silicon rectifiers and diodes generally have an operating and storage temperature range of -65° C to +200° C. The unijunction transistor has an operating temperature range of -65° C to +140° C and a storage temperature range of -65° C to +175° C. The silicon controlled switch (G. E.) has an operating temperature range of -65° C to +150° C, and a storage temperature range of -65° C to +200° C. Microdiodes and microtransistors have operating and storage temperature ranges of -55° C to +150° C, or slightly greater. Other small signal or switching transistors exhibit operating and storage temperature ranges of -65° C to +200° C (storage temperatures extend to +300° C in some cases). Microelectronic functional devices have operating and storage temperature ranges of -55° C to +125° C.

3.3 Temperature Range of Present Circuitry

The storage temperature applies to long term storage, a sterilization period, or any other period when the circuitry is not electrically energized. Because no power is being dissipated under this condition, the storage temperature range of the circuitry corresponds to the smallest storage temperature exhibited by any component of the circuitry. This means that a storage temperature range of -65° C to+150° C is possible if any component discussed in the previous section (except functional microelectronic devices) is used.

However, if functional microelectronic components are used, then the storage temperature range is restricted by them to -55° C to +125° C.

The operating temperature range applies to the circuitry when it is electrically energized. The lower operating temperature limit of the circuitry corresponds to the lower operating temperature limit of the components. This is obviously true because the power dissipation can only increase the temperature. However, the upper operating temperature limit of the circuitry must be below the upper operating temperature limit of the components as specified by the manufacturer. This is needed to allow for the internal heating produced by power dissipation.

Internal power dissipation is most severe for the power switching devices. For example, a silicon controlled rectifier conducting 10 amperes could exhibit a power dissipation of 10 watts. Thus, a controlled rectifier with a maximum operating temperature of +125° C and a thermal resistance of 2° C/W would have a temperature rise of 20° C between junction and case. The temperature rise between case and ambient with a reasonable heat sink could be another 20° C. Thus, it is apparent that the upper limit of the ambient temperature would be about +80° C. Thus, the maximum ambient operating temperature range of circuitry using microelectronic functional devices and silicon controlled recitifers would be -55° C to +80° C.

3.4 Selected Temperature Range

The lowest and highest temperature involved in the operating regime of a spacecraft have been indicated. Also, the practical temperature range for the type of circuitry desired when implemented by state-of-the-art components has been indicated. Because the possible temperatures exceed the maximum practical temperature range for which the circuitry can be designed, it appears that the maximum practical temperature range should be the design objective. This is an operating temperature range of -65° C to +80° C and a storage temperature range of -65° C to +150° C if microelectronic functional devices are not used. However, if microelectronic functional devices are used, then the operating temperature range is -55° C to +80° C and the storage temperature range is -55° C to +125° C.

It is, of course, generally well appreciated that high temperature operation of solid state circuitry has an adverse effect on reliability. Therefore, the capability of circuit operation or survival at the extremes of the selected temperature range should not be construed as making unnecessary either better thermal control techniques to reduce the range or improved solid state components to better withstand the extreme temperatures.

3.5 Effects of the Actual Thermal Environment

The temperatures which have been specified for the circuitry are ambient temperatures. They are based upon specified device limits and experience with solid state switching circuitry used in free air at sea level on the earth's surface. Ambient temperature is the average temperature of the medium surrounding an object. However, ambient temperature alone cannot describe the entire thermal configuration of an object because the temperature of the medium surrounding an object is not necessarily related to the heat radiation and conduction effects from nearby heat sources. Thus, the entire thermal environment must be known to describe the thermal conditions surrounding an object. Thermal environment is the condition of (1) fluid type, temperature, pressure, and velocity; (2) surface temperature, configurations, and emissivities; and (3) all conductive thermal paths surrounding an object. Unfortunately, the actual thermal environment cannot be determined at this time. Therefore, it is necessary to provide data derived from experimental laboratory work that will be meaningful to the installation designer who must install the circuitry in a space craft. This can be done by specifying the maximum allowable component surface temperatures and the thermal load produced by the circuitry.

4. LOGIC AND CIRCUIT DESIGN

4. 1 Design Philosophy

Circuit development utilized only commercially available devices which were representative of the present state of the art. For example, microelectronic devices were used in the logic circuitry. However, it was not intended to confuse a preliminary circuit development project with a device development project. Device development efforts would not only lead to high cost and considerable time delay, but in view of the present state of the art, were unnecessary. Thus, only commercially available microelectronic devices were used. In addition, special devices such as the silicon controlled switch which can reduce circuit complexity and increase reliability were used. Because of the susceptibility of semiconductor devices to supply voltage fluctuation, regulation has been provided for the supply voltages where necessary.

4. 1. 1 Logic Design

Treating the portion of the systems within the boundaries previously defined as a "black box", it was possible to write a description of the logical dependency of the outputs on the states of the inputs. A basic criteria of the logic design was to minimize the power switching required. In the electromechanical system logic was performed at a high power level, but the solid state system performs all logic at a low power level. Thus, only the power switches that were absolutely necessary have been used. Also, high current, multi-pole, multi-throw input switches have been replaced by low current, single-pole, single-throw switches.

A decision was made to develop the control circuitry with T. I. Solid Circuit types SN514, SN513, and SN512 as the primary devices. Special devices (SCS's, unijunction transistors, etc.) have been used where the Solid Circuits were not suitable, as, for example, in the SCR firing circuits and special delay circuits. They are preferred to the microtransistor circuits because fewer passive devices are needed. The SN514 is a dual NOR/NAND network that can be described as two isolated logic functions with a common B+ terminal. It has a maximum fan-in of 3 and fan-out of 5 per function. The SN512 is a single NOR/NAND network with a maximum fan-in of 6 and fan-out of 5. The SN513 is an SN512 with an emitter-follower output at terminal 9 which increases the fan-out capability to 25. The SN514 can be used as low fan-in NAND/NOR gates, as inverters, and, properly interconnected, as dc flip-flops. The SN512 can be used where a higher fan-in requirement exists, and the SN513 may be used where a higher fan-out requirement exists. An outstanding advantage of the T. I. Solid Circuit over other microelectronic functional devices is the very small power dissipation (7 mw@ V_{cc} =+6V).

Also, they are smaller and lighter.

Throughout this report, unless otherwise specified, all NAND and NOR gates are one section of an SN514. If more than three inputs are needed, an SN512 is used. The supply voltage to the Solid Circuits is +6 vdc ± 10% and is the same voltage furnished to the input switches. Many of the flip-flops used in the system are an SN514 interconnected as shown in Figures 7A and 7B. S is the set input, R is the reset input, and P is the preset input. A truth table for the dc flip-flop is given in Table 3. The equivalent output circuit for a Solid Circuit is shown in Figure 7C.

TABLE 3

DC Flip-Flop Truth Table

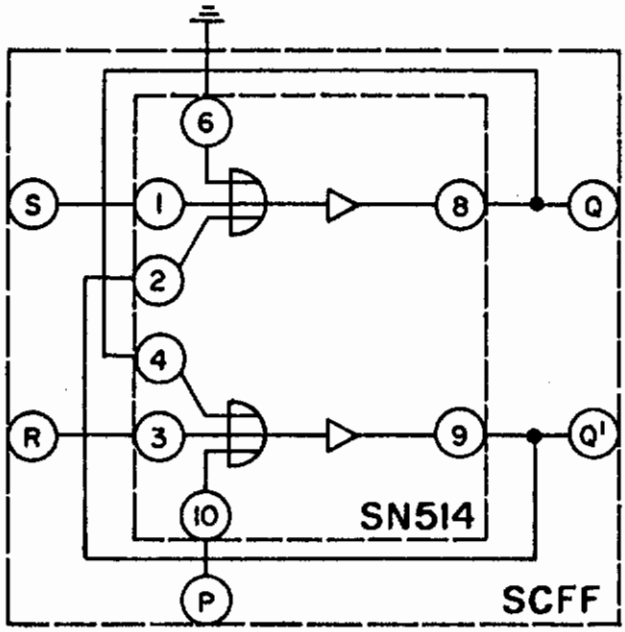
Inputs		Outputs	
R	S	Q	Q'
0	0	previous state	
0	1	0	1
1	0	1	0
1	1	0	0

Note: One (1) represents high voltage.

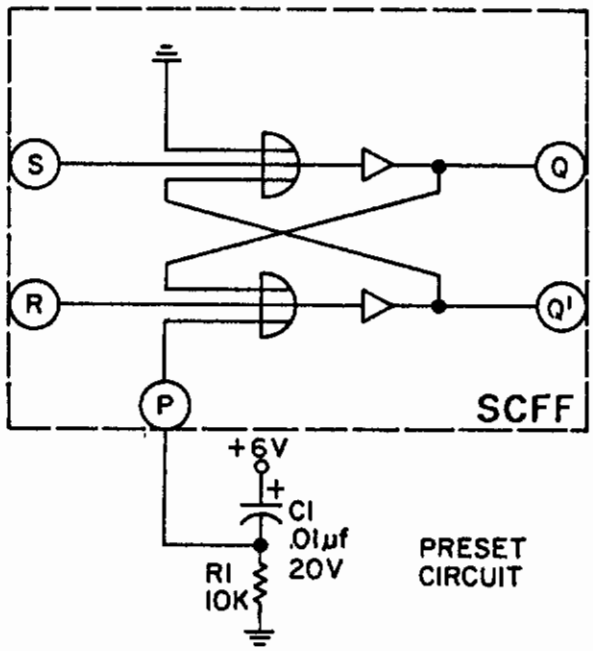
4.1.2 Control Circuit and Power Switch Design

The selection of components that would function as power switches was carefully considered. The RCA 2N1484 and 2N1486 silicon power transistors were used for dc loads below 2 amperes and the Westinghouse 2N2226 was used for dc loads greater than 2 amperes but less than 10 amperes. Silicon controlled rectifiers have been used wherever their advantages may be realized. For example, they are used as ac static switches in the TR section of the dc power system. The G. E. C40 SCR has been used where load currents are more than 10 amperes but less than 20 amperes and the G. E. C60 has been used where load currents exceed 20 amperes.

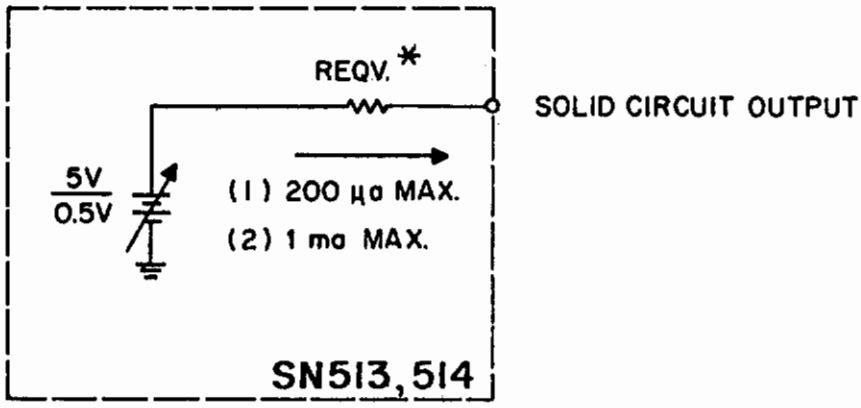
In addition to the SCR's and the power transistors, the circuitry uses unijunction transistors (2N491B), silicon controlled switches (3N60), and complementary silicon transistors (2N718 and 2N722). Examples of the use of unijunction transistors are several time delay circuits of the anti-ice system. They have the following logical characteristic: if the input exists continuously for a specified time period, then an output signal should appear; if the input vanishes before the time period has expired, then no output should appear. This timing delay has been designed as a unijunction transistor circuit and



(a) INTERCONNECTION OF SN514 TO FORM A DC FLIP-FLOP.



(b) SIMPLIFIED REPRESENTATION OF A DC FLIP-FLOP WITH PRESET CIRCUIT.



* (1) SN513 REQV. = 1.2 KΩ
(2) SN514 REQV. = 6K Ω

(c) EQUIVALENT SOLID CIRCUIT OUTPUT STAGE.

Figure 7. Solid Circuit Flip-Flop and Equivalent Output Stage.

provides the desired function with a minimum of circuit complexity. The silicon controlled switch is used in a binistor mode in preference to a binistor. It is a superior replacement capable of higher current and higher temperature operation.

Transistor minimum gain h_{FE} figures, which were arrived at through a conservative analysis of device specifications, are presented in Table 4.

TABLE 4

Transistor Minimum Gain (h_{FE}) Figures

Type	I_c	h_{FE} (min)
2N718	1 ma	10
2N718	10 ma	20
2N722	1 ma	10
2N722	10 ma	20
2N1484	1.2 a	20
2N1486	1.2 a	20
2N2226	5.0 a	100
2N2226	10.0 a	60

4.1.3 Overload Protection

Basically, the protector consists of a current detector, a bistable device, and a power switching device. It is illustrated in Figure 8. An overload current produces a voltage output from the differential amplifier that is sufficient to cause the dc flip-flop to change state and produce a positive signal into the negative AND gate. The result is that the normal control input can no longer provide a close signal to the power switch. The protector, once actuated, remains open until manually reset. However, it has been designed so that it is not possible to close the circuit by holding down the reset button while an overload condition exists. Thus, trip-free solid state circuit breakers were achieved.

4.1.4 Parts Data

The data given here is not complete in itself and must be used in conjunction with the schematics and their applicable notes. However, unless otherwise specified on the schematics or their applicable notes:

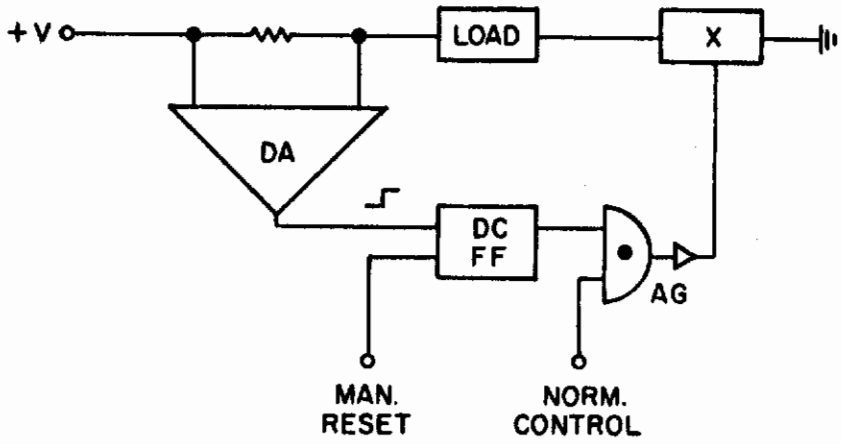


Figure 8. DC Overload Protection Technique

(1) Resistors

(a) All resistors are Allen-Bradley, 1/4 watt, 5% carbon composition.

(b) All 1/4, 1/2, and 1 w resistors are Allen-Bradley types CB, EB, and GB, respectively.

(c) All 1/8 w resistors are 1%, wire wound RN60C, IRC.

(d) Resistors with RS or RH designations are wire wound, Dale.

(e) All potentiometers are type 3280L-1, Bourns.

(2) Capacitors

1.2 uf, 35 v	150D125X9035B2	Sprague
2.2 uf, 35 v	150D225X9035B2	Sprague
0.01 uf, 20 v	150D103X9020A2	Sprague
10 uf, 20 v	150D106X9020B2	Sprague
4.7 uf, 35 v	150D475X9035B2	Sprague
0.18 uf, 35 v	150D184X9035A2	Sprague
0.011 uf, 20 v	151D113X9020W2	Sprague
68 uf, 35 v, 20%	TAS686M035POG	Mallory
0.47 uf, 50 v	150D474X9050A2	Sprague
30 uf, 70 v, 10%	130D306X9070T2	Sprague
2.2 uf, 20 v	150D225X9020A2	Sprague
100 uf, 30 v, 20%	132D107C2030T4	Sprague
0.11 uf, 20 v, 10%	151D114X9020W2	Sprague
11 uf, 70 v, 10%	130D116X9070F2	Sprague
22 uf, 35 v, 20%	TAS226M035POF	Mallory

(3) Transistors

(a) All NPN transistors are 2N718.

(b) All PNP transistors are 2N722.

(c) All unijunction transistors are 2N491B, G.E.

(d) All silicon controlled switches are 3N60, G.E.

(4) Diodes

All diodes are Transitron types.

(5) SCR's

All SCR's are G.E. types.

(6) Solid Circuits

All gates and inverters are one section of a T.I. SN514.

(7) Switches

(a) overload reset: SPST, N.O., momentary contact, Grayhill 39-1

(b) Input to logic

(1) SPDT, on/on, Cutler-Hammer 8816-K9
(2) SPDT, on/off/on, Cutler-Hammer 8802-K6

(8) Transformers
(a) All C40 gate transformers are Sprague 31Z204.
(b) All C60 gate transformers are Pulse Engineering PE2231.

(9) DC Overload Circuit
(a) All nichrome resistors are per Table 8.
(b) All dual NPN transistors used in differential amplifiers are 2N2223, Fairchild.

(10) AC Overload Circuit
T13, 14, 15 - special transformers
core - Magnetics, Inc. 55206-A2
wdg. A - 25 turns, AWG 24
wdg. B - 850 turns, AWG 30

(11) AC to DC Power Supplies

T1 (TR)	#11278 Per T. O. 8C14-6-S-3
PS1-T1	Special Transformer, Freed Three phase, 210 v L to L input, 400 Cps Secondary #1, 22v L to L, 300 ma max. dc out Secondary # 2, 14 v L to L, 650 ma pulse dc out, 33% D. C. Conforms to MIL Specs
PS2-T1	Chicago, 4MS-1208

4.2 DC Power System

The discussion of the dc power system has been divided into three parts: (1) abstract logic; (2) detailed logic; and (3) circuit design and operation.

4.2.1 Abstract Logic

The dc power system is a non-sequential one since all outputs depend only on the present inputs and not on any previous state of the system. The dc power system may be thought of as being made up of two kinds of elements: current switching elements and voltage sensing elements. Figure 9 is the abstract logic diagram of the power switching circuits of this system and shows the current switching elements.

There are two kinds of current switching elements. Points numbered from 2 through 5 in Figure 9 represent dc switching elements (there is no point 1). Points numbered 6 through 9 in the figure represent three-phase ac switching

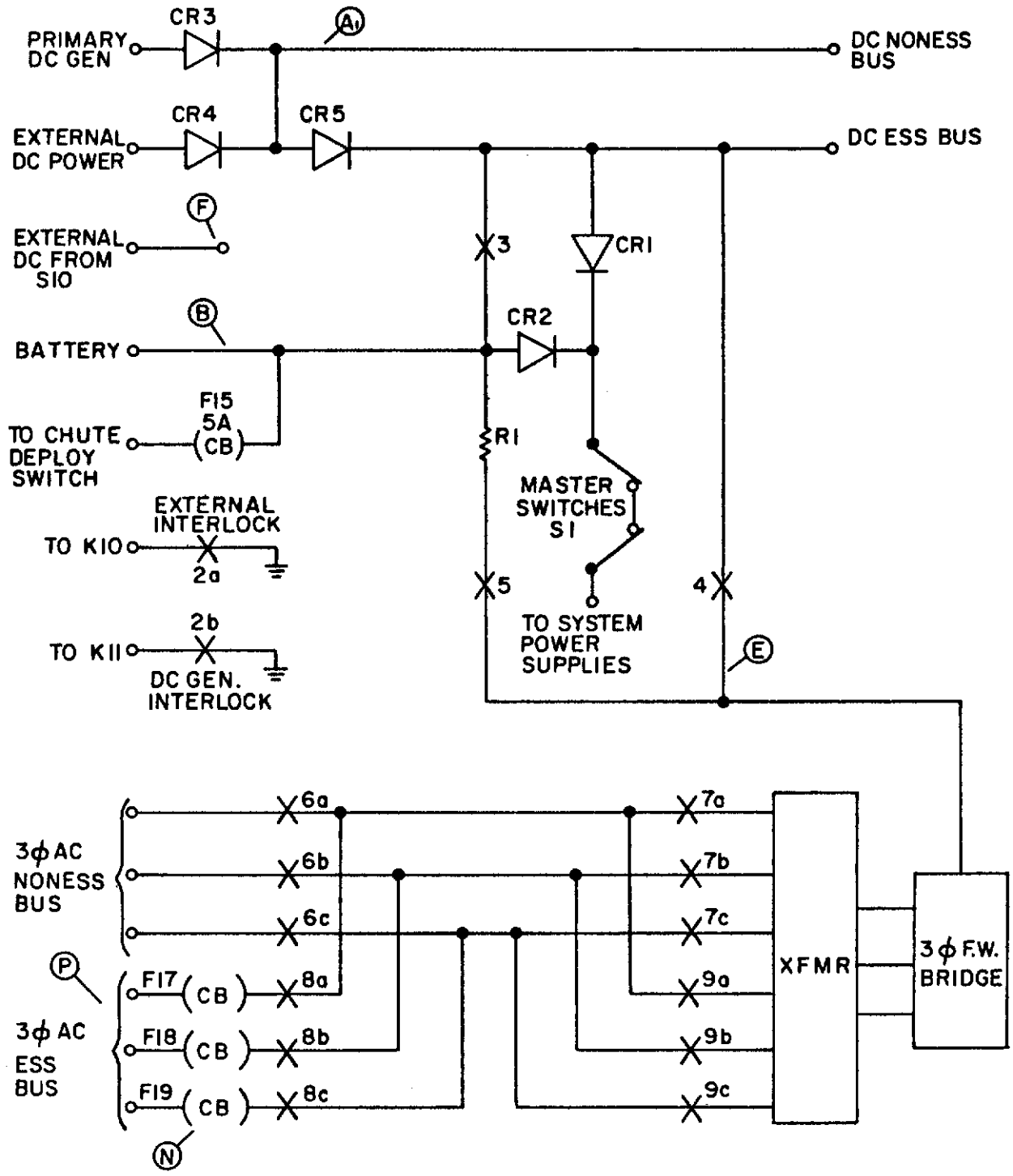


Figure 9. Abstract Logic for Power Switches of the DC Power System.

elements. The symbol (CB) represents a solid state circuit breaker.

Table 5 lists the logical conditions for operating the switches shown in the abstract logic diagram. As a preliminary step to the detailed logic design, the data given in Table 5 was converted to graphic form and is presented in Figure 10 as the abstract logic for the control circuits.

The isolating diodes CR3, CR4, and CR5 have been used in preference to active devices. Switches X2a and X2b are used to provide interlocking so that when external dc power is applied, the dc generator cannot be applied also. Voltage detectors are shown at F and A_1 and current sensors are shown at N. Turn-off of switches has been incorporated into the logic circuits in order that some assurance can be given that a switch will be open when another is closed.

4.2.2 Detailed Logic

The dc power system has been divided into two parts. They are the dc control section and the transformer rectifier (TR) section, as illustrated in the detailed block diagram, Figure 11. Power for the dc control circuits is derived from the battery or the dc essential bus while power for the TR section is derived from the ac essential bus.

The dc control section consists of X2a, the external power interlock, X2b, the dc generator interlock, X3, the battery to dc essential bus switch, and the chute deploy overload protector. The power switch, X2a, is operated by an amplifier, AP1, which is switched directly from an input (F) derived from the external dc source. The power switch, X2b, requires two conditions for operation. These conditions are actuation of the generator switch (G) and absence of external dc voltage ($\overline{F}$). These negative going inputs are supplied to a NAND gate (AG1) where a positive signal is produced and applied to the X2b amplifier circuit, AP2, which turns on X2b. X2a or X2b will only remain on as long as the proper inputs are applied to their respective control circuits.

X3 is a silicon controlled rectifier (SCR). The inputs required for turn-on of X3 are the test switch not actuated (H) and the absence of voltage on the dc nonessential bus ($\overline{A1}$). These negative going inputs are fed to a NAND gate (AG2) and then to an inverter (IV 1). The negative going output from IV 1 is applied to an SCR firing circuit, FC1, which is a unijunction transistor connected as a relaxation oscillator. The positive pulse output from the firing circuit is applied to the gate of X3 for turn-on. The battery is now connected to the dc essential bus. When X3 turn-off is desired, the conditions for X3 open need only be met and TO1 applies a reverse voltage across X3 for turn-off.

TABLE 5

Logical Definitions and Conditions for the DC Power System

Inputs	Definition
A_1	More than +17 v ± 20% on the dc nonessential bus (PG)*
C	Master switches closed**
D	AC emergency power disconnect relay in "Emergency AC Power On" Position (NG)*
E	TR Output: E1 = 28 v, E2 = 36 v
F	More than +17 v ± 20% external dc present (PG)*
G	Generator switch actuated (NG)*
H	Test switch not actuated (normally closed)
J	Air data converter switch in "Greater than 280 Knots" Position
N	Less than 5 amperes flowing per phase on ac essential bus
P	Voltage present on ac essential bus**

Switch Control Conditions

Switch	Close	Open
X2a	F	$\overline{F}$
X2b	$C \cdot G \cdot \overline{F}$	$\overline{C}+\overline{G}+F$
X3	$C \cdot H \cdot \overline{A}_1$	$\overline{C}+\overline{H}+A_1$
X4	$P \cdot H \cdot \overline{A}_1$	$\overline{P}+\overline{H}+A_1$
X5	$P \cdot H \cdot A_1$	$\overline{P}+\overline{H}+\overline{A}_1$
X6	$P \cdot (\overline{J}+\overline{D}+A_1)$	$\overline{P}+(J \cdot D \cdot \overline{A}_1)$
X7	$P \cdot A_1$	$\overline{P}+\overline{A}_1$
X8	$N \cdot P \cdot \overline{A}_1 \cdot J \cdot D = N \cdot \overline{X6}$	$\overline{N}+X6$
X9	$P \cdot \overline{A}_1$	$\overline{P}+A_1$

Note: * NG means negative going, PG means positive going.
** C and P are inherent conditions since control circuit power is dependent upon these conditions.

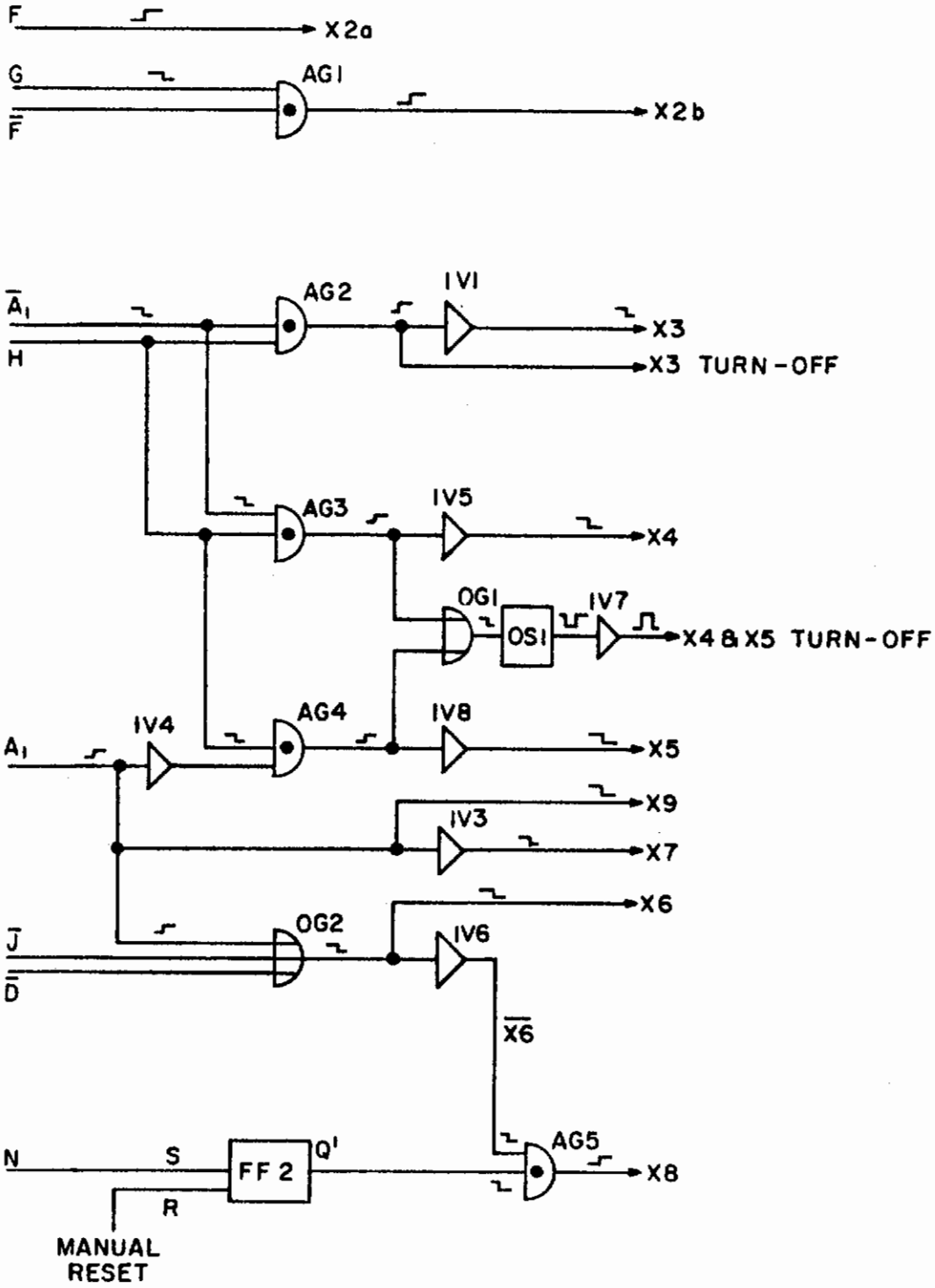


Figure 10. Abstract Logic for Control of the DC Power System.

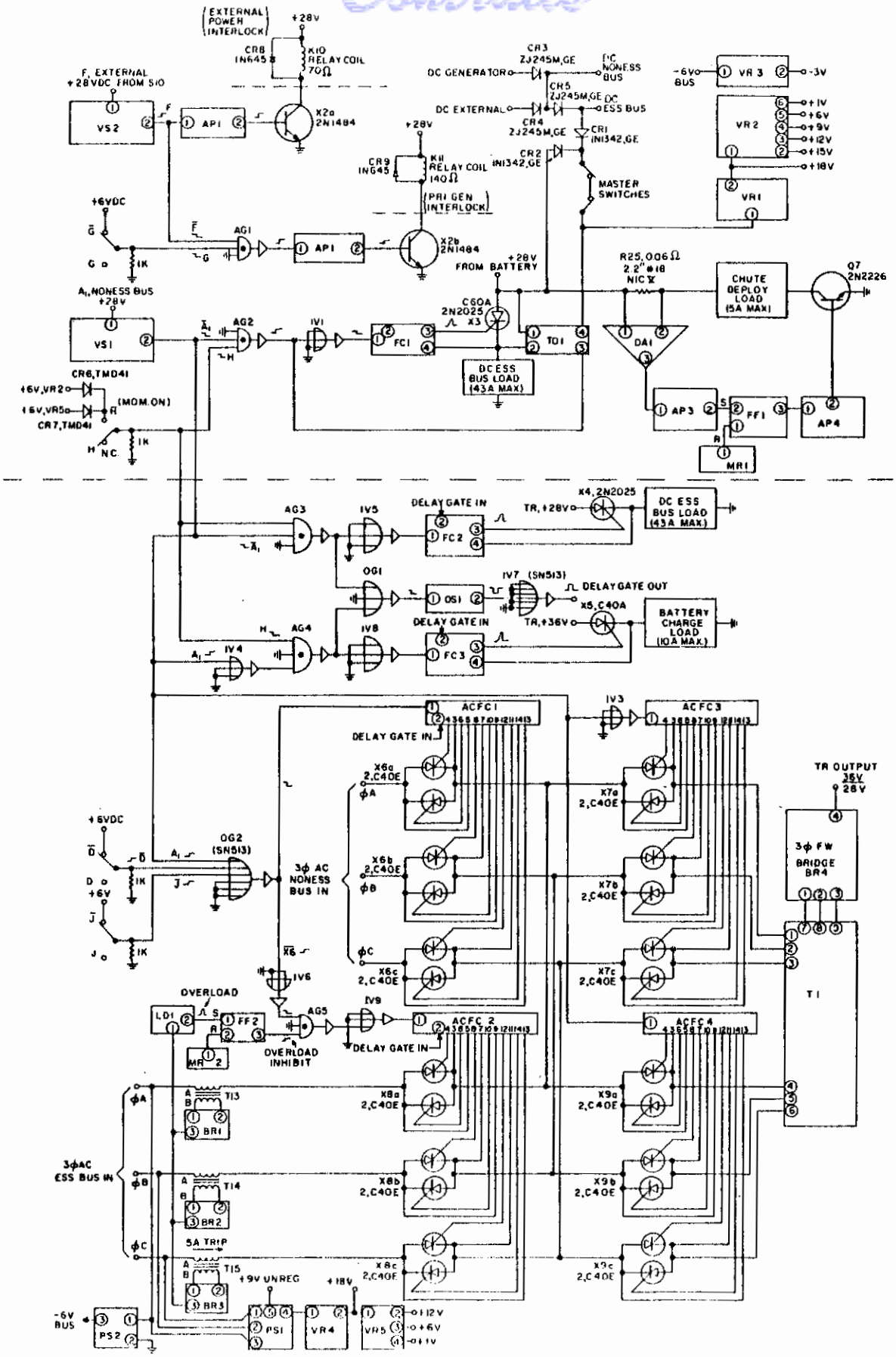


Figure 11. Detailed Block Diagram of the DC Power System.

The remaining circuits in the dc control section of the dc power system are the chute deploy overload protective circuits. Excess current is sensed by a differential amplifier, DA1, which is connected across a series resistor. This signal is amplified by AP3 and then applied to the input of a bistable multivibrator, FF1, which turns off a power transistor, Q7, which is in series with the chute deploy load. After tripping, FF1 must be manually reset like a conventional circuit breaker.

The transformer rectifier section consists of the TR to dc essential bus switch (X4), the TR to battery switch (X5), the ac nonessential bus switch (X6), the ac essential bus switch and overload protector (X8), the normal rectifier input switch (X7), and the emergency rectifier input switch (X9).

X4 turn-on requires that the test switch is not actuated ($\overline{H}$) and that voltage is not present on the dc nonessential bus ($\overline{A}_1$). The input $\overline{A}_1$ is derived by VS1, a voltage detection circuit which detects the potential on the dc nonessential bus line. Both of these inputs are applied to AG3. The output from AG3 is inverted by IV5 and then applied to the firing circuit, FC2. Simultaneously, the same input which is applied to IV5 is applied to OG1, inverted, and used to trigger OS1. OS1 provides a delay gate used to turn off X6, X8, FC2, and FC3 in order to assure turn-off of X4 and X5 preceding any turn-on signal to either switch. After the delay gate inhibit action is complete, FC2 produces a firing pulse to turn on X4, thereby connecting the rectifier output to the battery for charging.

Turn-on of X5 requires inputs H and A_1. The input from A_1 is inverted and then applied to AG4; H is applied directly. The output from AG4 is inverted by IV8 and then applied to the firing circuit, FC3. Simultaneously, the same input which is applied to IV8 is applied to OG1 and another delay gate is produced. After the delay gate is removed, FC3 produces a firing pulse to turn on X5, thereby connecting the rectifier output to the dc essential bus.

X6a, b, and c are pairs of SCR's connected as static ac switches between the three phase ac nonessential bus and the TR input. Any of three inputs are required for X6 turn-on. These inputs are A_1, $\overline{D}$, or $\overline{J}$ and are applied to OG2. The output from OG2 is applied to ACFC1 which provides turn-on signals for X6.

The conditions for turn-on of X8a, b, and c are $\overline{X6}$ and less than 5 amperes flowing in each leg of the ac essential bus (N). The input to ACFC1 is inverted by IV6 and applied to AG5 along with a signal from the ac overload detection circuits. If both inputs to AG5 are negative, AG5 produces an output which is inverted by IV9 and then applied to ACFC2 which turns on X8. If an overload occurs while the ac essential bus is supplying the TR, the overload is detected

by BR1, 2, 3, and LD1. Then FF2 is set which removes one of the inputs to AG5. Without the required inputs, AG5 produces an output which inhibits ACFC2 allowing X8 to turn off.

X7 and X9 are also ac static switches. X9 is turned on when there is no voltage present on the dc nonessential bus. It supplies the transformer taps which produce the emergency TR output of +28 vdc. X7 is on when there is voltage present on the dc nonessential bus. It supplies the transformer taps which produce the normal TR output of +36 vdc for battery charging.

4.2.3 Circuit Design

Direct coupling is used throughout the control circuits except for two cases. First, the input to OS1 requires a pulse of short duration and here RC coupling has been used. Second, the SCR firing circuits are transformer-coupled to the SCR gates due to isolation requirements. These and all other circuits designed to accomplish the control and switching tasks set forth in the previous sections will be discussed in the following sections.

4.2.3.1 Power Supplies and Regulators

In order to improve reliability, the dc power system makes use of redundancy in that two separate primary power supplies are used: one to supply the dc control section and another to supply the TR control section. A negative bias supply has also been incorporated and is used by both sections. Schematics of the power supplies and regulators are shown in the Figures 12, 13, and 14.

The dc power system requires a number of different voltages for proper operation. Table 6 presents the current requirements for the dc power system. These voltages are derived from both the dc essential bus and the ac essential bus. This redundancy in power supplies should tend to increase reliability. Since circuit performance was a primary consideration, the negative bias supply was added to provide some additional assurance of low leakage after temperature cycling and component aging.

The dc control section of the dc power system obtains its voltages from series regulators operating from the dc essential bus. VR1 is an emitter follower feedback regulator with current limiting capability which provides +18 vdc from a source which can vary from +27 vdc to +33 vdc. In the event of an overload, the total voltage across the emitter-base junction of Q1 and R3 reaches the zener voltage of CR1. Zener diode CR1 then goes into conduction to divert base current from Q1 and prevent any further increase in load current. VR2 provides +15 v, +12 v, +9v, and +6 vdc from the regulated +18 vdc line. These are series regulators of the open-loop type which obtain their reference voltages from a string of zener diodes CR3 - CR7. The +1 v

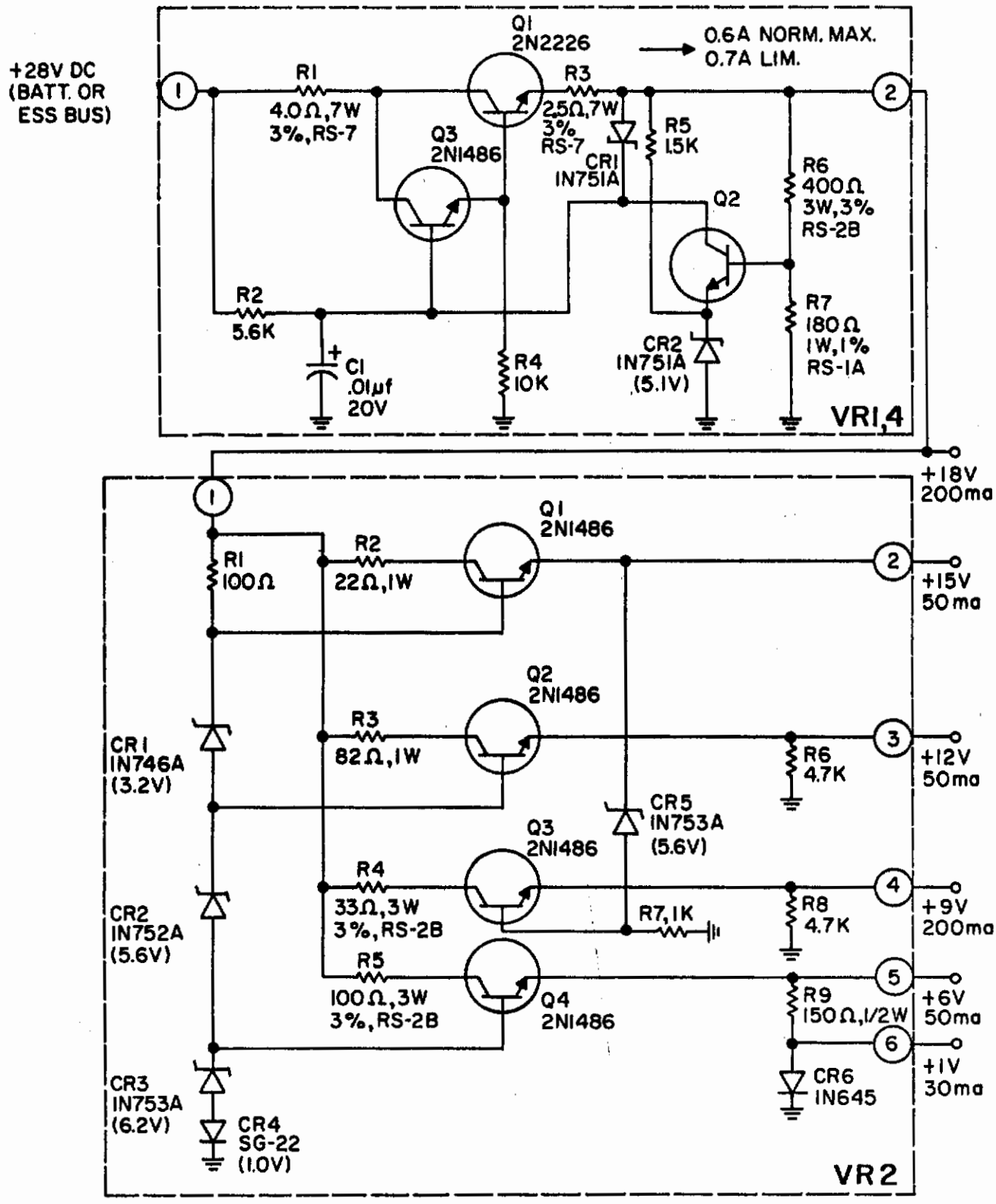


Figure 12. Voltage Regulators (VR1, 2, 4).

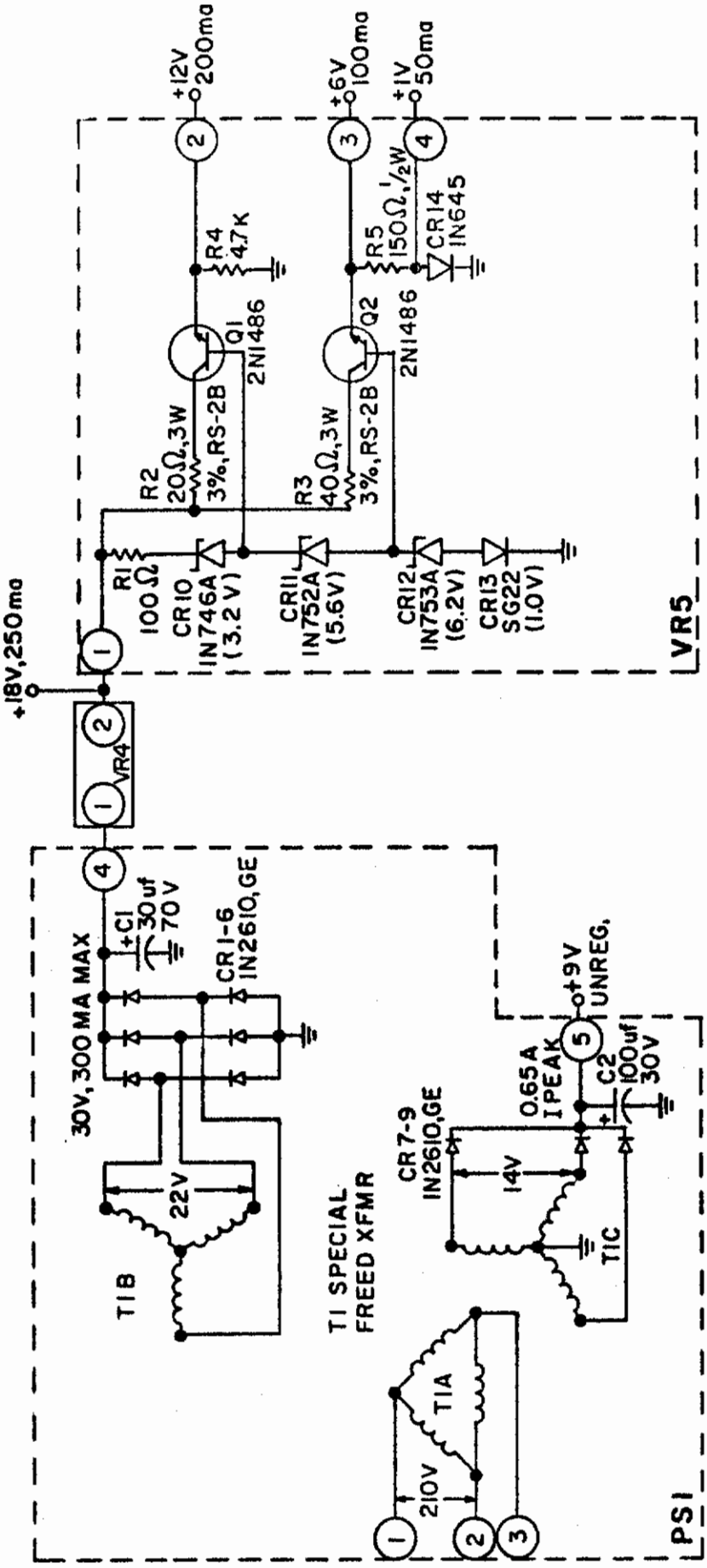


Figure 13. AC to DC Power Supply and Regulator

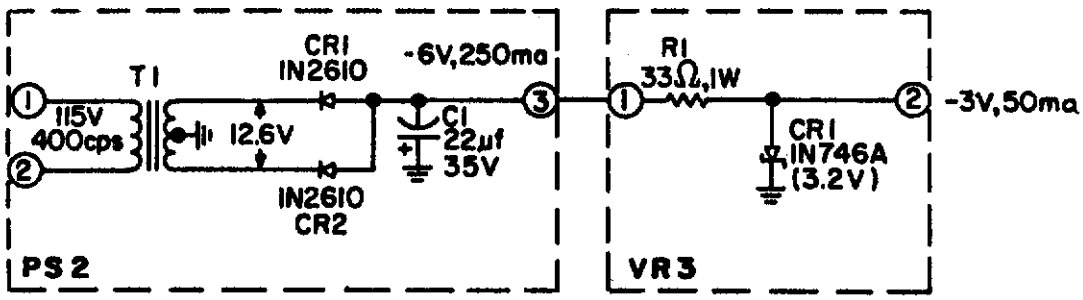


Figure 14. Negative Power Supply and Regulator

TABLE 6

Current Requirements for DC Power System in MA

Volts	DC Switching Section (from battery or dc ess. bus)	TR Switching Section (from ac ess. bus)
+18	100	150
+15	15	0
+12	20	120
+ 9	100	0
+ 6	20	50
+ 3	0	20
+ 1	15	20
- 3	20	0
Total	290 max	360 max

source is derived from the +6 v line by a diode shunt regulator.

The TR section of the dc power system obtains its voltages from PS1, VR4, and VR5. PS1 is a three phase ac to dc supply which provides +28 vdc and +9 vdc unregulated. The +9 vdc unregulated is used to supply the output pulse driver, Q5, of the ac firing circuits. The +28 vdc unregulated is used to supply VR4 which is identical to VR1 and produces a regulated output voltage of +18 vdc to VR5. VR5 is basically the same as one half of VR2, and provides +12 v, +6 v, and +1 vdc. Thermal conditions for the transistors of VR1, VR2, VR4, VR5 are presented in Table 7.

The negative bias supply, PS2, derives its input voltage from one phase of the ac essential bus and provides an output voltage of -6 vdc to VR3 which is a -3 vdc shunt regulator. In order to increase reliability it would be desirable to provide the negative voltage supply with an input derived from a voltage source used by a section. The dc to dc converter, CV30, described in the alternate circuits section of this report, would work very well in this application. For example, -3 vdc could be derived directly from the dc essential bus for use as a bias supply for the dc control section of the dc power system.

4.2.3.2 Voltage Sensors

VS1 and VS2 sense voltage presence on the dc nonessential bus and on the external dc input. A schematic of the voltage sensor is presented as Figure 15. These circuits are resistive voltage dividers with zener diodes as level detecting devices. A 5.6 v zener diode was selected due to the inherently low temperature coefficient at this zener voltage; therefore, the potential at which reverse breakdown occurs is fairly stable over a wide temperature range.

The circuit has been designed to produce an output of less than 0.3 vdc with an input of less than +17 vdc and an output greater than +2.5 vdc with an input which is more than +26 vdc. These values were arrived at after taking into consideration the dc bus variation and the Solid Circuit input requirements. The +13 vdc zener diode, CR2, provides transient protection for both CR1 and the Solid Circuits which are connected to the voltage sensor output. The output voltage may not exceed +8 vdc.

4.2.3.3 SCR Firing Circuit (FC1, FC2, FC3)

The schematic of the dc SCR firing circuit is shown in Figure 16. It is a unijunction relaxation oscillator with its frequency determining capacitor shunted with a switching transistor. As long as the transistor conducts, there

TABLE 7

VR1, VR2, VR4, VR5 Thermal Conditions

	Unit	T_j max (° C)	T_j sel (° C)	P_{dis} [1] (watts)	θ_{jc} (° C/W)	T_{case} (° C)	θ_{ca} (° C/W)
VR1, 4	Q1	+ 150	+ 125	30 [2]	0.5	110	1
	Q2			Not Applicable			
	Q3			Not Applicable			
VR2	Q1	+ 200	+ 175	0.1	7	174	94
	Q2	+ 200	+ 175	0.1	7	174	94
	Q3	+ 200	+ 175	0.4	7	172	92
	Q4	+ 200	+ 175	0.2	7	173	93
VR5	Q1	+ 200	+ 175	0.4	7	172	92
	Q2	+ 200	+ 175	0.4	7	172	92

Note 1: Power dissipation at maximum load and + 80°C ambient.

Note 2: Q1 dissipation only is specified for failure condition of short circuit on output.

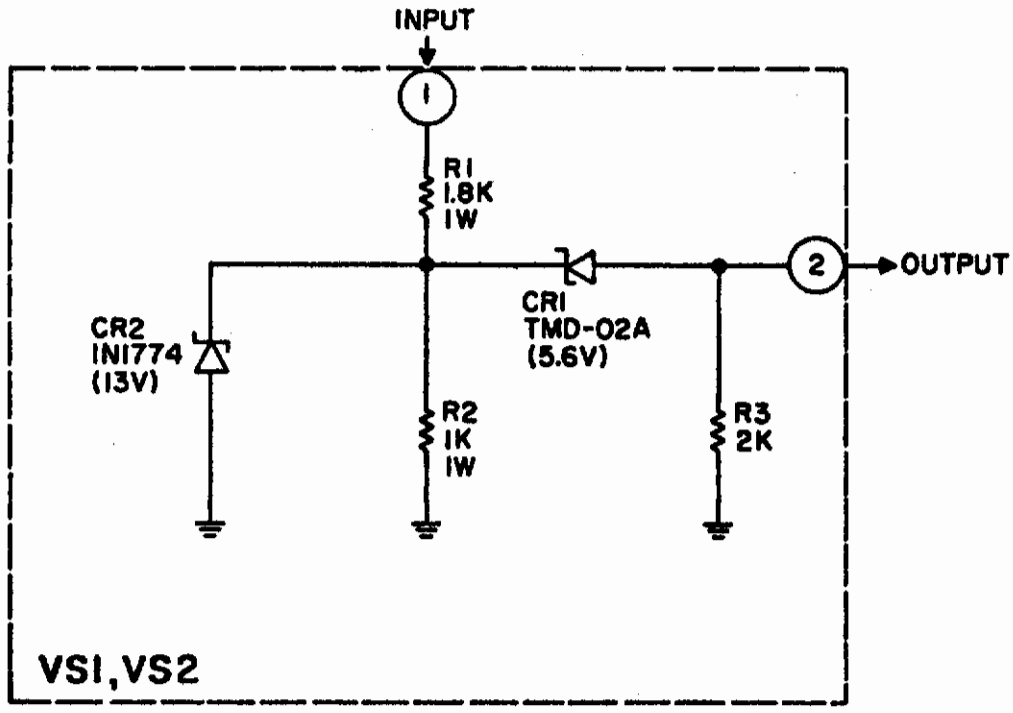


Figure 15. Voltage Sensor

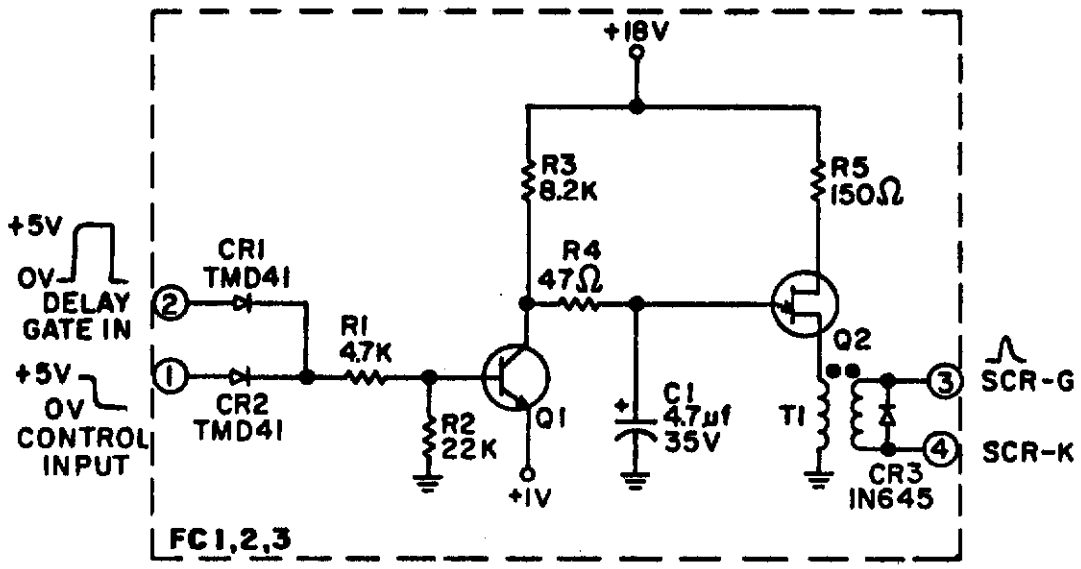


Figure 16. SCR Firing Circuit

is no output from the oscillator. When the switching transistor is turned off by a negative going control input, the unijunction is allowed to oscillate at a rate determined by the capacitor C1 and resistor R3. The output pulse is transformer coupled from B1 of Q2 to the SCR gate. Since the firing circuit is astable, it continues to pulse the SCR gate; therefore,if a load transient should occur which reverse biases the SCR, the next cycle of the firing circuit will turn the SCR back on, thereby maintaining continuity from the emergency supply (battery and TR) to the load.

4.2.3.4 X3 Turn-off Circuit (TO1)

X3 is turned off by driving the X3 cathode positive with respect to the anode. The schematic of the SCR turn-off circuit is shown in Figure 17. C3 of TO1 charges to the battery voltage through R7 and remains charged under normal operation. C4 of TO1 charges to the dc essential bus voltage through R6 and also remains charged under normal operation. When an emergency occurs which turns on X3, the charge on C3 and C4 tends to equalize through X3. While X3 is on, the control input is positive causing Q1 to conduct, thereby holding C1 below the firing point of Q2. If the dc nonessential bus voltage now becomes available (A_1) or the test switch is actuated ($\overline{H}$), the control input to TO1 goes negative permitting Q2 to fire. The pulse which is generated at B1 of Q2 is transformer coupled to the gate of Q3 causing Q3 to conduct. When Q3 conducts, C3 discharges through Q3 and R6, raising the Q3 cathode voltage to approximately +28 vdc; now C3 and C4 are effectively in series and their charges add. This causes the cathode of X3 to go to approximately +56 volts. This reversal of voltage across X3 causes a reverse current to flow through X3, thereby turning X3 off. C2 is used as a supply for Q2 in case turn-off of X3 is required after opening the master switch. R7 is large enough to limit the current through Q3 after discharge of C3 to below the holding current of Q3; therefore, Q3 turns off and C3 can recharge to the battery voltage.

4.2.3.5 X2a and X2b Interlock Amplifiers (AP1, AP2)

Figure 18 is the schematic of the interlock amplifier. AP2 differs from AP1 only in that AP2-R4 is 3,300 ohms and AP2-R6 is 270 ohms. AP1 and AP2 provide sufficient gain to saturate X2a or X2b power switches when the proper control inputs are present. Both amplifiers have input impedances of 6,000 ohms and require inputs of 0.2 ma.

The input to AP1 is derived from the external dc input by VS2. When the output of VS2 goes to +2 vdc, the amplifier provides sufficient output to saturate X2a, which then energizes the external power interlock relay, K10. K10 is external to the solid state matrix as defined by system bounds.

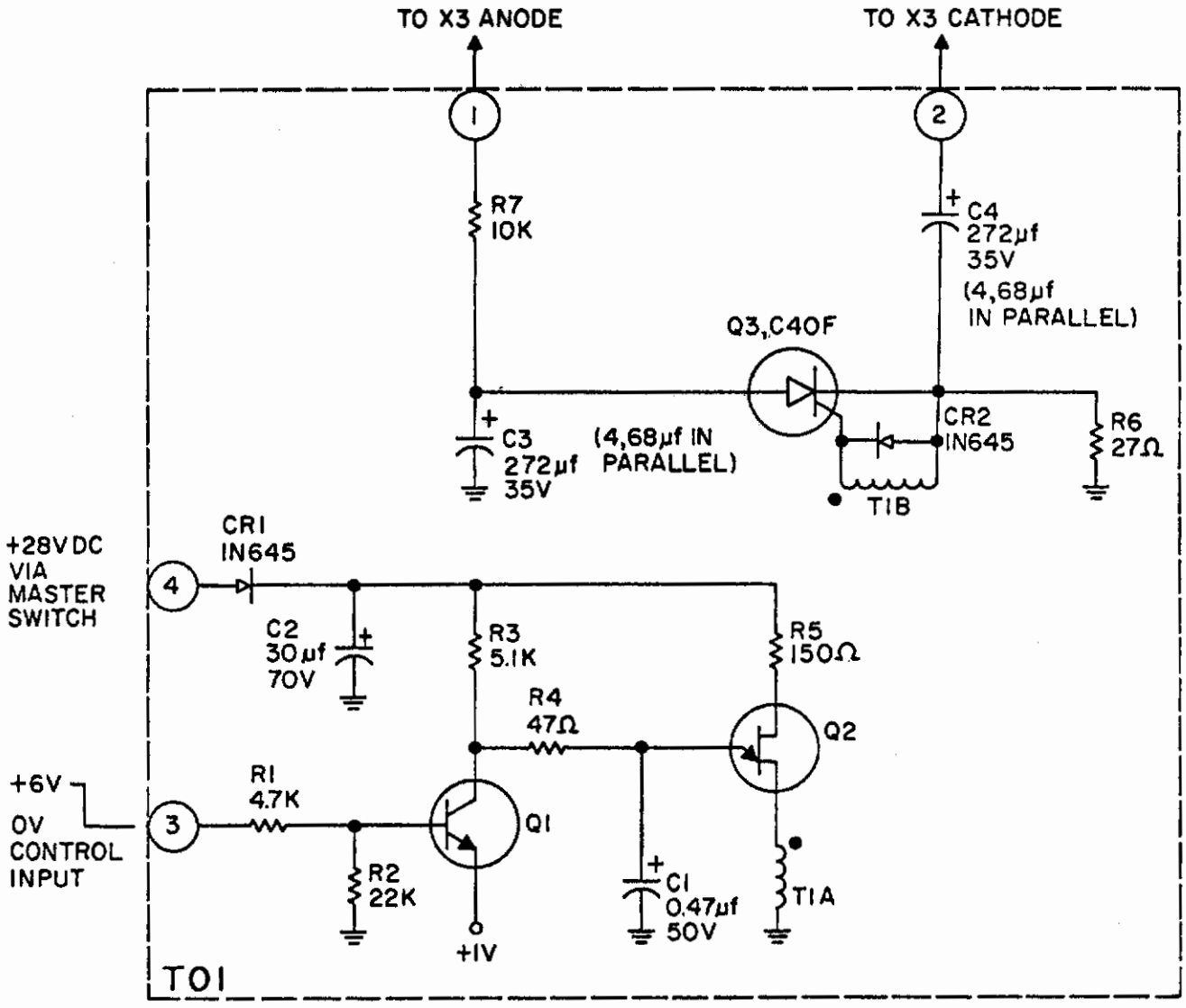
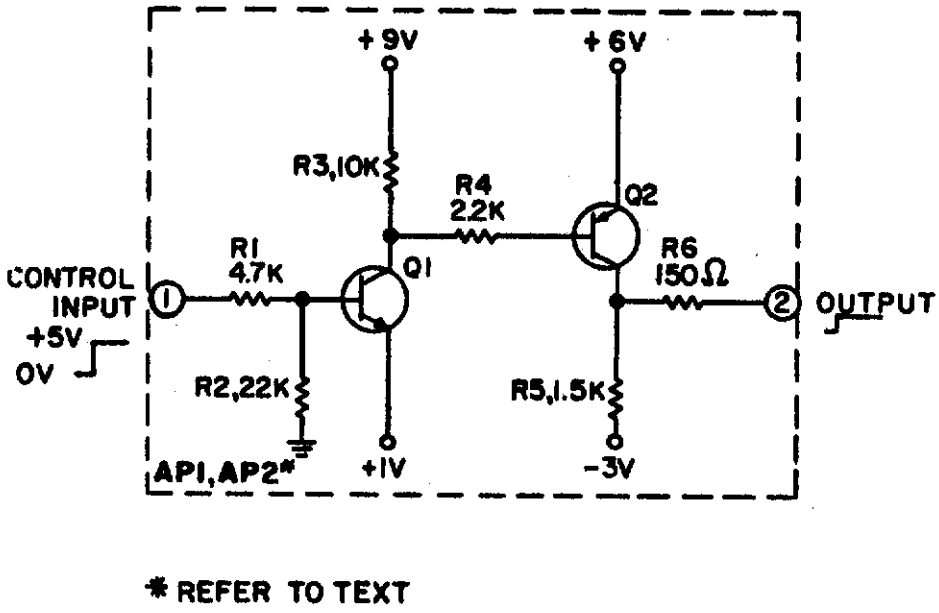


Figure 17. X3 Turn-Off Circuit.



* REFER TO TEXT

Figure 18. Interlock Amplifier

The input to AP2 is derived from VS2 and the generator switch (G). When both of these inputs are less than +0. 3 vdc, AG1 produces an input for AP2. When this input is present the amplifier provides sufficient output to saturate X2b, which energizes the primary generator interlock relay, K11. K11 is external to the solid state matrix as defined by system bounds.

4. 2. 3. 6 Chute Deploy DC Overload Circuit

The chute deploy load requires overload protection. The chute deploy overload circuit consists of a differential amplifier (DA1), a dc amplifier (AP3), a silicon controlled switch connected in a bistable configuration (FF1), a manual reset (MR1), and a driving amplifier (AP4). The schematic of the dc overload circuit is shown in Figure 19; some applicable notes are given in Table 8. During normal operation, the chute deploy load is less than 5 amperes and Q7 is maintained in saturation by AP4. The input to DA1, which is the voltage drop across current sensing resistor, RS, is less than 0. 3 vdc. Q1B of DA1 is conducting due to the 5 ohm bias resistor, R7, in the input voltage divider; therefore, the output voltage from DA1 is less than +9 vdc and Q1 of AP3 is reverse biased. Q2 of AP3 is also reverse biased; hence, no output is present at AP3-2. The output from AP3 is connected to the set input of FF1 and under normal operation Q1 of FF1 is not conducting.

If an overload should occur, causing the voltage drop across RS to exceed 0. 3 vdc, Q1B of DA1 begins to turn off and Q1A begins to conduct. This action causes the output from DA1 to go more positive causing conduction of Q1 and Q2 of AP3. A +3 vdc output becomes available at the set input of FF1 and it fires Q1 of FF1. When Q1 turns on, FF1-3 goes to +2 vdc. This reverse biases Q1 and Q2 of AP4, thereby interrupting the chute deploy circuit.

MR1 is the dc overload manual reset circuit. When S1 of MR1 is closed, C1 and C2 charge and momentarily remove anode voltage from Q1 of FF1. If the overload condition no longer exists, the input to FF1 is no longer positive and FF1 resets. If the overload still exists, FF1 is immediately turned on again to repeat the previously described interrupting action. The charge and discharge times of C1 and C2 of MR1 have two effects. First, it prevents an operator from holding the chute deploy circuit on during overload by holding S1 closed. Second, it prevents repeated resetting without a waiting period between reset attempts.

Since the chute deploy circuit is complex, an alternate circuit has been developed and is shown in Figure 64 of the alternate circuits section of this report.

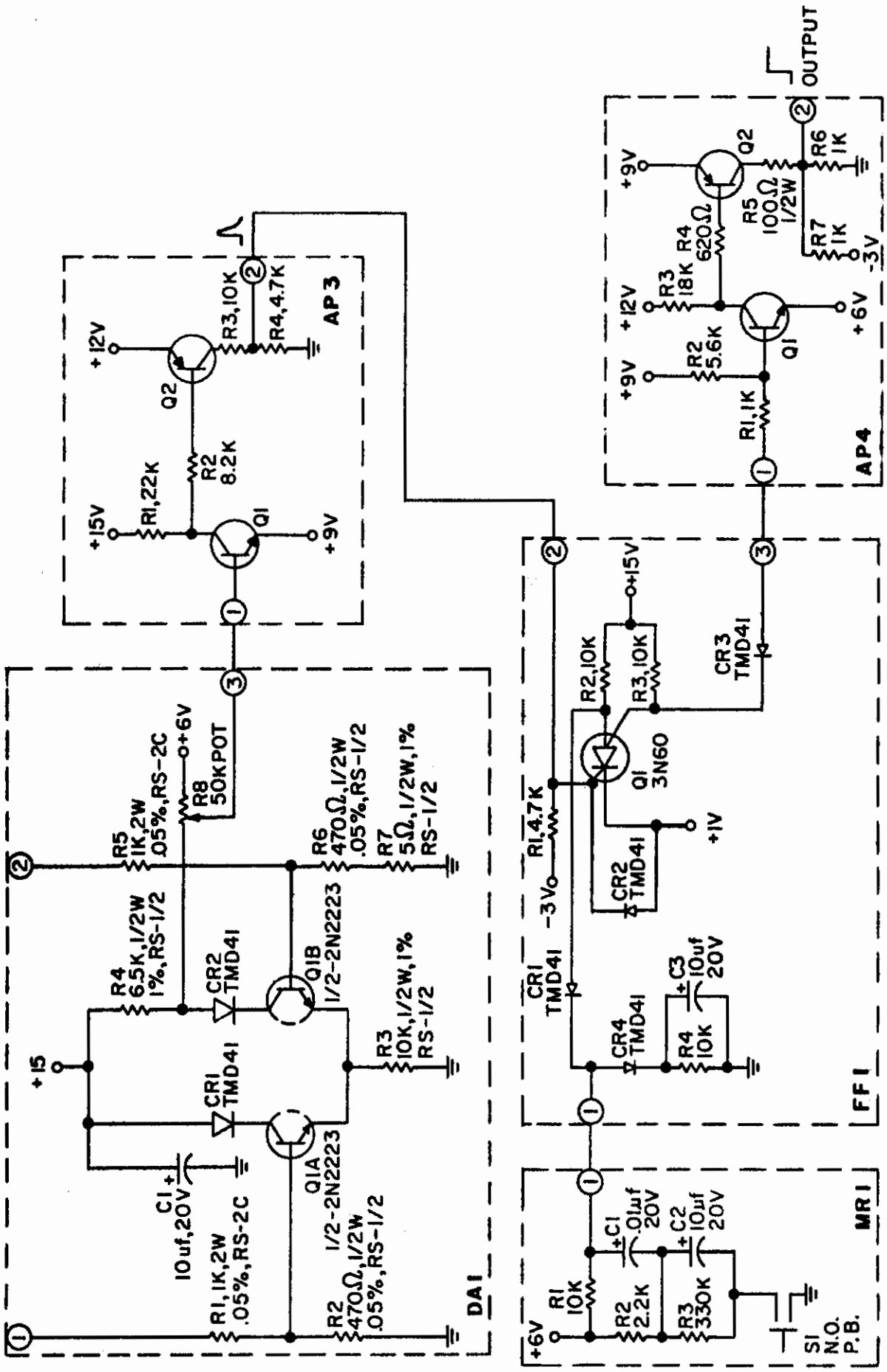


Figure 19. DC Overload Circuits

TABLE 8

Notes Applicable to the DC Overload Circuit

1. $R_s = \frac{300\ MV}{I_{trip}}$ Use Nichrome V, Driver-Harris

Wire Size	56 ohms/Ft at +20°C	I for +200°C and 1.04 x Factor
24	1.61	2A
18	0.41	5A
14	0.16	10A

I_{trip}	Wire	Length	Resistance (ohms)
1.2A	#24	1.9"	0.25
1.6A	#24	1.4"	0.187
2.5A	#24	0.9"	0.12
5.0A	#18	1.8"	0.06
9.0A	#14	2.5"	0.033
10.0A	#14	2.2"	0.030

2. 200 mv drop at I_{rated}; 300 mv drop at I_{trip}.

3. Power requirements

Volts	I (ma)
+15	3
+12	3
+ 9	2
+ 6	6

4.2.3.7 Delay Gate Multivibrator (OS1)

OS1 is a monostable multivibrator which provides a 10 millisecond delay gate. This gate is used to turn off X4 and X5 by removing the TR output voltage for this period. It does this by inhibiting the control input signals to FC2 and FC3. The schematic of OS1 is presented as Figure 20.

When OS1 is in its stable state (no input), Q1 is conducting and Q2 is off, and the OS1 output is +6 vdc. The input to OS1 is either a change from +0.3 v to +5 v or from +5 v to +0.3 v. This input is differentiated by C1, R1, or C2, R2. A negative going change is applied to Q1 base or a positive going change is applied to Q2 base. In either case, Q1 is turned off and Q2 is turned on; this causes the OS1 output to go to +0.1 V. This action is terminated after 10 milliseconds by the charging of coupling capacitor, C3, and the circuit then reverts to its stable state.

4.2.3.8 AC Switch and AC Firing Circuit

Each three phase ac switch shown in the detailed block diagram, Figure 11, is made up of three pairs of C40 SCR's connected in a parallel front to back configuration. These switches are controlled by ac firing circuits which are illustrated in Figure 21. These firing circuits consist of a control transistor, Q1, a 33KC relaxation oscillator, Q2, and pulse amplifiers, Q4 and Q5. When the control input to the firing circuit is zero volts, Q2 oscillates and produces pulses. These pulses are amplified and transformer-coupled to the ac switch gates. Since the period at 33KC is 33 microseconds, a gate pulse will be delivered within 33 microseconds of the time where the SCR anode to cathode voltage passes through zero.

Line commutation is used for ac switch turn-off. In other words, every half cycle one SCR of each pair is reverse biased. If the gate signal should be removed the SCR will not be turned on again during the next half cycle; therefore, the ac switch will turn off in a maximum of one-half cycle. At 400 cps this is 1.25 milliseconds.

4.2.3.9 AC Overload Circuit

The ac overload circuit is made up of current sensors, a level detector, and a flip-flop. It works in conjunction with the ac switch described in the previous section. Refer to Figure 22 for the schematic of the ac overload detection circuits. X8 is the only ac switch which incorporates overload protection. The current sensor is comprised of three current transformers: T13, T14, and T15, and three bridge rectifiers, BR1, BR2, and BR3. Under normal operation, less than 5 amperes per phase flows from the ac essential bus. When this is the case, less than 10 v peak dc is developed at the input to the voltage level

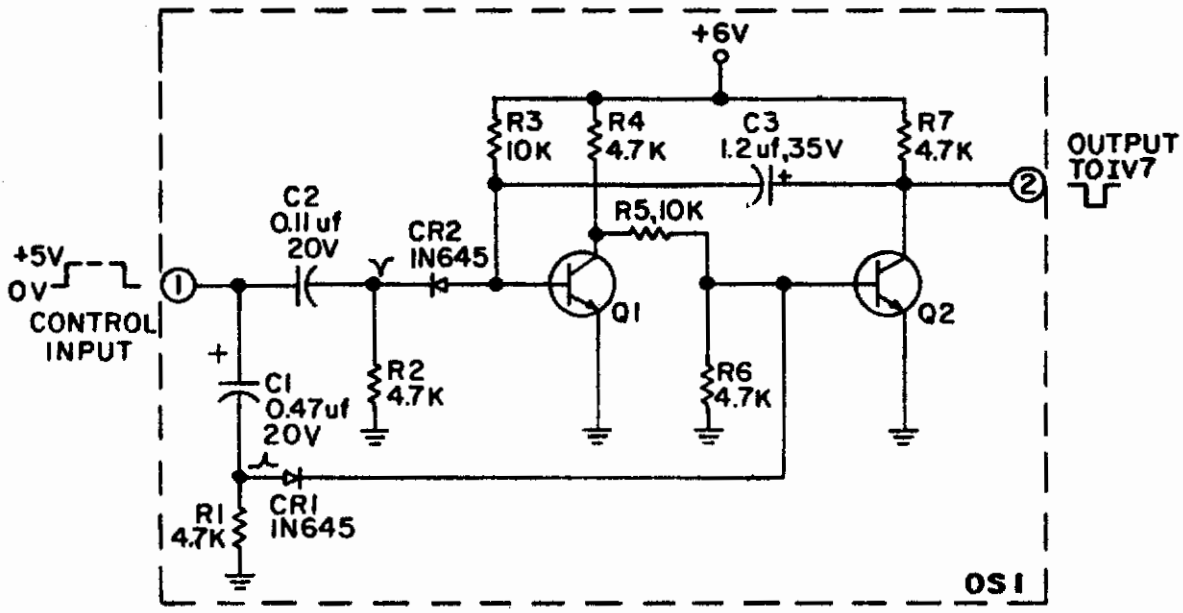


Figure 20. Delay Gate Multivibrator

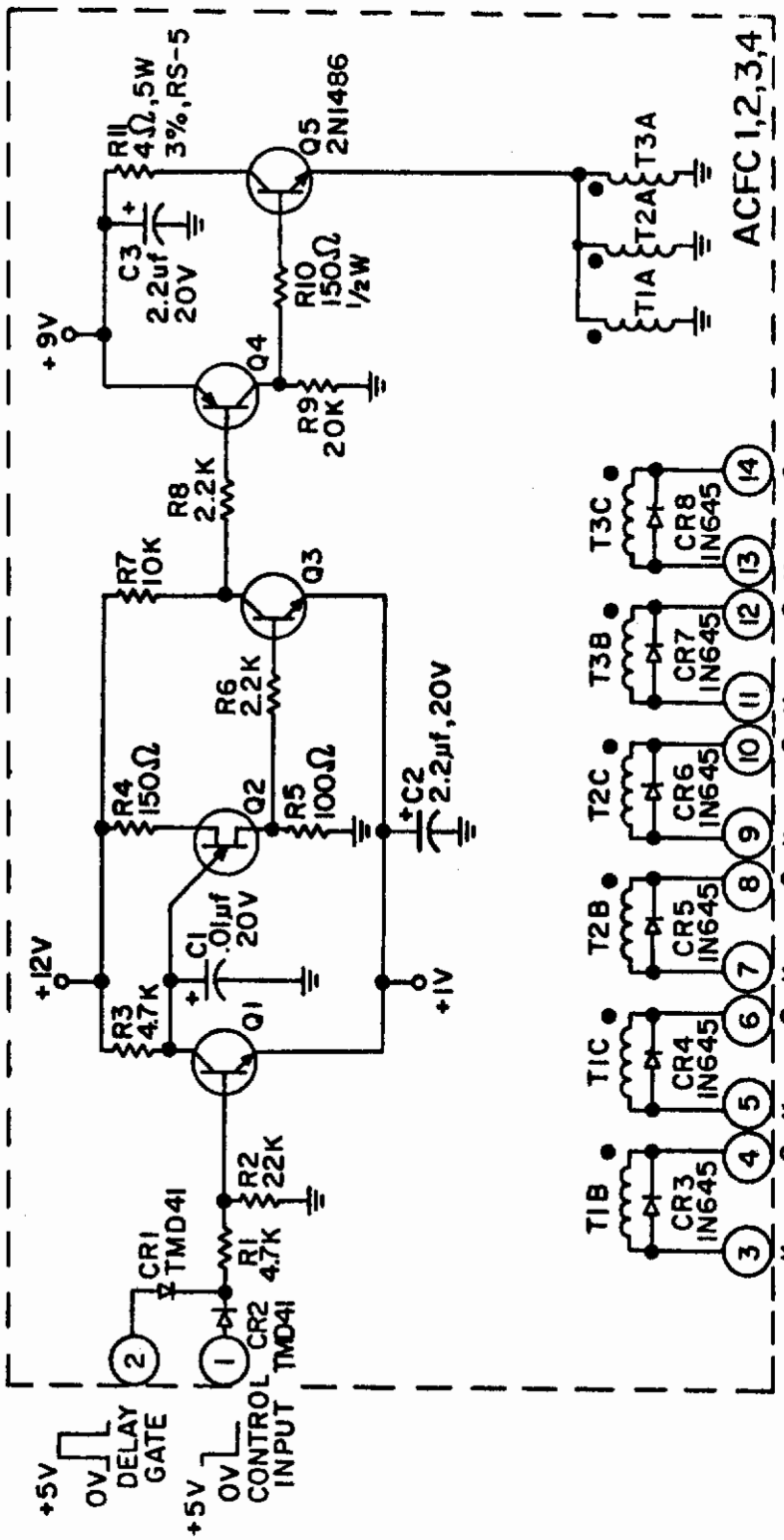


Figure 21. AC Switch Firing Circuit

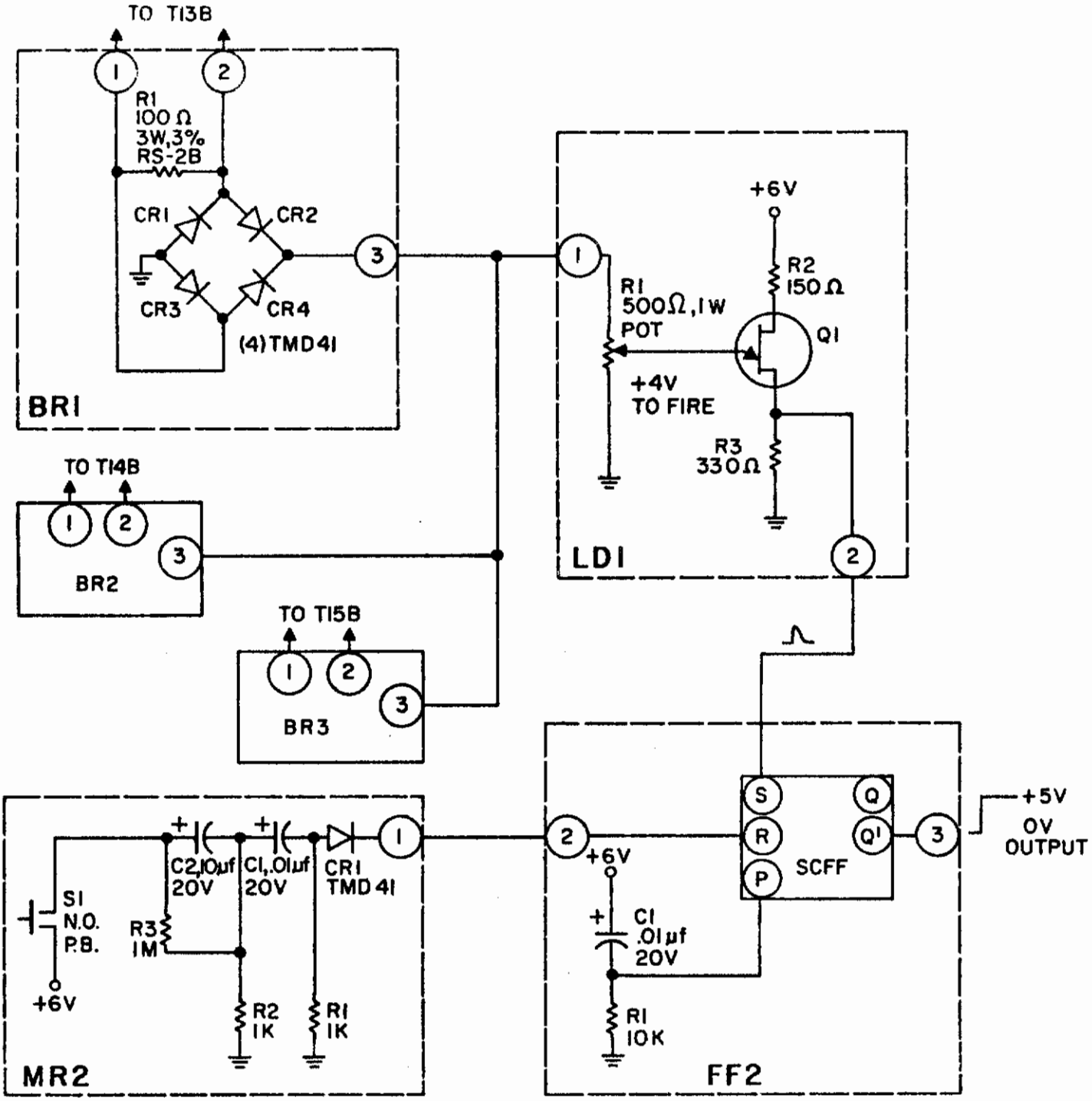


Figure 22. AC Overload Circuits

detector, LD1.

The current transformers which were used were designed and constructed as special transformers. The turns ratio provides approximately a 35 to 1 current step-down; hence, approximately 150 ma flows in the secondary with 5 amps flowing in the primary. This secondary current flowing through R1 develops the voltage which is used as an input to LD1.

The core selected for T13, 14, 15 is made of molybdenum permalloy. The inductance change for this type of core is less than ± 0.75% from -55 to +80° C. The magnetic properties of this type of core will not be damaged by temperature cycling as long as the Curie temperature of the magnetic material is not exceeded. This is well within the temperature requirements.

To further explain the circuit operation, R1 of LD1 acts as a voltage divider and is adjusted so that Q1 of LD1 fires when more than 5 amperes rms flows in any phase of the ac essential bus. If less than 5 amperes flows, there is no output from LD1 to set FF2; hence, there is no inhibit signal to AG5 and X8 conducts normally.

If an overload occurs, the peak voltage developed by BR1, BR2, and BR3 is greater than +10 volts causing Q1 of LD1 to fire, which in turn sets FF2 (input $\overline{N}$). FF2 then provides an inhibit signal to AG5 which allows X8 to turn off by line commutation.

MR2 is the ac overload manual reset circuit. When S1 is closed after an overload has occurred, C1 and C2 charge providing a reset pulse to FF2. If the overload still exists the circuit again trips out; if the overload no longer exists, FF2 remains reset and awaits the next overload signal. The charge and discharge times of C1 and C2 of MR2 have two effects. First, it prevents an operator from holding X8 on during overload, Second, it prevents repeated resetting without a suitable waiting period between reset attempts.

4.2.3.10 Transformer T1 and Bridge Rectifier BR4

T1 is the three phase, Y to Δ, voltage step-down, transformer with tapped primary winding which is used by the original system. Input tap switching is accomplished by X7 and X9. The schematic representation of T1 and BR4 is presented as Figure 23. Inputs 1, 2, and 3 are used when the TR output is +36 vdc for battery charging, Inputs 4, 5, and 6 are used when the TR output is +28 vdc and supplies the dc essential bus. BR4 is a conventional three phase, full-wave, bridge rectifier whose output ripple is less than 4%. Each rectifier conducts for 180 degrees and the average dc current per rectifier is 0.333 x the dc output current, or a maximum of 0.333 x 43A = 14.3 average amperes per rectifier.

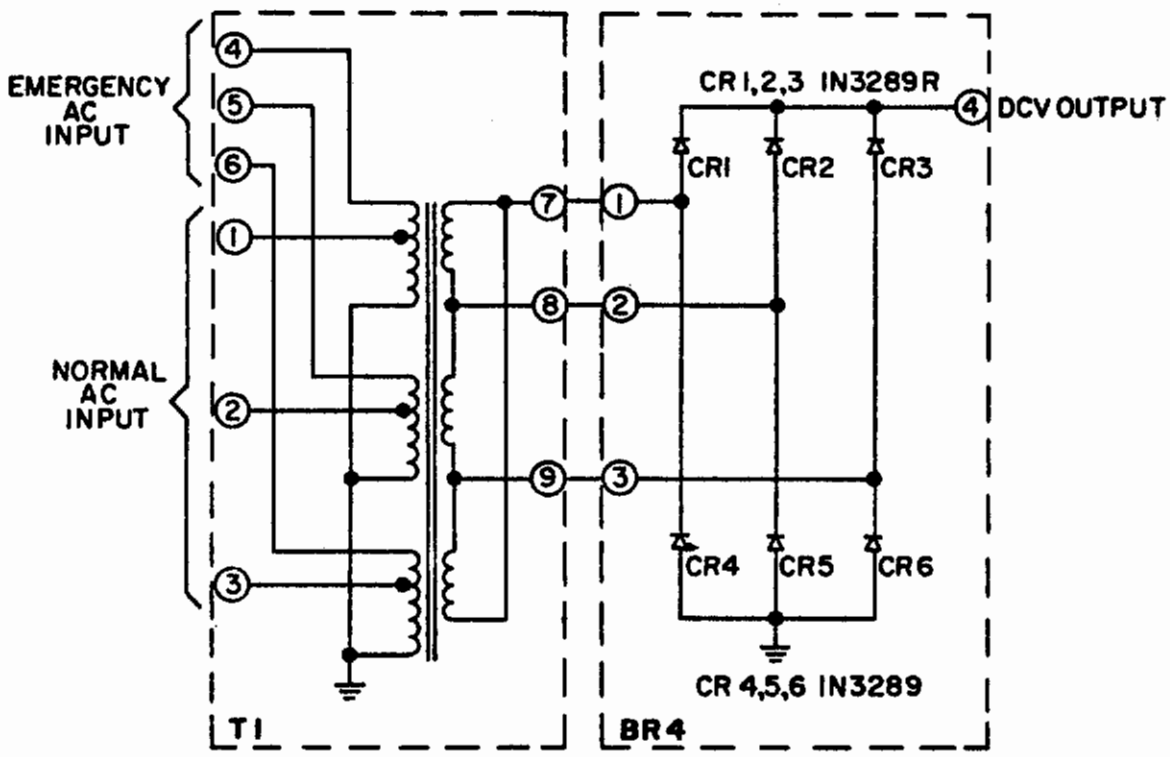


Figure 23. Transformer-Rectifier

4.2.3.11 Power Switches

Both power transistors and SCR's have been used in the dc power system for reasons previously discussed in section 4.1.2. An important consideration in the application of a solid state device is the thermal environment in which it is to operate. Table 9 provides information which was used to select heat sinks for the devices and to determine the feasibility of using any particular device for a particular switching task.

4.2.4 Description of Operation - DC Power System

The DC Power System is a power distribution central which performs the switching of power from four dc sources to either the dc nonessential bus and/or the dc essential bus under normal and various emergency situations. The four sources of dc power are: (1) the primary dc generator, (2) the emergency battery, (3) the transformer-rectifier, and (4) an external source.

Input information is provided to the system from switches, voltage detectors, and current detectors. Certain switch closure and voltage presence conditions cause power handling switches to close or open, thereby distributing power from the correct source to the proper bus.

4.2.4.1 Normal Power-on Sequence

Closure of the master electrical power switches provides the system's regulated dc to dc power supply with dc voltage from the battery. A portion of the system control circuitry then receives its power from this regulated supply. Now the system is prepared to handle its switching tasks. If voltage presence is sensed at F,[1] the external source is activated through a triode power transistor X2a. External power is then applied to the dc essential and nonessential buses from the external supply through isolating diodes.

If external voltage is not present at F, the primary dc generator may be activated by closure of the generator switch (G)[1]. Closure of G and the absence of external voltage at F are the conditions necessary to cause triode power transistor X2b to conduct. This activates the primary dc generator. Power is then applied to the dc essential and nonessential buses from the primary dc generator through isolating diodes, CR4 and CR5. Once voltage is present on the dc essential bus from a source other than the battery, the regulated dc to dc power supply will be supplied from either the battery or the dc essential bus, depending

[1] Refer to Abstract Logic Diagrams, Figures 9 and 10.

TABLE 9

DC Power System Power Switch Thermal Conditions

Switch	$T_{j\ max}$ (°C)	$T_{j\ sel}$ (°C)	P_{dis}[1] (watts)	θ_{jc} (°C/W)	T_{case} (°C)	Max. θ_{ca} (°C/W)
X2a	200	175	0.5	7.0	172	183.0
X2b	200	175	0.2	7.0	173	468.0
X3	150	150	55.0	0.4	128	0.9
X4	150	150	55.0	0.4	128	0.9
X5	125	125	10.0	2.0	105	2.5
X6abc	125	125	3.0	2.0	115	7.0
X7abc	125	125	1.5	2.0	122	28.0
X8abc	125	125	3.0	2.0	115	7.0
X9abc	125	125	3.0	2.0	115	7.0
Chute Deploy (Q7)	150	125	0.5	0.5	121	5.0

Note 1: Power dissipation at maximum load and 80°C ambient.

upon which source is at the highest potential. This is achieved by virtue of the diode arrangement of CR1 and CR2.

With the application of ac power to the ac essential bus, the regulated ac to dc power supply is activated and power is then applied to the ac control circuitry.[2] Under normal conditions, the ac emergency disconnect relay is not in the "Emergency Pwr. On" position ($\bar{D}$); this causes X6 to go to its low impedance state. Also, voltage is present on the dc nonessential bus (A_1); this causes X7 to conduct. Thus, the transformer is supplied from the ac nonessential bus through X6 and X7, which are the normal TR input switches.

X5 is in its low impedance state when the battery is being charged. The conditions required to turn on X5 are power applied to ac control circuits (P), test switch closed (H), and more than +17 vdc on the dc nonessential bus (A_1). Normally these conditions would be present; hence, X5 turns on and the battery is charged from the transformer-rectifier.

4.2.4.2 Emergency Operation

There are four emergency conditions which must be provided for by the dc power system: (1) failure of the primary dc generator, (2) failure of the primary ac generator, (3) failure of both the primary ac and dc generators, and (4) engine failure.

Primary DC Power Supply Failure

If the primary dc generator should fail, voltage is no longer present on the dc nonessential bus and condition $\bar{A}_1$ exists. The input $\bar{A}_1$ to X9 provides control to produce a TR output of +28 vdc, X3 turns on and the battery now powers the dc essential bus. Concurrently, turn-on conditions for X4 have been met and the control signal is conducted to both the SCR firing circuit (FC2) and to the delay gate multivibrator (OS1). OS1 puts out a 10 millisecond turn-off pulse to X6 and X8. Since X6 and X8 are turned off, X4 and X5 are not forward biased for the duration of this pulse so both X4 and X5 revert to their non-conductive states. At the termination of the delay gate, the TR output again goes to +28 vdc and X4 turns on. The three phase bridge rectifier and the battery are now supplying the dc essential bus.

Primary AC Power Supply Failure

If the primary ac generator should fail, the ac nonessential bus becomes

[2] Refer to all circuits below dotted line in Detailed Block Diagram, Figure 11.

inactive and the ac emergency disconnect relay goes to the "Emergency AC Power On" position (D). Since the ac nonessential bus is inactive, X6 is no longer forward biased and so failure of the primary ac generator will stop the battery from being charged.

Failure of Both Primary DC and AC Supplies

If both primary supplies fail, condition D is present once more and voltage is no longer present on the dc nonessential bus ($\bar{A}_1$). Providing the ADC switch is in the "Greater than 280 Knots" position (J), the control signal is no longer present to keep X6 on, so X6 will turn off. With X6 off, conditions are correct for X8 turn-on. The dc essential bus is then supplied by the battery and the TR.

If the airspeed drops below 280 knots ($\bar{J}$), X8 is turned off. Thus, the load is removed from the ac emergency generator and the dc essential bus is supplied from the battery alone.

Engine Failure

If the engine fails in flight and is free to windmill, the TR will be connected to the ac essential bus through X8 as long as airspeed is above 280 knots as mentioned in the preceding paragraph. Under these conditions, the battery and the TR will supply power to the dc essential bus. When airspeed drops below 280 knots, condition $\bar{J}$ is present; this condition would normally mean turn-on of X6 but since the ac nonessential bus in inactive, X6 will not conduct. Under these conditions, the dc essential bus is powered by the battery alone.

4.3 Anti-ice System

The discussion of the anti-ice system is divided into the following three parts: (1) abstract logic; (2) detailed logic; and (3) circuit design.

4.3.1 Abstract Logic

This system is a sequential machine since the output states depend not only on the present input states but also on the history of input states. In particular, there are two critical delays within the system. These are an 18 second (nominal) probe clearing time and a 60 second (nominal) anti-ice cycle time. There is also a 4 second delay memory element in connection with the warning light to prevent premature operation during transient conditions. In order to describe adequately the behavior of the system it is necessary to bring these delay and memory elements explicitly into the description of the system.

Inspection of the original anti-ice schematic shows that the duct lip anti-ice valve and the opening coil of the engine anti-ice valve motor share a common electrical line. Furthermore, the logical conditions for actuating these units are identical to the logical conditions for actuating the radome anti-ice valve, the upper air intake heater, and the lower air intake heater, although all these units are electrically isolated from one another through separate fuses. The logical condition for closing the engine anti-ice valve is the inverse of the condition for opening the valve. The relevant condition depends solely on the output of the ice detector interpreter unit and the setting of the anti-ice switch.

A second independent output of the system is the ice detector probe heater. The condition for starting the probe heater is identical with the condition for actuating the various anti-ice units when the anti-ice switch is in automatic. The probe heater is not operated, however, when the anti-ice switch is in manual nor is it turned off at the same time that the anti-ice period is completed.

A third independent output condition of the system is the actuation of the engine anti-ice warning lights. This condition occurs when the detector probe fails to clear in less than 18 seconds after operation of the probe heater, or when the engine anti-ice valve fails to actuate within 4 ± 1 seconds of the start of an anti-ice period. It also occurs for a number of other circumstances that will be shown in diagrammatic form later in this section.

Of the seven inputs to the system listed in the section on system boundaries, all except the engine anti-ice valve limit switches have logically distinct functions. The valve limit switches serve only to operate the engine anti-ice latch relay. This relay provides logical fan-out capacity for indication of the valve position but does not of itself introduce new logical functions. The essential dc bus enters into the logical network inasmuch as failure of the anti-ice control fuse will operate the warning light if the anti-ice switch is in the manual position. Similarly, failure of the ice detector interpreter fuse on the dc nonessential bus (or total failure of the dc nonessential bus) will operate the warning light if the anti-ice switch is in the automatic position.

Consideration of the sequence of operations shows that a flip-flop-like storage element is required in connection with the operation of the anti-ice equipment. This requirement arises because the conditions for initiation of this operation are not sustained throughout the operation. Similarly, a flip-flop- like storage element is required in connection with the ice probe switch to distinguish between the case when the probe indicates ice continuously and the case when the probe indicates a new formation of ice.

Figure 24 expresses the relationship between the variables in diagrammatic form. Conditions and definitions are presented in Table 10. This diagram is only one of several ways of expressing the logic of the anti-ice system.

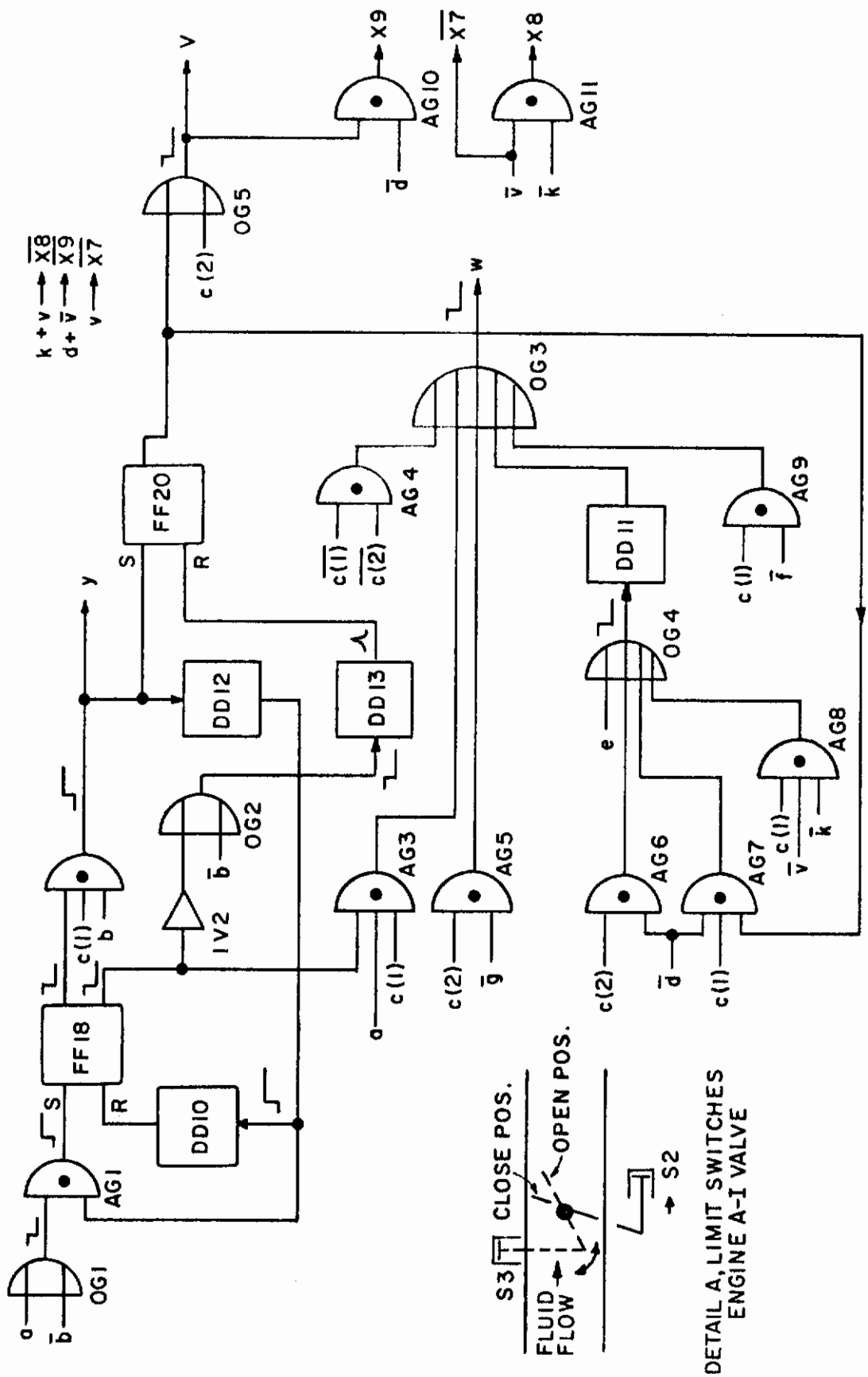


Figure 24. Abstract Logic for Control Circuits of the Anti-ice System.

TABLE 10

Conditions and Definitions for Control Logic

1. Inputs

   a. Ignition relay actuated (PG)

   b. Pressure switch in the ice position (NG)

   c. A-I switch (3 position): (1) auto position (PG); (2) manual position (PG); and (3) off

   d. Limit switch S3 in valve open position

   $\bar{d}$. Limit switch S3 not in valve open position (NG)

   e. Test switch actuated (PG)

   f. Ice detector power available (PG)

   g. A-I control power available (PG)

   k. Limit switch S2 in valve closed position

   $\bar{k}$. Limit switch S2 not in valve closed position

2. Outputs

   v. Energize a-i equipment

   w. Energize a-i warning light

   y. Energize probe heater

   n. Energize case heater

3. X9 as output means a close signal to X9. $\overline{X9}$ as output means an open signal to X9.

4. NG means negative going and PG means positive going.

5. When valve closes fully it makes S2. When valve opens fully it makes S3.

The relationship between this diagram and any circuit that may be developed is purely in the realm of overall logical equivalence. The flip-flop labelled FF18 in Figure 24 is used to remember whether the ice detector interpreter has been reset after icing in the probe. The flip-flop labelled FF20 is used to remember that an anti-ice cycle has started after conditions initiating the cycle have lapsed.

An abstract logic diagram was also developed for the power circuits. This is given in Figure 25 and the notes that apply to it are given in Table 11. This diagram shows the loads which must be switched by the anti-ice system. It divides them into those which are powered from the nonessential bus and those which are powered from the essential bus. Also, it indicates that separate power supplies will be used for the circuitry which operates nonessential bus power switches and that which operates essential bus power switches. This is made necessary by reliability considerations. In fact, a prerequisite for a high reliability switching system is the independence of various parts of the system insofar as possible.

This logical design is intended to reproduce faithfully the action of the original system. No changes have been made in the behavior of the anti-ice system to simplify the logic even though such changes might be operationally acceptable.

4.3.2 Detailed Logic

The detailed logic diagram for the control circuits is presented in Figure 26. It should be noted that $\bar{f}$ was ice detector power not available and $\bar{g}$ was a-i control power not available when converting the original control system into an abstract logical equivalent. When the control system is considered in a more detailed manner, it becomes necessary to make $\bar{f}$ indicate nonessential bus circuit power not available and $\bar{g}$ indicate essential bus circuit power not available.

The detailed logic diagram can be regarded as an expanded version of the abstract logic diagram. The purpose of this expansion was to indicate the specific techniques of circuitization that would be employed to implement the desired functions. Toward this end, the following are shown: (1) the inverters normally associated with the NAND/NOR gates used; (2) resistor and ground connections required by the gates; (3) input switch connections; (4) signal polarities; and (5) division of the overall detailed logic of the control circuits into warning system, ice detector, and (unmarked) essential parts of the system other than the warning system. This division is necessary for proper connection to the appropriate gates of the several power supplies that must be provided.

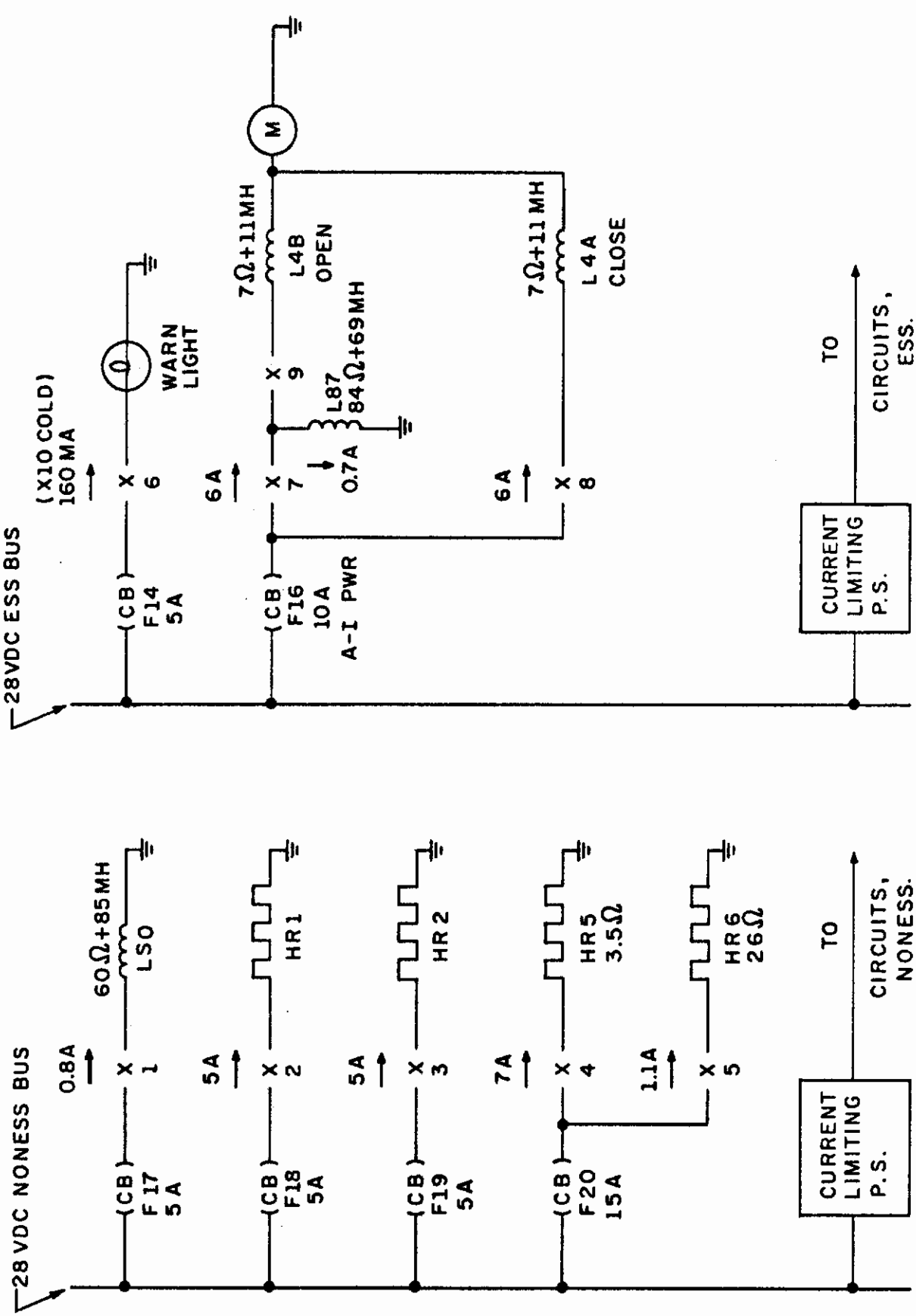


Figure 25. Abstract Logic For Power Circuits of the Anti-ice System.

TABLE 11

Notes - Abstract Logic, Power Circuits

1. Switch Control

Switch	Close	Open
X1	v	$\overline{v}$
X2	v	$\overline{v}$
X3	v	$\overline{v}$
X4	y	$\overline{y}$
X5	+7° C min	+23° C max
X6	w	$\overline{w}$
X7	v	$\overline{v}$
X8	$\overline{v} \cdot \overline{k}$	k+v
X9	$v \cdot \overline{d}$	$d+\overline{v}$

2. X5 closes on decreasing temperature at +7° C minimum and opens on rising temperature at +23° C maximum.

3. Resistances of loads are given for +25° C. At -55° C, the coil resistances will be 30% less because assumed to be copper; but the heater loads will be only 1% less because assumed to be nichrome.

4. Currents shown are maximum values based on -55° C temperature and +31 vdc bus voltage.

5. A-I control fuse (F15) does not appear because it has no direct equivalent in the solid state system.

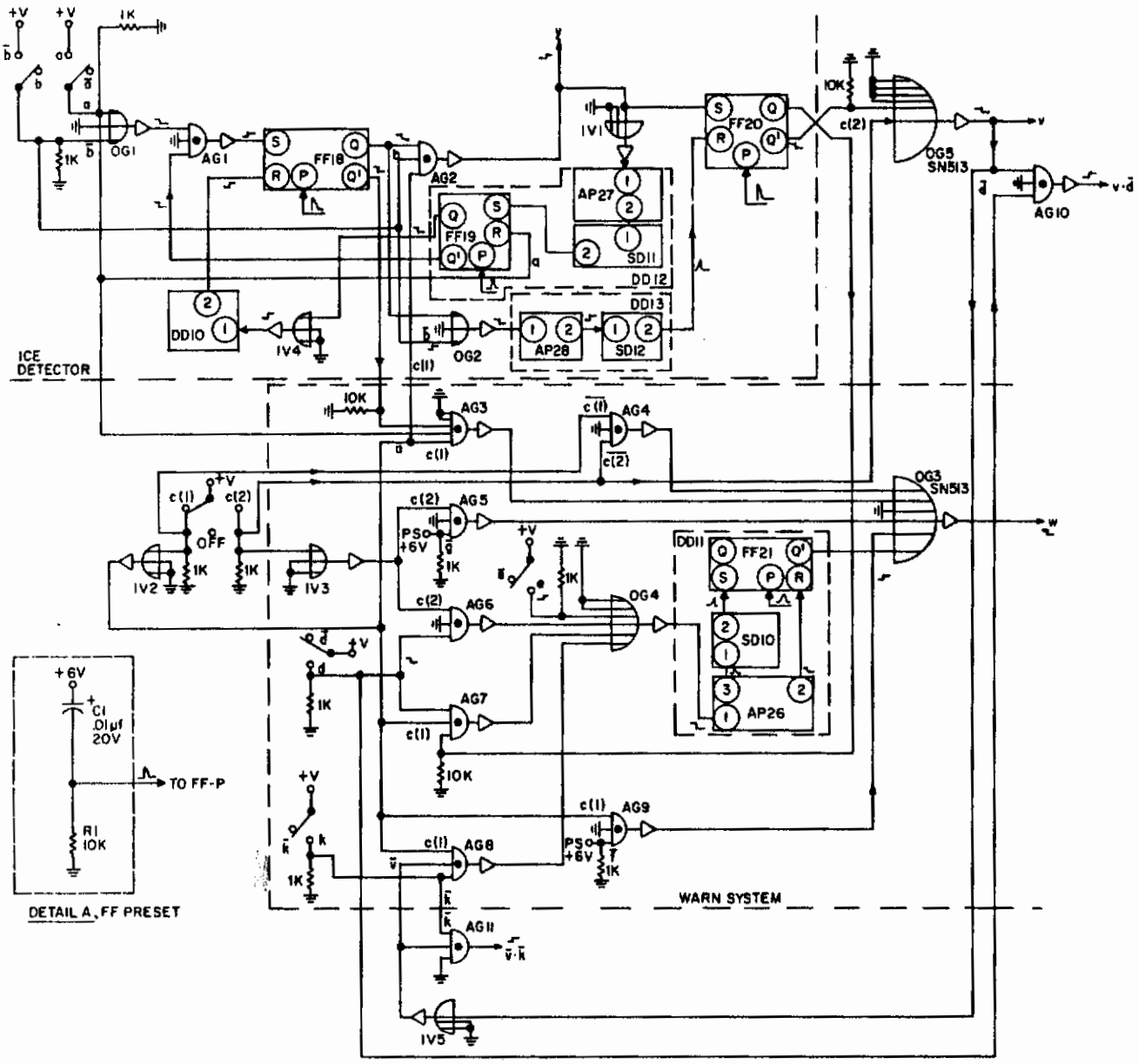


Figure 26. Detailed Logic for Control Circuits of the Anti-ice System.

Referring to the ice detector section of Figure 26, note the inputs a or $\bar{a}$ from the ignition relay and b or $\bar{b}$ from the ice detector switch. Either the input a or $\bar{b}$ prepare the control section of the ice detector for an automatic anti-ice cycle by setting FF18 via OG1 and AG1. The cycle is then initiated by input b at AG2. The output from AG2 is y which energizes the probe heater and also sets FF20. The output Q' from FF20 energizes the anti-ice equipment via OG5 output v. Once the anti-ice cycle is intiated, y exists until input $\bar{b}$ becomes present or 18 seconds has elapsed. DD12 is an 18 second delay which provides an output in the latter case to deactivate the probe heater and energize the warning lights when in the automatic mode or operation, c(1). DD13 is a 60 second delay which is initiated via OG2 at the completion of probe de-ice, $\bar{b}$, or at the end of the 18 second delay period determined by DD12. The output from DD13 resets FF20, thereby removing the output v and de-energizing the anti-ice equipment. Outputs $v \cdot \bar{d}$ (open valve) and $\bar{v} \cdot \bar{k}$ (close valve) are also initiated by the ice detector section since they are dependent upon v and $\bar{v}$. DD10 is a reset delay which only assures that the set signal is removed from FF18 before the reset signal is applied. The ice detector section is inhibited when in the manual mode of operation, c (2), by one of the inputs to AG2; however, OG5 receives an input directly from the anti-ice switch and output v is present as long as as the anti-ice switch is in position c (2).

Referring to the warning system section of Figure 26, note inputs $\bar{a}$ and FF18-Q'. These inputs exist after engine ignition and more than 18 seconds of probe de-icing without satisfactory clearing of the ice detector probe. When these inputs are present while in the automatic mode, AG3 provides an output which activates the warning lights via OG3 output w. The warning lights are also activated when the anti-ice switch is off via AG4 and OG3. If essential bus circuit power is removed while in manual, or nonessential bus circuit power is removed while in automatic, the warning lights are activated due to the outputs from AG5 and AG9, respectively. DD11 is a 4 second delay which has been incorporated in order to provide a warning light signal if the motor-driven valve circuit requires more than 4 seconds for opening or closing the valve. AG6 provides a signal via OG4 which starts the 4 second delay when in the manual mode of operation and the valve limit switch S3 is not in the valve open position. AG7 provides a signal via OG4 which starts the 4 second delay when in the automatic mode of operation and S3 is not in the valve open position. AG8 provides a signal via OG4 which starts the 4 second delay when in the automatic mode of operation and the valve limit switch S2 is not in the valve closed position. The test switch input e also initiates the 4 second delay via OG4. If the input to DD11 remains low for 4 seconds, a set signal is provided to FF21. Output Q' from FF21 activates the warning lights via OG3. If the input to DD11 does not remain low for 4 seconds the warning lights are never turned on and if the input to DD11 should go positive at a time later than 4 seconds, FF21 is reset and the warning lights are de-activated.

The detailed logic for the power circuits is presented in Figure 27. This diagram shows the location of the current sensing resistor, load, and power switch for each load. It also indicates the tripping current for each load as opposed to the normal maximum current. This maximum was computed on the basis of highest bus voltage and lowest ambient temperature. The technique for simulation of the motor-driven engine anti-ice valves is also shown. The purpose of KD10 and KD11 is to delay the closure of d or k switches with respect to the closure of X9 or X8. Thereby, the motor operating time of the actual circuit is simulated. The closure of d or k is fed back to the control circuits to signal completion of valve operation. This causes the appropriate power switch to cease conduction.

The block diagram for the anti-ice system is presented in Figure 28. The power for the circuitry that operates the nonessential bus power switches is developed from one set of power supplies. The power for the circuitry that operates the essential bus power switches is developed from a second set of power supplies. In addition, a further separation occurs between the warning circuit and the other essential bus circuits. A negative 6 volt source has been added and power regulated from it. The presence of such a negative voltage is desirable if leakage is to be minimized. The overload protection technique for the power switches is identical to that used in the dc power system and as described in Section 4. 1. 4 of this report. The anti-ice system used two basic amplifiers to drive the power switches depending upon the power switch load requirements and power switch gain.

4. 3. 3 Circuit Design

The following circuits have been designed to accomplish the control and switching tasks set forth in the previous sections and in the system specification.

4. 3. 3. 1 Power Supplies and Regulators

In order to improve reliability, the anti-ice system makes use of separation and redundancy in its power supplies and regulators. Power for the nonessential circuits is derived from the nonessential bus via VR14, VR13, and likewise power for the essential circuits is derived from the essential bus via VR10, VR11, VR12. Additional separation exists in that a separate regulator is used for the essential warning lights.

Since the power supplies used in the anti-ice system are basically the same as those of the dc power system, refer to Section 4. 2. 3. 1 for an explanation of regulator operation, and to Figures 12, 14, and 29. VR1 of the dc power system is the same as VR10 and VR14 of the a-i system except for the following: in VR10 and VR14, R1 = 10 ohms, 3%, RS-7; R6 = 300 ohms, 3%,

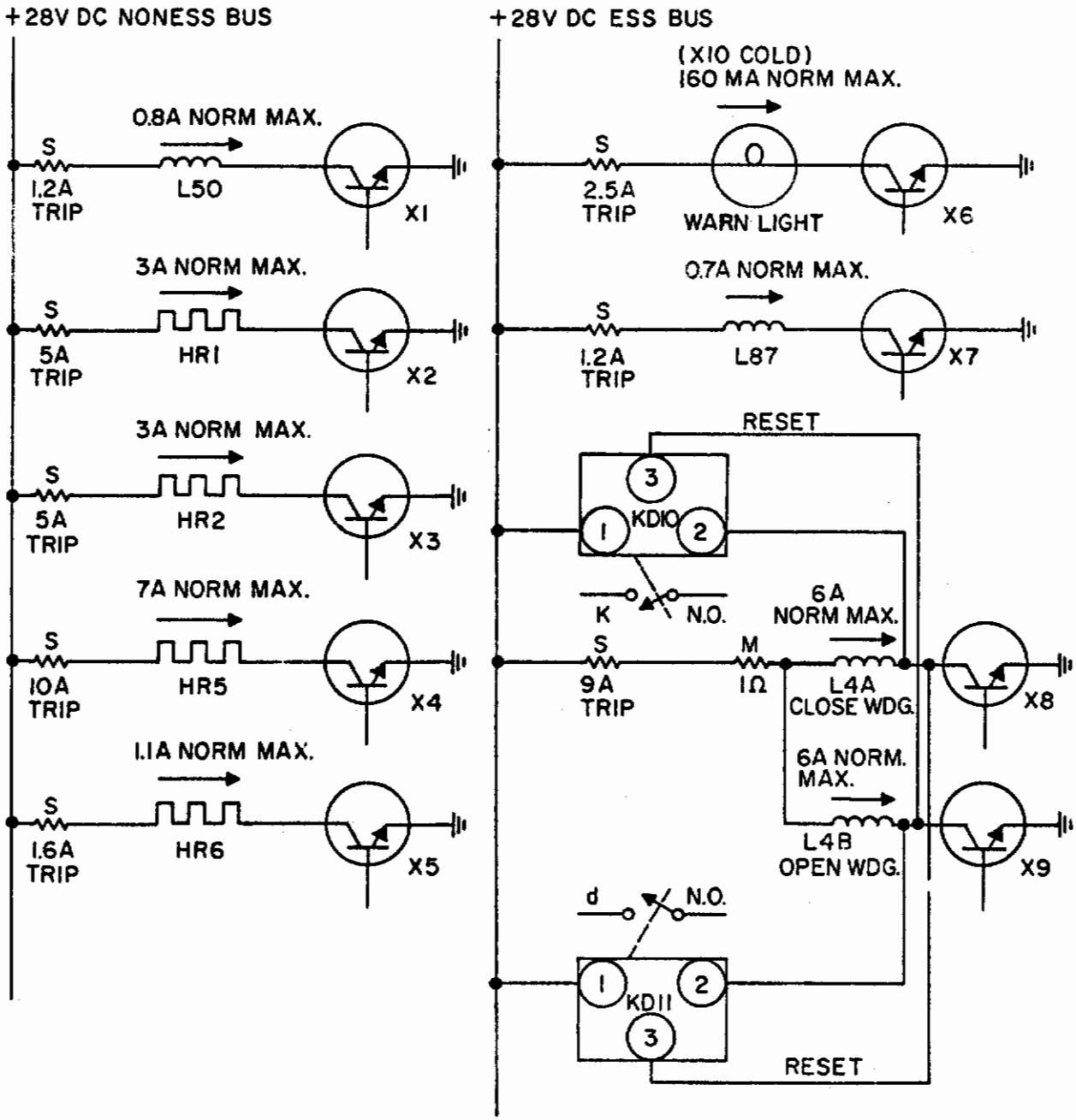


Figure 27. Detailed Logic for Power Circuits of the Anti-ice System

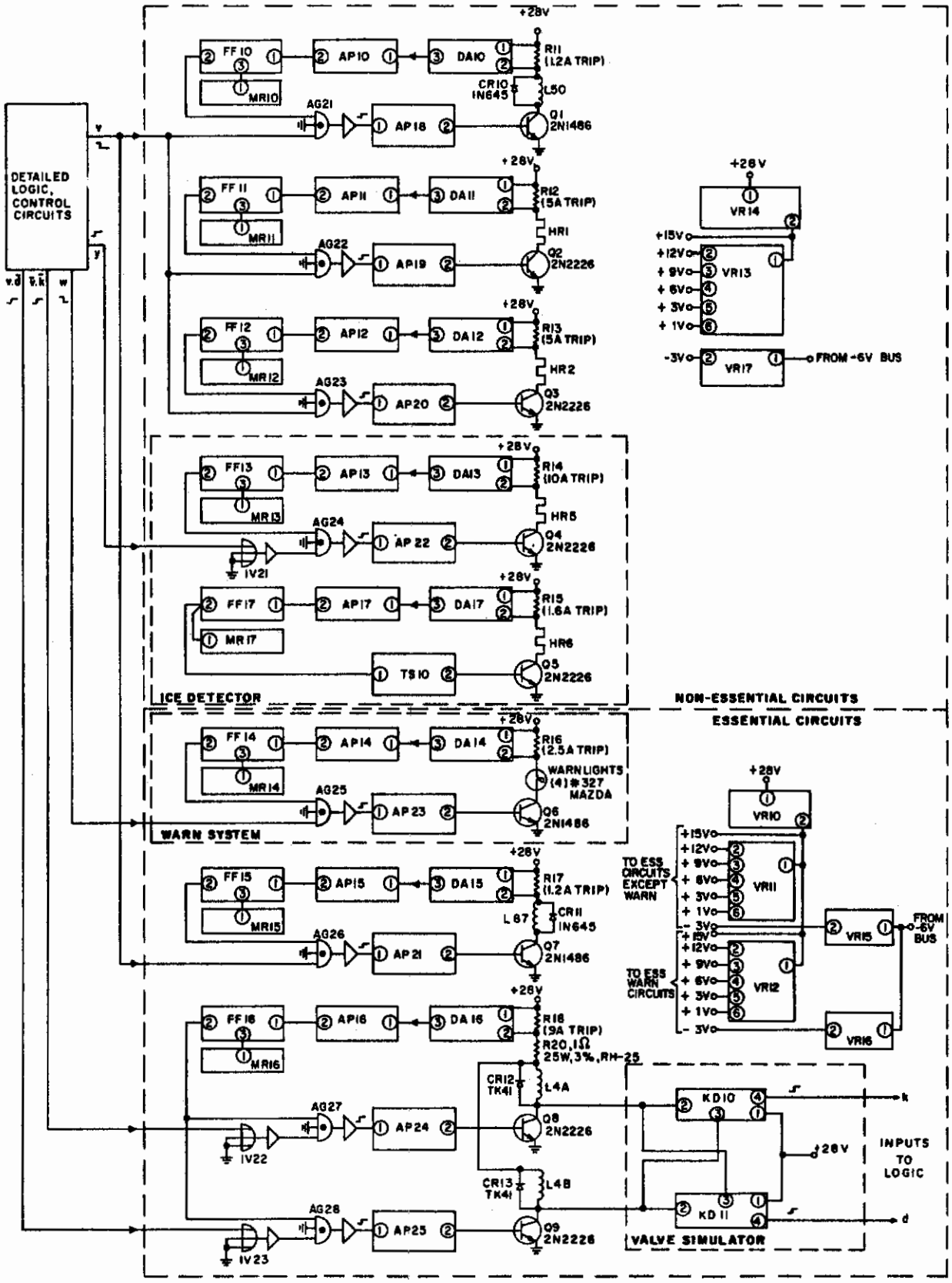


Figure 28. Block Diagram of the Anti-ice System

RS-2B; and CR1 is a 1N750A. VR15 and VR17 are identical to VR3 of the dc power system while VR16 only differs in that R1 = 220 ohms. Note that in Figure 29, VR12 differs from VR11, 13 in R3 = 40 ohms, 3%, RS-2B because the +9 volt output requirement is 100 ma rather than 600 ma.

The total power requirements for the anti-ice system circuitry are given in Table 12. The requirements are given separately for the essential bus circuits and the nonessential bus circuits. In addition, the essential bus circuit requirements are further divided into those for the warning circuits and those for the other circuits. This divided listing is in accordance with the sectional arrangement of power supplies that was previously presented. Thermal conditions for the a-i regulators are presented in Table 13.

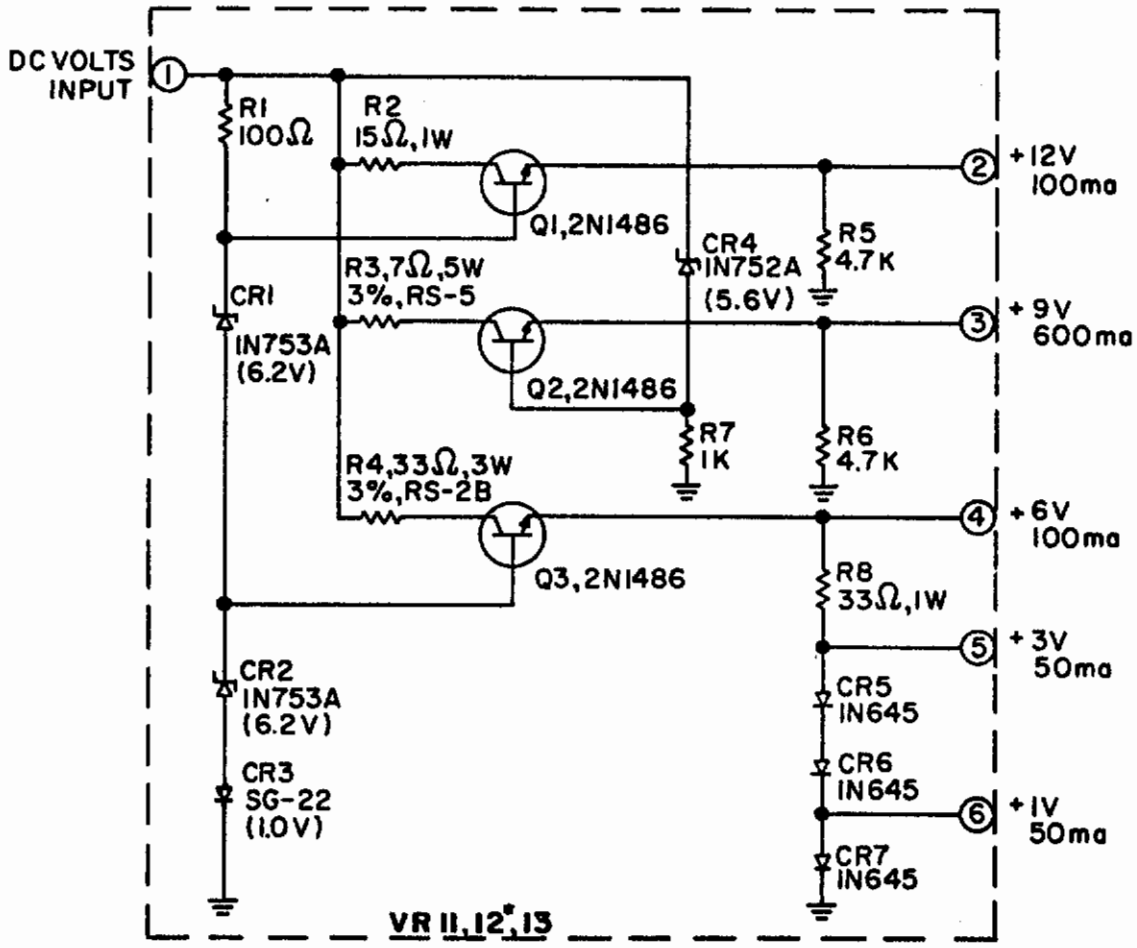
4.3.3.2 DC Overload Circuit

The schematic of the dc overload circuit has been presented in Figure 19. Refer to Section 4.2.3.6 for detailed information concerning the differential amplifier and the following dc amplifier operation. The only difference between the anti-ice overload circuit and the dc power system is the bistable element. The bistable element used in the anti-ice system is presented in Figure 30. In the dc power system a silicon controlled switch is used while in the anti-ice system a Solid Circuit flip-flop is used except in the case heater overload circuit. Here an SCR is used in an attempt to simplify the bistable element.

4.3.3.3 Delay Circuits

The delay circuits are shown in Figures 31 and 32 and in block form in Figure 26. DD11, 12, and 13 use basically the same circuit. Each of these delay circuits receives an input from a Solid Circuit gate or inverter. This input is amplified and inverted by a three stage amplifier. Thus, a negative going input produces a positive going output signal to the special delay circuit (SD). This causes the timing capacitor to charge via the timing resistors. If the negative input signal is present for a longer time than is required to charge the capacitor to the unijunction's peak point voltage, then a pulse is produced by the unijunction.

DD11 is the 4 second delay and consists of AP26, SD10, and FF21. If DD11 receives a negative going input which remains for 4 seconds, a positive output is produced which activates the warning light system. If the input should go positive at some time after the 4 second delay, FF21 is reset by a reset pulse from AP26 and the warning light system is deactivated. DD12 is the 18 second delay and consists of AP27, SD11, and FF19. If DD12 receives a negative going input which remains for 18 seconds, a positive going inhibit output and a negative going reset output are produced. These outputs are used to de-energize the probe heater and to activate the warning light system. The



* Refer to text

Figure 29. Voltage Regulators (VR 11, 12, 13)

TABLE 12

Power Requirements for the Anti-Ice Systems

	Current in MA		
	Essential Bus		Nonessential Bus
Volts	Warning Circuits cc and pc	Other Circuits cc and pc	cc and pc
+15	16	12	72
+12	14	26	80
+ 9	62	466	400
+ 6	66	42	70
+ 3	0	0	18
+ 1	6	3	14
- 3	6	45	64
Total	170	621	718

Note: cc - control circuits; pc - power circuits.

TABLE 13

Regulator Thermal Conditions

	Unit	T_j max (°C)	T_j sel (°C)	P_{dis} (watts)	θ_{jc} (°C/W)	T_{case} (°C)	Max θ_{ca} (°C/W)
VR10, 14	Q1	150	125	30	0.5	110	1
	Q2			Not Applicable			
	Q3			Not Applicable			
VR11, 12, 13	Q1	200	175	0.2	7.0	173	93
	Q2	200	175	1.2	7.0	165	85
	Q3	200	175	0.4	7.0	172	92

Note: Dissipation shown for VR10, 14 Q1 is for shorted output. Dissipation shown for other transistors is at full rated load (T_a = +80°C).

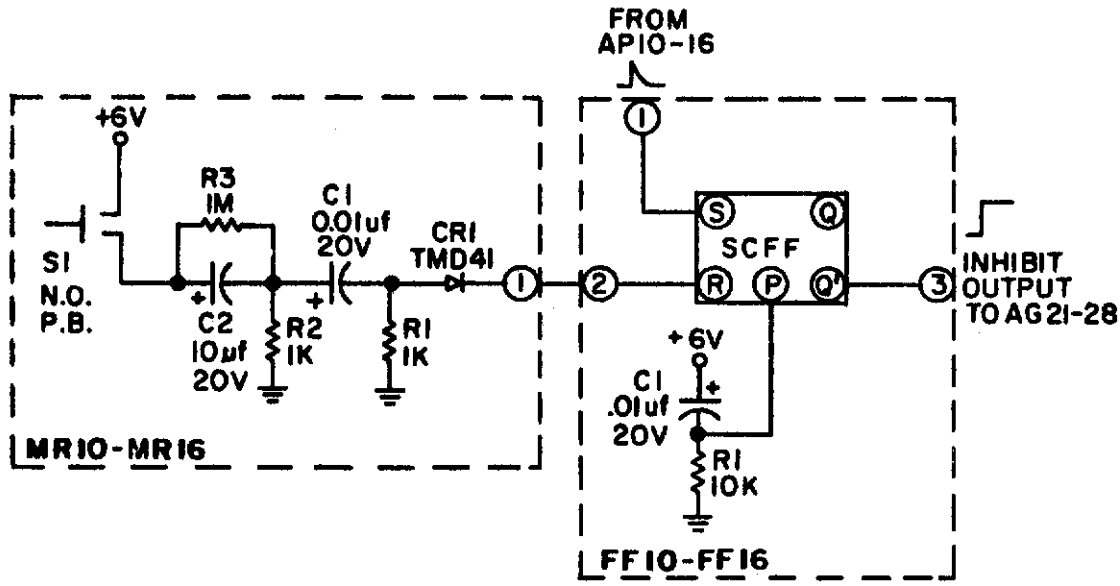


Figure 30. Anti-ice Overload Flip-Flop and Manual Reset Circuit

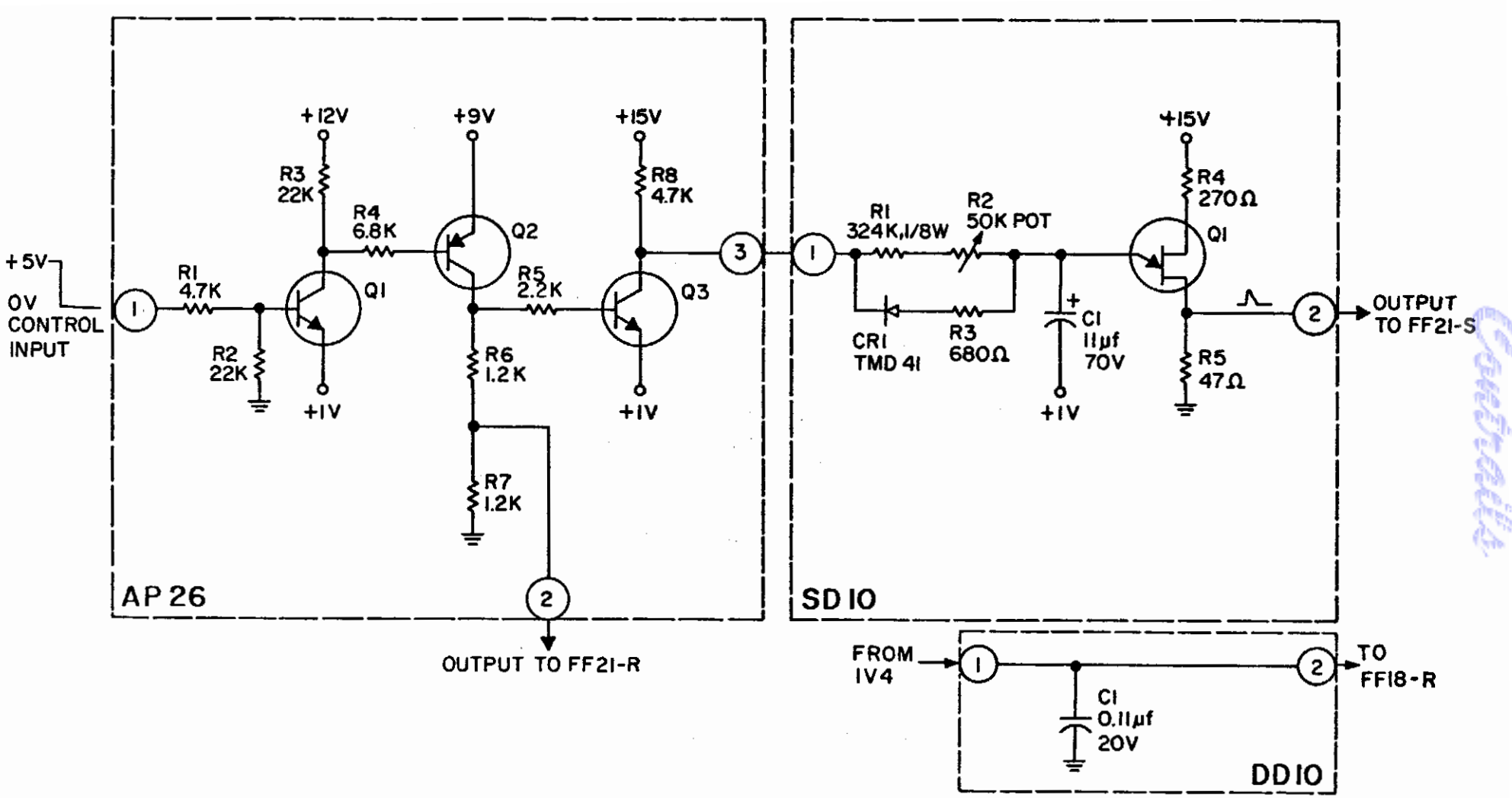


Figure 31. Four Second Delay and Reset Delay Circuits

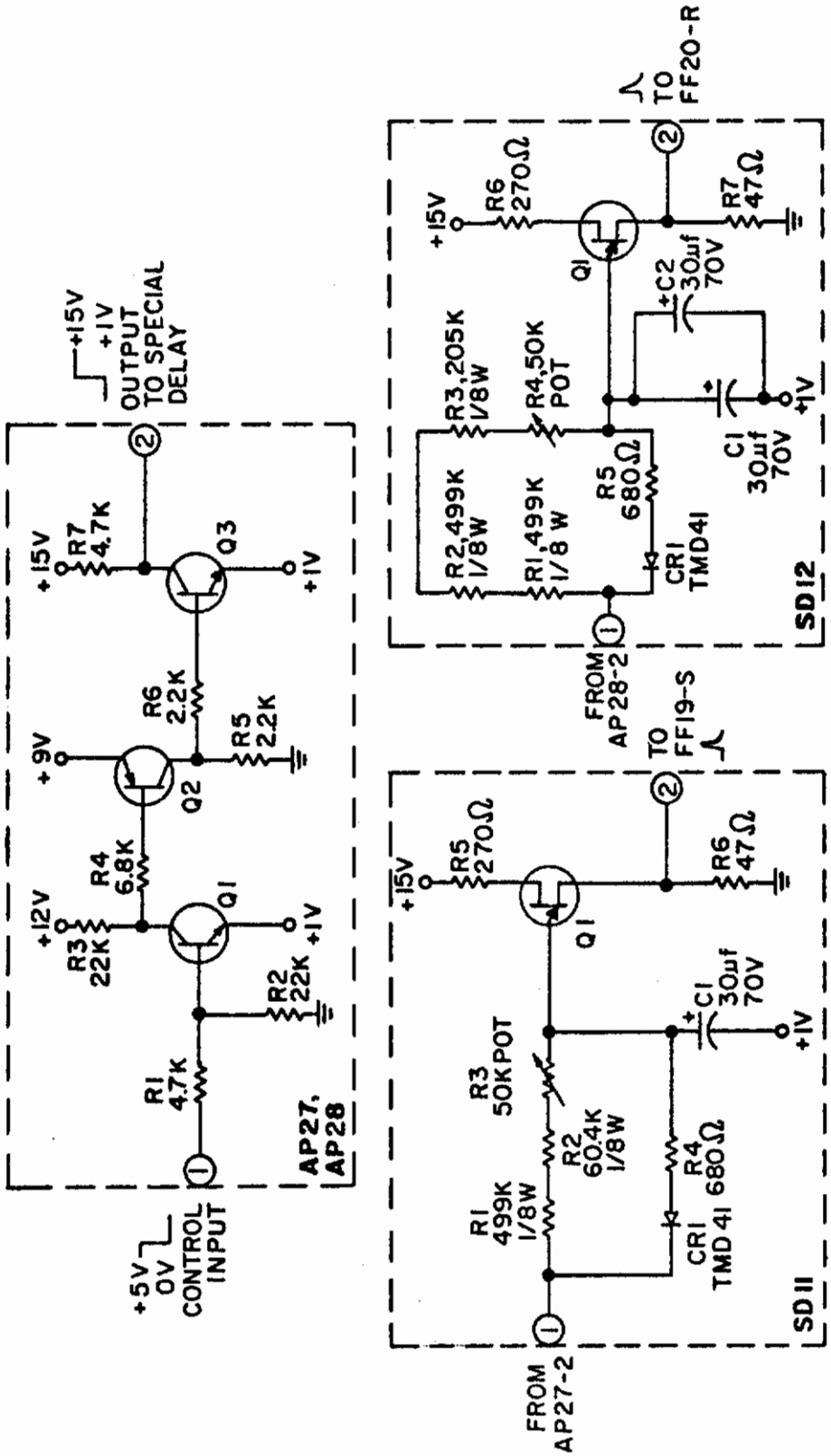


Figure 32. Eighteen and Sixty Second Delay Circuits

reset input to DD12 comes from the ignition input rather than from the input to the amplifier as was the case with DD11. DD13 is the 60 second delay and consists of AP28 and SD12. After the negative going input to DD13 has remained for 60 seconds a positive output pulse is produced which resets FF20, thereby deactivating the anti-ice equipment. DD10 provides a short delay in the order of 50 microseconds to provide time for the inhibit signal to be applied to AG1 before the reset signal is applied to FF18.

4.3.3.4 Case Heater Temperature Sensor, TS10

The schematic of the temperature sensor control circuit is shown in Figure 33. It provides temperature sensing and control for the case heater power switch, Q5. RT1 is a thermistor which functions as a temperature sensitive element. It is part of a voltage divider which provides bias to a two stage amplifier, Q1 and Q2. The input amplifier is necessary because the unijunction input current requirement when operating in the bistable mode (past the valley point on the characteristic curve), was in the order of 15 to 20 ma. This current, if allowed to flow through the thermistor, will cause serious self-heating problems and tend to produce an unstable situation. If the case temperature falls below $+15^{0}$ C, the resistance of RT1 becomes large enough to forward bias the base-to-emitter junction of Q1. When Q1 conducts, Q2 is allowed to conduct causing Q3 to fire. When Q3 fires, Q5 is switched into saturation. The case heater is then supplied with power. This condition is maintained until the resistance of RT1 decreases sufficiently to turn off Q3 and Q5. This occurs at approximately $+20^{o}$ C.

4.3.3.5 Motor-driven Valve Simulation

Figure 34 shows a circuit which was used to simulate the operating time of the motor-driven valve. KD10 and KD11 are identical circuits. KD10 provides simulation for valve closed information and KD11 provides simulation for valve open information. The schematic of this circuit and the anti-ice block diagram form the basis for the following discussion of operation.

When +28 vdc is initially supplied to the system, $\overline{v}$ and $\overline{k}$ are present; therefore, the valve close switch (Q8) conducts and the control input to KD10-2 becomes low, while the control input to KD11-2 remains at +28 vdc. Q1 of KD10 does not conduct so C1 begins to charge toward the peak point of Q2. The charging time of C1 is determined by the RC time constant made up of C1, R4, and R5. This time can be varied with R5 from 1 second to 10 seconds.

When C1 has charged to a potential equal to the peak point voltage of Q1, Q1 fires and energizes K1. Actuation of K1 causes KD10-4 to go to +6 vdc which is the k input to the system. KD10-3 is already at +28 vdc; hence, K1 is held in the actuated position. Since input k (valve closed) now exists instead

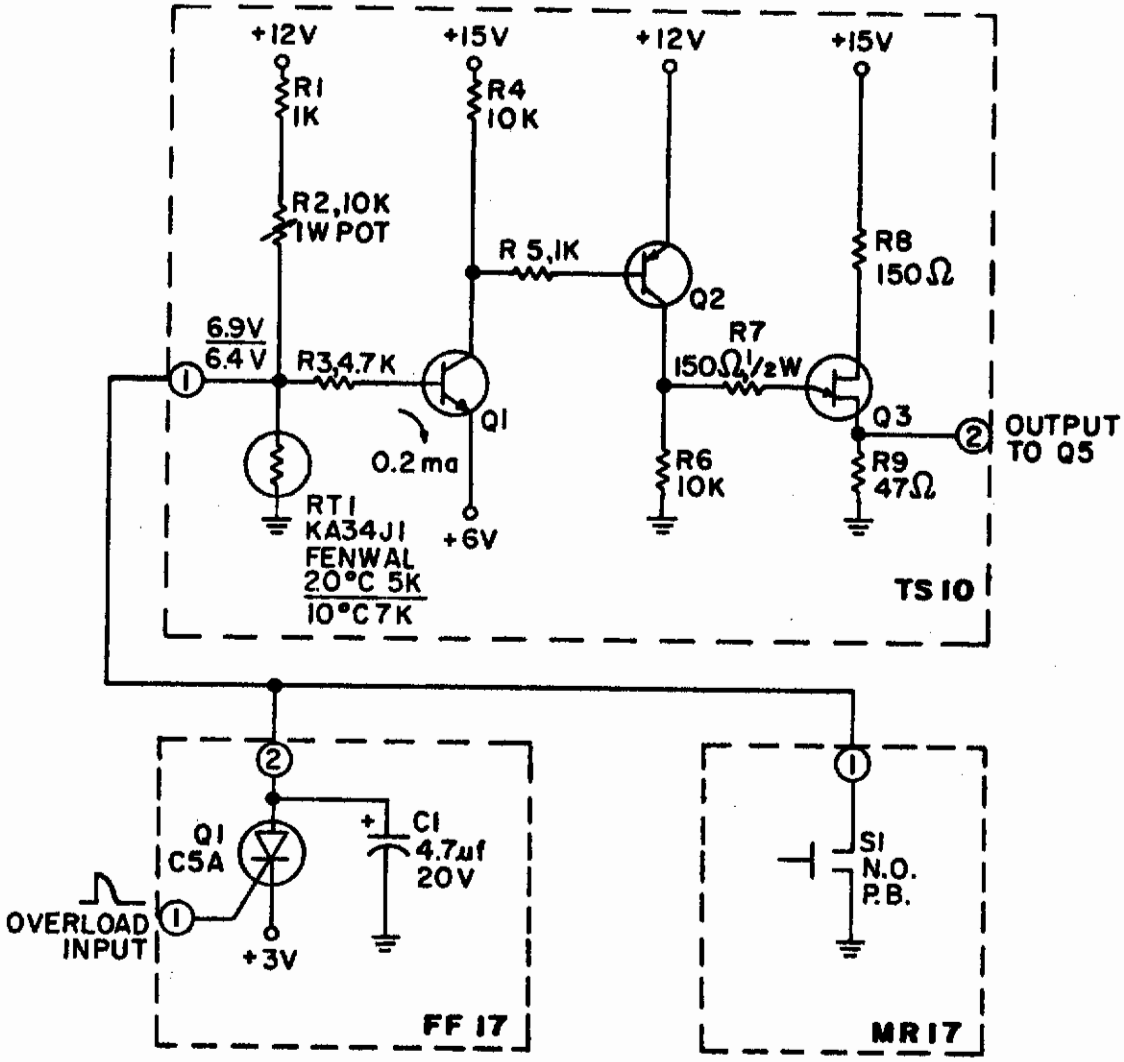


Figure 33. Temperature Sensor with Overload Flip-Flop and Reset Circuits

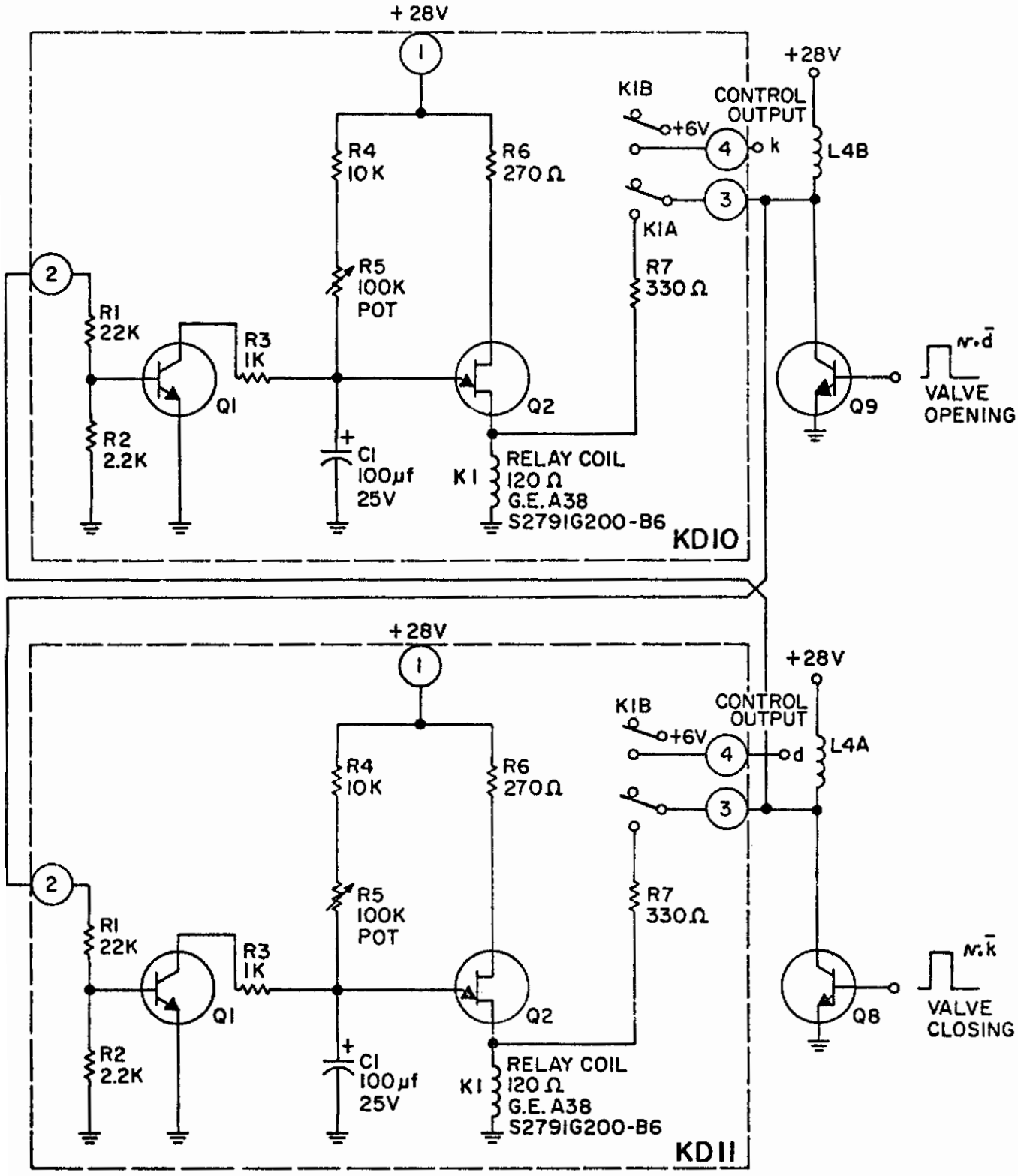


Figure 34. Simulation of Motor-driven Valve Operation

of $\bar{k}$, Q8 is turned off and KD10-2 goes to +28 vdc causing Q1 of KD10 to conduct. As long as Q1 conducts, the emitter of Q2 is held below the peak point voltage required to fire Q2.

The circuits now remain in this stable state where KD10-K1 is energized and KD11-K1 is not. Now suppose that condition v becomes present. Since KD11-K1 is not actuated, condition $\bar{d}$ is also available. Inputs v and $\bar{d}$ are the conditions necessary for conduction of Q9, valve open switch. When Q9 conducts, KD10-3 and KD11-2 go to approximately +$\bar{1}$v. This removal of +28 v at KD10-3 unlatches KD10-K1; therefore, k goes to $\bar{k}$. The input at KD11-2 turns off KD11-Q1 permitting KD11-C1 to start charging. When C1 reaches the peak point voltage of Q1, Q1 conducts and energizes KD11-K1 causing $\bar{d}$ to change to d. This turns off Q9; hence, KD11-K1 is latched in. The circuits are now in their other stable state. In effect, these two circuits simulate the three possible states of the motor-driven valve which are: (1) valve closed, (2) valve open , (3) valve not open or closed. The first two states are the previously mentioned stable states and the third is the charging times of KD10-C1 and KD11-C1, depending upon whether the valve is opening or closing.

4.3.3.6 Power Switches and Associated Driving Amplifier Circuits

The anti-ice block diagram shows the relationship between the control circuits and the power switches. AP18 through AP25 are interface amplifiers which provide sufficient gain to drive the power switches into saturation when the proper control signals are present. Refer to Figure 35 for the schematic of AP18-21. AP22-25 differs from this in that R6 is 3, 300 ohms R8 = 33 ohms (3%, RS-5), and Q3 is a 2N1486. These amplifiers present an input impedance of 6, 000 ohms to the control circuits and provide a current gain of 300 in the case of AP18-21 and 750 in the case of AP22-25.

In some cases more than one power switch amplifier operates from the same control input. However, the overload protective circuits provide separate inputs to their respective circuits through AND gates so that an overloaded power circuit is cut off, regardless of the state of the control input. The amplifier power requirements are presented in Table 14 and the power switch thermal conditions are presented in Table 15.

4.3.4 Description of Operation

The anti-ice system can be thought of as having two modes of operation, automatic and manual, and an off condition depending upon the position of the anti-ice switch. The following sections describe the operation of the anti-ice system under normal conditions and warning light operation.

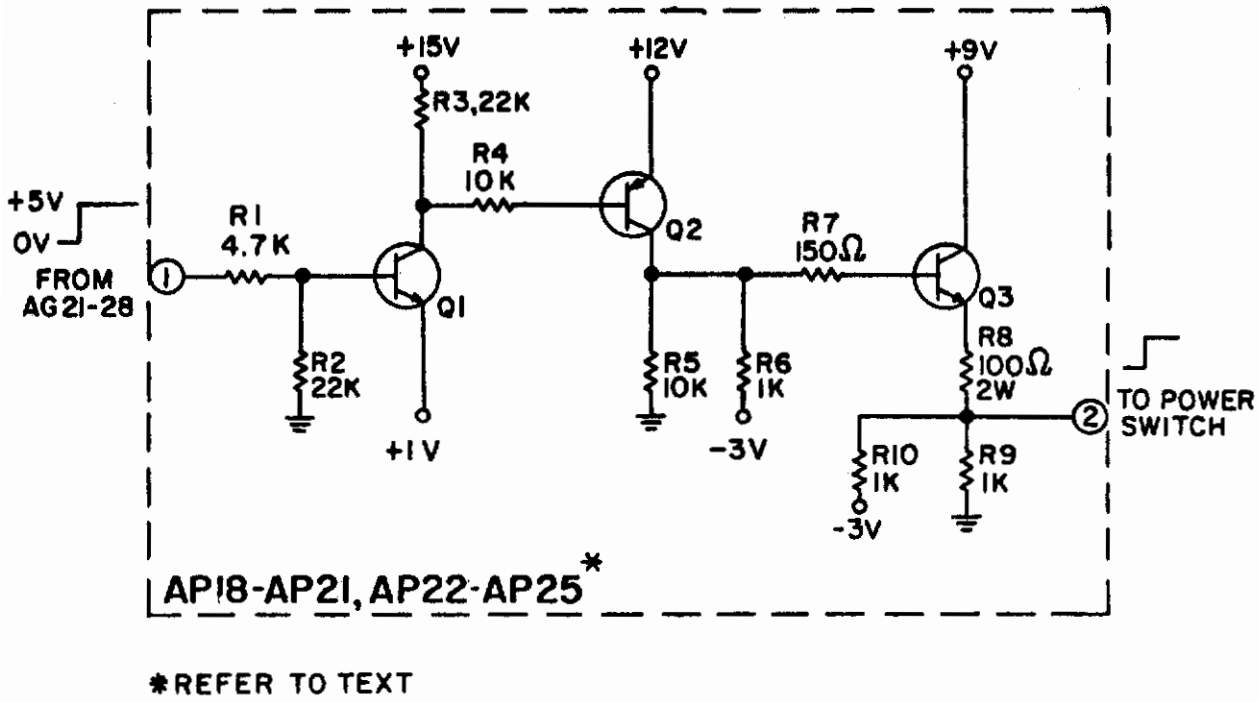


Figure 35. Power Switch Driving Amplifier

TABLE 14

Amplifier Power Requirements (AP18-25)

Volts	I_{load} (MA) Amplifiers AP18 - 21	I_{load} (MA) Amplifiers AP22 - 25
+15	1	1
+12	15	1
+ 9	60	200
+ 1	1	1
- 3	15	15

TABLE 15

Anti-ice Power Switch Thermal Conditions

Switch	$T_{j\ max}$ (°C)	$T_{j\ sel}$ (°C)	P_{dis} [1] (watts)	θ_{jc} (°C/W)	T_{case} (°C)	Max θ_{ca} (°C/W)
Q1	200	175	1.4	7.0	165	61.0
Q2	150	125	9.0	0.5	120	44.0
Q3	150	125	9.0	0.5	120	44.0
Q4	150	125	35.0	0.5	107	0.77
Q5	150	125	1.0	0.5	124	44.0
Q6	200	175	1.8	7.0	162	45.0
Q7	200	175	1.4	7.0	165	61.0
Q8	150	125	29.0	0.5	110	1.0
Q9	150	125	29.0	0.5	110	1.0

Note 1: Power dissipation at maximum load and 80°C ambient.

4. 3. 4. 1 Automatic Mode c(1) Operation

As the name implies, the automatic mode utilizes automatic control for producing the various system outputs. Refer to Figure 36 for a graphical representation of the following description of operation. This chart shows the output states relative to the various input conditions during normal operation. At time t zero, power is applied, and the motor-driven valve attempts to close if it is open. At time t 1, which is activation of the aircraft ignition, a de-icing cycle is initiated. The ice detector probe clears in less than 18 seconds and after 60 seconds the anti-ice equipment is deactivated. At time t 2 on the sequence chart, icing has occurred and input "b" becomes present. This input produces outputs "y" (energize probe heater) and "v" (energize anti-ice equipment). Then "v" and "$\bar{d}$" (anti-ice valve not open) cause the valve drive motor to open the motor-driven valve via Q9. In less than 18 seconds, t 3, output y has caused the probe to clear, thereby removing the input ($\bar{b}$) ; hence, y is changed to $\bar{y}$. Output v remains present for 60 seconds after the probe clears to insure complete removal of ice. After this 60 second period, $\bar{v}$ and (anti-ice valve not closed) cause the valve drive motor to close the motor-driven valve via Q8 in less than 4 seconds. This completes the de-icing cycle at t 4.

The power on sequence is quite similar and is shown on the sequence chart beginning at time t zero and ending before t 2.

4. 3. 4. 2. Manual Mode c(2) Operation

In the manual mode, the operator overrides the automatic control, inhibits the ice detector probe de-ice, and determines the duration of the de-icing cycle with the anti-ice switch.

4. 3. 4. 3 Off Condition

In the off condition, the anti-ice system is inoperative and the warning lights are turned on to inform the operator of this fact.

4. 3. 4. 4 Warning Light Operation

The warning lights inform the operator of improper operation of the anti-ice system, icing conditions which will not clear automatically, and when the system is inoperative, Refer to Figure 37 for a graphical representation of the following description of operation. This chart shows the output state of the warning light relative to the various input conditions. At time t zero, with the anti-ice switch in the off position, an output "w" is present. Output w is the turn-on control signal to the warning light power switch. When the anti-ice switch is returned to the manual mode of operation, the warning lights go off. At time t 1, while in manual, condition $\bar{g}$ exists (essential circuit power not

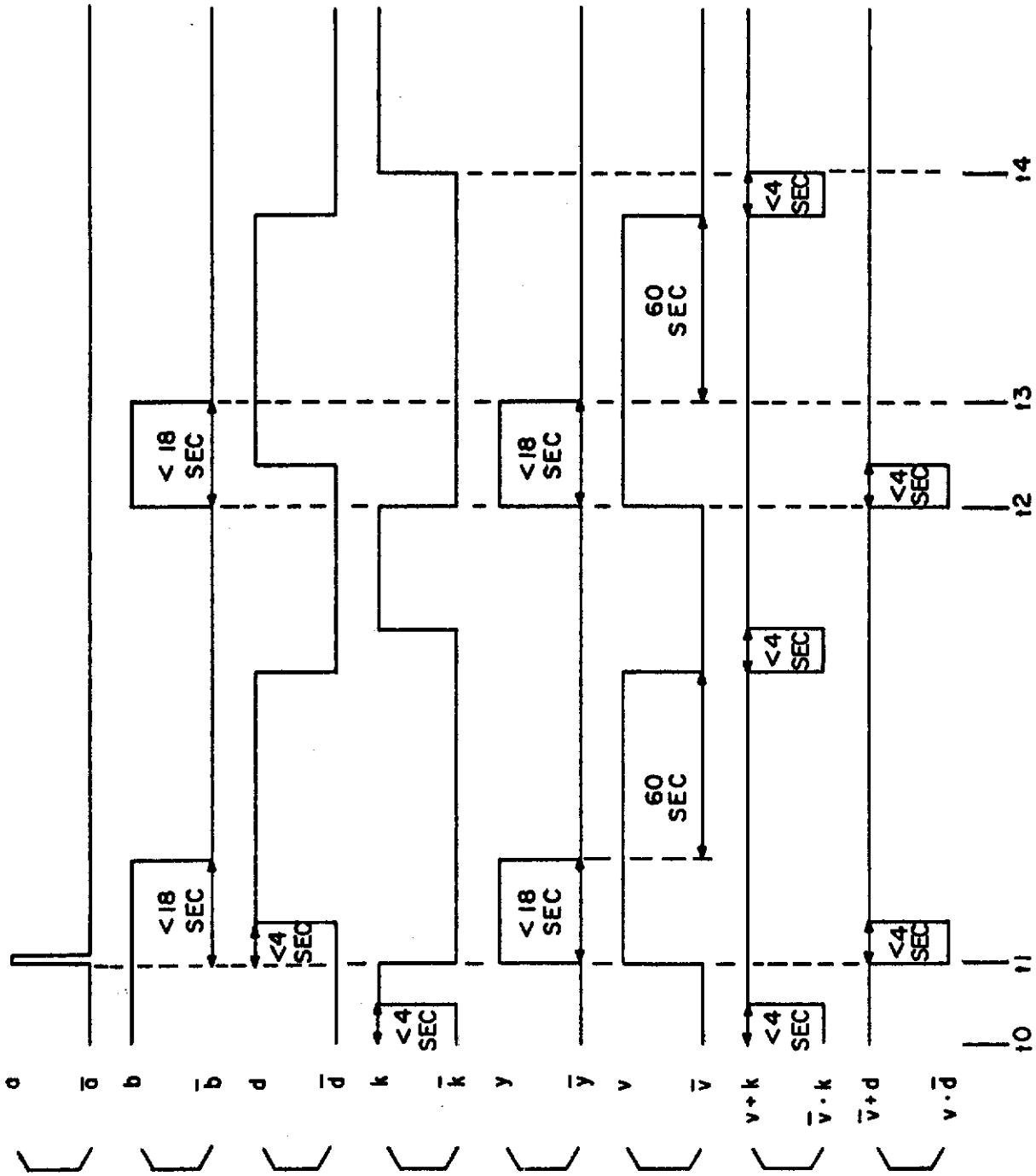


Figure 36. Normal Operation, Auto-mode Sequence Chart

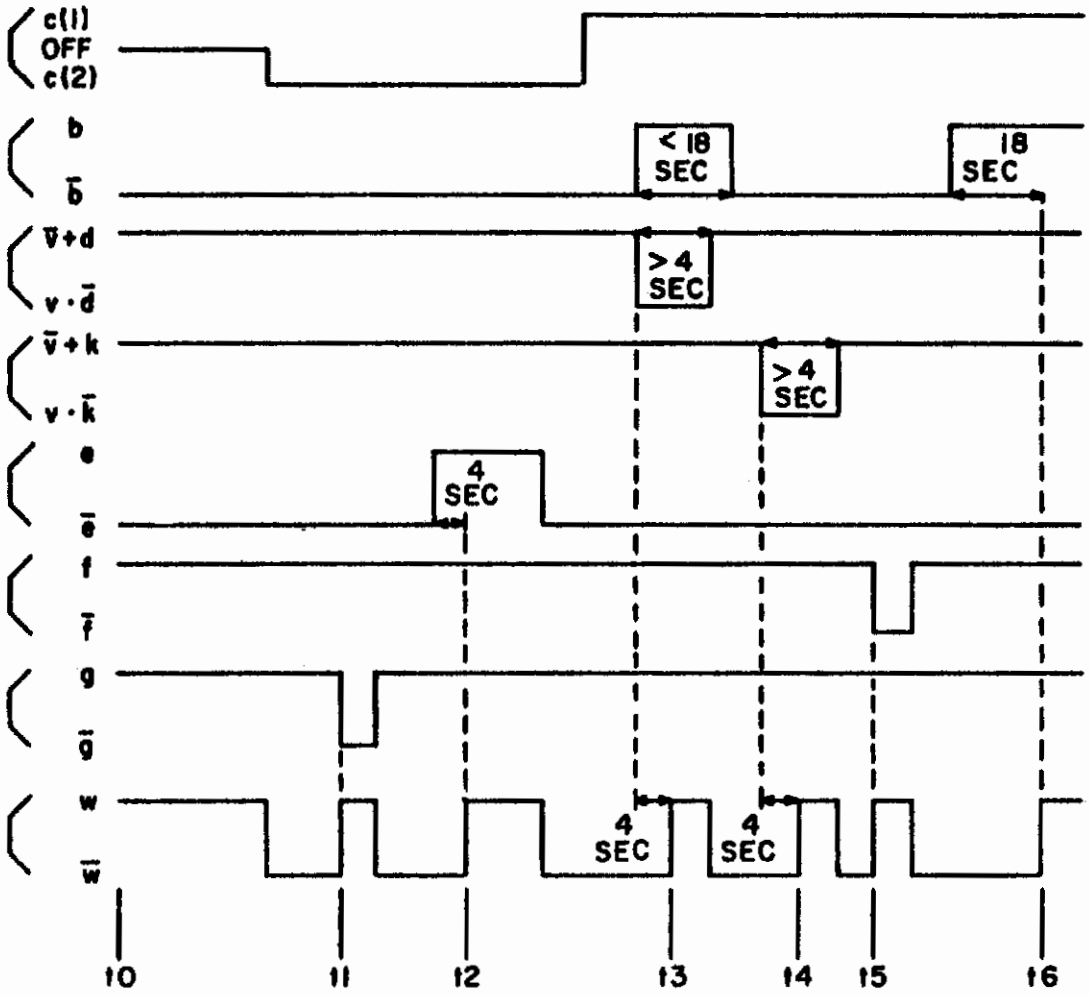


Figure 37. Warning Light Operation Sequence Chart

available); then the warning lights come on. When essential circuit power again becomes available, the warning lights go out. At time t 2, which is 4 seconds after the test switch has been depressed, the warning lights come on. When the test switch is released, the warning lights go out. At time t 3, while in the automatic mode c (2), the motor-driven valve has been attempting to open for more than 4 seconds. The warning lights come on and remain on until the valve is completely open. At time t 4, the motor-driven valve has been attempting to close for more than 4 seconds. The warning lights come on and remain on until the valve has closed completely. At time t 5 condition $\bar{f}$ occurs which is nonessential circuit power not available; the warning lights come on and remain on until the power is available once more. At time t 6, icing has occurred and the ice detector probe does not clear in the required 18 seconds. The warning lights come on and remain on while in the automatic mode or until the aircraft ignition switch is again actuated to initiate another de-icing cycle.

5. SPECIFICATION, SOLID STATE MATRIX

5.1 Scope

This specification covers a type of solid state matrix which could be used as a replacement for the master dc electrical power transmission link and the surface and engine air anti-ice power transmission link of the F-106B aircraft.

5.2 Applicable Documents

The following documents form a part of this specification to the extent specified herein:

Technical Manual	T.O. 1F-106A-2-10
Technical Manual	T.O. 1F-106A-2-6
HIAD	ARDCM 80-1
USAF Contract	AF 33(657)-8688

5.3 Requirements

5.3.1 Electrical

5.3.1.1 System Input Power

The input power required for system operation is:

+28 vdc ± 0.7 v, 1 amp max. (dc nonessential bus)
+30 vdc ± 3 v, 1 amp max. (dc essential bus)
115 vac ± 6 v (line to ground), 3 phase (insensitive to phase rotation), 400 ± 20 cps, 0.5 amp max. (ac essential bus)

5.3.1.2 System Output Loads

The output loads for power handling devices are:

DC Power Section

X2a (external interlock)	0.4 amp dc
X2b (dc generator interlock)	0.2 amp dc
X3 and X4 (dc essential bus load)	43 amp dc for 5 sec 33 amp dc for 1 min 28 amp dc for 15 min
X5 (battery charging load)	10 amp dc
X6a, b, c (ac nonessential to TR)	3.4 amp/phase
X7a, b, c (TR normal input)	1.0 amp/phase

DC Power Section (Cont'd)

X8a, b, c (ac essential bus to TR)	3.4 amp/phase
X9a, b, c (TR emergency input)	3.4 amp/phase
Chute Deploy (Q7)	5.0 amp dc

Anti-ice Section

X1 (radome a-i valve switch)	0.8 amp
X2 (HR 1 switch)	3.0 amp
X3 (HR 2 switch)	3.0 amp
X4 (HR 5 switch)	7.0 amp
X5 (HR 6 switch)	1.1 amp
X6 (warning light switch)	0.16 amp normal, 1.60 amp surge
X7 (duct lip a-i valve switch)	0.7 amp
X8 (a-i valve close switch)	6.0 amp
X9 (a-i valve open switch)	6.0 amp

5.3.1.3 Control Inputs and Definitions

The system inputs shall be:

DC Power Section

A_1	More than + 17 vdc ± 20% on dc nonessential bus
C	Master switches closed
D	AC emergency power disconnect relay in "Emergency AC Pwr On" position
F	More than +17 vdc ± 20% external dc present
G	Generator switch actuated
H	Test switch not actuated
J	Air data converter switch in "Greater than 280 knots" position
N	Less than 5 amps per phase flowing on ac essential bus
P	AC voltage present on ac essential bus

Anti-ice Section

a	Ignition relay actuated
b	Pressure switch in the "ice" position
c	Anti-ice switch - three positions
	c_1 Automatic
	c_2 Manual
	c_3 Off

Anti-ice Section (Cont'd)

d	Motor driven valve limit switch (S3) in valve open position
e	Test switch actuated
f	Nonessential bus circuit power available
g	Essential bus circuit power available
k	Motor driven valve limit switch (S2) in valve closed position

5.3.1.4 System Outputs

With the system inputs as defined by the original schematics contained in T.O. 1F-106A-2-10 the system outputs shall be:

DC Power Section

Operate X2a	Permits actuation of dc primary generator.
Operate X2b	Permits actuation of external power source.
Operate X3	The battery will be connected to the dc essential bus.
Operate X4	The transformer-rectifier (TR) output will be connected to the dc essential bus. Its output will be 29.1 ± 1.9 vdc with an ac line variation of ± 6 vac.
Operate X5	The TR output will be connected to the battery. Its output will be 36 ± 0.5 vdc with an ac line variation of ± 2 vac.
Operate X6	The TR will receive its input power from the ac nonessential bus.
Operate X7	AC power is applied to the normal TR input.
Operate X8	The TR will receive its input power from the ac essential bus.
Operate X9	AC power is applied to the emergency TR input.

Anti-ice Section

Operate X1	Permits actuation of the radome anti-ice valve (L50) via the forward MLG switch.
Operate X2	Supplies power to the lower air intake heater (HR1) to sections B and C directly and to section A via the aft MLG switch.
Operate X3	Supplies power to the upper air intake heater (HR2).
Operate X4	Supplies power to the probe heater (HR5).
Operate X5	Supplies power to the case heater (HR6) to maintain case temperature at +15 ± 8°C.
Operate X6	Supplies power to the engine anti-ice warning lights.
Operate X7	Actuates the duct lip, anti-ice valve (L87).

Anti-ice Section (Cont'd)

Operate X8	Supplies power to the motor which closes the engine a-i valve.
Operate X9	Supplies power to the motor which opens the engine a-i valve.

5.3.1.5 Output Switch Power Dissipation

The output switch power dissipation under maximum loading conditions at an ambient temperature of +80° C will be:

DC Power Section

Switch	Maximum Power Dissipation (watts)
X2a	0.5
X2b	0.2
X3	55.0
X4	55.0
X5	10.0
X6a, b, or c	5.0
X7a, b, or c	1.5
X8a, b, or c	5.0
X9a, b, or c	5.0
Chute Deploy (Q7)	8.0

Anti-ice Section

Switch	Maximum Power Dissipation (watts)
X1	1.4
X2	9.0
X3	9.0
X4	35.0
X5	1.0
X6	1.8
X7	1.4
X8	29.0
X9	29.0

5.3.1.6 Overload Protection

The solid state matrix makes use of solid state overload protection. The dc protective circuits will trip in less than 100 microseconds, and the ac protective circuit will trip in less than 1.25 milliseconds. Both are manually resettable.

DC Power Section

Protective Circuits	Trip Current
Chute Deploy	5.0 amp dc
AC essential bus to TR	5.0 amp rms/phase

Anti-ice Section

Protective Circuits	Trip Current
Radome a-i valve (L50)	1.2 amp dc
Lower air intake heater (HR1)	5.0 amp dc
Upper air intake heater (HR2)	5.0 amp dc
Probe heater (HR5)	10.0 amp dc
Case heater (HR6)	1.6 amp dc
Engine a-i warning lights	2.5 amp dc
Duct lip a-i valve (L87)	1.2 amp dc
Engine a-i valve motor	9.0 amp dc

5.3.2 Temperature

5.3.2.1 Temperature Ranges

Operating temperature range: -	$-55^{\circ}C$ to $+80^{\circ}C$
Storage temperature range: -	$-55^{\circ}C$ to $+125^{\circ}C$

5.3.2.2 Power Switch Thermal Considerations

Most of the power switching devices in the system must be mounted on adequate heat sinks in order to maintain safe junction temperatures. The thermal resistivity case to ambient (θ_{ca}) given is a maximum figure which should not be exceeded. Therefore, the thermal conditions listed should be used as a guide when choosing the proper heat sinks. Thermal conditions given are when $T_a = +80^{\circ}C$ and maximum power is being dissipated.

DC Power Section

Switch	Max T_c ($^{\circ}C$)	Max θ_{ca} ($^{\circ}C/W$)
X2a	172	183.0
X2b	173	468.0
X3	128	0.9
X4	128	0.9
X5	105	2.5

Anti-ice Section

Switch	Max T_c ($^{\circ}C$)	Max θ_{ca} ($^{\circ}C/W$)
X1	165	61.0
X2	120	4.4
X3	120	4.4
X4	107	0.77
X5	124	44.0

DC Power Section			Anti-Ice Section		
Switch	Max T_c (°C)	Max θ_{ca} (°C/W)	Switch	Max T_c (°C)	Max θ_{ca} (°C/W)
X6a, b, c	115	7.0	X6	162	45.0
X7a, b, c	122	28.0	X7	165	61.0
X8a, b, c	115	7.0	X8	110	1.0
X9a, b, c	115	7.0	X9	110	1.0
Chute Deploy (Q7)	121	5.0			

5.3.3 Design Criteria

5.3.3.1 Power Supply Regulation

All internal regulated voltages supplied to the system will be within ±10% tolerance over the range of line voltage variation and temperature.

5.3.3.2 Logic Circuit Device Ratings

Device (T.I.)	P_{dis} (mw at 25°C)	Max V_{cc} (volts)	Turn-on Input V (volts)	Turn-off Input V (Volts)	Loading per logic stage Fan-in	Fan-out	Ambient temp (°C)	Wt (gram)
SN512	7	8	2.5	0.3	6	5	-55 to +125	0.1
SN513	7	8	2.5	0.3	6	25	-55 to +125	0.1
SN514	14	8	2.5	0.3	3	5	-55 to +125	0.1

5.3.3.3 Power Switch Leakage

The maximum leakage current which may flow will be less than 1% of the normal load current value, or 5 milliamperes, whichever is the greater.

5.3.3.4 Power Switch Saturation Resistance

The maximum saturation resistance of the power switches will be less than 10% of the load resistance.

5.4 Experimental Evaluation Procedure

5.4.1 Purpose

The purpose of the experimental evaluation phase of this project is to determine how well the solid state matrix performs over the specified temperature and voltage ranges, and to indicate which areas of the system require redesign effort in order to meet predetermined specifications. The following procedure is prepared as a guide to follow while performing this experimental evaluation.

5.4.2 Testing Approach

Since the value of constructing duplicate circuits during a program of this nature is doubtful and duplication tends to increase complexity and expense, testing and analysis will be undertaken in three sections. These are as follows: (1) the dc control section of the dc power system; (2) the experimental TR control section of the dc power system; and (3) the experimental anti-ice system. The dc control section of the dc power system consists of all circuits above the horizontal cutting line on the detailed block diagram. The experimental TR control section consists of the following: (1) X8a, b, and c; (2) ac overload detection circuits; (3) ACFC2; (4) X4 and X5; (5) FC2 and FC3; (6) OS1; (7) T1, BR4, PS1, PS2, VR4, VR5; and (8) All logic gates and inverters shown on the detailed block diagram below the horizontal cutting line. The experimental anti-ice system consists of the following: (1) all logic gates and inverters shown on the detailed control logic diagram; (2) Q5, Q6 and their associated amplifiers and overload circuits; (3) Q8, Q9 and their associated amplifiers; (4) KD10 and KD11; and (5) VR10, VR11, and VR15.

5.4.3 Test Equipment

The following is a list of test equipment to be used during the experimental evaluation of the solid state matrix and a brief description of each type:

Volt-Ohm-Milliammeter, Triplett Model 630

DC Accuracy 3%
DC volts sensitivity, 20,000 ohms/volt

Volt-Ohm-Milliammeter, Weston Model 980

DC accuracy 2%
AC accuracy 3%
DC volts sensitivity, 20,000 ohms/volt
AC volts sensitivity, 1000 ohms/volt

5.4.3 Test Equipment (Cont'd)

DC Ammeter, Weston Model 931

Accuracy 1/2%

AC Ammeter, Weston Model 904

Accuracy 1/4% to 1000 cps

DC Shunts, Weston

2 amp, 5 amp, 15 amp, and 50 amp

DC Ammeter, Weston Model 45

Accuracy 1/4%

Current Transformers, Weston Model 461

25 - 500 cps
Accuracy 1/4%

Oscilloscope (with HP152A dual channel amplifier), Hewlett-Packard Model 150A

Pass Band:	DC to 10 mcps
Sensitivity:	0.05 v/cm to 50 v/cm
Input Impedance:	1 megohm shunted with 30 pf
Calibration Sweep:	3% accuracy
Amplitude, Calibration:	3% accuracy (peak to peak)

True RMS Volt-Ammeter, Model THACH Sensitive Research

Accuracy 0.2% to 4KCPS

Temperature Indicator, Leeds and Northrup

Accuracy $\pm 1^{\circ}F$

AC Voltmeter, Hewlett-Packard Model 400D

Accuracy 2%

5.4.3 Test Equipment (Cont'd)

Transient Voltage Indicator, Trott Model TR741B

Accuracy ± 2%
May be calibrated at specific voltages to ± 1/4%
Detection Sensitivity: DC to 1 microsec at above accuracy;
0.5 microsec at reduced accuracy
Input Impedance: 1 megohm shunted by 5 pf.

Stopwatch, Galco

1/10 sec intervals

DC Power Supply, Sorenson Model MA 28-125

18 - 36 vdc, 125 amps
Regulation 1%

Motor-Generator, Type N324P, S324P,
Continental Electric Co.

208 - 225 v line to line, 36.5 amps
three -phase ac, freq 410 cps

Three-Phase Variac, General Radio Model W-10

10 amp capacity
210 vac line to line input

AMF Special Test Equipment

Solid Circuit Mounting Fixture, Figure 38, Section 6
Input Simulator, Figure 39, Section 6
Motor Driven Valve Simulator, Figure 34, Section 4
Motor Driven Valve Simulated Load, Figure 51, Section 6
DC Simulated Load, Figure 41, Section 6

5.4.4 DC Control Section Tests

5.4.4.1 DC Regulators (VR1, 2)

A complete evaluation of the dc regulator is necessary preceding further system tests to insure a stable, dependable source for the various voltages required by the solid state matrix.

Circuit Voltages

Record voltages on all transistors in the circuit under no load conditions.

Regulation

Monitor the regulator input voltage and the output voltages with dc voltmeters. Monitor the various load currents with dc milliammeters. Set the input voltage at +28 vdc and record the output voltages at no load and full load for the various outputs.

Repeat the above regulation measurements at the input voltage extremes of + 27 vdc and + 33 vdc.

Repeat the above regulation measurements at the temperature extremes of + 80°C and -55°C.

Power Device Case Temperature

Attach a thermocouple to the case of VR1-Q1, the series regulating element, and monitor case temperature with full load applied. If necessary, install Q1 in a separate environmental chamber and raise the ambient temperature until the case temperature reaches + 110°C. Check for satisfactory performance of Q1 at this elevated temperature. Use temperature sensitive paint to ensure that VR2-Q1 through Q4 case temperatures do not exceed the safe design limits.

Current Limiting

Increase load on + 18 volt output until this output voltage begins to decrease in order to maintain a constant current. Record load current at which limiting begins and maximum current with output short circuited. Also, monitor case temperature to assure that thermal damage does not occur.

5.4.4.2 Negative Power Supply (PS2) and Regulator (VR3)

Monitor the ac volts in to the power supply, the -6 vdc out of the power supply, the -3 vdc regulated out of the shunt regulator, and the load current.

Set the input ac volts at 115 vac and record -6 v output and -3 v output at no load, 50 ma load, and 70 ma load.

Repeat the above measurements at the line voltage extremes of 109 and 121 vac.

Repeat all the above measurements at the temperature extremes of + 80°C and -55°C.

5.4.4.3 Operational Test

Make the following tests with the complete dc control section of the dc power system operating. Connect the control input simulator to the dc control section logic circuits and check for proper operation with all input combinations as outlined in Section 4.2.1, Table 5, "Logical Conditions and Definitions for the DC Power System."

5.4.4.4 Chute Deploy DC Overload Circuit

Circuit Voltages

Record voltages on all transistors when operating normally and when the circuit has been tripped out.

Tripping Current

Monitor load current and essential bus voltage. Adjust bus voltage to + 27 vdc and increase load current slowly until circuit trips. Record load current at trip point.

Repeat the above test at + 28 vdc and + 33 vdc. Repeat all of the above tests at the temperature extremes of + 80°C and -55°C.

Power Switch (Q7)

With Q7 installed in a separate temperature chamber, adjust load current until 3 amps flows. While monitoring Q7 cases temperature, increase the chamber temperature until a Q7 case temperature of + 120°C is reached. Record Q7 V_{ce} with Q7 on. Turn off Q7 and increase chamber temperature until a temperature (equal to case temperature and junction temperature) of + 150°C is reached. Record leakage current.

5.4.4.5 X2a, X2b, and Associated Amplifiers (AP1, 2)

Note if X2a and X2b operate when the correct logic inputs are present.

Circuit Voltages

Record voltages on all transistors with X2a and X2b in both the on and off conditions.

X2a Power Switch

Record X2a V_{ce} in the on condition with a load current of 400 ma flowing at the extremes of temperature of + 80°C and -55°C. Record leakage current with X2a off and at high temperature.

X2b Power Switch

Record X2b V_{ce} in the on condition with a load current of 400 ma flowing at the extremes of temperature of + 80°C and -55°C. Record leakage current with X2b off and at high temperature.

5.4.4.6 Battery Switch (X3), FC1, and TO1

Observe operation of X3 when correct logic inputs are present; note proper turn-off by TO1.

Circuit Voltages

Record voltages on all transistors with X3 off and X3 on.

Maximum Load Capability

Monitor load current and essential bus voltage. Set bus voltage at + 27 vdc and adjust load current to 30 amps. Attempt turn-off by removing one of the control inputs. Continue to change load current and attempt turn-off until a maximum current is achieved which may be controlled. Record this current reading. Repeat the above test at + 28 vdc and + 33 vdc essential bus voltage.

Repeat all of the above tests at the temperature extremes of + 80°C and -55°C.

Power Switch (X3)

Record X3 V_{ce} with a load current of 40 amps flowing and monitor X3 case temperature. If necessary, install X3 in a separate temperature chamber and increase chamber temperature until T_{case} is +125°C. Turn X3 off and measure leakage current.

5.4.4.7 Voltage Sensor (VS1, VS2)

Monitor input and output voltages. Adjust input voltage until output voltage equals 0.3 volts and record input voltage. Increase the input voltage until the output voltage equals 2.5 volts and again record input voltage. Increase the input voltage to + 33 vdc and record the output voltage.

Repeat the above test at the temperature extremes of + 80°C and -55°C.

5.4.4.8 General Performance

Change the various inputs and note operation of various power switches watching for interaction between circuits and improper operation of dc control section in general.

5.4.4.9 Storage Test

Remove voltage from the essential bus and increase temperature of chamber to +125°C. Allow the dc control section to remain in the chamber at +125°C for a sufficient time for all components to reach the ambient temperature. Reduce temperature to + 25°C and perform an operational check to assure proper circuit operation.

5.4.5 Experimental TR Control Section

5.4.5.1 General Information

Make the few circuit changes required to change VR1, 2 previously tested to VR4, 5. Since VR1, 2 are basically the same as VR4, 5, performance testing is not necessary. However, check output voltages to see that they are within ±10% of the designed values.

Make the following tests with the experimental TR control section of the dc power system operating.

5.4.5.2 Three Phase AC to DC Power Supply (PS1)

Monitor PS1 ac input voltage and dc output voltage. Monitor load current. Set the input voltage at 109 vac and record the output voltage at no load and 300 ma.

Repeat the above measurements at 115 v in and 121 v in.

Repeat all the above measurements at the temperature extremes of +80°C and -55°C.

5.4.5.3 Operational Test

Connect the control input simulator to the TR control section logic circuits and check for proper operation with all input combinations as outlined in the table titled "Logical Conditions for the DC Power System."

5.4.5.4 AC Switch (X8) and Firing Circuit (ACFC2)

Circuit Voltages

Record voltages on all transistors with ac switch off and on.

Firing Circuit Performance

Provide a 4 amp load for each section of the ac switch. Apply control inputs which turn on X8 and observe waveform at gate of each SCR in switch. Note amplitude and duration of gate trigger.

AC Switch Performance

Measure V_{ak} rms of the ac switch while turned on with case temperature at + 125°C.

Note load voltage waveform out of ac switch. Turn off ac switch and increase chamber temperature until the case temperature of each SCR is approximately + 125°C. Measure leakage current through switch under these conditions.

5.4.5.5 AC Overload Circuit

Circuit Voltages

Record circuit voltages with the ac switch off and on.

Tripping Current

Monitor load current and detector supply voltage. Increase load current slowly until circuit trips. Record load current at trip point.

Repeat the above test at the temperature extremes of + 80°C and -55°C.

5.4.5.6 Delay Gate Multivibrator(OS1)

Circuit Voltages

Record circuit voltages on all the transistors of OS1.

Delay Gate Width

Measure duration of delay gate at the temperature extremes of +80°C and -55°C.

Delay Gate Performance

Since X4 and X5 turn-off is determined by the delay gate, use this as a criteria for delay gate performance.

5.4.5.7 TR to Essential Bus Switch (X4) and FC2

Observe operation of X4 when correct logic inputs are applied.

Circuit Voltages

Record circuit voltages on all transistors.

Power Switch Performance

Monitor case temperature of X4 and increase chamber temperature until case temperature is +125°C. Measure V_{ak} of X4 when turned on with a 43 amp load. Turn X4 off and measure leakage current.

5.4.5.8 TR to Battery Switch (X5) and FC3

Observe operation of X5 when correct logic inputs are applied for turn-on and turn-off.

Circuit Voltages

Record circuit voltages on all transistors.

Power Switch (X5) Performance

Monitor case temperature of X5 and increase chamber temperature while X5 is on with 10 amp load, until case temperature is +105°C. Measure V_{ak} of X5 when turned on with a 10 amp load. Turn X5 off and measure leakage current.

5.4.5.9 Storage Test

Remove voltage from TR control section and increase chamber temperature to +125°C. Allow the TR control section to remain in the chamber at +125°C for a sufficient time for all components to reach the ambient temperature. Reduce the temperature to +25°C and perform an operational check to

assure proper circuit operation.

5.4.6 Experimental Anti-ice System

5.4.6.1 General Information

Make the few circuit changes required to change VR4, 5 of the previous section to VR10, 11. Since VR10, 11 are basically the same as VR4, 5, extensive testing of VR10, 11 is not necessary. Also, VR15 is identical to VR3 so no further testing of the negative voltage source is necessary.

Make the following tests with the complete experimental anti-ice system operating.

5.4.6.2 Operational Test

Connect the input simulator to the anti-ice system logic circuits and check for proper operation with all input combinations as outlined in the anti-ice sequency charts, Figures 36 and 37.

5.4.6.3 Time Delay Circuits

Circuit Voltages

Record voltages on all transistors with and without their respective control inputs.

Time Delay Performance

With circuits at $+25^{\circ}C$ adjust the delays for 4 seconds, 18 seconds, and 60 seconds.

Measure the time delays at the specified temperature extremes.

5.4.6.4 Warning Light Circuit

Circuit Voltages

Record voltages on all transistors with and without control input to AP23.

Power Switch Performance

With the normal lamp load applied measure Q6 V_{ce} in an ambient temperature of $+80^{\circ}C$. Turn off Q6 and measure leakage current at a case temperature of $+80^{\circ}C$.

5.4.6.5 Warning Light Overload Circuit

Circuit Voltages

Overload circuit voltages have been previously recorded; refer to dc overload section of dc power system.

Tripping Current

Monitor load current and essential bus voltage. Adjust bus voltage to + 27 vdc and increase load current slowly until circuit trips. Record load current at trip point.

Repeat the above test at + 28 vdc and + 33 vdc. Repeat all of the above tests at the temperature extremes of + 80°C and -55°C.

5.4.6.6 Motor Driven Valve Circuit

Circuit Voltages

Record circuit voltages on all transistors of the associated amplifiers with and without control inputs.

Power Switch Performance

With a 6 amp load applied measure Q8 and Q9 V_{ce}. Monitor case temperatures and increase ambient temperature until case temperature is + 115°C. Record V_{ce}.

Turn off power switches and raise ambient temperature to + 125°C. Record leakage current.

5.4.6.7 Temperature Sensor (TS10)

Circuit Voltages

Record voltages on all transistors above and below temperature switching point.

Sensor Performance

Vary temperature of thermistor over the range of + 7 to + 23°C and record temperatures at which on and off switching takes place.

Power Switch Performance

With a 1.6 amp load applied measure Q5 V_{ce}. Monitor Q5 case temperature with ambient temperature at + 80°C. Turn off Q5 and increase ambient temperature until the case temperature is at the same temperature as measured above. Record the leakage current.

5.4.6.8 Case Heater Overload Circuit

Circuit Voltages

Record voltages on all transistors under normal operation and after tripping.

Tripping Current

Monitor load current and essential bus voltage. Adjust bus voltage at + 28 vdc and increase load current slowly until circuit trips. Record load current at tripping point. Repeat the above test at the voltage and temperature extremes.

5.4.6.9 Storage Test

Remove voltage from the experimental anti-ice system and increase chamber temperature to + 125°C. Allow the anti-ice system to remain in the chamber at + 125°C for a sufficient time for all components to reach the ambient temperature. Reduce the temperature to + 25°C and perform an operational check to assure proper circuit operation.

6. EXPERIMENTAL EVALUATION DATA

Detailed test data for the solid state matrix is presented in the following sections. In general, the circuits operated properly as designed but in a few cases modifications of the original design were necessary. In some cases data was taken before and after modifications; where this is the case both sets of data have been given. Included in this section are drawings of waveforms which have been faithfully reproduced from photographs taken during testing. These photographs were unsuitable for direct reproduction. A standard transient voltage indicator was used during evaluation to insure that no fast transients were occurring which were not detectable on the oscilloscope.

A mounting chassis for the Solid Circuits was designed and fabricated and is shown in Figure 38. It incorporates transient over-voltage protection in the form of a 10 ohm resistor and a 6.8 volt, 10 watt, zener diode. The Solid Circuits themselves were mounted on printed circuit boards as illustrated in Figure 39. These boards plug into jacks on the mounting chassis. After a circuit was mounted on a board, it was tested in the test circuit of the Solid Circuit mounting chassis to insure that it was operating properly. In addition to the solid circuit mounting chassis, an input simulator was constructed to provide input signals to the control circuits and is shown in Figure 39.

The large dc loads (dc essential bus, battery charging, etc.) were simulated with combinations of Eagle nichrome heating elements as shown in Figure 40. Both 125 v, 600 w and 125 v, 1 KW units were used. The 600 w unit is 26 ohms and the 1 KW unit is 15.7 ohms. Since these units were originally intended to operate at 125 v, their temperature of operation was considerably reduced when operating at 28 v. Therefore, the load resistance change due to heating was practically zero. The smaller dc loads were simulated with carbon and wire wound resistors.

Refer to the experimental evaluation procedure of the equipment specification, Section 5 of this report, for a detailed listing of test equipment used during testing and an explanation of test methods. In particular, note that tests were conducted separately for the dc control section, experimental TR section, and experimental a-i section.

6.1 DC Control Section

Figure 41 shows the test set-up used for the high temperature runs of this section; note the use of a separate temperature chamber containing the heat sinked power switches. The temperature of the chamber containing the sinked device was increased until the case temperature of the device was at its maximum allowable value. The temperature of the chamber

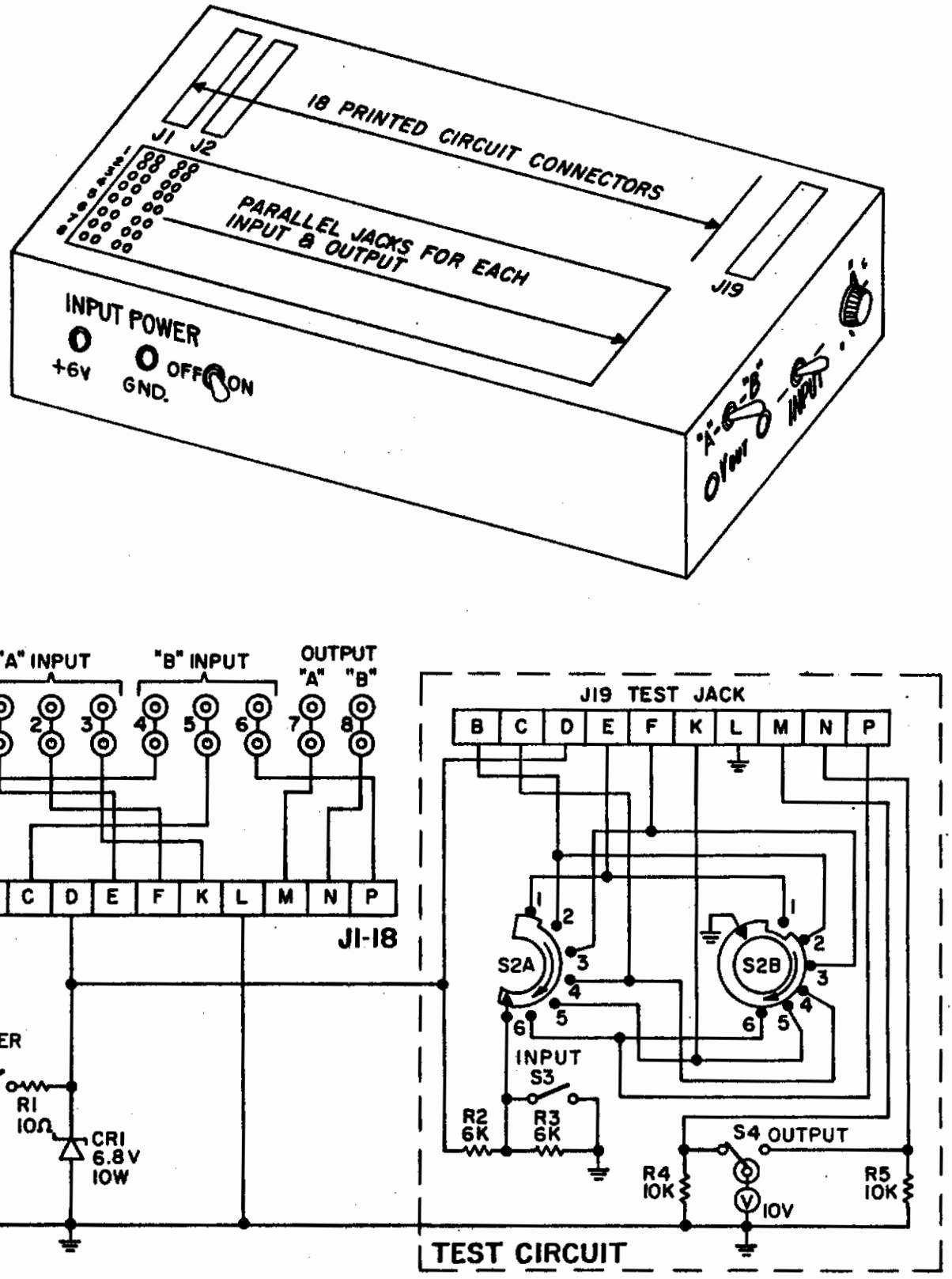
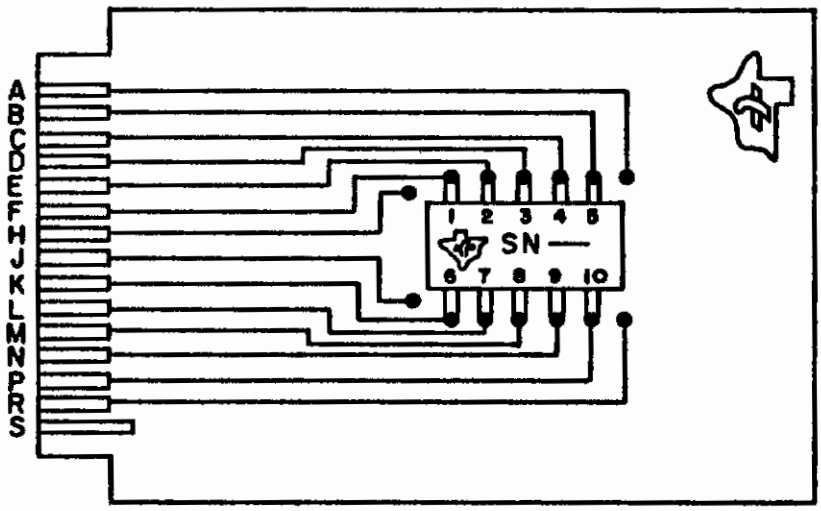
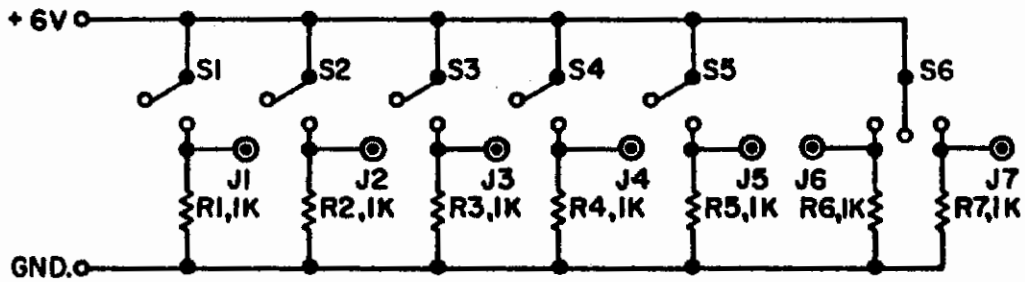


Figure 38. Solid Circuit Mounting Chassis



(a) Solid Circuit Mounting Board



(b) Input Simulator

Figure 39. Solid Circuit Breadboard Mounting Board and Input Simulator

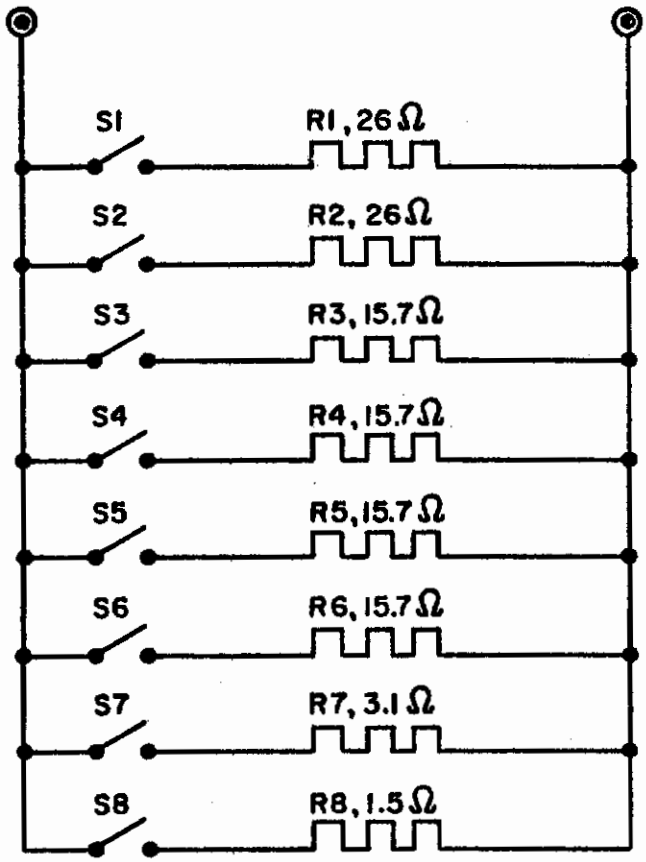


Figure 40. DC Simulated Load

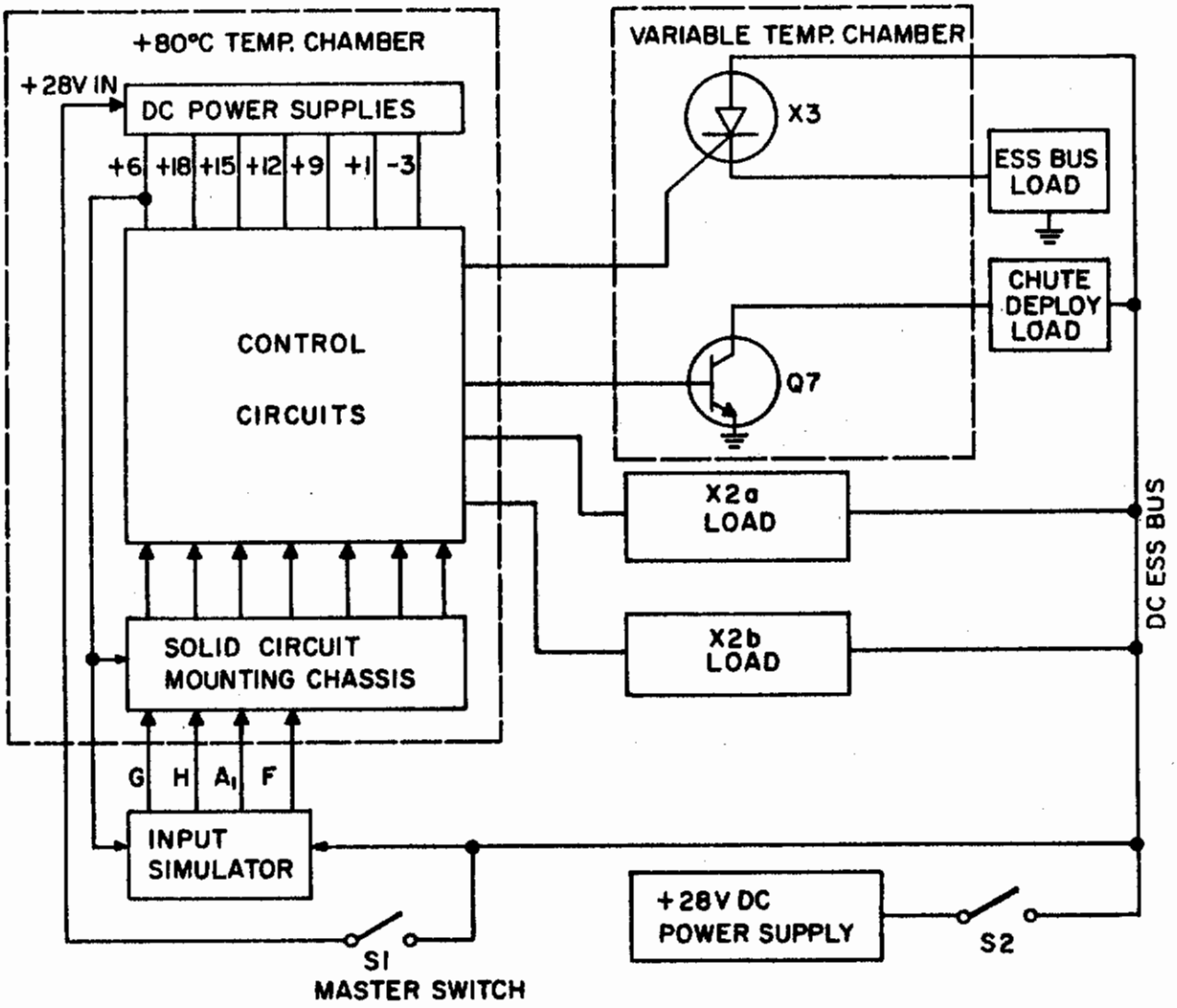


Figure 41. Test Set-up for DC Control Section High Temperature Run

containing the control circuitry was increased to + 80°C. Then the circuit was tested for proper operation. The advantage of this procedure is that it permitted a direct check of performance at the maximum allowable design case temperature. This would be difficult to achieve otherwise. All case temperatures were measured with a thermocouple bridge; however, temperature sensitive paint was used on all power devices as a safety precaution.

6.1.1 DC Power Regulator (VR1, VR2)

The dc power regulator shown in Figure 12 was constructed. A few preliminary operating checks were made and it was found necessary to modify the design to achieve satisfactory operation. After satisfactory operation was achieved, the no-load current drain was measured as about 100 milliamperes. The circuit voltages were also measured and are given in Table 16. Performance data was then taken for the dc power regulator and is given in Table 17. The readings in parentheses in the +27°C column were obtained after the performance test had been performed. It was the result of a further design modification (the value of a single resistor, VR2-R5, was changed from 200 Ω to 100 Ω), made necessary by a circuit defect which was not noticed until after the greater part of the test data had been obtained. The readings in parentheses, which were taken after changing R5, are within 2% of the original readings and reflect the same regulation characteristics as the original readings; therefore, the complete performance test was not re-run.

The high temperature test was conducted for 2 hours at +80°C with full load applied. Q1, the series regulating element, had a case temperature of +105°C with full load applied over a 2 hour period. This was sufficiently close to the maximum design temperature of +110°C to make unnecessary any further correction. The case temperatures of VR2-Q1 through Q4 were not measured because they are not critical, since design calculations indicated that these units required a θ_{ca} of 90°C/W, or less. A preliminary test indicated that the 2N1486 when mounted with the hardware provided has a θ_{ca} of only 24°C/W at 0.7 watts dissipation. Thus, these units neither required a heat sink nor have one.

The final test of regulator performance was for proper current-limiting operation. It was found that Q1 begins to limit current at 720 ma, and that the maximum short circuit current was 1.1 amperes. Q1 had a case temperature of +114°C when operating on the bench under short circuit conditions.

6.1.2 Negative Power Supply (PS2) and Regulator (VR3)

The negative power supply and regulator circuits are shown in Figure 14, and were evaluated at no load, 50 ma load, and 70 ma load over the tempera-

TABLE 16

DC Regulator (VR1, VR2) Circuit Voltages at No Load and +27°C

Circuit	Location	Voltage (vdc)
VR1	Q1C	27.2
	B	19.1
	E	18.5
	Q2C	19.7
	B	5.5
	E	4.9
	Q3C	27.2
	B	19.7
	E	19.1
VR2	Q1C	17.9
	B	16.0
	E	15.4
	Q2C	17.8
	B	12.7
	E	12.2
	Q3C	17.8
	B	10.0
	E	9.3
	Q4C	11.0
	B	6.8
	E	6.3

TABLE 17

DC Regulator (VR1, VR2) Performance Data

Volts in (vdc)	Volts out at +80°C (vdc)	Volts out at +27°C (vdc)	Volts out at -55°C (vdc)	Output Section
27	17.3	18.0 (17.7)	18.5	18 v output
28	17.5	18.1 (17.8)	19.0	at full load
33	17.6	18.4 (17.9)	19.1	of 200 ma
27	17.7	18.4 (17.8)	--	18 v output
28	--	18.4 (17.9)	18.7	at no
33	17.9	18.6 (18.0)	19.2	load
27	14.8	15.0 (15.1)	15.2	15 v output
28	14.9	15.1 (15.1)	15.3	at full load
33	15.0	15.3 (15.2)	15.4	of 50 ma
27	15.2	15.4 (15.3)	--	15 v output
28	15.2	15.4 (15.3)	15.2	at no
33	15.4	15.5 (15.3)	15.6	load
27	11.6	11.7 (12.0)	11.8	12 v output
28	11.7	11.8 (12.1)	11.8	at full load
33	11.8	11.9 (12.1)	11.9	of 50 ma
27	12.2	12.2 (12.2)	--	12 v output
28	12.2	12.2 (12.2)	11.8	at no
33	12.3	12.3 (12.2)	12.0	load
27	8.5	8.8 (8.8)	8.9	9 v output
28	8.6	8.8 (8.9)	9.0	at full load
33	8.6	9.0 (8.9)	9.0	of 200 ma
27	9.3	9.3 (9.2)	--	9 v output
28	9.3	9.3 (9.2)	8.9	at no
33	9.4	9.4 (9.2)	9.1	load

TABLE 17 (Continued)

DC Regulator (VR1, VR2) Performance Data

Volts in (vdc)	Volts out at +80°C (vdc)	Volts out at +27°C (vdc)	Volts out at -55°C (vdc)	Output Section
27	5.7	5.9 (6.2)	5.9	6 v output
28	5.8	5.9 (6.2)	6.0	at full load
33	5.8	6.0 (6.2)	6.2	of 50 ma
27	6.3	6.3 (6.2)	--	6 v output
28	6.3	6.3 (6.2)	6.0	at no
33	6.4	6.3 (6.2)	6.1	load
27	0.6	0.65 (0.65)	0.65	1 v output
28	0.6	0.65 (0.65)	0.75	at full load
33	0.6	0.65 (0.65)	0.75	of 30 ma
27	0.65	0.70 (0.70)	--	1 v output
28	--	0.70 (0.70)	0.80	at no
33	0.65	0.70 (0.70)	0.80	load

ture range with a maximum variation of input voltage. During some preliminary tests the -3 vdc shunt regulator operated properly with an input voltage as low as -5 vdc. Performance data for the negative power supply and regulator is given in Tables 18A and 18B. After completion of testing, it became apparent that increased separation of the dc control section and TR section, hence increased reliability, could be obtained by using a dc to dc converter as PS2. Refer to Section 7, Table 44 for some performance data for a dc to dc converter which could be used in conjunction with a zener shunt regulator to provide the -3 vdc.

6.1.3 Chute Deploy DC Overload Circuit

The chute deploy overload circuit as shown in Figure 19 was constructed and evaluated while operating with the dc control section of the dc power system. The original design differed from Figure 19 in that AP3 had R2 as 3.3K, R3 as 2.2K, and R4 as 2.2K. Two sets of data were taken with this original design. First, the circuit voltages were measured and are given in Table 19. Normal refers to the condition of full rated load current applied without tripping. Tripped-out refers to the condition of trip-out due to overload (before any reset attempt).

Second, the variation of tripping current with line voltage and ambient temperature was measured and is given in Table 20. After this data had been taken, it was deemed desirable to modify the circuit; subsequent data applies to the modified circuit, which is that shown in Figure 19.

The tripping current variations for the modified overload circuit is presented in Table 21A. A graphical representation of Table 21A is presented as Figure 42. Saturation voltages for the Q7 power switch are presented in Table 21B. The leakage current was measured for the Q7 power switch while in the off condition. It was 0.7 milliamperes at a case temperature of +150°C, and 0.5 milliamperes at a case temperature of +130°C. Some performance data for the differential amplifier was taken at +27 and -55°C and is presented in Table 22 and again graphically in Figure 43.

Certain other features were also tested. For example, a 4 ampere load was removed and reapplied while the circuit was energized without causing a trip. Then power was removed and reapplied with a 4 ampere load on the line without causing a trip. When either primary power or logic circuit power was applied with the chute deploy switch 150% overloaded (7.5 amperes), a trip occurred in 3.0 milliseconds at +27°C and +80°C and in 4.0 milliseconds at -55°C. When a 150% overload condition existed and manual reset was attempted (after trip-out), the circuit tripped out again after conducting for only 50 microseconds at all temperatures. The circuit will trip in 50 microseconds if an overload occurs when the circuit is conducting normally. The increased

TABLE 18A

Negative Power Supply (PS2) Performance Data

Volts in (vac)	Volts out at +80°C (vdc)	Volts out at +27°C (vdc)	Volts out at -55°C (vdc)	Load (ma)
109	-6.8	-6.4	-6.4	No load
115	-7.2	-6.8	-6.7	↓
121	-7.5	-7.1	-7.1	↓
109	-6.7	-6.3	-6.3	50
115	-7.0	-6.7	-6.7	↓
121	-7.4	-7.1	-7.0	↓
109	-6.6	-6.3	-6.2	70
115	-6.9	-6.6	-6.6	↓
121	-7.4	-7.0	-6.9	↓

TABLE 18B

Negative Regulator (VR3) Performance Data

Volts in (vac)	Volts out at +80°C (vdc)	Volts out at +27°C (vdc)	Volts out at -55°C (vdc)	Load (ma)
109	-3.80	-3.75	-3.80	No load
115	-3.80	-3.80	-3.90	↓
121	-3.85	-3.80	-3.95	↓
109	-3.45	-3.40	-3.50	50
115	-3.50	-3.45	-3.60	↓
121	-3.60	-3.55	-3.70	↓
109	-3.30	-3.10	-3.40	70
115	-3.35	-3.20	-3.50	↓
121	-3.45	-3.30	-3.60	↓

TABLE 19

Chute Deploy Overload Circuit Voltages at +27°C

Circuit	Location	Voltage Normal(vdc)	Tripped Out Voltage(vdc)
DA1	Q1A/C	15.3	15.3
	B	8.3	8.4
	E	7.8	8.0
	Q1B/C	12.5	10.0
	B	8.3	8.5
	E	7.8	8.0
AP3	Q1C	15.3	15.3
	B	8.6	7.6
	E	8.8	8.8
	Q2C	0	0.3
	B	15.2	15.2
	E	12.2	12.2
FF1	Q1A	10.3	1.5
	GA	10.0	1.1
	C	0.7	0.7
	GC	0	0.3
AP4	Q1C	6.4	11.2
	B	6.8	2.8
	E	6.2	6.2
	Q2C	8.3	-0.5
	B	7.9	11.2
	E	8.8	8.8
	Q7C	1.5	28.0
	B	2.1	-0.5
	E	0	0

TABLE 20

Original Overload Circuit Performance Data

Ambient Temperature (°C)	Essential Bus Voltage (vdc)	Tripping Current (amps)	Volts across Rs at trip point (vdc)
+80	27	3.9	--
↓	28	4.0	--
	30	4.4	--
	33	4.9	--
+27	27	4.9	0.30
↓	28	5.0	0.30
	30	5.2	0.31
	31	5.4	0.32
	33	5.7	0.34
-55	27	7.6	--
↓	28	7.8	--
	30	8.3	--
	33	8.8	--

TABLE 21A

Modified Chute Deploy Overload Circuit Performance Data

Ambient Temperature (°C)	Essential Bus Voltage (vdc)	Tripping Current (amps)
+80	27	3.9
↓	28	4.0
↓	33	4.9
+25	27	4.6
↓	28	4.8
↓	33	5.7
-55	27	5.9
↓	28	6.2
↓	33	7.0

TABLE 21B

Saturation Voltages for the Q7 Power Switch while Conducting with 55 Milliamperes Base Drive

T_a (°C)	V_{ce} (vdc)	I_{load} (amps)
+85	1.35	3.0
+27	1.60	5.4
+27	1.70	6.3
-55	1.40	3.0

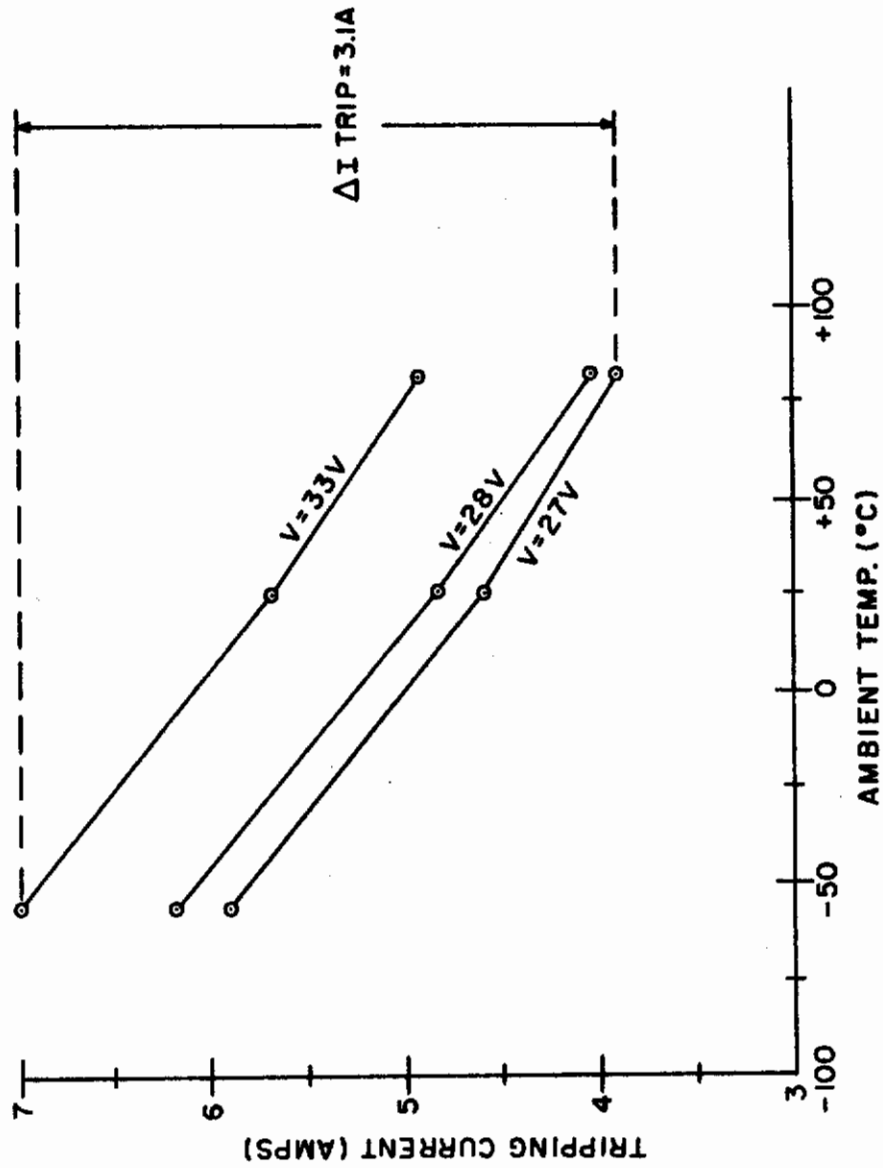
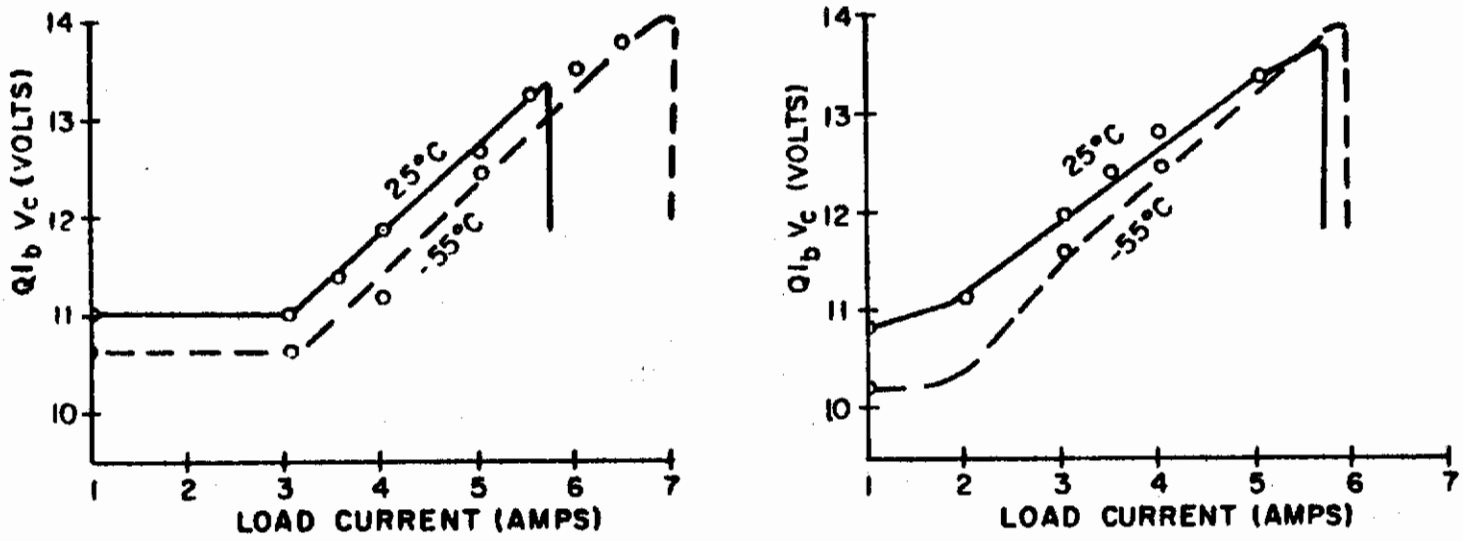


Figure 42. Modified DC Overload Circuit Performance

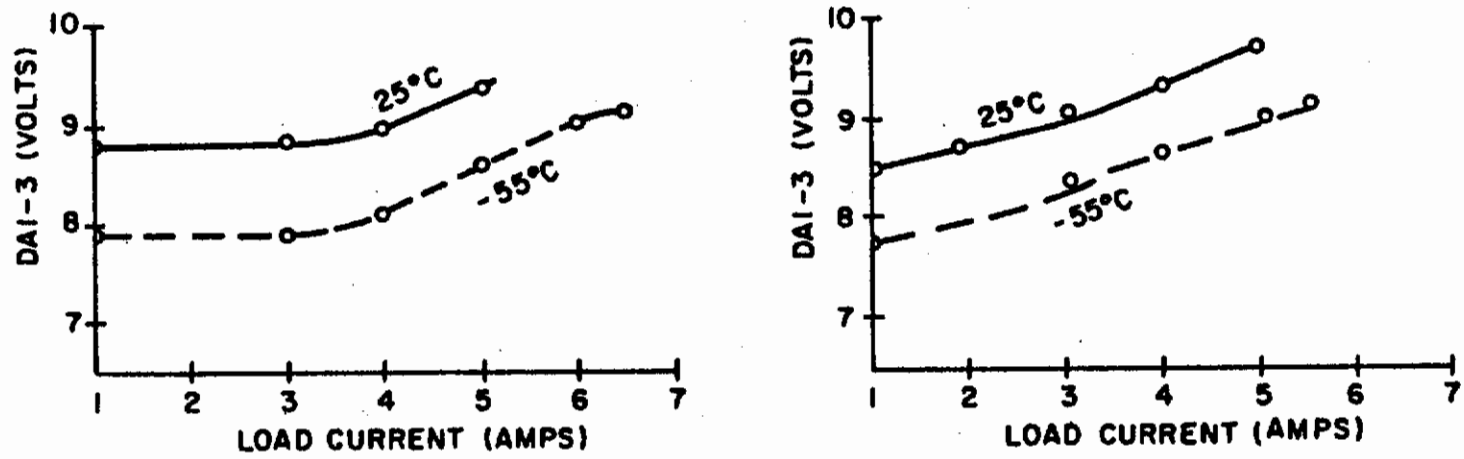
TABLE 22

Differential Amplifier (DA1) Performance Data

Ambient Temperature (°C)	Essential Bus Voltage (vdc)	Q1B V_C (vdc)	DA1 Output (vdc)	I_{load} (amps)
+25	27	10.8	8.5	1.0
		11.2	8.7	2.0
		12.0	9.1	3.0
		12.4	9.2	3.5
		12.8	9.4	4.0
		13.3	9.7	5.0
	33	11.0	8.8	1.0
		11.0	8.8	3.0
		11.4	8.9	3.5
		11.8	9.0	4.0
		12.7	9.4	5.0
		13.0	9.5	5.5
-55	27	10.2	7.7	1.0
		11.6	8.4	3.0
		12.5	8.7	4.0
		13.5	9.1	5.0
		13.7	9.2	5.5
	33	10.6	7.9	1.0
		10.6	7.9	3.0
		11.2	8.2	4.0
		12.5	8.7	5.0
		13.5	9.1	6.0
		13.7	9.2	6.5



(a) $Q1_b$ Collector Volts versus Load Current



(b) DA1 Output versus Load Current

Figure 43. Differential Amplifier Performance

time at turn-on is due to a self-induced delay to allow for control input switch contact bounce. A 10 to 15 second interval was required between manual reset attempts. This data was taken at +27 vdc and +33 vdc and was identical for both conditions.

6.1.4 X2a, X2b, and Associated Amplifiers (AP1, AP2)

X2a is the external power interlock and X2b is the dc generator power interlock. They are illustrated in the system block diagram, Figure 11. The relay coils in the collector circuit of X2a and X2b are outside the solid state matrix as defined by system bounds; however, they are shown to illustrate the addition of diodes across the coils for transient suppression. The amplifiers AP1 and AP2 are shown in Figure 18. Preliminary operating checks were conducted and a minor modification of AP1 was made; then circuit voltages were measured and this data is presented in Tables 23 and 24.

Performance of X2a and X2b control circuits was determined by checking for saturation of the output transistors when the proper control inputs were present. X2a switches on when F is present and off when $\overline{F}$ is present. X2b switches on when G and $\overline{F}$ are present and off when either $\overline{G}$ or F are present. Performance data for the power switches is presented in Tables 25A and 25B. In addition to this data, the X2b circuit was tested up to +90°C without negative bias with no noticeable degradation in performance.

6.1.5 Battery to Essential Bus Switch X3

Battery switch X3 can be regarded as consisting of X3 itself, its firing circuit, FC1, and its turn-off circuit, TO1, as shown in Figure 11. The turn-off circuit, TO1, is shown in Figure 17. The firing circuit for X3, FC1, is shown in Figure 16. These circuits were given a few preliminary operating checks, modified as required, and then performance tested while integrated into the dc control section of the dc power system. The dc firing circuit voltages are given in Table 26 and the turn-off circuit voltages are given in Table 27. Pertinent waveforms are presented in Figures 44 and 45.

Battery switch X3 operated well over the full temperature range. The maximum load current that could be turned off varied from 46 to 35 amperes; however, additional capacitance could be added to increase load turn-off capability under high and low temperature operation. Maximum turn-off capability for the battery switch as tested is presented in Table 28A. Saturation voltages are presented in Table 28B. The leakage current for the X3 power switch while in the off condition was measured. It was 3.5 milliamperes at a case temperature of +125°C. Since negligible power was being dissipated internally, the junction temperature was also about +125°C.

TABLE 23

External Power Interlock (X2a and AP1) Circuit Voltages at +27°C

Circuit	Location	X2a off (vdc)	X2a on with 365 ma load (vdc)
X2a	X2a/C	28.0	0.2
↓	B	- 2.55	0.8
	E	0	0
AP1	Q1C	8.4	0.85
↓	B	0	1.3
↓	E	0.7	0.7
↓	Q2C	- 2.55	5.8
↓	B	8.4	5.3
↓	E	6.2	6.2

TABLE 24

Generator Power Interlock (X2b and AP2) Circuit Voltages at +27°C

Circuit	Location	X2b off (vdc)	X2b on with 185 ma load (vdc)
X2b	X2b/C	28.0	0.1
↓	B	- 2.55	0.7
	E	0	0
AP2	Q1C	8.4	0.8
↓	B	0	1.35
	E	0.7	0.7
	Q2C	- 2.55	5.9
	B	8.3	5.4
↓	E	6.2	6.2

TABLE 25A

Performance Data for X2a and X2b when Conducting

Switch	Ambient Temperature (°C)	Bus Voltage (vdc)	Load Current (amps)	$V_{ce\ sat}$ (vdc)
X2a	+80	28	0.365	0.26
↓	+80	33	0.430	0.30
	+27	28	0.365	0.20
	-55	28	0.365	0.16
	-55	33	0.430	0.20
X2b	+80	28	0.185	0.13
↓	+80	33	0.218	0.15
	+27	28	0.185	0.10
	-55	28	0.185	0.07
	-55	33	0.218	0.10

TABLE 25B

Performance Data for X2a and X2b when Not Conducting

Switch	Case Temperature (°C)	Leakage Current (μamps)
X2a	+150	14
↓	+125	8
	+100	6
X2b	+150	14
↓	+125	8
	+100	6

TABLE 26

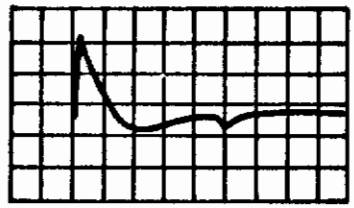
DC Firing Circuit (FC1) Voltages at +27°C

Location	X3 Off (vdc)	X3 On (vdc)
Q1C	0.8	8.0
B	1.3	0
E	0.7	0.7
Q2B1	0	+ 5 v pulse, 60 usec
B2	17.3	17.0
E	0.8	8.0

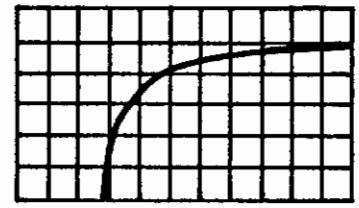
TABLE 27

X3 Turn-off Circuit (T01) Voltages at +27°C

Location	X3 Off (vdc)	X3 On (vdc)
Q1C	10.0	0.8
B	0.1	1.35
E	0.7	0.7
Q2B1	0	0
B2	23.8	23.5
E	10.0	1.2
Q3A	1.1	27.5
C	0.1	0

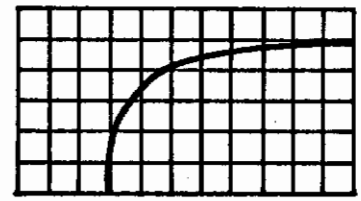


(a) X3 Gate
Vert. 1 v/division
Horz. 50 μ sec/division



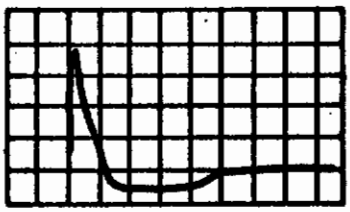
(b) X3 Cathode
Vert. 5 v/division
Horz. 5 μ sec/division

(c) TO1-Q3 Cathode
Vert. 5 v/division
Horz. 50 μ sec/division

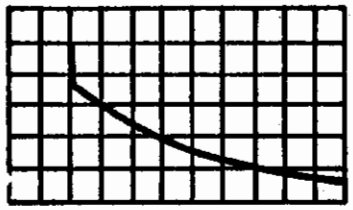


(d) TO1-Q3 Cathode
Vert. 5 v/division
Horz. 5 μ sec/division

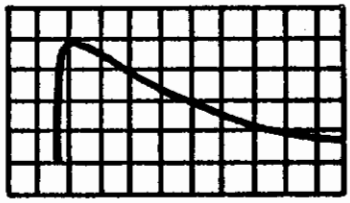
Figure 44. X3 Turn-On Waveforms



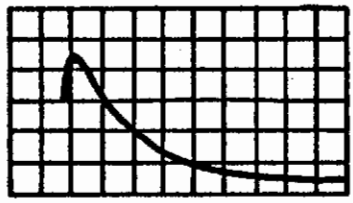
(a) TO1-Q3 Gate
Vert. 1 v/division
Horz. 50 μ sec/division



(b) TO1-Q3 Anode
Vert. 5 v/division
Horz. 20 μ sec/division



(c) TO1-Q3 Cathode
Vert. 5 v/division
Horz. 20 μ sec/division



(d) X3 Cathode
Vert. 10 v/division
Horz. 50 μ sec/division

Figure 45. X3 Turn-Off Waveforms

TABLE 28A

X3, FC1, and T01 Performance Data

Ambient Temperature (°C)	Essential Bus Voltage (vdc)	Max I_{load} Turned Off (amps)
+80	27	35
↓	28	35
	33	40
+25	27	38
↓	28	39
	33	46
-55	27	35
↓	28	36
	33	43

TABLE 28B

Saturation Voltages for the X3 Power Switch while Conducting 40 Amperes

Ambient Temperature (°C)	V_{ak} (vdc)
+80	1.45
+25	1.45
-55	1.40

6.1.6 Voltage Sensor (VS1, VS2)

The voltage sensor shown in Figure 15 was constructed, given some preliminary checks, modified, and evaluated. The performance data is given in Table 29.

6.1.7 DC Control Section Storage Test

A storage test was conducted by storing the entire dc control section at an ambient temperature of +122°C for approximately 2 hours. The temperature was then returned to +25°C and an operational check was performed. All circuits performed satisfactorily.

6.2 Experimental TR Control Section

The TR control section is shown in Figure 11. The experimental TR control section consists of X4, X5, X8, ac overload circuits, OS1, a regulated power supply, and the associated gates and firing circuits. This differs from the complete TR control section in that only one ac switch was constructed, although the control outputs to the other ac switches were monitored throughout the evaluation to assure proper operation of the complete logic section.

Extensive testing of the experimental TR control section began after completion of the tests of the dc control section. Test data is presented in the following sections.

6.2.1 Three Phase AC to DC Power Supply (PS1) and Regulators (VR4, VR5)

The three phase ac to dc power supply and regulators are shown in Figure 13. They were given some preliminary tests to assure proper operation when integrated into the experimental TR control section. The regulators which were used in conjunction with PS1 were the same regulators used during previous dc control section tests. Refer to Table 30 for the ac to dc power supply performance data and Tables 16 and 17 for regulator circuit voltages and performance.

A requirement exists for +9 vdc at 0.7 amp peak current to supply the output pulse amplifiers in the ac firing circuit. The circuit supplying it is shown in Figure 13 as T1c, CR7-9, and C2.

6.2.2 AC Firing Circuit

The ac firing circuit shown in Figure 21 was constructed and evaluated by using it as ACFC2 to control X8. The circuit voltages are given in Table 31. Using this type of firing circuit and with a primary line frequency of 400 cps, a maximum turn-on phase delay of less than 5° was observed.

TABLE 29

Voltage Sensor (VS1, VS2) Performance Data

Ambient Temperature (°C)	Bus Voltage (vdc)	Output Voltage (vdc)
+80	16.2	0.30
	17.0	0.47
	20.0	1.22
	24.8	2.50
	30.0	3.90
	33.0	4.70
+27	16.0	0.30
	18.5	0.50
	20.7	1.00
	26.5	2.50
	30.0	3.50
	35.0	5.00
-55	15.9	0.30
	17.0	0.55
	20.0	1.35
	24.4	2.50
	30.0	4.00
	33.0	4.80

TABLE 30

AC to DC Power Supply (PS1) Performance Data

Volts in (vac)	Volts out at +80°C (vdc)	Volts out at +27°C (vdc)	Volts out at -55°C (vdc)	Load
109	30.0	30.0	29.5	No load
115	31.9	31.5	31.5	↓
121	33.6	33.5	33.5	↓
109	25.6	26.0	26.5	Full load
115	27.1	27.2	28.0	at 300 ma
121	28.7	28.5	29.5	↓

The output pulse driver, Q5, dissipates pulses of approximately 0.65 watts peak power at a duty cycle of 33% or an average power dissipation of 0.215 watts. At an ambient temperature of +80°C, the case temperature of Q5 was + 100°C; therefore, the thermal resistivity from case to ambient of Q5 was 91°C/W.

6.2.3 AC Switch

The three phase ac switch appears in Figure 11 as X6, X7, X8, and X9. One ac switch having three sections (X8a, b, c) was constructed and evaluated. Pertinent waveforms are presented in Figure 46 and show the gate triggers which turn on the ac switch and the output load voltage. Note the slight discontinuity at the crossover point of the output waveform. This is the turn-on point and where the slight phase delay is experienced.

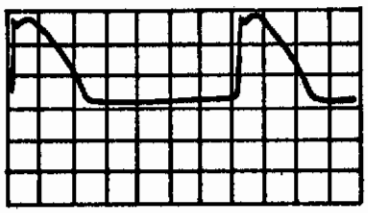
The voltage across the ac switch was measured at 1.5 V rms with a switch current of 4 amps rms/phase flowing and the case temperature at +125°C. Since the thermal resistance (θ_{jc}) is 2°C/W, and the power dissipation was 3 watts per SCR, the junction temperature rise of each SCR was 6°C above the case temperature. Thus, the junction temperature was +131°C. Leakage was measured for the ac switch in the off condition at an ambient and case temperature of +125°C. The leakage current which flowed during this test was 3 ma/phase.

The test load for the ac switch consisted of 500 ohms per phase per-loading, a three phase autotransformer, and the bridge rectifier with either

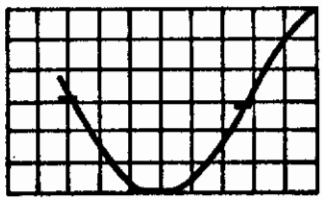
TABLE 31

AC Firing Circuit Voltages at +25°C

Location	AC Switch Off (vdc)	AC Switch On (vdc)
Q1C	0.8	5.6
B	3.4	0
E	0.7	0.7
Q2B1	11.0	10.6
B2	0.2	+1.3 V pulse, 8usec
E	0.8	5.6
Q3C	11.5	-9.0 V pulse, 6usec
B	0.2	+1.3 V pulse, 8 usec
E	0.7	0
Q4C	0.4	+8.0 V pulse, 5 usec
B	11.4	-6.0 V pulse, 8 usec
E	9.0	9.0
Q5C	9.0	-2.5 V pulse, 5 usec
B	0.4	+5.5 V pulse, 5 usec
E	0	+5.0 V pulse, 5 usec
Output	0	+3.0 V pulse, 12 usec



(a) AC Switch Gate Triggers
Vert. 1 v/division
Horz. 5 μ sec/division



(b) AC Switch Output Voltage
Vert. 50 v/division
Horz. 0.2 μ sec/division

Figure 46. AC Switch Waveforms

the battery charging load or the essential bus load. Figure 47 illustrates the simulation of the actual transformer.

6.2.4 AC Overload Detection Circuit

The ac overload detection circuit consists of T13, T14, T15, BR1, BR2, BR3, LD1, FF2, and MR2. All circuits except the transformers are shown in Figure 22. The ac overload circuit voltages are presented in Table 32.

TABLE 32

AC Overload Circuit Voltages at +25°C

Location	X8 Off (Volts)	X8 On (Volts)
T13, 14, 15 primary	0	0.5 V rms (r amp flowing)
BR1, 2, 3 output	0	10 vdc (5 amp flowing)
FF2 Q1B1	0	+3 v pulse (overload)
B2	5.8	5.8
E	0	+4 V pk (overload)

The maximum trip time experienced with a 150% overload (7.5 amps) was 1.2 milliseconds. The overload circuit performed satisfactorily when turned on into a short circuit. This applies over the complete temperature range. The overload circuit performance data is given in Table 33. Figure 48 illustrates rms tripping current variation with the variation of detector supply voltage over the specified temperature range.

Some spurious tripping of the ac overload circuit was experienced during preliminary testing. This was due to the 33 kcps pulses from the ac firing circuit. Shielding of gate leads, decoupling of supply leads, and some physical separation of LD1 and FF1 from the ac firing circuit corrected this problem.

6.2.5 Delay Gate Multivibrator (OS1)

The delay gate multivibrator is shown in Figure 20. It was given some preliminary operating checks and modified to improve performance. The circuit voltages for the modified circuit are presented in Table 34.

OS1 was evaluated while integrated into the experimental TR section and how well it performed its function is a measure of its performance. The pulse output from OS1 was 12 milliseconds wide at +80°C, 9 milliseconds wide at +25°C, and 8 milliseconds wide at -55°C. This pulse acts as the delay gate.

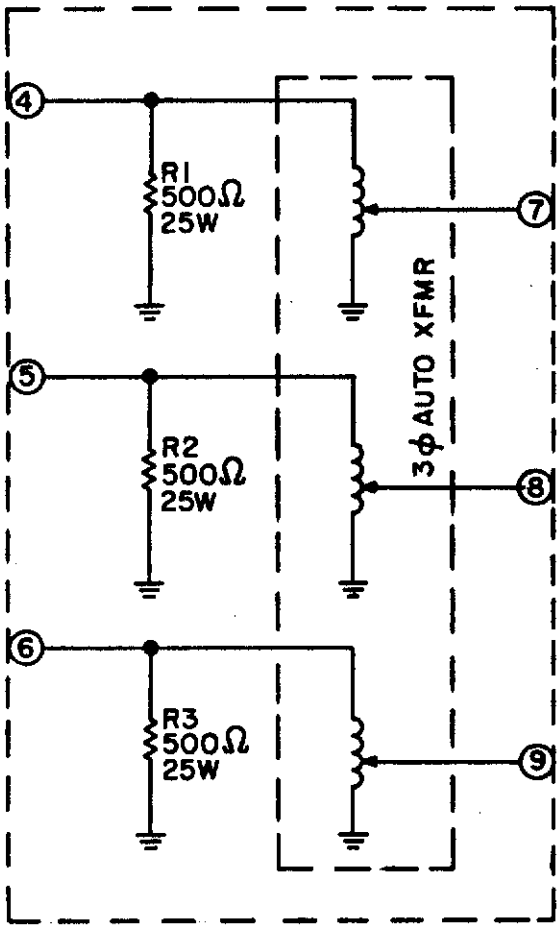


Figure 47. Simulation of TR Transformer, T1

TABLE 33

AC Overload Circuit Performance Data

Ambient Temperature (°C)	Detector Supply Volts (vdc)	I_{trip} (rms amps)
+80	5.6	4.55
↓	5.8	4.80
	6.0	4.85
	6.2	4.90
	6.4	5.05
+25	5.6	4.70
↓	5.8	4.90
	6.0	5.00
	6.2	5.10
	6.4	5.20
-55	5.6	5.00
↓	5.8	5.05
	6.0	5.10
	6.2	5.15
	6.4	5.20

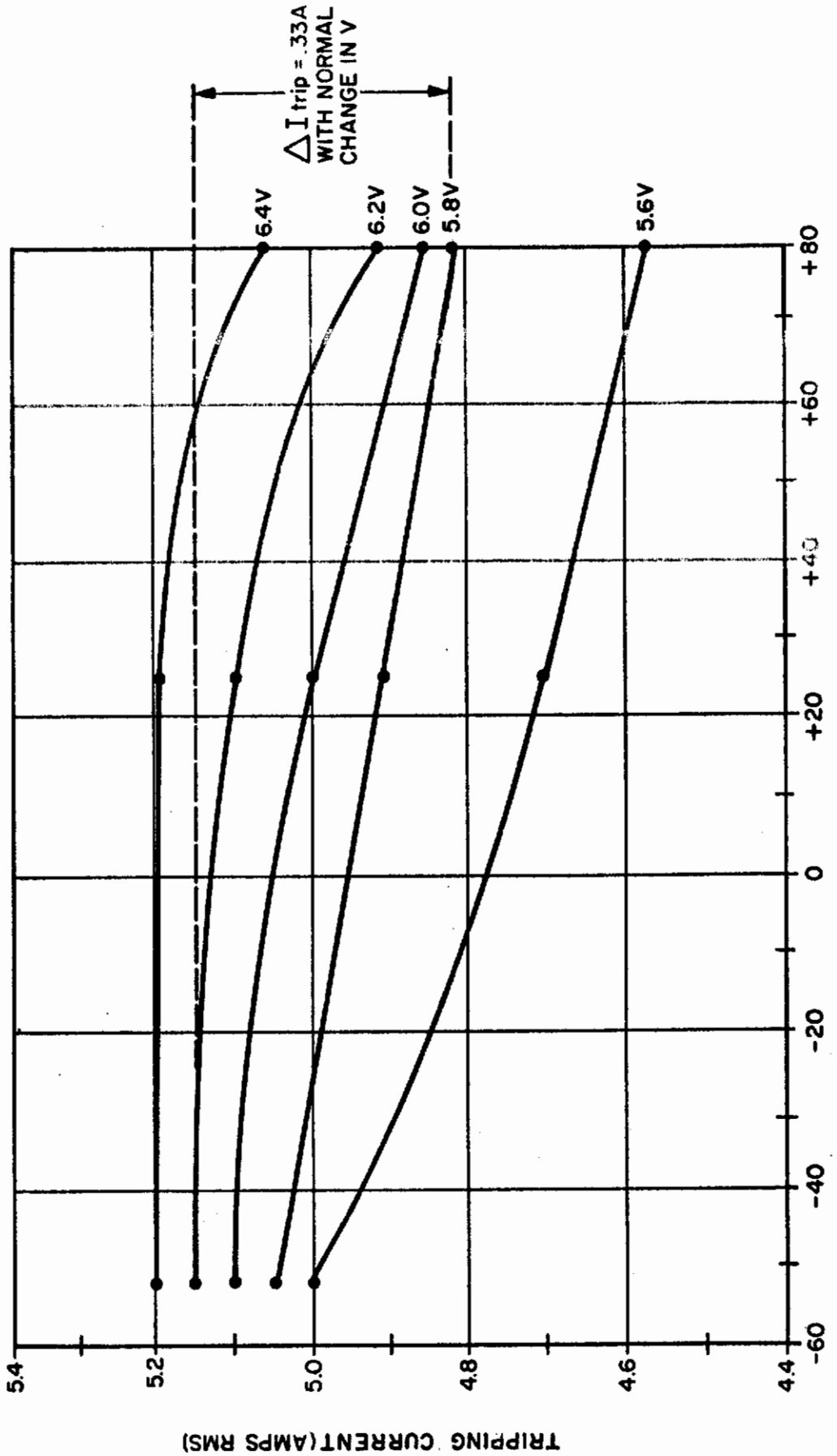


Figure 48. AC Overload Circuit Performance

TABLE 34

Delay Gate Multivibrator (OS1) Circuit Voltages at +25°C

Location	Stable State with Q1 Conducting (vdc)	Control Input Present (volts)
Q1C	0.1	+4 V pulse, 9 msec
B	0.7	-4 V pulse, 8 msec
E	0	0
Q2C	5.2	-4 V pulse, 9 msec
B	0.05	+0.5 V pulse, 9 msec
E	0	0

The functions which the delay gate performs are as follows: (1) it turns off either X6 or X8 depending on which is conducting at the time, thereby removing anode voltage from both X4 and X5; (2) it turns off FC2 and FC3 so that the system becomes insensitive to contact bounce in the logic switches. Thus, the delay gate from OS1 assures that all control circuits are stable before the correct power switch (X4 or X5) receives its turn-on signal. The delay gate pulse from OS1 performed its turn-off and delay functions satisfactorily; the logic provide proper control for the ac switch (X8) and at the simulated termination in place of X6.

6.2.6 X4 and X5 Firing Circuits (FC2, FC3)

FC2 and FC3 are identical to FC1 which was used in the dc control section tests. The circuit is shown in Figure 16 and circuit voltages are provided in Table 35. FC2 and FC3 were evaluated while integrated into the TR section. They were considered to have performed satisfactorily if their respective power switches functioned properly when the control inputs were correct for turn-on or turn-off. Both firing circuits performed satisfactorily over the specified temperature range.

TABLE 35

X4 and X5 Firing Circuits (FC2, FC3) Voltages at +25°C

Location	Power Switch Off (vdc)	Power Switch On (volts)
Q1C	0.8	7.4
B	1.3	0
E	0.7	0.7

TABLE 35 (Continued)

X4 and X5 Firing Circuits (FC2, FC3) Voltages at 25°C

Location	Power Switch Off (vdc)	Power Switch On (volts)
Q2B1	0	+5 V pulse, 60 usec
B2	17.3	17.2
E	0.8	7.4

6.2.7 X4 and X5 Power Switches

X4 and X5 are shown in Figure 11. They each consist of an SCR that is turned on by FC2 and FC3 respectively. The method of turn-off for X4 and X5 is to remove anode voltage. This is done by switching off the primary current to the TR by either X6 or X8 for 10 milliseconds with the delay gate. This has been accomplished at 20 amps for X4 and 10 amps for X5; all circuits operated satisfactorily.

The maximum load requirement for X4 is 43 amperes and for X5 is 10 amperes; thus, X4 was not tested at maximum load but X5 was. This was due to the current limitation of the autotransformer which was used to simulate T1 during testing. It limited the maximum load which could be placed on the TR section to approximately 20 amps dc. However, X4 is identcal to X3 in all respects except for the method of turn-off. Since X3 performed properly under a 43 amp load, X4 will also. All thermal data applying to X3 applies to X4 since the same maximum load exists, the same type SCR was used, and the same type heat sink was used.

X4 had an anode to cathode voltage drop of 1.2 v with a load of 20 amps when operating with a case temperature of +125°C. X5 had an anode to cathode voltage drop of 1.4 v with a load of 10 amps when operating with a case temperature of +110°C.

Leakage was measured by increasing T_a with the power switch on until T_c reached the maximum design value, then switching off and measuring leakage current. This method may not have been very accurate since the meter response was much slower than the thermal time constant of the SCR; however, the reading obtained is presented here as being in the same order of magnitude as the maximum leakage current. X4 exhibited a leakage current of 0.2 ma when the case temperature was +125°C. X5 exhibited a leakage current of 0.5 ma when the case temperature was +110°C.

6.2.8 Experimental TR Control Section Storage Test

A storage test was conducted by storing the entire experimental TR control section at an ambient temperature of +122°C for approximately two hours. The temperature was then returned to+25°C and an operational check was performed. All circuits performed satisfactorily.

6.3 Experimental Anti-ice System

The portion of the anti-ice system which was tested included the complete logic and control section, warning light section with overload protection, motor-driven valve section, and the temperature control with overload protection. DC power supplies, both positive and negative, were used to power these circuits; however, no new test data was taken because they are basically the same as the power supplies evaluated in the dc control section of the dc power system. The dc overload circuit performance was re-evaluated, but circuit voltages were not retaken. These voltages are the same as the dc overload circuit voltages recorded in the dc control section of the dc power system. After one minor logic modification, the detailed logic block of the control circuits performed as specified in the anti-ice sequence charts, Figures 36 and 37.

6.3.1 Time Delay Circuits

The time delay circuits are SD10, SD11, SD12, and associated amplifiers AP26, AP27, and AP28. They are illustrated in Figures 31 and 32. Circuit voltages are presented in Table 36. The time delay circuits were given a few preliminary operating checks, modified slightly to improve their performance, and then evaluated over the specified temperature range. The time delay performance data is presented in Table 37. Note that the performance data indicates that the delay variations experienced were well within the tolerances of the electromechanical equivalents.

The delays were adjusted and timed. The 4 second delay was adjusted for 4 seconds. The upper and lower limits of adjustment were +0.2 and -0.5 seconds, respectively. The 18 second delay was adjusted for 18 seconds. The upper and lower limits of adjustment were +1.0 and -1.0 seconds, respectively. The 60 second delay was adjusted for 60 seconds. The upper and lower limits of adjustment were +1.2 and -1.5 seconds, respectively.

6.3.2 Warning Light System

The warning system is shown in Figure 28, the anti-ice block diagram. It was evaluated while integrated into the anti-ice section by providing the proper inputs and observing operation of the warning lights. The warning

TABLE 36

Time Delay Circuit Voltages at +25°C

Circuit	Location	Input Present (vdc)	No Input Present (vdc)
AP26	Q1C	0.8	11.8
	B	1.3	0.15
		0.7	0.7
	Q2C	8.9	0
	B	8.4	11.8
	E	9.0	9.0
	To FF21-R	4.4	0
	Q3C	0.8	14.9
	B	1.4	0
	E	0.7	0.7
SD10	Q1B1	0	+4.5 V pulse, 1.5 msec
	B2	14.2	14.2
	E	0.7	+8.7 V ramp, 4 sec
AP27, AP28	Q1C	0.8	11.8
	B	1.3	0.15
	E	0.7	0.7
	Q2C	8.9	0
	B	8.4	11.8
	E	9.0	9.0
	Q3C	0.8	14.9
	B	1.4	0
	E	0.7	0.7
SD11	Q1B1	0	+4.5 v pulse, 4 msec
	B2	14.2	14.2
	E	0.7	+8.7 v ramp, 18 sec
SD12	Q1B1	0	+4.5 v pulse, 12 msec
	B2	14.2	14.2
	E	0.7	+8.7 v ramp, 60 sec

TABLE 37

Time Delay Performance Data

Delay (sec)	Actual Delay at +80°C (sec)	Actual Delay at +25°C (sec)	Actual Delay at -55°C (sec)
4	4.2	4.0	3.6
18	18.5	18.0	17.5
60	64.0	60.0	55.0

light amplifier, AP23, is shown in Figure 35. The amplifier circuit voltages are given in Table 38. The power switch, Q6, did not require a heat sink so it was evaluated at +80°C. With a normal load of 160 ma flowing Q6 saturation voltage was 0.1 volt; however, with 2 amps flowing or the equivalent to a surge condition the saturation voltage was 0.5 volt. When Q6 was off and at a case temperature of +80°C, 30 microamps of leakage current flowed.

6.3.3 Warning Light Overload Circuit

The warning light overload circuit is identical to the modified overload circuit of the dc power system except for the bistable element which in the case of the warning light circuit is a Solid Circuit flip-flop. For overload circuit voltages, refer to chute overload circuit, Table 19 in the dc power system.

The normal warning light current is approximately 160 ma but due to the load current transient which occurs at turn-on the overload circuit trip must be set at 2.5 amps. A graph showing lamp current vs. time is presented in Figure 49; also presented is the technique used in making the measurement. The circuit trips when applying power into a 150% overload (3.7 amps) in 5 milliseconds. This time is mainly determined by the contact bounce of the main power switch. It trips with manual reset into a 150% overload (3.7 amps) in 50 microseconds. Circuit performance data is presented in Table 39 and a graphical representation of tripping current variation with variations in bus voltage and temperature is presented in Figure 50.

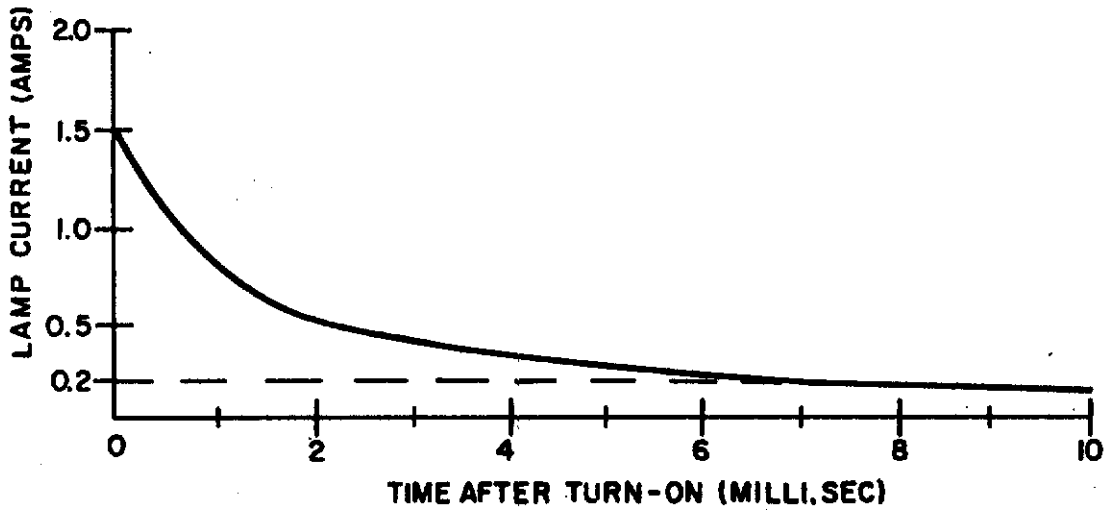
6.3.4 Motor-driven Valve Circuit

The motor-driven valve system is shown in Figure 28, the anti-ice block diagram. It was evaluated while integrated into the experimental anti-ice system. The valve simulator of Figure 34 was used to provide inputs simu-

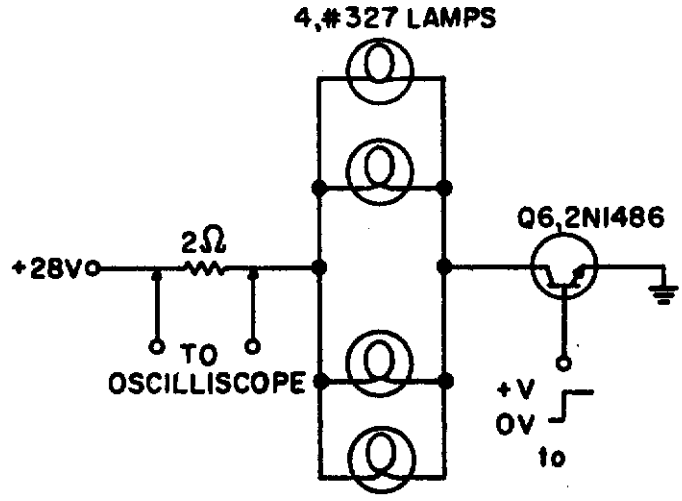
TABLE 38

Amplifier (AP21, AP23) Circuit Voltages at +25°C

Circuit	Location	Input Present (vdc)	Input Absent (vdc)
AP21, AP23	Q1C	0.8	14.8
↓	B	1.3	0
	E	0.7	0.7
	Q2C	11.9	- 2.2
	B	11.6	14.6
	E	12.1	12.1
AP21	Q3C	9.1	9.1
↓	B	9.6	- 2.2
	E	9.0	- 1.5
AP23	Q3C	9.1	9.1
↓	B	9.6	- 2.2
	E	9.0	- 1.5



(a) Lamp Current versus Time After Turn-On



(b) Method Used for Determining Lamp Surge

Figure 49. Lamp Current Surge at Turn-On

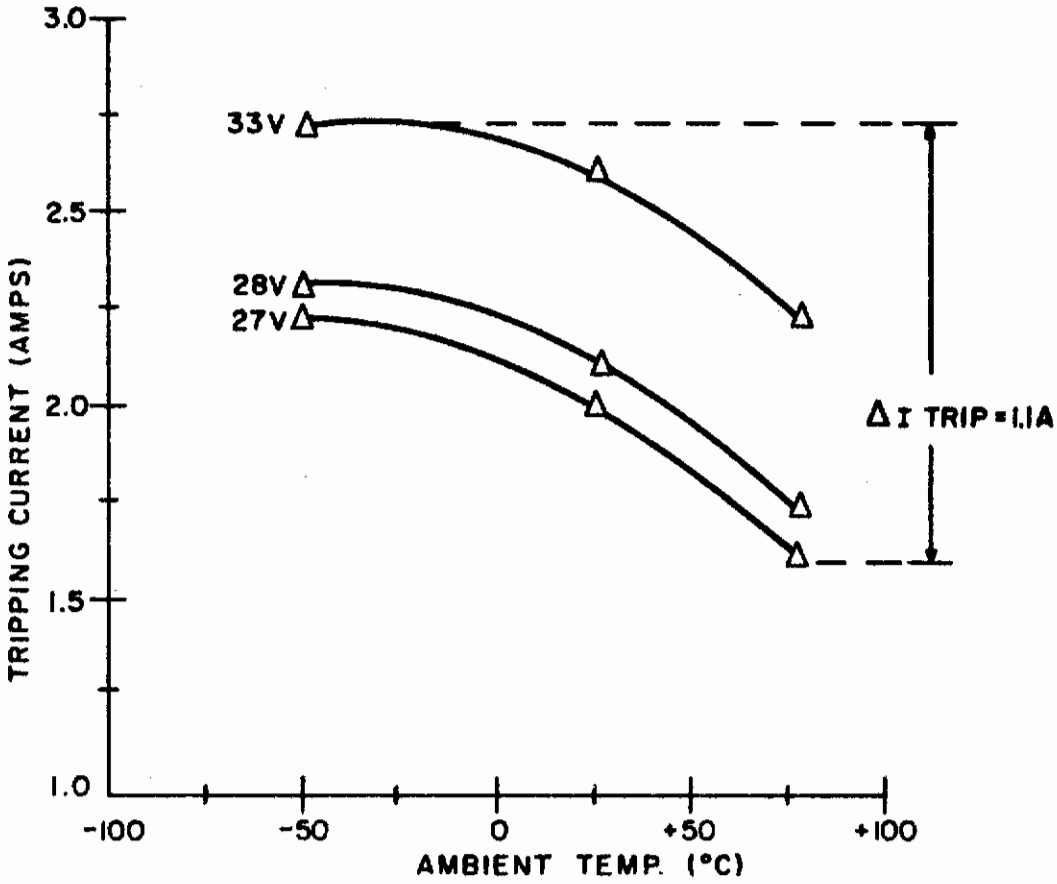


Figure 50. Warning Light Overload Circuit Performance

TABLE 39

Warning Light Overload Circuit Performance Data

Ambient Temperature (°C)	Essential Bus Voltage (vdc)	Tripping Current (amps)	Max. Load Turn-on (amps)
+80	27	1.6	1.5
↓	28	1.7	---
↓	33	2.3	2.1
+25	27	2.0	1.9
↓	28	2.1	---
↓	33	2.6	2.4
-55	27	2.2	2.1
↓	28	2.3	---
↓	33	2.7	2.6

6.3.4 Motor-driven Valve Circuit (Continued)

lating valve operation and the simulated valve load is shown in Figure 51. The circuit voltages for AP23 have been presented in Table 38 and power switch performance data is presented in Table 40.

TABLE 40

Performance Data for

Motor-driven Valve Power Switch (Q8 or Q9) while Conducting

V_{ce} (vdc)	I_{load} (amps)
1.25	2.5
1.45	3.0
1.60	3.5
1.80	4.5
2.30	6.0
2.80	8.0

Satisfactory operation was observed over the temperature range. The leakage current was measured when the power switch was in the off condition. It was

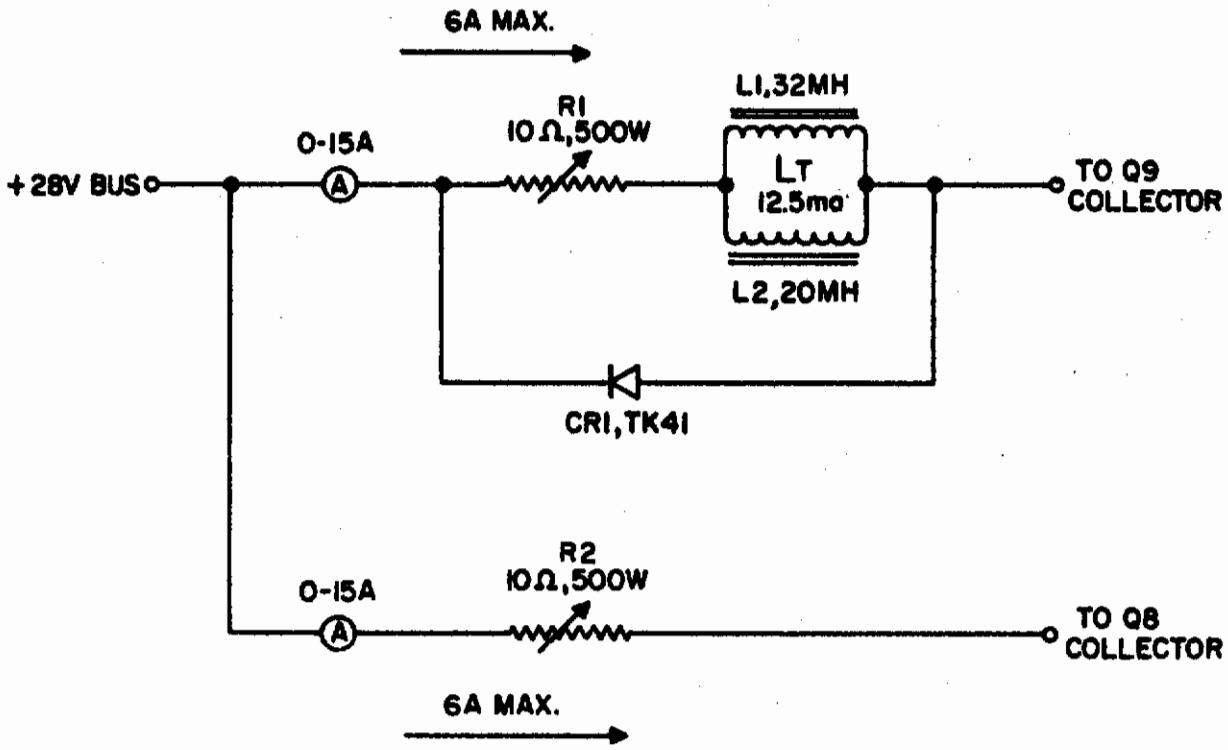


Figure 51. Simulation of Motor-driven Valve Load

1.5 milliamperes at a case temperature of +130°C. Since the internal power dissipation was negligible, the junction temperature was also about +130°C.

A general technique used to determine if the power switch was saturating was to increase the load current while observing the collector-to-emitter voltage. If that voltage increased linearly, then the switch was in saturation. This technique was used for Q9. Figure 52 is a graph of $Q9V_{ce}$ vs. $Q9I_c$ with I_b held constant.

6.3.5 Temperature Sensor (TS10)

The temperature sensor circuit controls the operation of the case heater, HR6. Its circuit is shown in Figure 33. It exhibited a snap-action turn-on with decreasing temperature at +13°C and a snap-action turn-off with increasing temperature at +18°C. This operation was entirely satisfactory. Circuit voltages for TS10 are presented in Table 41.

TABLE 41

Temperature Sensor (TS10) Circuit Voltages at +25°C

Location	Sensor at +23°C (vdc)	Sensor at +7°C (vdc)
Q1C	13.4	10.0
B	6.5	6.8
E	6.2	6.1
Q2C	1.5	11.8
B	13.4	11.4
E	12.1	12.1
Q3B1	0.1	1.5
B2	14.9	13.5
E	1.7	5.2

Normal circuit operational performance was determined as follows. First, the thermistor RT1 was suspended by its leads with a thermocouple mounted 1/2 inch away. Since +15°C is the design center of the allowable operating range, R2 was adjusted to turn on Q5 (with a load of 1.6 amps) at +13°C. Second, the turn-off temperature was determined; it took place at +18°C. TS10 switched Q5 on at +13°C in 30 microseconds with a temperature rate of change of -0.32°C/sec. (+21°C to +4.5°C in 55 seconds). TS10 switched Q5 off at +18°C in 40 microseconds with a temperature rate of change of +0.10°C/sec. (+4.5°C to +21°C in 170 seconds).

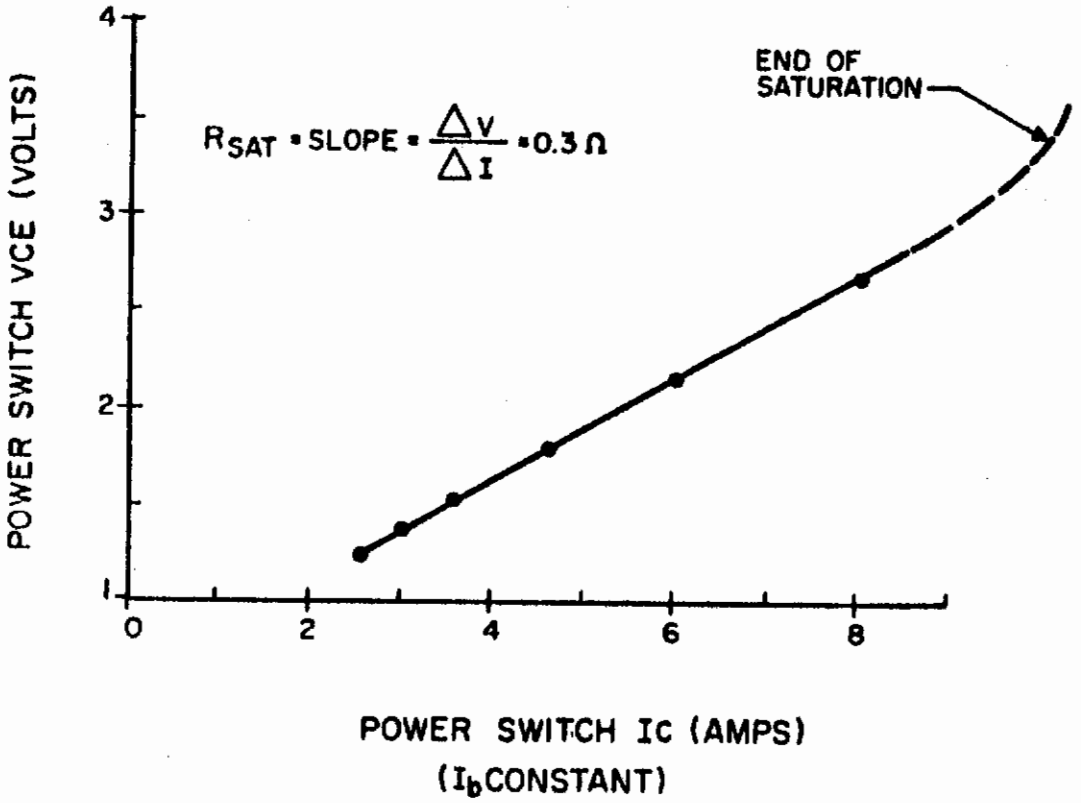


Figure 52. Determining Power Switch Saturation

In order to determine circuit performance over the specified temperature range, a 10K potentiometer was substituted for RT1 and then varied to the turn-on point when the reset of the circuit was at the temperature extremes. Then the values of RT1 were determined experimentally over the temperature range. The turn-on resistance value when the converted to a temperature equivalent based on the known temperature-resistance characteristics of RT1. A graph of RT1 resistance change versus temperature is shown in Figure 53.

At -55°C, a resistance greater than 9K ohms was required for turn-on; therefore, the equivalent temperature was +4°C. A resistance less than 6K ohms was required for turn-off; therefore, the equivalent temperature was +16°C.

At +80°C, a resistance greater than 5.1K ohms was required for turn-on; therefore, the equivalent temperature was +20°C. A resistance less than 4.9K ohms was required for turn-off; therefore, the equivalent temperature was +22°C.

Q5 does not require a heat sink and so its high temperature test was conducted at an ambient temperature of +80°C. With Q5 conducting and a case temperature of +115°C with a load of 1.6 amps, the saturation voltage was 1.1 volts. With Q5 off and a case temperature of +115°C, the leakage current was measured as being 0.5 ma.

6.3.6 Case Heater Overload Circuit

The overload detection circuit used in conjunction with TS10 is identical to DA1 and AP3 of the dc power system. This circuit differs from the warning light overload circuit in FF17, the bistable element. FF17 is an SCR which shunts RT1 when an overload occurs; this reverse biases Q1 of TS10; thereby turning off Q5. Refer to Section 6.1.3 for circuit voltages. Table 42 gives overload circuit performance data and Figure 54, is a graphical presentation of this data.

TABLE 42

Case Heater Overload Circuit Performance Data

Ambient Temperature (°C)	Essential Bus Voltage (vdc)	Tripping Current (amps)	Max. Load Turn-on (amps)
+80	27	1.18	1.15
↓	28	1.27	---
	33	1.68	1.64

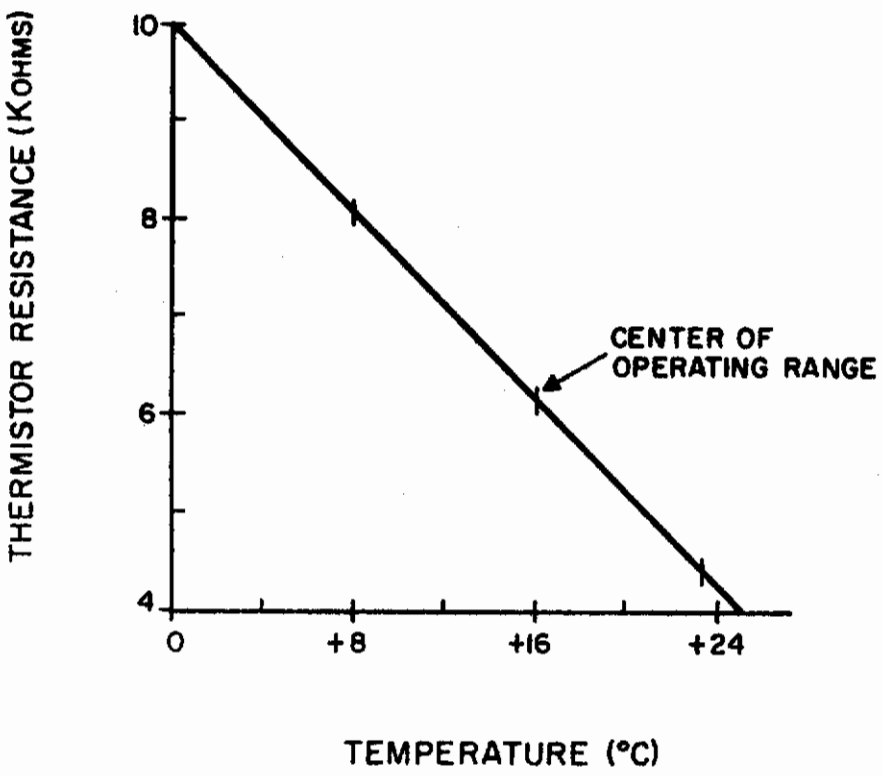


Figure 53. Resistance Variation of TS10-RT1 with Temperature

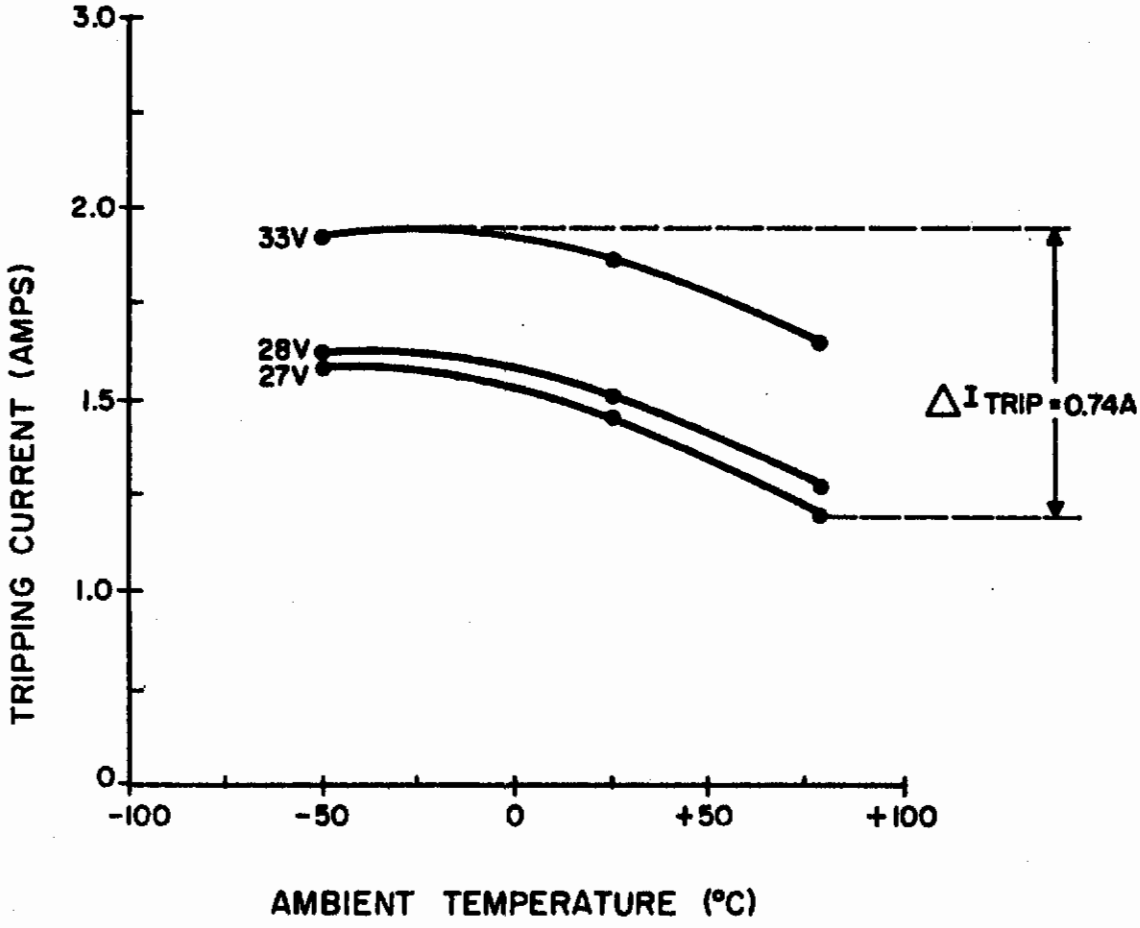


Figure 54. Case Heater Overload Circuit Performance

TABLE 42 (Continued)

Case Heater Overload Circuit Performance Data

Ambient Temperature (°C)	Essential Bus Voltage (vdc)	Tripping Current (amps)	Max. Load Turn-on (amps)
+25	27	1.46	1.40
↓	28	1.50	---
↓	33	1.86	1.85
-55	27	1.57	1.52
↓	28	1.60	---
↓	33	1.92	1.88

6.3.7 Experimental Anti-ice Section Storage Test

A storage test was performed by increasing the temperature of the entire experimental anti-ice section to +122°C for two hours, then returning the temperature to +25°C. The circuit performed satisfactorily after storage at +122°C.

7. ALTERNATE CIRCUITS

The alternate circuits are divided into two distinct classifications: (1) circuits which were part of the original design and proved to be undesirable for some reasons during testing; and, (2) circuits which were developed after the planned testing program.

Failures of the original equivalent solid state systems were always in terms of overall circuits rather than circuit components. Thus, an analysis of the cause of failure must be in terms of the inadequacy of a particular circuit for a particular task, rather than any component deficiency within a particular circuit. The systems described in sections 4 through 7 of this report were the modified and successful versions. However, the original solid state designs differed in several types of circuits.

The cause of failure for several of the original circuit designs is discussed here. The corrective action is represented by the technique employed in the tested systems.

With respect to the new alternate circuits, no cause of failure can be considered. Rather, the advantage of these circuits over those used in the tested systems must be considered.

7.1 Alternate Circuits from Original Design

In most cases where circuits were eliminated from the original design, complete performance tests were not performed; therefore, complete data is not available.

7.1.1 Phase Controlled Rectifier

The schematic of the phase controlled rectifier is shown in Figure 55. This circuit was designed to provide outputs of +36 vdc, +28 vdc and zero volts in order to eliminate tap switching of the TR transformer. Means were incorporated to provide automatic compensation for line voltage fluctuations and for phase unbalance without closed loop feedback.

CR7, 8, and 9 supply positive voltage to the control circuits whenever the anode voltage of an SCR swings positive with respect to ground. When the TR output is to be +36 vdc, Q6 conducts, and R9 and R10 control the firing angle. The firing delay angle in this case approaches zero. When the TR output is to be +28 vdc, Q6 is off and R11 is inserted in series with R9 and R10; hence, the delay angle is increased causing the effective output voltage to be reduced. When Q7 conducts, C2 is shunted and the peak point voltage of Q5 is not reached; therefore, no firing signal is developed

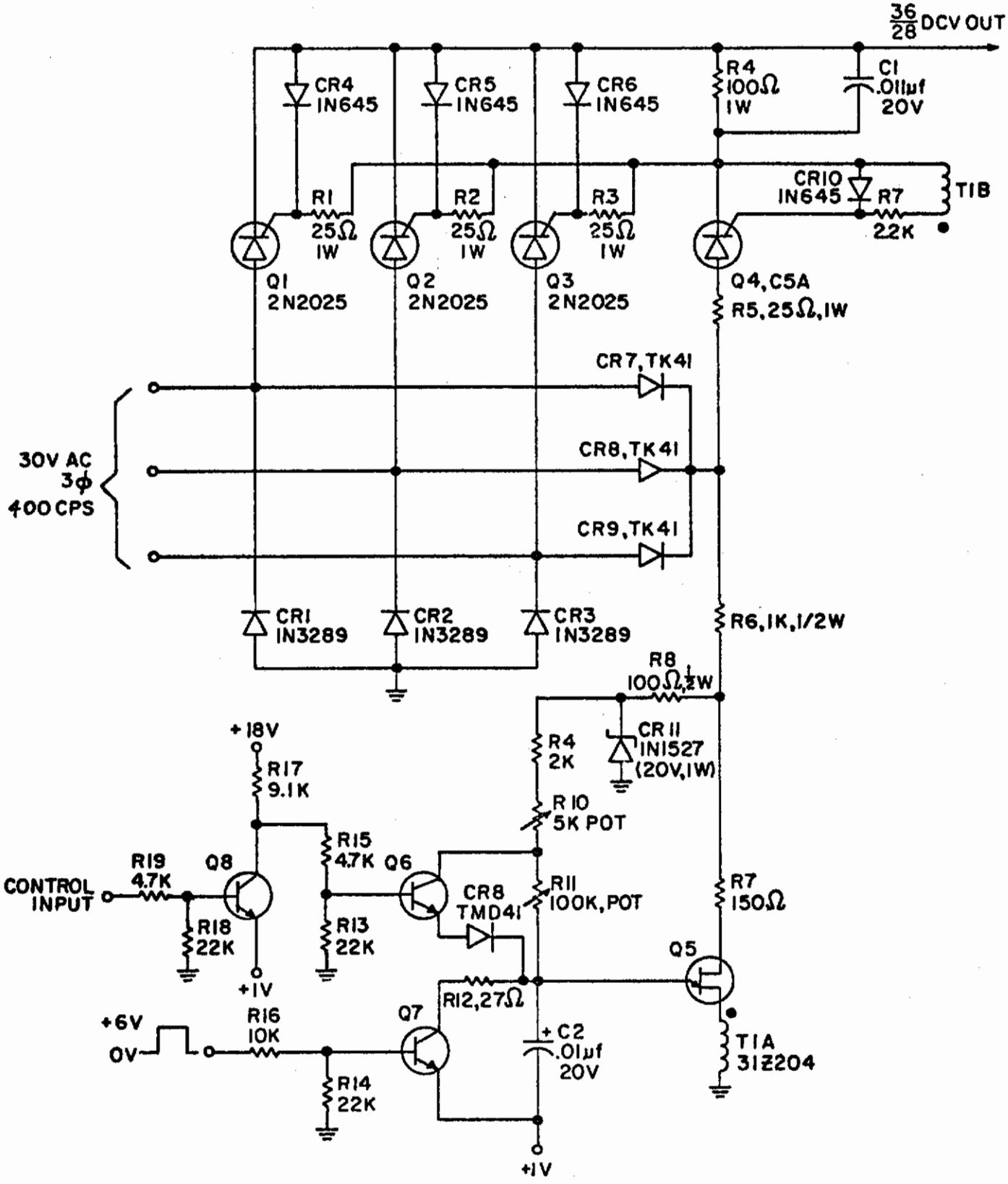


Figure 55. Phase Controlled, Full-Wave Bridge Rectifier

and the TR output is zero.

The phase controlled rectifier was eliminated from the original system due to the requirement of reproducing the electromechanical system outputs. In the electromechanical system the three phase bridge rectifier output ripple would be less than 4% without filtering. However, the phase controlled rectifier had 48% ripple when supplying the dc essential bus. A preliminary design for a choke input filter to reduce the ripple to less than 4% was prepared. The physical characteristics of the choke were determined to be 35 pounds and 230 cubic inches. Thus, it was decided to eliminate the phase controlled rectifier. However, if the nature of the dc essential bus load is such that the ripple problem can be disregarded, the circuit did perform satisfactorily at +25°C.

7.1.2 TR Detection Circuit

The schematic of the TR detection circuit is shown in Figure 56. Originally, it served as a logical detector for E_2 and E_1. However, in an attempt to enhance circuit reliability by decreasing circuit complexity, the logic inputs were revised in order to delete the requirement for the TR detection circuit; now A_1 and $\bar{A}_1$ replace E_2 and E_1.

The E_1 logic input was present when the nonessential bus voltage was greater than the following: (1) 18.5 vdc at +80°C; (2) 21.5 vdc at +25°C; (3) 23.5 vdc at -55°C. The E_2 logic input was present at +25°C when the voltage on the nonessential bus was greater than 33 vdc. Detailed performance data for the TR Detection Circuit is presented in Table 43.

TABLE 43

TR Detection Circuit Performance Data at +25°C

V_{in}(vdc)	E_1(vdc)	E_2(vdc)
18.5	0.5	0.0
20.7	1.0	0.0
26.5	2.5	0.0
30.0	3.5	0.7
35.0	5.0	1.7

7.1.3 Original AC Switch and Firing Circuit

The schematic of the original ac switch and firing circuit is shown in Figure 57. The original ac switch combined the characteristics of square-loop core materials with the characteristics of the SCR. If no current flows in T2-C, then both T1 and T2 are saturated by current flowing in their res-

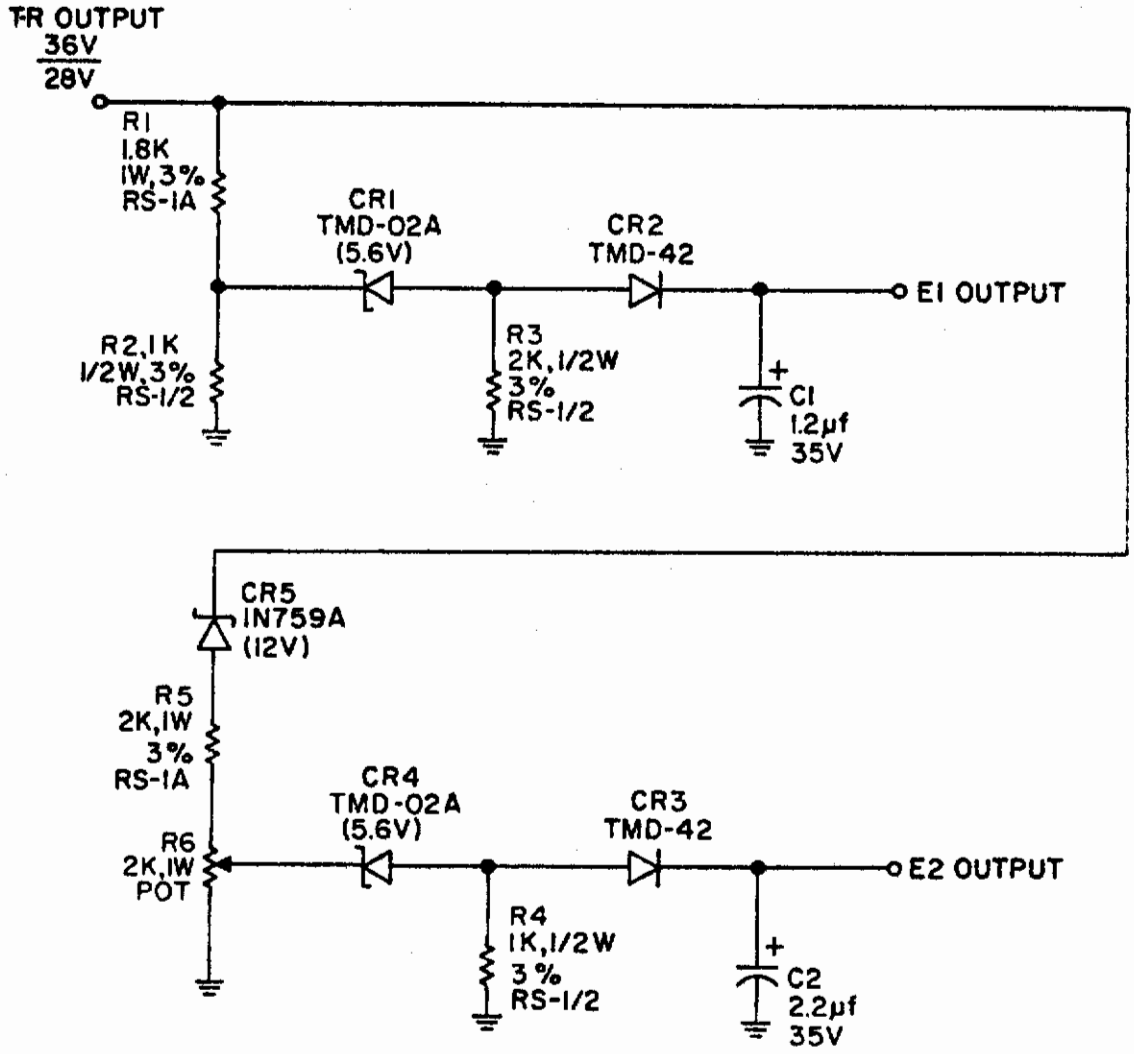


Figure 56. TR Detection Circuit

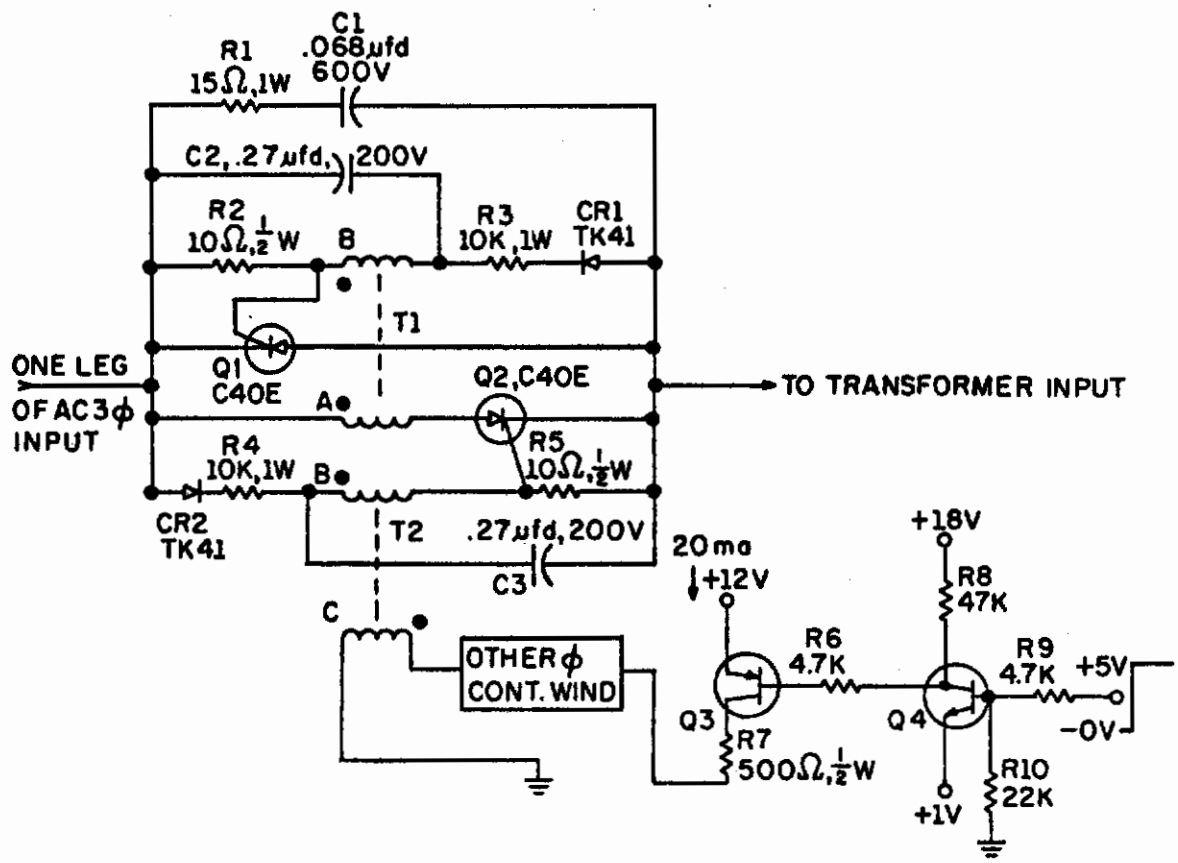


Figure 57. Original AC Switch and Firing Circuit

pective B windings during alternative halves of the voltage cycle. The gate voltage is limited to less than 0.25 volts; hence, neither SCR fires and no current flows to the load.

If current is now made to flow through T2-C, this core will reset. When the anode of Q4 starts to swing positive, T2-B will sustain part of the supply voltage and C3 will charge. Core 2 will saturate, discharging C3 through the gate of Q4. This turns on Q4 and current is delivered to the load. When Q4 conducts through T1-A, it resets core 1 and Q3 will fire on the following half cycle. R1 and C1 act as a filter to prevent line transients from triggering the switch. Transistors Q1 and Q2 provide control for the ac switch. As long as Q1 conducts, the ac switch remains in the conducting state; when Q1 is turned off, the ac switch turns off within one-half cycle by line commutation.

This circuit configuration proved unsatisfactory due to the relatively long delay angle. Since the delay angle was long, the output voltage waveform was quite distorted and the voltage across the switch rose to approximately 100 volts by the time the SCR fired. This high voltage rate of change with respect to time is undesirable with a reactive load.

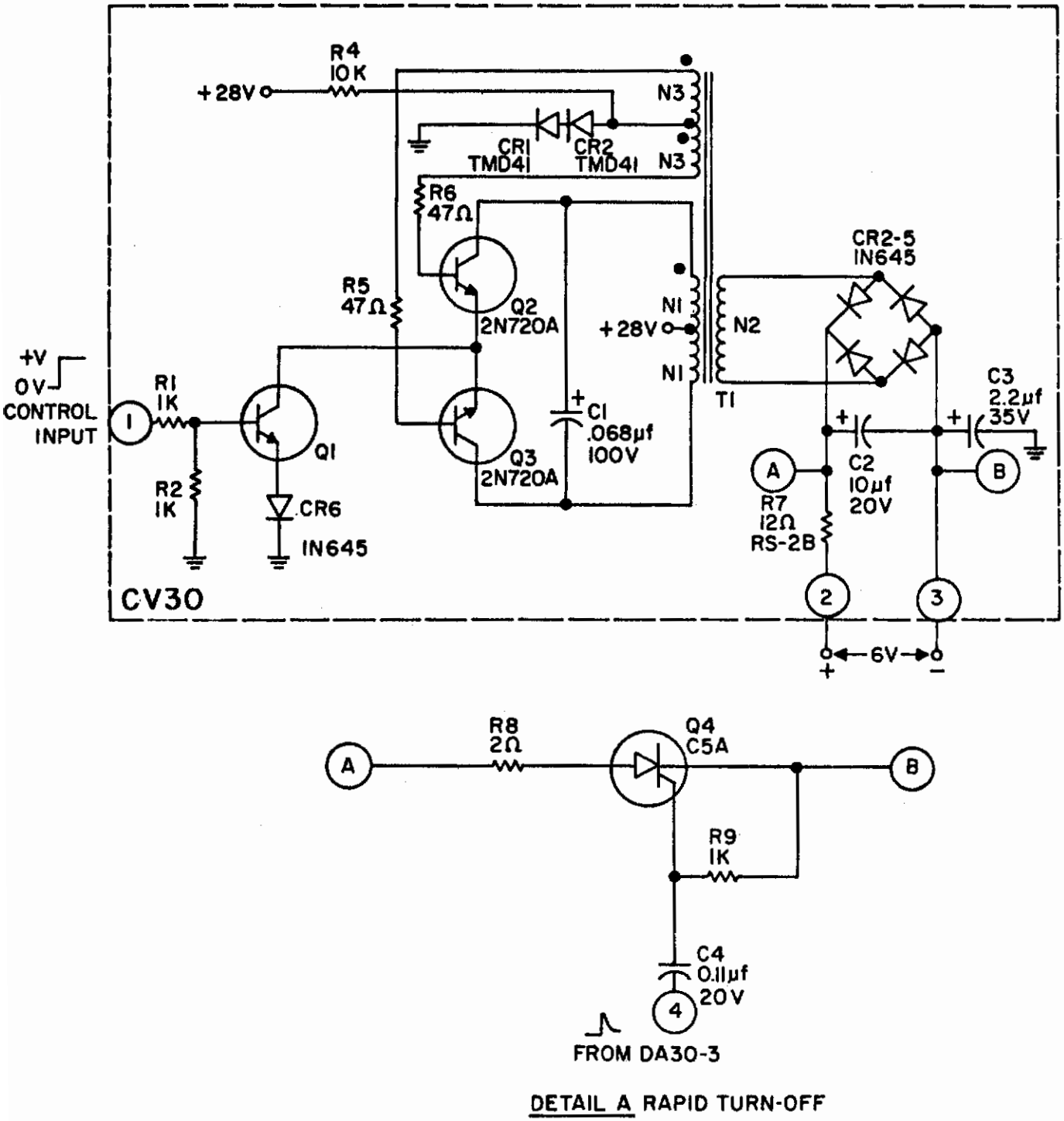
The circuit exhibited poor regulation characteristics in that a change in load from 1 amp to 2 amps caused a 10 V rms change in output voltage due to variation of the delay angle. The control current was quite critical requiring a narrow operating range of 15 ma ± 5 ma at + 25°C; this unsatisfactory condition might be eliminated with additional work on the magnetic firing circuit. Leakage current with the switch open was approximately 40 ma, primarily due to the filter made up of R1 and C1.

7.2 New Alternate Circuits

The following data is presented here to illustrate what may be done to improve further on the tested systems.

7.2.1 DC to DC Power Converter, CV30

A +28 vdc to 6 vdc power converter was designed and constructed for two reasons. First, to serve as a negative bias supply in conjunction with a zener shunt regulator. Second, to permit using a power switch in an emitter-follower configuration. The schematic of the dc to dc converter is shown in Figure 58. Some pertinent load and line regulation data is provided in Table 44. Note that V_{out} is the unregulated voltage out of the converter and not V_{out} of the shunt regulator.



DETAIL A RAPID TURN-OFF

Figure 58. DC to DC Power Converter

TABLE 44

DC to DC Converter Performance Data at +27°C

Vin (vdc)	V_{out}(vdc) No Load	V_{out}(vdc) 50 ma Load	V_{out}(vdc) 100 ma Load	V_{out}(vdc) 150 ma Load
27	5.7	5.0	4.8	4.7
28	5.9	5.2	5.0	4.9
30	6.4	5.7	5.5	5.4
33	7.2	6.4	6.1	6.0

When using the converter as a power supply, the input control amplifier Q1 may be eliminated and the emitters of Q2 and Q3 grounded. Q2, Q3, T1, C1 make up a 2.5 KC oscillator whose frequency is determined by T1. T1 consists of a square orthonol core, Magnetics, Inc., 50007-2A, where N1 is 65 turns of #28, N2 is 15 turns of #28, and N3 is 8 turns of #28. T1 is approximately 1.25 inches in diameter and 0.5 inches thick. N3 is the feedback winding which sustains oscillation. R4, CR1, and CR2 provide initial turn-on bias to assure that the circuit begins to oscillate with the application of 28 vdc. The 2.5 KC square wave output is transformed to a lower voltage by the turns ratio of N1 to N2. It is rectified by CR3 through CR6, and filtered by C2 and C3; the final dc output is current limited by R7.

7.2.2 Emitter-follower Power Switch

The converter described in section 7.2.1 was used as a power source to provide base drive to a power switch (2N2226) used in an emitter-follower configuration. Five milliamperes into the base of Q1 controls the converter and the power switch. The data given in Table 45 shows that the power converter provided sufficient base drive to saturate the power switch up to approximately 15 amps.

TABLE 45

Emitter-Follower Power Switch Performance Data at +25°C

Power Switch On		Power Switch Off	
I_{load}(amps)	$V_{ce\ sat}$(vdc)	$T_j = T_{case}$(°C)	$I_{leakage}$(ma)
2	1.10	+ 150	0.85
5	1.40	+ 100	0.40
7	1.75	+ 80	0.30
10	2.20		
15	(Load current limiting)		

The use of an emitter-follower as a power switch is shown in Figure 59. It also shows a cycling overload system which will be discussed in detail in a later section.

Q4 shown in detail A of Figure 58 provides a low resistance discharge path for C2 in order to decrease power switch turn-off time when operated as an emitter-follower. Without Q4, approximately 8 to 10 milliseconds elapse before turn-off is completed due to the discharge of C2 through the base-emitter junction of the power switch. When Q4 is used, turn-off is accomplished in 0.6 to 0.8 milliseconds. Of course, there may be cases where rapid turn-off would be a disadvantage, such as with a highly inductive load or where radio frequency interference becomes a prime consideration.

7.2.3 Improved DC Overload Circuit

7.2.3.1 Stabilized and Simplified Detector and Amplifier

An attempt to improve the operation and simplify the circuitry of the modified dc overload circuit was undertaken. It resulted in the improved version of the differential amplifier and bistable element shown in Figure 60. The data which indicates the improvement in performance is presented in tabular form in Table 46 and graphically in Figure 61.

The change to a balanced differential amplifier improved the temperature characteristics and the use of an SCR as the bistable element and amplifier resulted in considerable circuit simplification.

Note the increase in trip current that occurs with an increase in voltage in. This increase permits fusing closer to normal current flowing with any given V_{in} (assuming that the normal load resistance is constant). For example, suppose the normal load was 10 amps at 28 vdc in. If the input voltage is increased to 33 vdc, the load current will also increase by the ratio 33/28. Therefore, with 28 V_{in} and 10 amps flowing it would still be necessary to fuse at (33/28) (10) or 11.8 amps as the minimum fusing current. Thus, if the trip point did not increase with input voltage, then the fusing point at all voltages would have to be greater than the load current with 33 volts in.

7.2.3.2 Simplified Chute Deploy Overload Circuit

A simplified chute deploy overload circuit is shown in Figure 62; it could be used in place of the original chute deploy overload circuit. With the power switch on, Q2 $V_{ce\ sat}$ was 1.4 vdc and Q2 V_{be} was 2.1 v. After tripping occurred Q1 V_{ak} was 0.8 vdc and V_{be} was 0.05 vdc. At +27°C the tripping current varied with bus voltage as follows: (1) 4.8 amperes at 27 vdc; (2) 5.1 amperes at 30 vdc; and (3) 5.5 amperes at 33 vdc.

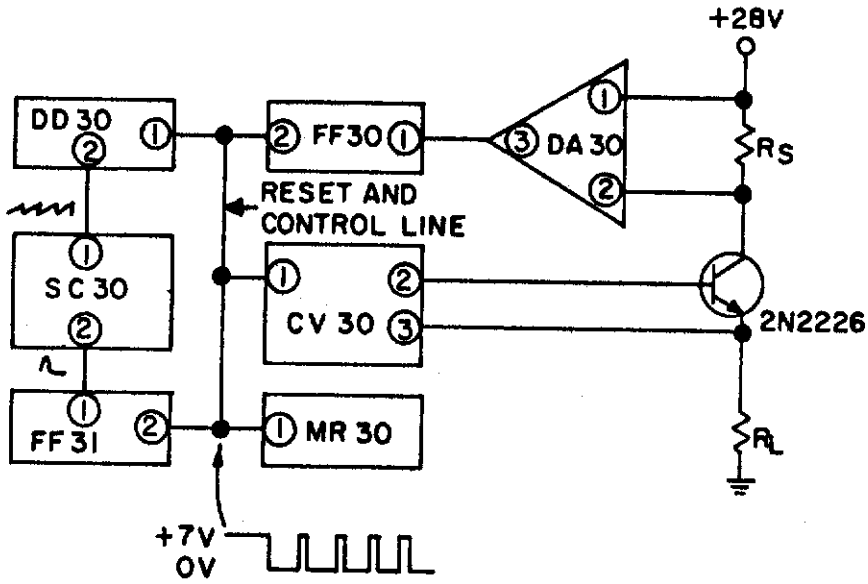


Figure 59. Emitter-Follower Power Switch with Cycling Overload System

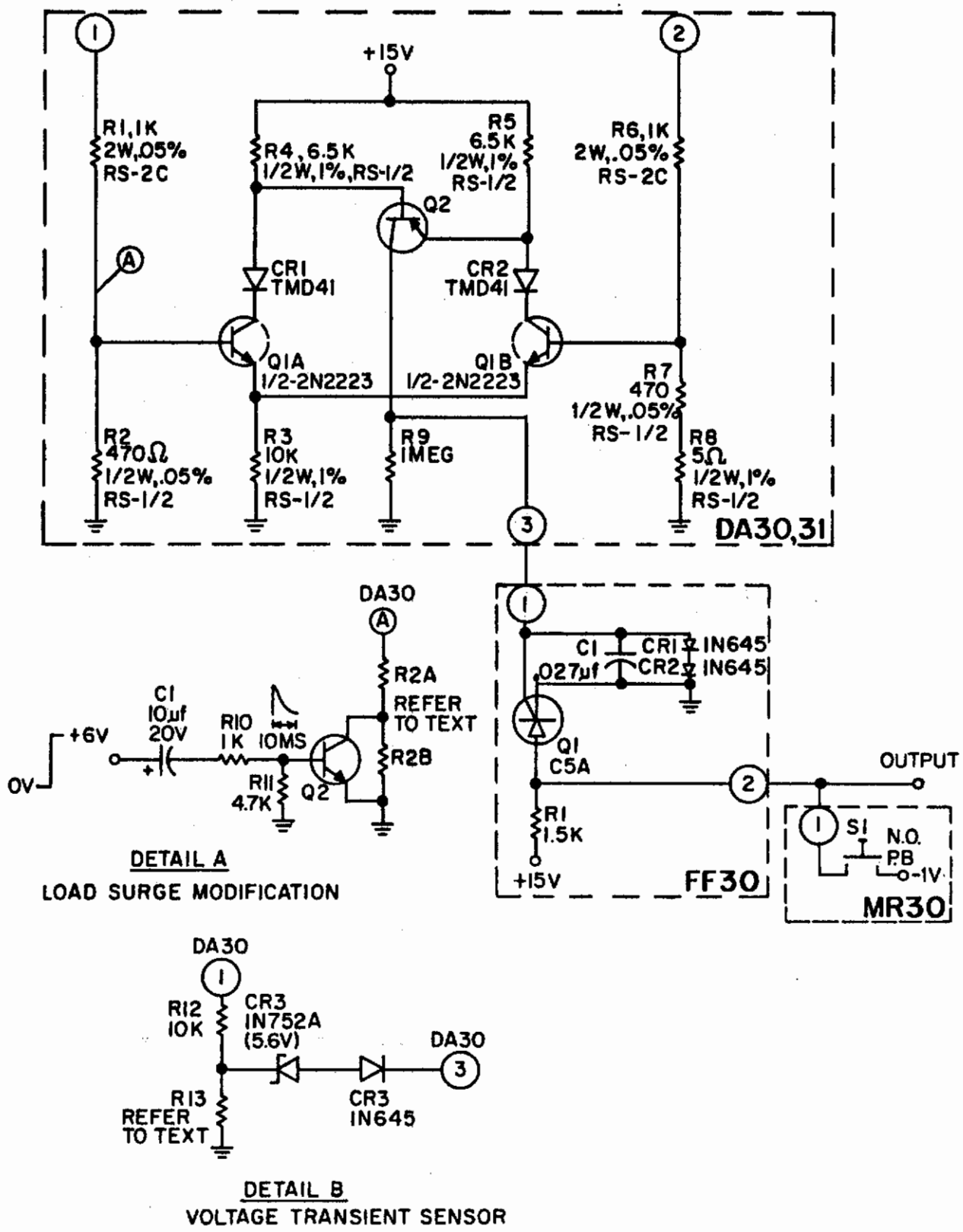


Figure 60. Improved DC Overload Detector and Flip-Flop

TABLE 46

Improved DC Overload Circuit Performance Data

T_A (°C)	V_{in} (vdc)	I_{trip} (amps)	V_{Rs} (vdc)
+80	27	2.85	0.230
↓	28	2.90	0.240
	30	3.10	0.250
	33	3.40	0.270
+25	27	2.85	0.230
↓	28	2.90	0.240
	30	3.10	0.250
	33	3.35	0.265
-20	27	2.80	0.220
↓	28	2.90	0.230
	30	3.05	0.250
	33	3.30	0.260
-40	27	2.80	0.220
↓	28	2.90	0.230
	30	3.05	0.250
	33	3.30	0.260
-55	27	2.80	0.220
↓	28	2.90	0.230
	30	3.05	0.250
	33	3.30	0.255

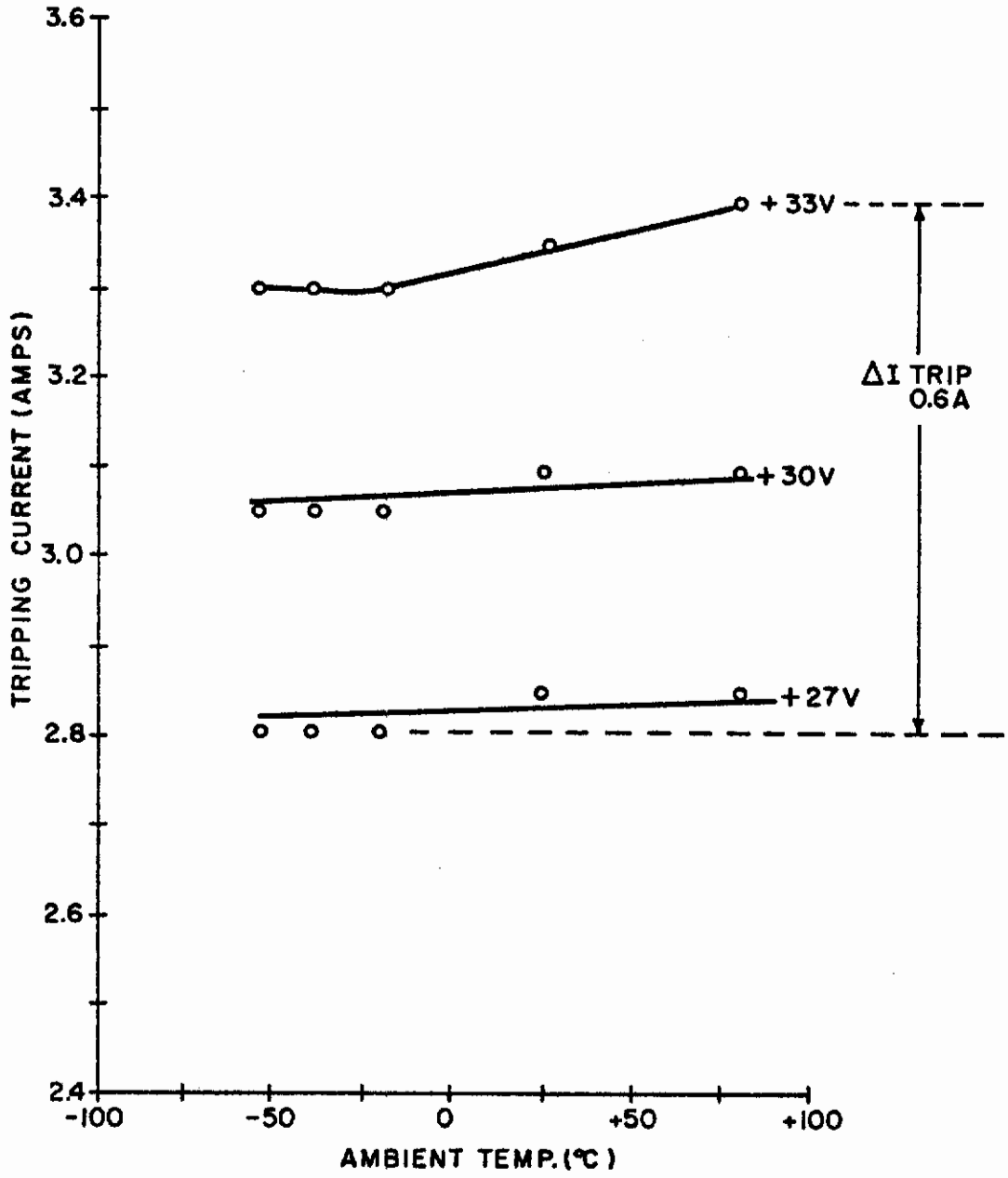


Figure 61. Improved DC Overload Circuit Performance

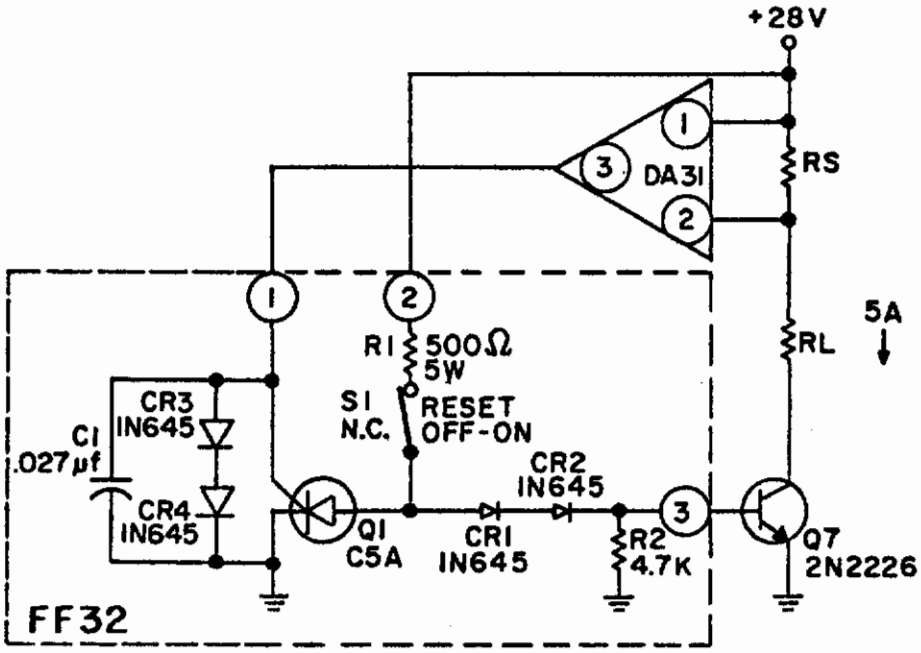


Figure 62. Simplified Chute Deploy Overload Circuit

When the power switch was in the off condition at +27°C ambient, the leakage current was measured as 0.6 milliamperes. CR1 and CR2 were used to assure that the V_{be} of the power switch after tripping was below the required V_{be} for power switch turn-on. If a negative voltage was used for bias, CR1 and CR2 could be deleted from this circuit. S1 was used for on-off control and manual reset.

7.2.3.3 Transient Cut-out Capability

One of the advantages of a transistorized overload circuit is the inherently fast trip time, but this advantage may prove to be a disadvantage when transients, either load or source, are present. For example, if the load is capacitive in nature or a lamp load, many times the steady state current may flow at the time of turn-on. A modification was devised which increases the tripping current for a predetermined time after turn-on and then returns to normal operation. This modification is shown as detail A of Figure 60. If for example, R2a = 429Ω and R2b = 42Ω, then the tripping current at turn-on is 7.4 amps while the normal trip is 0.9 amps. Also, if R2a = 393Ω and R2b = 77Ω, then the tripping current at turn-on is 14.5 amps while the normal trip is 1.1 amps. This data was taken at +25°C in order to demonstrate the feasibility of this technique.

If voltage transients are present, it may also be desirable to trip the overload circuit. Detail B of Figure 60 is a modification which will sense an over-voltage condition and trip the overload circuit. When R13 of detail B is 1K, a trip signal is developed when the bus voltage reaches +42 v. If R2 = 470Ω, then tripping occurs when the bus voltage reaches + 68 v. If R2 = 330Ω, tripping occurs when the bus voltage reaches + 90 v.

7.2.3.4 Cycling Overload System

Since it may be undesirable to remain tripped out after a source voltage transient has occurred, a circuit has been developed which trips at normal overload current, waits 20 milliseconds, then automatically resets but trips again in less than 0.8 milliseconds if an overload still exists. This recycling continues at intervals of 20 milliseconds for about 80 milliseconds. If the overload condition still exists after 80 milliseconds, the circuit trips out and requires a manual reset. Figure 63 is the schematic of the 20 millisecond delay, the 80 millisecond delay, and the final bistable element.

This recycling circuit was integrated with the improved differential amplifier, dc to dc converter, and emitter-follower configuration. It performed satisfactorily during tests performed at +25°C. Figure 59 is a block diagram showing the integration of the various circuits to achieve the desired cycling operation. DD30 is the 20 millisecond delay which is initiated by an overload. Each time DD30 provides an output pulse to automatically reset FF30 by causing Q3 to conduct, a negative pulse is applied to the base

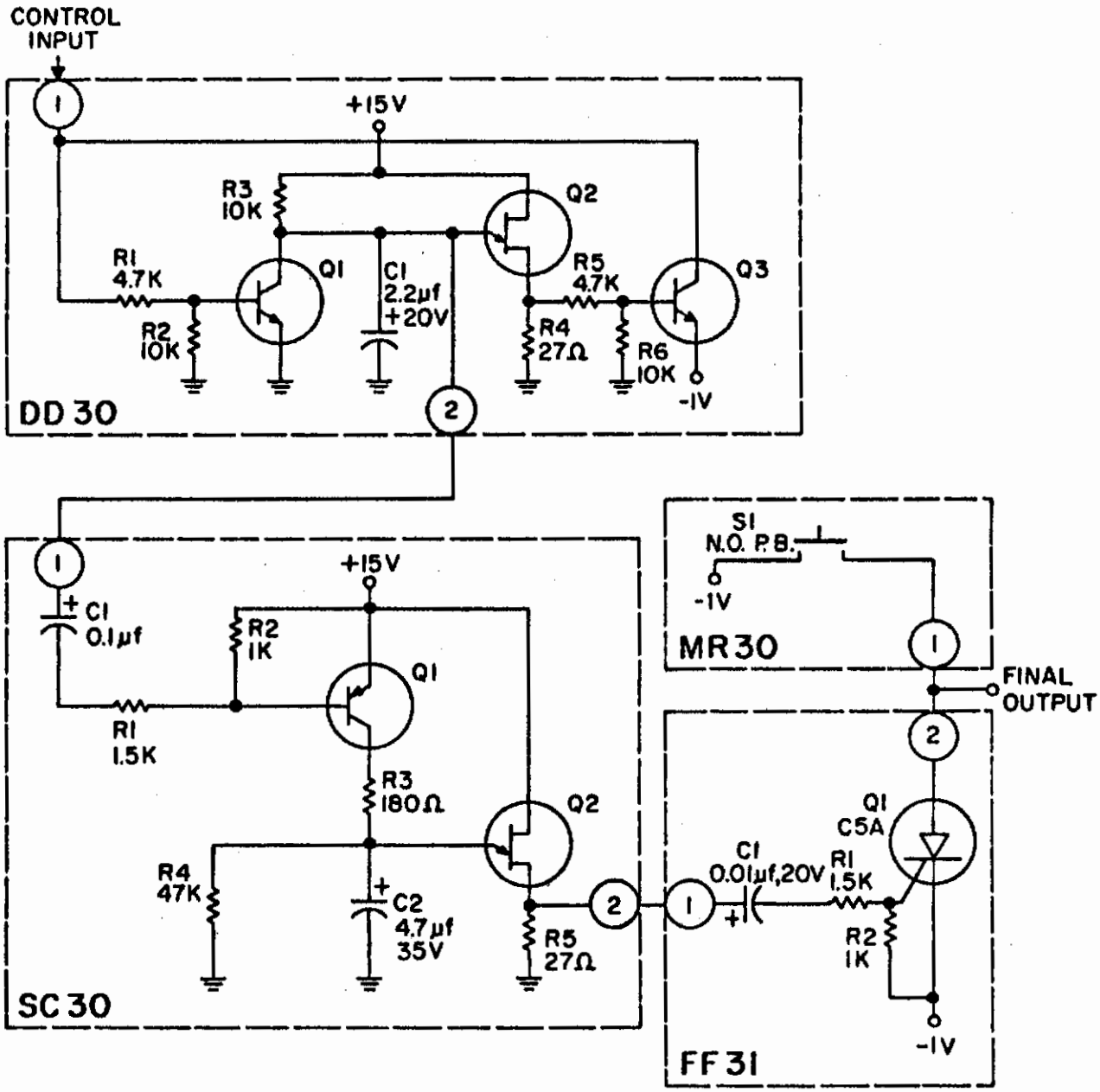


Figure 63. Cycling Overload Circuits

of Q1 in SC30. SC30 is a staircase generator which requires 4 cycles of DD30 before producing an output pulse which sets FF31, thereby causing the power switch to finally remain off until manually reset. If the overload is a transient condition which is removed before the completion of the 80 millisecond staircase, the circuit is automatically reset and again prepared to provide normal overload protection. The time required for recycling may be varied by changing the value of DD30 - C1 and R3. The total number of cycles before final trip may be varied by changing the values of SC30 - R1, R2, and C2.

8. CONCLUSIONS AND RECOMMENDATIONS

The feasibility of a solid state transmission link has been demonstrated. The solid state equivalents of the original electromechanical systems operated properly. The logical characteristics of the original systems were reproduced and the load capacity of the original systems was attained.

The use of solid state power switches rather than electromechanical units results in higher leakage currents, larger forward voltage drop, and a greater susceptibility to transient and RFI disturbances. This is a result of the characteristics of solid state devices. It is unrealistic to expect exact duplication in such things as open and closed contact resistance. However, increased reliability and life can be achieved by the application of solid state techniques. Thus, the undesirable characteristics must be evaluated against the advantageous features.

The control circuitry of the solid state system is more complex than in the electromechanical system. However, circuit and logic consideration indicate that higher reliability would exist in the solid state system. The low level logic and control circuits of a solid state system present no significant problem within the context of present day devices and design techniques. The operating temperature range of -55°C to +80°C is quite realistic for the logic and control circuits when designed around silicon semiconductors.

The power supply for the electromechanical system does not require special circuits. The power supply for the solid state system does require them and this is a disadvantage. This disadvantage can be minimized by reducing the number of separate voltages required to a minimum.

Solid state overload protection can be accomplished; it is most desirable where the rapid turn-off characteristic of the solid state protector are required. For example, in cases where the conventional breaker operating time would be too long to protect semiconductor circuits.

Further studies should be conducted with regard to transients, RFI and reliability. The designed system encountered no transient difficulties. However, it was tested under laboratory conditions and it was not subjected to the stress of transients and RFI from other equipments. Thus, further information is desirable regarding the transient and RFI disturbances generated by the system, as well as the susceptibility of the system to such disturbances that originate elsewhere. As regards reliability, every effort was made to employ conservative design techniques but no numerical calculations of reliability were made. This would be desirable.

8.1 Improvements to Designed Systems

A number of improvements can be made in the designed system. First, custom microcircuits should be used for both logic and linear operations that were performed with conventional parts. For example, the delay gate multivibrator could be a microcircuit; also, the differential amplifier could be a microcircuit. Second, efforts should be made to reduce the number of parts per function. An example of this is the dc overload circuit. The original used 42 parts; the alternate used 23 parts and also exhibited much better performance. Third, smaller parts could be used. For example, power resistors can now be obtained in smaller sizes than those used in the designed systems. Fourth, the types of devices used should be reduced. For example, the designed systems use both TMD41 and TMD42 diodes, but TMD42 diodes could replace TMD41 units. Fifth, the values of common resistors and capacitors that are used should be reduced. For example, the systems use different but almost equal resistor values such as 4.7K and 5.1K, or 20K and 22K; both the 5.1K and 20K values could be replaced by 4.7K and 22K values, respectively.

8.2 Solid State Transmission Links

In considering the extent of advantage of a solid state transmission link, it was useful to divide the transmission link into the following sections: (1) power switches; (2) control circuits for power switches; (3) power supplies for the control circuits; and (4) circuit protectors. Thus, it was possible to compare electromechanical and solid state transmission links on a sectional basis and thereby obtain a more significant overall evaluation. Further, it permitted a sectional comparison between solid state systems used for dc switching and those used for ac switching.

8.2.1 Power Switches

In the electromechanical system a power switch consisted of mechanical relay contacts. Commonly used relays and switches can withstand 240 volts rms steady state, 1000 to 1800 volt transients, and have a line voltage drop of the order of 0.1 volts in high current applications. In the open condition, mechanical contacts have a resistance which, for practical purposes, is infinite.

The solid state system has an SCR or a power transistor as a power switch. Controlled rectifiers are available that can withstand 500 volts steady state and 600 volts transient. Their forward voltage drop is 1 to 2 volts. Medium and high current controlled rectifiers have leakage currents under high temperature, open-gate conditions that range from 1/2 to 14 milliamperes, depending on the type.

Silicon power transistors are available that can withstand 400 volts

steady state of transient. Their line voltage drop is the product of their saturation resistance and the current they are conducting. For example, a unit with a 0.2 ohm saturation resistance that is conducting 5 amperes has a voltage drop of 1 volt. The saturation resistance can be as low as 0.03 ohms, and a variety of types are available with maximum saturation resistances ranging from 0.3 to 0.5 ohms. Medium and high current silicon power transistors have leakage currents under high temperature, reverse bias conditions that range up to 20 millamperes.

It is interesting that in several cases in the dc power system, it was possible to provide the necessary characteristics with only a rectifier rather than a power switch. For example, it was desired that power applied to the dc nonessential bus be transmitted also to the dc essential bus. However, under a failure condition, emergency power is supplied to the dc essential bus but should not reach the dc nonessential bus. This was achieved with a rectifier which acted as a high power steering diode.

It would have been possible to obtain low voltage dc from the 115 vac by use of a phase-controlled SCR bridge connected directly to the ac line. Thus, the TR transformer could have been eliminated. This was not done for two reasons. First, failure of the amplitude control circuit could place 115 volts on the 28 vdc bus. Second, a considerable problem of filtering would exist.

The theoretical limits of operation for a single solid state power switch are 150 amperes average at 800 vdc, or 235 amperes rms at 800 volts peak. The tested limits, dictated by system requirements, were 43 amperes at 28 vdc, and 5 amperes at 115 vac line-to-neutral (208 volts line-to-line), 3 phase, 400 cps. In any practical application, the limits will be determined by the cooling techniques available and the transient conditions existent.

8.2.2 Control Circuits

In the electromechanical system, the control circuitry for the power switch consists of the relay coil and often other power switches. The control circuitry of the solid state system has many more components. However, these components can be of much higher reliability than electromechanical components. Further, there is no dependence on other power switches. That is, in the electromechanical system a good deal of the logic is performed at high current levels by relay contacts operating in series. In the solid state system this undesirable condition is completely avoided by performing all logic at low current levels with highly reliable solid state devices.

Control circuitry for SCR power switches generally requires 1/2 to 1/4 the current required for the control circuitry of a high gain transistor power switch in the same application. This is an advantage of controlled rectifiers

over power transistors.

The input to both the solid state and the electromechanical control system is a group of mechanical contacts. However, as described in a previous section, the switch inputs to the electromechanical system are characterized as high current, multi-pole, multi-throw units whereas the switch inputs to the solid state system are low current, single-pole, single-throw units. This is another reliability advantage.

8.2.3 Power Supplies

In the electromechanical system the control circuitry operates directly from the main voltages. In fact, the power supply for the control circuitry is usually the same power source that is being switched. In the solid state system the power supply for the control circuitry must be furnished with special circuits. This is a disadvantage but one which can be minimized by requiring a minimum number of control voltages with the minimum possible current requirements. The derivation of the control voltage from the power source being controlled should be retained.

A practical solid state switching system should include a negative voltage source for biasing the power switches in the cut-off condition. This is desirable with SCR power switches and is almost a necessity with transistor power switches. In the solid state systems which were designed, the power supply for the control circuitry is separated into several parts. Each one is energized from the power source that is being switched.

8.2.4 Circuit Protectors

Solid state circuit protectors use many more components than the conventional aircraft fuses of the electromechanical system. An evaluation of them, however, should distinguish between ac lines and dc lines, because the problem of solid state protection is quite different for them. The first aspect of the problem is fault current detection. In ac lines it can be accomplished with a current transformer operating into a level detector. It is simple, accurate, and has low power dissipation. In dc lines detection requires a sensing resistor operating into a level detector. Either the resistor must have a large voltage drop of the order of 2 volts, or the level detector must be a critical circuit operating from a low level signal.

The second aspect of the problem is fault current interruption. In ac lines the current transformer's primary and an SCR power switch can be placed in the hot side of the line. Thereby, adequate protection for all fault conditions is achieved. In dc lines the sensing resistor and a transistor power switch also can be placed in the hot side of the line. However, the power switch requires a converter to furnish driving current.

The ac solid state protectors of the designed systems used the ac scheme discussed above; they were satisfactory. However, the dc solid state protectors of the designed systems left a good deal to be desired. First, the detection was complex. Second, the tested systems used ground switching for both control and protection. Thus, the source and load are not protected against a short to ground in the load or its wiring; however, both the source and the switch are protected against internal load shorts.

A number of possibilities were considered to correct this difficulty and the most promising scheme was selected. It is presented as the alternate dc overload circuit of section 7. The first problem is solved by a greatly simplified arrangement for detection, amplification, and reset. The second problem is solved by incorporating the alternate dc overload circuit into the emitter-follower power switch which is discussed in the alternate circuits section. Thus, dc overload protection is furnished adequately and simply.

8.3 Hybrid Systems

A hybrid system is probably best for many control and distribution applications at this time. As a first step, solid state control circuitry could be used to drive power handling relays. Thereby, the following advantages could be achieved: (1) all logic would be performed at low levels in the control circuitry so that no power switches need be in series to perform high level logic; (2) small signal wires could replace large current carrying wires; (3) multi-pole, multi-throw input switches carrying significant currents could be replaced by single-pole, single-throw input switches carrying small currents. The solid state control circuitry could consist of microelectronic functional devices or other types of solid state circuits.

As a second step, small currents could be switched with solid state power switches now and large currents could be switched solid state in the future. For the time being, currents too large to be switched by solid state devices (due to the power dissipation problem), could be switched with electromechanical devices. Replacement of these devices with solid state devices could be done on a module basis. The protection of the solid state power switches could be accomplished with a hybrid fusing scheme (for example, an SCR crowbar circuit) or a wholly electromechanical fusing scheme (high speed current limiting fuses). However, as a final step toward solid state transmission links, wholly solid state circuit protectors would be provided.

8.4 Special Applications

There are several special applications that can be considered. These include solid state circuit protection in several forms and certain logical functions. At the present time fuses smaller than 1 ampere exhibit frequent failure under

vibration and shock. This represents an ideal opportunity for the application of solid state fusing techniques. Electromechanical 3-phase circuit breakers are provided as mechanically linked assemblies of single circuit breakers. They are regarded as unsatisfactory. This would be an excellent application for solid state circuit protectors, particularly where moderate currents are encountered.

Conventional time delay relays are widely used. However, time delays are a logical operation that can be performed with solid state circuitry. The time delays for the designed systems were satisfactory with a tolerance of ± 10% over the temperature range. However, the techniques used can be refined to provide a tolerance of ± 1%.

Precision relays are presently used in some military equipments for sensing functions. An example is a single-pole, double-throw relay with on/off/on positions. It is required to pull-in at 0.46 milliamperes ± 20% and to drop-out at 10% below the pull-in value; the direction of pull-in is determined by the polarity of the coil voltage. This particular relay has long represented a problem in equipment production. It is entirely feasible and desirable to replace it by a trouble-free system that is either partly or totally solid state.

APPENDIX I

DESIGN MANUAL

The purpose of this manual is to guide the engineer in the design and application of solid state power switching systems. It will present design criteria, problem areas, and installation and packaging considerations for application of solid state transmission links in advanced aerospace vehicles.

Although this appendix is designated as a design manual, it should be used in conjunction with the main text. Together, they provide an excellent guide for the engineer who wishes to design and apply a solid state transmission link. Thus, numerous references are made throughout the appendix to the figures, tables, and data of the main text. This appendix serves several functions:

(1) it outlines the procedures for developing a solid state transmission link;
(2) it references pertinent information and examples in the main text;
(3) it presents information to permit intelligent selection of devices and techniques from among the possible choices;
(4) it presents background information that led to the choices of the matrix program.

I.1 GENERAL APPROACH

The problem of providing a solid state switching system can exist in either of 2 forms. First, the solid state system may be intended as a replacement for an existing electromechanical system. Second, the solid state system may be intended to be an original system never before constructed. Regardless of which form is being considered, the problem is exactly the same. In either form, it is necessary to provide 2 sets of data, or information. First, the desired system operation must be described. Second, the loads on the system must be specified. Thus, the basic approach is an overall functional analysis. If the system is being developed for the first time this is the only available approach. If the system is being developed to replace an existing electromechanical system, then it is the only efficient approach.

The overall functional analysis produces a system wherein there is no precise component equivalence with respect to the electromechanical system. The overall system is simply viewed as a black box with the outputs specified in terms of the inputs.

A chief objective of the solid state system is to perform all logic at a low level. In the electromechanical system logic was performed at a high level by switches and relay contacts in series. However, this is undesirable from a reliability viewpoint. It should be eliminated in the solid state system by having all logic performed at a low-level by the transistor logic system. Power contacts are controlled by the output of this logic system, but no power contacts are required to operate in series. Each power contact is independent of the other power contacts in the system.

Relays, by their nature, have a mechanically preferred state to which they return when energizing power is cut off. Thus, breaking a wire to a relay will cause the relay to assume a known state, and the knowledge of this state can be used to assure fail-safe operation. For example, the ac relay, K4, in the dc power system of the main text (p. 9) is connected so that loss of power on the relay will cause the transformer primary to be connected to the ac essential bus. Therefore, partial failure of the system will leave the transformer connected to the last source of ac power that could fail. Similarly, not only will excessive accumulation of ice cause the ice detector interpreter of the main text (p. 20) to de-energize the ice detector indicator relay and thereby illuminate a warning light, but also failure of ice detector power will cause the same light to turn on and warn the pilot to use manual anti-icing procedures.

By contrast, solid state components, and in particular solid state flip-flops, do not have preferred conditions. A flip-flop will assume either of two positions when initially energized, and failure of power in solid state logic circuits may cause ambiguous indications depending upon the precise nature of the power failure. Much can be done to design around these limitations, but only at the expense of adding additional checking circuitry.

Restating the problem succinctly, when relay circuits are damaged, the relays tend to assume a known state which can be used to create fail-safe conditions. However, when solid state logic circuitry is damaged, there is usually no preferred state and therefore no opportunity to establish fail-safe conditions. Careful circuit design of the logic circuits may ameliorate this problem, and a serious attempt should be made toward this end.

A good solution to the problem of electrical power switching may be to use ac distribution to the fullest extent possible. Thus, a single SCR could be efficiently employed for control, rectification where required, and fault current interruption when necessary. If a battery is used as an emergency power source, then dc switching is necessary for the dc essential bus. This is the case in the F-106B. However, an alternate method for developing emergency power for vehicles operating in the atmosphere is to use a ram-air turbine. The use of a ram-air turbine rather than a battery would make possible complete ac distribution.

I.2 SYSTEM DESCRIPTION

The system description is the first step in providing the required system. It consists of 3 parts as follows: (1) verbal description of operation; (2) definition of bounds; (3) definition of system loads. These are discussed in the following paragraphs.

The system should first be described verbally. An example of this is given in the main text where the system description was given for the Matrix Program under the heading of ANALYSIS OF SCHEMATICS, pp 4-24. The verbal description of operation for the dc power system and the anti-ice system was given on pp 5-11 and pp 16-21 respectively. This description should be complete, clear, and unambiguous with respect to the desired operation and various modes of the system.

Any system or subsystem is connected to its environment through input and output channels. It is possible to extend the scope of a system by redefining the system to include some sources of input signals or sinks of output signals. Also it is possible to contract the scope of a system by redefining the system to exclude some elements within the originally defined system which receive input signals or transmit output signals. Thus, the precise definition of any system is largely arbitrary and is simply made in the most convenient way for the purpose at hand.

The definition of bounds can be given either by general rules or by explicit and precise statements. Rules were given in the main text as boundary criteria for the systems considered there, and then used to establish the system bounds. Generally, the definition of system bounds consists of these 2 steps.

The output loads of the system must be carefully listed. They should include the current peaks and nature of the load. The resistance, inductance, or capacitance must be specified. It is important that the maximum loads be specified under the worst conditions. For example, under maximum bus voltage and minimum resistance, as would occur at low temperature where the resistance is a minimum. Also, the power switch has to be designed to withstand the peak currents that exist because of the very short time constant of semiconductor devices.

I. 3 ABSTRACT LOGIC DESIGN

The abstract logic design represents a condensation of the data acquired during the system description phase. It should present all essential facts and it does this in a fraction of the space required by the system description. The abstract logic will be either a combinational or sequential system. In a combinational system, the present outputs depend only on the combination of present inputs. In a sequential system, the present outputs depend on past inputs as well as the present inputs.

I. 3. 1 General Data

Boolean algebra, binary numbers, and switching circuits all become involved in the development of the logic design. This is because they all possess a "common denominator" -- "two". Binary numbers utilize the radix 2. In Boolean algebra, a variable is allowed to assume only one of 2 different values. Switching circuits are circuits that have 2-state intelligence because they require signals to exist in only 2 widely separated states. Such circuits are valuable because signal accuracy is non-critical, and reliable performance can be achieved with wide circuit tolerances.

Although binary numbers, Boolean algebra, and switching circuits represents 3 distinctly different concepts, their "common denominator" of two often brings them together. A given electronic system may contain many switching circuits, and the manner in which these circuits are interconnected may be expressed mathematically via a set of Boolean functions. Also, Boolean algebra may be employed to express the logic or intelligence of certain control operations and sequences of events that occur in the electronic system. As regards binary arithmetic, a part of the system may be involved in counting or in performing arithmetic operations with binary numbers.

The basic operations of Boolean algebra are a special form of negation, a special form of addition, and a special form of multiplication. The negation is the NOT operation. It can be written as $\bar{c}$ and read as not c. The addition is the OR operation. It can be symbolized with a plus sign. A typical expression would be b+c, which is read as b or c. The multiplication is the AND operation which is symbolized by a dot. A typical expression would be $b \cdot c$, which is read as b and c. This product is true (or 1) if, and only if, both a = 1 and b = 1. In an open and closed application of 2 switches (a and b) in series, the resultant switching combination $a \cdot b$ is closed if, and only if, both individual switches are closed (a = 1 and b = 1).

Since Boolean variables can assume only one of 2 values, functions of only a few variables are readily studied by evaluating the function for all

possible sets of variable values. When all possible sets of variable values are tabulated alongside the corresponding function values, the resultant chart is called a truth table. Truth tables for the NOT, OR, and AND functions are given in Table I-1.

TABLE I-1

Truth Tables of Fundamental Operations

Variable Values			Functions		
			NOT	OR	AND
a	b	c	$\bar{a}$	a + b + c	abc
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	1

Boolean algebra can be applied only after a knowledge of the 3 basic operations (NOT, OR, and AND) and of what is forbidden (subtraction and division). However, formal recognition of certain fundamental identifies which stem directly from the basic operations, facilities the application of the algebra. These fundamental identities include elementary propositions, associative, commutative, and distributive laws, and DeMorgan's theorem. DeMorgan's theorem states that $\overline{(a + b)} = \bar{a}\,\bar{b}$, or that $\overline{ab} = \bar{a} + \bar{b}$. It was extensively used in the development of the abstract logic for the dc power system of the main text.

Venn diagrams are graphical illustrations of Boolean equations. They are of little value in themselves for the development of the logic system required by the application under consideration. However, they have led to techniques which are useful for reduction. These techniques will be discussed in the following section.

The abstract logic design for the dc power and anti-ice systems of the Matrix Program are given in the main text on pp 52-54 and 83-87 respectively. The dc power system is combinational and a few remarks about it may be instructive. The abstract logic diagram for the power switches was prepared

first as shown in Figure 9. Second, a table of logical definitions and conditions was prepared as shown in Table 5. The logical definitions were simply a listing of the inputs to the system, plus a definition of the input symbols. Then the switch control conditions were tabulated. Each power switch was listed with the conditions that determined if it was open or closed. The abstract logic diagram of the control system as shown in Figure 10 was then prepared from Table 5. This completed the abstract logic design for this combinational system.

The anti-ice system is sequential and was handled somewhat differently. The abstract logic diagram for the control circuits (Figure 24) was prepared directly from a study of the system description. This was desirable because it is difficult to deal symbolically with a sequential system. At the same time, a list of definitions for the inputs and outputs of the control system was made (see Table 10). Subsequently, the abstract logic diagram for the power circuits (see Figure 25) was prepared. Finally, a listing was made (see Table 11) of the power switch control conditions as well as supplementary data. This completed the abstract logic design for the anti-ice system.

The abstract logic design need not fully account for checking and fail-safe provisions of a system but merely duplicates the overall action of the original system. The logic diagrams and the definitions may be used, however, to illustrate some of the error checking possibilities of the solid state system. For example, in the dc power system appearance of +28 vdc on the nonessential bus (see Figure 9) calls for the opening of points 3 and 4, a TR output of +36 vdc, and the closing points 5, 6, and 7. In the event of a partial failure of this set of operations, however, serious consequences could occur. For example, a TR output of + 36 vdc, without 3 and 4 in the high impedance state could put 36 volts on the dc essential bus. The safe solution to this difficulty lies in adding voltage detectors and logical conditions to the network. Thus, a voltage detector at A_1 which senses the application of +28 vdc to the dc nonessential bus can be used to set points 3 and 4 to the high impedance state. Similar design procedures can be followed with respect to other possible failure conditions.

A second example of possibilities for error, which are not so easily guarded against by good logical design, relates to the ac essential and non-essential buses. Consider the triple-pole, double-throw relays, K3 and K4, in the emergency dc power pack of the original system (see Figure 2). These relays have a preferred position which they will assume mechanically if their coils are de-energized. That is, relays will assume a known state upon failure of the source voltage or of any connections to the relay. These particular relay circuits are fail-safe in the sense that any interruption of the respective control circuits will switch the transformer input to the ac essential bus and the output to +28 vdc. These conditions are safe because even with a partial

failure of the control system, ac will be supplied to the transformer and high voltage (36 volts) will not appear on the dc essential bus. Now, solid state components do not have a preferred failure condition. To make the points designated 6 and 8 in Figure 9 operate in the same fashion as K4, the analogous part of the original system, requires that failure of control power put point 8 in the low impedance state and point 6 in the high impedance state. If this kind of operation is possible to achieve, it will be up to the designer of the solid state circuits to do so; the logical designer can only point out that the problem exists. Once the logical designer knows the characteristics of the circuits he will have at his disposal, he can provide whatever measures of failure protection are obtainable with those circuits.

The logical statements of the abstract design should be understood as being nondescriptive of the contents of the black box. Design of the internal workings to meet the logical constraints depends largely upon the kind of circuits chosen and the degree and mode of redundancy required to meet reliability criteria. That is to say, a specification of the correct operation of a black box can say nothing about how the black box should behave when operating incorrectly. Yet the fail-safe and self-checking features of the system only have meaning when all possible modes of failures have been considered. Modes of failure, in turn, depend upon components and circuits which were used. The abstract logic, therefore, describes only the correct behavior of the solid state systems.

The design of basic circuit elements (switches and detectors) and an analysis of possible modes of failure is required before the final logic design is undertaken. Decisions should be made as to the best means of protection against failure. Consideration should be given also to the fact that solid state switches, unlike relays, do not have infinite impedance when open; therefore, acceptable values of leakage current should be determined.

I.3.2 Minimization

Reduction refers to the process of reducing the size of a given Boolean function. Frequently, the size of a function is considered to be a measure of the number of literals (including repeats) appearing explicity. That is, a (b + c + d) is considered to be smaller than its mathematical equivalent ab + ac + ad. The first form contains 4 literals, and the second form contains 6 literals (counting the repeated a). The first form can be circuitized with 2 logic gates whereas the second form requires 4. If a function is to represent an assemblage of physical components (as suggested by the logic diagram) reduction techniques are of value for investigating different functionally equivalent systems from such standpoints as number of elements, standardization, number of elements between input and output, and uniformity of alternative signal paths.

Reductions may be achieved through algebraic manipulation of the given function with the aid of the fundamental identities. These reductions are achieved through trial-and-error methods. However, systematic aids to reduction do exist. The value of reduction is that it complements efforts toward minimization, which is defined often as the process of finding the form of a given functioned expression that can be implemented at the lowest cost.

A variety of minimization techniques are available. Two of the more popular are the Karnaugh map and the Veitch map. However, they have a major disadvantage in that the Boolean function obtained from them is basically dependent on the skill of the user. More formalized techniques exist which have the disadvantage of being more time-consuming but also have the great advantage of always leading to the simplest sum-of-products representation of any given Boolean function. Therefore, a technique of this type is recommended. The particular method that will be illustrated is Ledley's adaptation of the Quine-McClusky method of simplification.

Ledley's adaptation of the Quine-McClusky method of simplification can be applied as follows. Suppose that it is desired to minimize a logic diagram for which the Boolean function is $Z = (A + \overline{B})\overline{C} + (\overline{B} + C)\overline{A} + (A + C)B$. Binary numbers can be used to provide a designation number for this function. The designation numbers for the elementary elements are assigned first, and this assignment is called a basis. One such basis for a system of 3 elementary elements is

		0123	4567
#A	=	0101	0101
#B	=	0011	0011
#C	=	0000	1111

where the heading numbers merely number the positions of the columns of the basis and "A'" means the designation number of A.

The designation number of a Boolean function is found by logical addition wherein $0 + 0 = 1$, $0 + 1 = 1$, $1 + 0 = 1$, and $1 + 1 = 1$ without carry, and by logical multiplication wherein $0 \cdot 0 = 0$, $0 \cdot 1 = 1 \cdot 0 = 0$, and $1 \cdot 1 = 1$. Thus, the designation number of $Z = (A + \overline{B})\overline{C} + (\overline{B} + C)\overline{A} + (A + C)B$ is found as follows:

		0123	4567
#A	=	0101	0101
#B	=	0011	0011
#C	=	0000	1111
$\#(A + \overline{B})\overline{C}$	=	1101	0000
$\#(\overline{B} + C)\overline{A}$	=	1000	1010
$\#(A + C)B$	=	0001	0011
#Z	=	1101	1011

The simplest sum-of-products representation is found as follows. First, display only the columns of the basis that correspond to the units of the given designation number:

0	1	3	4	6	7
0	1	1	0	0	1
0	0	1	0	1	1
0	0	0	1	1	1

Second, arrange these columns in order by the number of units contained in each column:

0	1	4	3	6	7
0	1	0	1	0	1
0	0	0	1	1	1
0	0	1	0	1	1

Third, combine pairs of columns that differ only in a single row and mark the differing row with a dash. Thus, a μ-unit column need be compared with only $\mu + 1$ columns. This gives the following:

0, 1	0, 4	1, 3	4, 6	3, 7	6, 7
-	0	1	0	1	-
0	0	-	-	1	1
0	-	0	1	-	1

Fourth, when further re-combining is not possible, make a prime implicant chart by listing the function equivalents of the designation numbers of the columns that cannot be combined:

	0	1	2	3	4	5	6	7
$\overline{B}\overline{C}$	x	x						
$\overline{A}\overline{B}$	x				x			
$A\overline{C}$		x		x				
$\overline{A}C$					x		x	
AB				x				x
BC							x	x

Fifth, select the prime implicants that produce the given designation number with the least number of operations. This is given by $\overline{A}\overline{B} + A\overline{C} + BC$. Thus, $Z = (A + \overline{B})\overline{C} + (\overline{B} + C)\overline{A} + (A + C)B$ has been simplified to $Z = \overline{A}\overline{B} + A\overline{C} + BC$. A detailed discussion of this technique is given in reference 8.

I.3.3 References

The following references provide detailed information on logic design.

(1) S.H. Caldwell, Switching Circuits and Logical Design, John Wiley, New York, 1958

(2) R.K. Richards, Arithmetic Operations In Digital Computers, Van Nostrand, Princeton, 1955

(3) M. Phister, Jr., Logical Design of Digital Computers, John Wiley, New York, 1958

(4) G. Maley and J. Earle, The Logic Design of Transistor Digital Computers, Prentice-Hall, Englewood Cliffs, N.J., 1963

(5) Y. Chu, Digital Computer Design Fundamentals, McGraw-Hill, New York, 1962

(6) I. Flores, Computer Logic, Prentice-Hall, Englewood Cliffs, N.J., 1960

(7) H. Gray, Digital Computer Engineering, Prentice-Hall, Englewood Cliffs, N.J., 1963

(8) R.S. Ledley, Digital Computer and Control Engineering, McGraw-Hill, New York, 1960

I. 4 DEVICE SELECTION

After the completion of the abstract logic design, it is desirable to select the circuit devices that will be used to implement the desired functions. The circuit devices needed include semiconductor devices and other devices such as resistors and capacitors. The semiconductor devices can be divided into two major groups: (1) power handling; and (2) control circuit. The power handling devices are in 3 categories: (1) silicon controlled rectifiers; (2) power transistors; and (3) power rectifiers. The control circuit devices can be considered in 3 groups: (1) discrete; (2) functional; and (3) custom designed devices. The factors to consider in selecting devices will be considered in the following paragraphs.

Available devices today are made of either germanium, silicon, or gallium arsenide. Germanium devices have a temperature range of about -55°C to + 100°C. Silicon devices have a temperature range of -55°C to +200°C. Gallium arsenide devices have a temperature range of -55°C to +400°C; however, very few devices constructed of this material are available.

It is desirable to determine first the material that should be used on the basis of the temperature range. Although germanium can withstand a junction temperature of +100°C, practical considerations make it desirable to use silicon devices when the ambient temperature range is greater than +55°C. Thus, the choice will be to use either germanium devices or silicon devices. If silicon devices are used, then it may be desirable to use gallium arsenide devices too, insofar as they are available. Of course, there is no absolute prohibition against selecting devices of each material if some special considerations should make it attractive.

An intelligent selection of devices prior to the detailed logic and circuit design requires three things: (1) a familiarity by the designer with the available devices; (2) an awareness of what can be done with those devices; (3) knowledge of the functions required by the abstract logic design.

A characteristic of digital systems is that they tend to be largely repetitious, with the same few circuits appearing over and over again. It follows that a relatively small number of components will serve to construct a large and complex system. Advantage should be taken of this fact to restrict the number of devices used to as few as possible. For example, in the Matrix Program, only silicon devices were used and relatively few types were needed. The main text discusses this selection in some detail. An evaluation of semiconductor devices is given in the main text on pp 25-39. Power handling devices and control circuit devices are discussed in the main text, pp 26-29 and 29-39 respectively.

It should be remembered that the primary considerations in the selection of power devices and circuits should be (1) low saturation resistance, hence low power dissipation, (2) capability to handle the required loads under extremes of temperature, (3) ease of control (turn-on and turn-off) under various load conditions, and (4) adequate voltage ratings. Silicon controlled rectifiers are recommended for ac switching since turn-off is efficiently accomplished by line commutation and high peak reverse voltage ratings are readily available. On the other hand, power transistors are recommended for dc switching because the turn-off and fault protection problem is simplified.

I. 5 DETAILED LOGIC DESIGN

Once the primary logic element has been selected, it is possible to begin the detailed logic design. This must make provision for proper signal polarity throughout the system. Also, the fan-in and fan-out capability of the primary logic element must be observed.

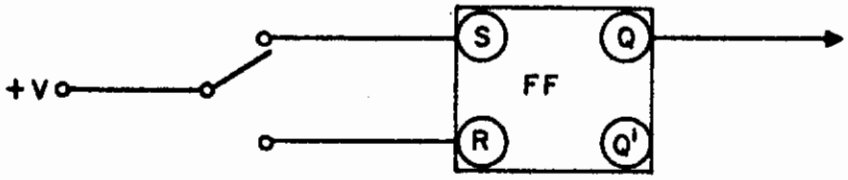
The detailed logic design can be regarded as an expanded version of the abstract logic design. The purpose of this expansion is to indicate the specific techniques of circuitization that will be employed to implement the desired functions. The detailed logic of the dc power system and the anti-ice system of the matrix program is given in the main text on pp 54-59 and 87-92 , respectively. Reference to the main text will show that the detailed logic design consisted primarily of developing the detailed block diagram. Its development was based on the following 3 items:

(1) abstract logic diagram for power switches
(2) table of logical definitions and conditions
(3) abstract logic diagram for control

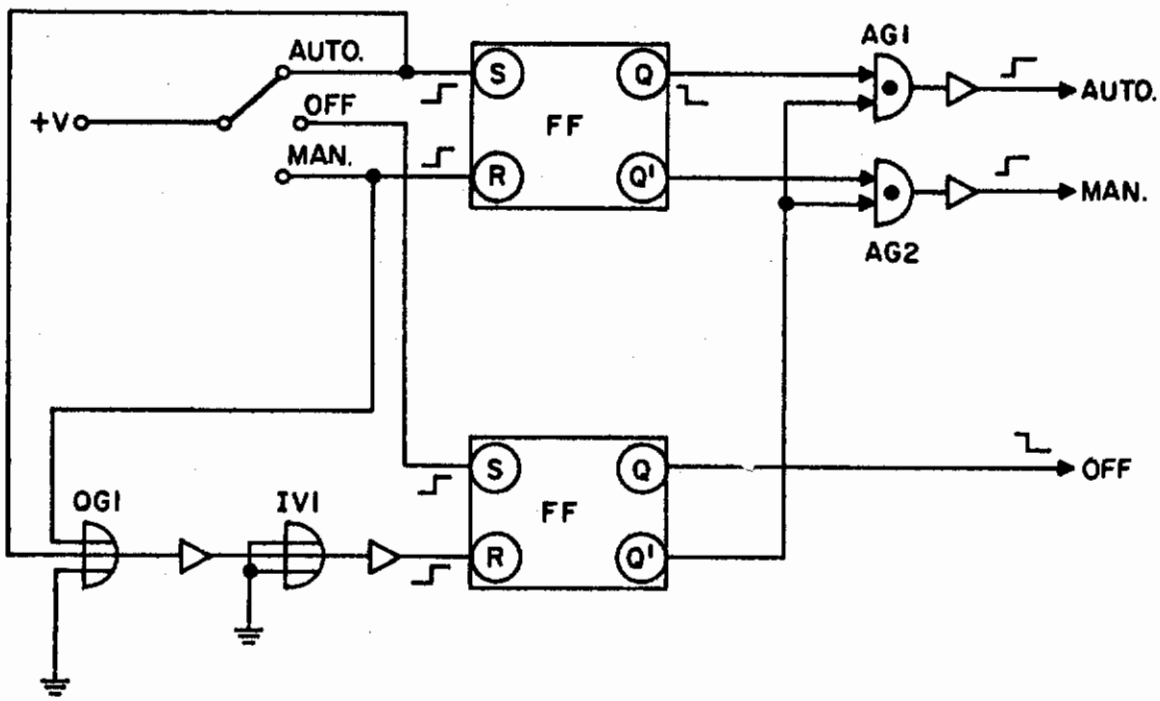
In the detailed block diagram, the power switches and input switches are shown for the first time as specific devices. Also, their firing circuits or driving amplifiers are shown. It should be noted that the input switches can be quite different from their nominal equivalents in the electromechanical system. The designer has complete freedom of choice regarding state assignment and switch position. Thus, an input defined as "generator switch actuated" can be represented by either an open or closed switch position, whichever is more convenient for circuitization.

Although switches can be used to provide inputs to the solid state systems in a manner similar to that used for the electromechanical systems, significant advantages exist with the solid state systems. First, the current requirements are reduced. Second, multi-pole switches are replaced with single-pole switches because the logic circuitry provides fan-out capacity. Third, double-throw switches are replaced with single-throw switches. Thus, high current, multi-pole, multi-throw switches are replaced by low current, single-throw switches.

Contact bounce of the input switches may be a problem. Techniques for eliminating this problem are shown in Figure I-1. The scheme shown in Figure I-1(a) can be used for one-and 2-position switches. The scheme shown in Figure I-1(b) can be used for 3-position switches. It is interesting that during the matrix program no difficulties were produced by the contact bounce of the input switches.



(a) SWITCH INPUT CIRCUIT



(b) THREE POSITION SWITCH INPUT CIRCUIT

Figure I-1. Circuits to Eliminate Problems of Input Switch Contact Bounce

The technique to be used for circuit protection must be established before the detailed logic design can be completed. Solid state overload protection may be provided either by current limiting, current interruption, or load switching. Load switching is applied in the case of regulator circuits where the series element cannot block the full applied voltage. Load switching circuits are not desirable where direct current interruption is satisfactory. Further, current interruption is preferable to current limiting which places a high power dissipation requirement on the power switching device. Thus, the solid state overload protector should provide current interruption.

I. 6 CIRCUIT DESIGN

The first approach to circuit design should be a preliminary design produced on paper; its detail will be determined by the time available, information available on the subject, and the skill of the designer. After this preliminary design is complete, the circuitry should be constructed and evaluated. During evaluation, modifications are usually required to make the design operational and/or to improve its performance. In many cases, optimum performance may not be necessary and only certain predetermined specifications need be met; however, optimum performance and reliability usually go hand in hand. Therefore, if time and finances permit, circuit optimization is highly desirable. The following sections discuss the circuit requirements for a solid state distribution system.

I. 6. 1 Logic Circuits

The logic circuits should consist primarily of a selected type of microelectronic functional device. Since the logic elements themselves are circuit blocks and only require interconnection, the greater part of the logic section may be constructed directly from the detailed logic diagram.

However, the detailed logic diagram may require certain circuit operations which can not be accomplished by the primary logic element and it may become necessary to design some special circuits. Therefore, circuit design in the logic section will be limited to the special circuits which may be required. Some examples of special circuits which may not be easily implemented using the selected logic elements are time delays and voltage level sensors. They are discussed in the following sections.

I. 6. 1. 1 Time Delays

A simple, stable delay circuit may be designed using a unijunction transistor and a RC time constant. When the delay is to begin, the capacitor in the unijunction emitter circuit is allowed to begin charging and the delay continues until the peak point voltage is reached, at which time the unijunction fires producing a pulse which sets a flip-flop. Refer to Figure 31 of the main text for an example of this type of delay circuit.

Control of this delay circuit is achieved by a control amplifier which gates the charging source on or off. Some consideration must be given to the leakage current of capacitor C1, especially when the delay exceeds a few seconds; also, the temperature coefficients of the charging resistors and C1 must be considered for good temperature stability. A low impedance discharge path is also desirable where the delay may be turned off during the delay cycle.

This is accomplished by a low value resistor with diode insolation from the charging path. The delay time will be approximately one RC time constant; it is determined in Figure 31 by C1, R1 and R2. Delays of this type up to a few minutes are feasible.

I.6.1.2 Voltage Sensors

A simple voltage sensor may be designed around the characteristics of the zener diode. This technique was used in the Matrix Program. In order to provide good temperature stability, a zener voltage of about 5 volts should be selected. The circuit is designed to provide an output when the bus voltage exceeds 17 vdc. The point where the output from the sensor is sufficient to provide an input to the logic elements is determined by the resistive voltage divider, the zener voltage, and the input characteristic of the logic element.

I.6.2 DC Power Switching

I.6.2.1 The Power Switch

There are 3 possibilities for the dc power contact: (1) an NPN silicon power transistor; (2) a PNP silicon power transistor; and (3) a silicon controlled rectifier.

PNP silicon power transistors are not a realistic choice considering the present state of the art; therefore, the dc power switch may be either an NPN power transistor or a silicon controlled rectifier. The advantages of controlled rectifiers in this application when compared to power transistors are as follows:

(1) lower drive power requirements;
(2) higher surge current capability;
(3) lower leakage current and less dependence on biasing voltage.

The disadvantages are as follows:

(1) require a commutating capacitor and a second controlled rectifier or some other special turn-off technique;
(2) require a separate high voltage charging source for the commutating capacitor to avoid the otherwise present inability to turn off a controlled rectifier which is being turned on into a short circuit.
(3) may exhibit higher power dissipation at a given current;
(4) have higher thermal resistances than power transistors of comparable size;
(5) generally have lower storage and operating temperature.

Gain, collector to emitter saturation voltage, and leakage current are important considerations when designing the power switch. The gain determines the amplification required between the logic circuits and the power switch. The saturation voltage and load current determine device power dissipation; hence, they effect thermal considerations such as heat sink design and the total thermal environment. Although leakage current is undesirable, some leakage current will always flow. In order to minimize leakage, it may be necessary to utilize a bias supply; however, the amount of leakage acceptable will be dependent upon the individual system requirements.

I.6.2.2 Power Switch Driving Circuits

After the logic circuit design is complete and the power switch has been selected, it becomes necessary to consider the interface problem which usually exists between the logic circuits and the power switching device. This problem is primarily one of gain; therefore, an amplifier is required. For example, consider the 200 microampere output from the SN514 T.I. Solid Circuit. Obviously, this output must be amplified if it is desired to switch currents in the order of amperes.

I.6.2.2.1 DC Amplifiers

If the power switch is a transistor, a continuous driving signal must be maintained to keep the power switch saturated. This requirement is met by use of a dc amplifier which provides sufficient current gain to maintain saturation.

The first step is the selection of transistors which will conform to the system specification. Consideration must be given to forward current transfer ratio (h_{FE}), maximum allowable junction temperature, DC breakdown voltage, maximum collector current, collector saturation voltage, and any other parameters which may be suggested by the requirements of the system specification. It may be desirable to select a complementary pair (NPN, PNP) of transistors to permit a greater degree of flexibility in interstage coupling. In the Matrix program the 2N718 (NPN) and the 2N722 (PNP) transistors were selected as a complementary pair.

The T.I. application notes and data sheets for the solid circuits state that the SN514 has a fan-out capability of five solid circuits, where each circuit input impedance is in the order of 20K ohms. Therefore, an SN514 will safely drive an equivalent impedance of approximately (1/5) (20)K ohms or 4K ohms. Since the maximum transfer of current was of primary importance, the series input resistance of the first amplifier stage should be selected as 4.7K ohms. A base to ground shunt resistance should be selected as a ground

return in order to minimize leakage current. This resistor is typically 22K ohms as a compromise between leakage and gain considerations.

In order to determine the maximum collector current which may flow in this first stage while maintaining the saturated condition, it is necessary to determine the equivalent solid circuit output impedance. Given information states that the output voltage from the SN514 is + 5 volts open circuit and + 2 volts with a fan-out of 5 solid circuits. Since the input impedance of 5 solid circuits in parallel is approximately 4K ohms, the following relationship provides a workable design value of output impedance.

$$R(\text{out}) = \frac{(V \text{ open} - V \text{ out})}{V \text{ out}} (R_{1N}) = \frac{(5v-2v)4K\Omega}{2v} = 6K \text{ ohms} \qquad (1)$$

The 2N718 (NPN) transistor was used as the first amplifier because if the first amplifier stage is on when the solid circuit output stage is off less power is dissipated in the active device portion of the solid circuit. Also, if a PNP transistor were used as the first amplifier, both the first amplifier stage and the SN514 collector circuit would contribute current to the active device portion of the solid circuit.

In order to compute the base current available to the first amplifier stage, a conservative value of V_{be} = 1V is first obtained from the 2N718 specification, and the emitter bias is set at + 1V. The following relationship will then provide the maximum output current available from a SN514 gate.

$$I \text{ out} = \frac{(V_{open} - V_{be} - V_e)}{(R \text{ out} + R \text{ series})} = \frac{(5v-1v-1v)}{(6K + 4.7K)} = 280 \mu a \qquad (2)$$

Approximately 80 μa of this current will flow through the base to ground shunt (22K ohm) which leaves 200 μa as base drive.

A conservative gain figure of 10 is obtained from the 2N718 specification; therefore, with a 200 μa input signal, 2 ma becomes the maximum collector current which may flow while maintaining device saturation. The second amplifier stage will have a maximum base current of 2 ma available. This next amplifier then becomes a 2N722 (PNP) transistor making use of complementary symmetry to reduce coupling complexity. The gain of the 2N722 with a collector current greater than 10 ma is 20; hence, 40 ma becomes the maximum collector current which may flow in the second amplifier. This process is repeated as

many times as required in order to provide sufficient drive to the dc power switch. The same procedure may be used with the SN513 solid circuit if a lower output impedance device is desired, since the SN513 equivalent series output resistance is 1.2K ohms or 1/5 that of the SN514.

I.6.2.2.2 DC to DC Converter

The previous section outlines the procedure for designing a dc amplifier to drive a transistor power switch. It should be noted that the dc amplifier must drive the power switch when it is connected as a common emitter stage. This is ground switching and may be undesirable; therefore, a power converter may be designed to act as a driving source when the power switch is connected as a common collector stage. This is positive line switching. The schematic of a dc to dc converter is presented in Figure 58 of the main text.

The following steps may be followed when designing a single transformer dc to dc converter:

(1) Determine requirements such as conversion frequency, load current, load voltage, and source voltage.
(2) Select transistors whose maximum ratings are at least twice the supply voltage.
(3) Design the transformer which is the heart of the converter.

As an example, the following outline was used when designing the dc to dc converter shown in Figure 58.

(1) Requirements:

Source voltage = 30 vdc, Output voltage = 6 vdc
Output current = 150 ma, Conversion frequency = 2 to 5 KCPS

(2) Transistors:

The 2N720A was selected. The minimum h_{FE} is 40 and the maximum collector - emitter voltage is 80 volts.

(3) Transformer:

(a) $V_{N1} = 30$ v, $V_{N2} = 6$v, $I_{N2} = 150$ ma
$N1:N2 = V_{N1}:V_{N2} = 5:1$, therefore
$I_{N1} \approx \frac{I_{N2}}{5} = 30$ ma. If a feedback voltage of 3v is assumed, $N1:N3 = V_{N1}:V_{N3} = 10:1$

(b) A core of square orthonol material was selected. Some of the characteristics of this core are:
B_s = 16K gauss when H = 0.4 oersteds
Area = 0.26 cm^2, Magnetic Path length = 6.5 cm

(c) Sufficient primary turns were used to drive the core into saturation. Since NI = 0.79 HM_L, NI = 70 turns as a first approximation. Then from the turns ratios N2 = 14 turns and N3 = 7 turns. A slight adjustment in the number of turns and the turns ratio was necessary to provide satisfactory performance; however, the final values used were quite close to this first approximation. The final values were N1 = 65 turns, N2 = 15 turns, and N3 = 8 turns.

(d) The operating frequency will be:

$$\text{Freq} = \frac{V_{N1} \times 10^8}{4B_sA(N1)} = 2.4 \text{ KCPS} \qquad (3)$$

Experimentally, the converter frequency was found to be 2.5 KCPS.

I.6.2.2.3 SCR Control Circuits

If the power switch is an SCR rather than a transistor, the control circuits have some distinct differences. Unlike the transistor, the SCR requires only a pulse when turn-on is desired. However, it is desirable to continuously pulse the SCR gate to insure sustained conduction if line transients and load variations may be encountered which might inadvertently turn off the SCR.

Firing Circuit

The unijunction transistor is an ideal device for use in SCR firing circuits. It has a stable firing voltage, a low firing current, and good temperature stability. The unijunction is used in a controlled relaxation oscillator configuration. When the SCR is to be fired, the oscillator is allowed to free-run. When the SCR is to be turned off, the oscillator must be turned off. This is accomplished by shunting the capacitor with a transistor, thereby, holding down the emitter voltage of the unijunction. Refer to Figure 16 of the main text for the schematic of an SCR firing circuit.

The conditions for oscillation are:

$$\frac{V_{supply} - V_{peak\text{-}point}}{R3} > I_{peak\text{-}point} \tag{4}$$

$$\frac{V_{supply} - V_{valley}}{R3} < I_{valley} \tag{5}$$

These conditions are very broad and permit a range of R3 from 2K to 2M ohms. R5 is used for temperature compensation, and 150 to 300 ohms is a good working range for experimental selection. However, its value may be calculated from the following equation:

$$R5 \approx \frac{0.4R_{BB}}{\eta V_{supply}} \tag{6}$$

The minimum value of C is dependent upon the type of SCR, unijunction base - one impedance, and unijunction supply voltage. The maximum supply voltage is 35 volts. Within the limits of C = 2 to 5 μfd, the following equation may be used to determine the minimum supply voltage required to fire a C60 series SCR when using transformer gate coupling.

$$V_{min} = 19 - 0.3;\text{(C in } \mu f,\ V \text{ in volts)} \tag{7}$$

Within the limits of C-2 to 5 μfd, 10 volts is the minimum supply volts required to fire a C40 series SCR when using transformer coupling. The maximum supply voltage is 35 volts.

After selection of C1, the pulse recurrent frequency of the firing circuit is determined by R3. The frequency of oscillation may be nominally determined by the following formula:

$$Freq = \frac{1}{(R3)(C1)};\ (R \text{ in ohms, } C \text{ in farads}) \tag{8}$$

SCR Turn-Off Techniques

When turn-off is desired, the gate signal must be removed; hence, the control to the firing circuit must reflect this requirement. In fact, if rapid turn-off is required it may be necessary to reverse bias the gate during turn-off. Two techniques were used in the Matrix program for turning off SCR dc static switches.

One technique was to reverse bias the SCR from anode to cathode for approximately 50 microseconds. This was accomplished by charging two capacitor banks to +28 vdc, and then connecting them from bus to ground with a control SCR. Refer to Figure 17 of the main text for the schematic of this turn-off circuit. The capacitance required is dependent upon the load, the source impedance, and the type of SCR to be turned off. The values used in Figure 17 were determined experimentally.

The second technique used was the removal of anode voltage, thereby, causing the forward current to decrease below the holding value. The anode voltage was removed for approximately 10 milliseconds. This was possible since the source voltage was derived from a rectifier whose input ac was controlled by ac switches. These switches were opened for 10 milliseconds which caused the anode voltage to decrease to zero.

I. 6. 2. 3 DC Overload Circuits

The initial consideration in the design of the DC overload circuit is one of current sensing. Hall effect devices were considered as sensing elements. The devices considered were the Hall generator and the magneto-resistor. The Hall generator is a four terminal device which when oriented properly in a magnetic field and provide with control current will produce a voltage. The magnetoresistor is a two terminal device whose resistance changes with changes in magnetic induction. Either of these devices could be used to sense the magnetic field created by a dc current; however, the Hall generator requires a magnetic induction of approximately 10 kilogauss to produce an output voltage of 0. 4 volts. This would require considerable amplification to produce a usable signal. Also, a magnetic yoke would be required to concentrate the field into a flux density of the order of 10 kilogauss, since the current range in question is from 0 to 10 amperes.

In the case of the magnetoresistor, at least 3 kilogauss is required in order that a usable resistance change may be obtained. However, over the temperature range of 0 to 50°C (with the field held constant), the resistance will double; therefore, considerable temperature compensation would be necessary. The apparent advantage is one of isolation since these devices are not directly connected into the circuit where current is to be sensed.

Due to the previously mentioned disadvantages, the Hall effect devices are not recommended as the current sensing device. A more desirable technique is a resistor in series with the load; the voltage drop across the resistor is amplified by a differential amplifier.

The differential amplifier offers a good temperature stability since the base to emitter voltage change with temperature is compensated for in the differential configuration. The most satisfactory performance was obtained with a balanced differential amplifier using the Fairchild 2N2223 dual NPN transistor. The inputs to the amplifier were derived from voltage dividers connected on each side of a series current sensing resistor, R_S.

The value of R_S lies between two limits. The upper limit is determined by the maximum voltage drop permissible which was established as 0.5 volts. The lower limit is determined by the minimum signal which may be easily handled in the differential amplifier. The lower limit was set at 0.2 volts. Therefore, 0.3 volts was selected as the tripping level. Various values of R_S were then selected depending upon the desired tripping current.

The recommended dc overload detector is shown in Figure 60 of the main text. The input voltage divider resistors were selected to act as a low impedance source compared to the emitter resistance of 10K ohms. The divider string on the load side was favored by 5 ohms or an input voltage difference of 90 millivolts with no load current flowing. The divider resistors have a tolerance of 0.05% to insure this voltage difference. Since the load side is favored, the transistor on that side conducts under no load conditions. This circuit can be adjusted for any trip current simply by changing the value of R8. The larger it becomes, the greater the trip current will be. The load surge modification of detail A is very useful and is discussed on p.196.

The overload detector can be used with a power switch in either the positive or negative side of the line. However, in a negative ground system the emitter-follower power switch of Figure 59 (with or without the cycling system) should be used for complete fusing protection.

An alternate power switch scheme for dc fusing would be to use a PNP silicon power transistor as the power switch. Its emitter would be adjacent to the bus and the sensor and load would be in the collector circuit. However, a turn-off bias more positive than the +28 vdc source is needed, but this source could be developed by use of an oscillator and rectifier operating from the +28 vdc. Also, the current requirement on this higher voltage source could be minimized by use of a compound connection (Darlington configuration) for the power switch. A drawback to this scheme is that PNP silicon transistors, although now available at 5 amperes and 85 watts, cannot match the performance of NPN silicon power transistors. Germanium PNP

power transistors are available in 50 ampere sizes, but germanium has an unsatisfactory temperature range.

I.6.3 AC Power Switching

AC power switching may be accomplished with either power transistors or SCR's; however, the inverse voltage ratings available in SCR's make them a more attractive choice where the line voltage is greater than 50 volts. Therefore, this discussion will be limited to ac switching with SCR's.

I.6.3.1 Design Philosophy

In order to analyze the problem of ac switching, consideration must be given to the following: line voltage, line current, source frequency, and load voltage waveform. Line voltage, line current, and line transient conditions must be considered in the selection of the SCR. Source frequency becomes a consideration when selecting a control technique and also determines an upper limit of operation since line commutation is suggested as a turn-off technique; therefore, turn-off time should be short when compared with 1/2 period of the source frequency. The desired load voltage waveform must be considered since some turn-on delay is encountered which tends to introduce distortion into the load waveform.

Three phase switching is primarily the same as single phase switching except additional power switches and control circuits are required. One difference might be mentioned. If the three phases are to be controlled from a single control circuit, additional power will be necessary to provide gate excitation to the SCR's in parallel.

I.6.3.2 Specific Circuits

I.6.3.2.1 The Power Switch

In order that a full cycle of power will be delivered to the load, the ac switch must use an inverse parallel configuration as illustrated in Figure 11 of the main text. This connection provides a current path on both halves of the input voltage cycle. The load current and the period of conduction will determine the series of SCR selected. The load voltage and transient conditions will determine which SCR of any particular series is selected. For example, at a conduction angle of 180 degrees and a maximum stud temperature of +100°C, the G.E. C40 series is capable of an average forward current of 8 amperes, while the C60 series is capable of 57 amperes. The C40F has a repetitive peak reverse voltage rating of 50 volts, while the C40E PRV is 500 volts.

An analysis of SCR current requirements when used as an AC switch follow: Some fundamental relationships are:

Parameter	Full Sine Wave	Half Sine Wave
RMS V or I	0.707 peak	0.5 peak
Av V or I	0.637 peak	0.319 peak
RMS/Av V or I	1.1	1.57
RMS Pwr	1 unit	0.5 unit

Now consider the 3 phase, 115/208 vac input to the transformer-rectifier of the dc power system of the matrix program (see Figure 2).

$$P = \sqrt{3}\, EI \cos\theta \approx 1.732\, EI \text{ (primary)} \tag{9}$$

$$P = 43\text{ A} \times 28\text{V} = 1210\text{W (load)} \tag{10}$$

$$\text{therefore, } 1.732\, EI = 1210\text{W} \tag{11}$$

$$I = \frac{1210}{(1.732)(208)} = 3.36\text{ A rms} \tag{12}$$

$$I \text{ peak} = 1.414 \times I \text{ rms (for a full-wave sine wave)} = 4.75\text{ A pk} \tag{13}$$

$$I \text{ rms/SCR} = 0.5 \times I \text{ peak (for a half-wave sine wave)} = 2.37\text{ A rms/SCR} \tag{14}$$

$$I \text{ av} = I \text{ rms} \times \frac{1}{1.57} \text{ (for a half-wave sine wave)} = 1.51\text{ A av/SCR} \tag{15}$$

The average forward current per rectifier was needed because this is the value forming the abcissa of the charts presented as part of an SCR specification.

$$\text{By formula, } \frac{I\text{pri}/\phi = 1.4 \times \text{av. load I} \times \text{sec. leg V}}{\text{pri. line V}} \tag{16}$$

$$I \text{ rms}/\phi = \frac{(1.4)(43)(0.428)(28)}{208} = 3.36\text{ A rms}/\phi \tag{17}$$

This agrees with the former rms value of 3.36A.

I.6.3.2.2 SCR Control Circuits

The SCR requires a gate signal which is positive with respect to the cathode for turn-on. This gate signal may be synchronized to the line frequency of free-running at a much higher frequency than the source. The synchronized technique has the advantage of a constant delay angle; however, more sophisticated control circuitry is required and synchronization must take place at the time the line voltage passes through zero to minimize the delay angle. This type of synchronization becomes difficult at line frequencies of 400 cycles per second and above. At line frequencies of 60 cycles per second, a magnetic synchronization technique is possible; however, at higher frequencies a free-running oscillator appears to produce the most favorable results.

Magnetic Firing Circuit

The magnetic firing circuit is dependent on the switching action of square-loop cores. Refer to Figure 57 of the main text for an example of this technique. Sufficient control current must flow in the "C" winding to overcome the residual magnetism of the core. This control current may be computed from the following equation:

$$I_C = \frac{0.8\, H_o M_L}{N_c} \text{ amps} \qquad (18)$$

H_o of the previous equation is in oersteds and is taken from the material magnetization curve where B = zero; M_L is the mean length of the magnetic path in centimeters. N_c is the total number of turns on the control winding.

The number of turns which make up the A winding (in-line winding) must be sufficient to reset the core when the opposite SCR is conducting under minimum loading conditions.

$$N_A > \frac{(0.8)\,(2H_s)\,(M_L)}{I \text{ min.}} \text{ turns} \qquad (19)$$

The number of turns which make up the B winding must be sufficient to saturate the core to maintain the open condition of the ac switch according to the following equation.

$$N_B = \frac{0.8\, H_S\, M_L}{I_B} \text{ turns} \qquad (20)$$

I_B is the 1/2 cycle average current through the B winding.

Free-Running Firing Circuit

The program used this technique to provide gate control for the ac switches. Figure 21 of the main text illustrates a 33 kcps oscillator and pulse amplifier which supplies sufficient gate drive to sustain each 3 phase switch. One period at 33 kcps is 33 microseconds and 33 microseconds is equivalent to 4.75 degrees at 400 cps; therefore, 4.75 degrees becomes the maximum firing delay experienced with this circuit. If a sinusoidal voltage waveform is assumed, then the anode to cathode voltage cannot exceed 13.4 volts at the time when the SCR is turned on.

The output delivered to the pulse transformer load is a + 5.5 volt, 10 microsecond pulse. Approximately 0.65 amps of emitter current flows during this 10 microseconds. Since one period is 33 microseconds, the output amplifier has a duty cycle of 33%. The following analysis was performed to arrive at the maximum allowable thermal resistivity from case to ambient of the output pulse driver Q5.

The peak allowable power with a finite heat sink is:

$$P_p = \frac{T_j \text{ max} - T_a \text{ max}}{\frac{\theta_{jc}}{C_{pjc}} + \frac{\theta_{ca}}{C_{pca}}} \qquad (21)$$

where

C_{pjc} = transistor coefficient of power

C_{pca} = heat sink coefficient of power

The maximum junction temperature which the transistor will stand is + 200°C (per 2N1486 specification) and a maximum of + 175°C was selected as a conservative design figure. The peak load current is 0.65 amps and the collector-to-emitter voltage while conducting is 1 volt; therefore, the peak power is 0.65 watts. Where the pulse width is short compared to the heat sink thermal time constant as it is in this case,

$$C_{pca} \approx \frac{100}{\text{duty cycle in \%}}; \qquad (22)$$

therefore, $C_{pca} \approx 3.33$. From curves presented in Figure 2-24 of reference 8, it is found that $C_{pjc} = 4.0$, and from the transistor specification, $\theta_{jc} = 7^{\circ}C/W$.

Rewriting the equation given previously:

$$\theta_{ca} = \left[\frac{(T_j - T_a)}{P_p} - \frac{\theta_{jc}}{C_{pjc}} \right] C_{pca} \qquad (23)$$

$$\theta_{ca} = \left[\frac{(175 - 80)}{0.65} - \frac{7}{4} \right] (3.33) = 476^{\circ}C/W \text{ maximum} \qquad (24)$$

Since the calculated value of $\theta_{ca} = 476^{\circ}C/W$, no heat sink was required for Q5. Experimental evidence later established that θ_{ca} of the 2N1486, when operated with the hardware provided, was far below this maximum value. Therefore, a satisfactory thermal environment for Q5 was assured.

I.6.3.2.3 AC Overload Circuit

Current Sensor

As with the dc overload circuit, the first consideration is given to the overcurrent sensing method. The method which seems to provide the most satisfactory results makes use of a current transformer with a bridge rectifier. The bridge rectifier peak output voltage then becomes directly proportional to the peak line current which flows.

The basic theory of a current transformer is the same as any other iron-core transformer. The voltage across the primary terminals is approximately the secondary voltage referred to the primary by the turns ratio. In fact, if exciting current and leakage flux are neglected, the primary and secondary currents are exactly inversely proportional to the number of turns in the 2 windings. For optimum current transformer operation, the load impedance should be constant and there should be zero leakage flux. The following paragraphs outline the transformer design procedure used during the Matrix program.

In order to minimize leakage flux, a toroid core configuration was selected and molybdenum permalloy was selected as a core material to achieve a better temperature stability and overall transformer accuracy. The "Magnetics, Inc. "55206-A2 core was selected. It is desirable to design the transformer and its load in such a way as to reflect a low impedance to the primary. A load impedance of less than 100 ohms is desirable and an output voltage of 10 V provides a workable level. If a secondary load impedance of 75 ohms is assumed, then 135 ma must flow to develop 10 volts. Since 5 amps may flow in the primary, the turns ratio becomes 37 to 1. If 35 to 1 is used, the primary voltage must be 0.3 volts. From Faraday's law with sinusoidal voltage conditions:

$$E = 4.44BAFN\,(10^{-8}) \tag{25}$$

$$\text{Primary turns} = \frac{(E_{primary})}{(4.44)BAF(10^{-8})} = \frac{0.3}{(4.44)(B)(0.221)(400)\,10^{-8}} \tag{26}$$

Assuming a value of $B = 3X10^3$ gauss as an operating flux density, 25 turns are required in the primary. From the turns ratio of 1 to 35, the secondary becomes 850 turns.

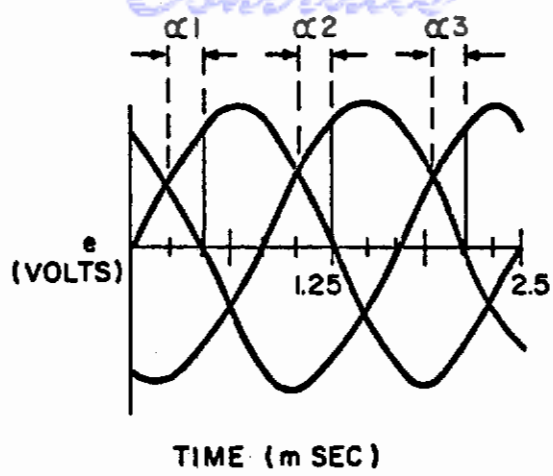
Level Detector

The output voltage level from the current transformer and bridge rectifier combination must be detected at the proper time to provide a trip signal to turn off the ac switch. A unijunction transistor was used as a level detector. This provides good temperature stability; however, the level detector supply voltage must be well regulated. A unijunction transistor is used as a detector. The emitter is connected to the center arm of a 500 ohm potentiometer which acts as a voltage divider and may be adjusted over a wide range of tripping current.

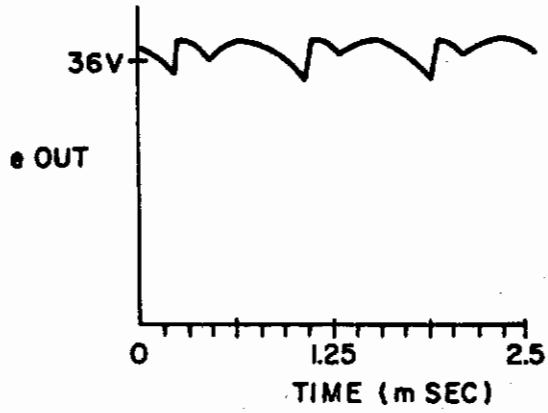
The unijunction output pulse sets a Solid Circuit flip-flop. The flip-flop output then becomes an inhibit signal to an "AND" gate in the ac switch control system. A disadvantage of the unijunction level detector is the requirement for a low impedance source so the unijunction will switch into the valley region when the peak point voltage is reached.

I.6.4 Three-Phase FW Controlled Bridge

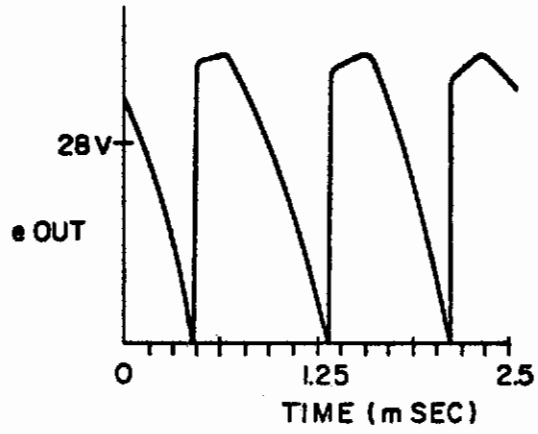
The phase controlled rectifier may be used to provide a variable voltage output. A schematic of a 3 phase, full wave, controlled rectifier bridge is given in Figure 55 of the main text. Figure I-2(a) shows the three phase



(a) Input Voltage



(b) Output Voltage ($\alpha = 10^{o}$)



(c) Output Voltage ($\alpha = 58^{o}$)

Figure I-2. Waveforms of the Phase-Controlled Bridge

input voltage waveform; α is the firing delay angle which must be less than 120° and $\alpha 1 = \alpha 2 = \alpha 3$. By changing α the effective output voltage is changed. The following formula shows the relationship between dc output volts, ac input volts, and the delay angle.

$$V_{dc} = 0.675 \text{ Vrms } (1 + \cos \alpha) \qquad (27)$$

If there were a requirement for two voltage output levels, 36 vdc and 28 vdc, the transformer secondary voltage and the delay angle must be determined as follows:

(1) Assume a minimum delay angle $\alpha = 10^{\circ}$ and vdc output = +36 v. From the above formula V rms must equal 27 v line to line. Figure I-2(b) shows the output ripple waveform where $\alpha = 10^{\circ}$.

(2) Assume Vdc = + 28 v and V rms = 27 v; then again using the above formula $\alpha = 58^{\circ}$. Figure I-2(c) shows the output ripple waveform with $\alpha = 58^{\circ}$.

Since the + 28 vdc output of (2) has a high ripple content, it may be desirable to reduce this ripple by filtering. Note that Figure I-2(c) is the waveform to be filtered and that this waveform closely resembles a single phase, full wave bridge output where the effective frequency of the source is 600 cps and the ripple is 48%. If a choke input filter is used for good ripple reduction at large loads, then L must be greater than some value of critical inductance (L_c) to assure continuous current and to avoid resonance of 2nd and higher order harmonics.

Refer to chart 6.5 of reference 1 and extend this curve to provide a value of $R_L = 0.65$ ohms. Multiply the inductance scale by $\frac{60}{f}$ where f = 600 cps. Then from the graph, $L_c = 0.12$ millihenries. Since the load may vary over a wide range, it would be desirable to use a swinging choke to assure continuous current at light loads. Therefore, assume a load variation from 43 to 3 amps. With this load variation $L_{low} = 0.12$ mh and $L_{hi} = 1$ mh. Adding a safety factor, $L = 0.2/_2$mh and from the same chart R_b was selected as 100 ohms, 10 watt. Refer to chart 6.6 of reference 1 for the selection of C. If the maximum desired load voltage ripple is assumed to be 4% and $\omega = 2\pi f_{eff} = 3760$, then from the chart $\omega^2 L_{low} = 3$; therefore, C = 1000 μfd. The estimated weight of the filter choke is 35 pounds and the estimated volume is 230 cubic inches.

I.6.5 Power Supplies For Control Circuits

The control circuits of the solid state distribution system must be provided with operating voltages. It is desirable that the power for each control circuit be derived from the same bus that is being switched by the power switch

operated by the control circuit. For control circuits of the type used in the Matrix Program several operating voltages regulated to about ± 10% are needed.

Figure 12 of the main text shows a power supply consisting of a closed-loop regulator (VR1, 4) followed by an open-loop regulator (VR2). This acts as a power supply for control circuits operating power switches from +28 vdc. The purpose of the closed-loop regulator is to provide current-limiting. However, an alternate technique would be to use a power switch operated by the dc converter of Figure 58, p. 188 at this point. This would provide current interruption.

The open-loop regulator provides several voltages very efficiently. It consists of a series string of zener diodes from which emitter-followers are operated. The use of emitter-followers greatly reduces the power dissipation in the diode string.

Figure 13 of the main text shows a power supply consisting of a transformer, rectifier, and regulator combination. It is used to furnish power to control circuits that operate power switches connected to the ac bus. VR4 could be replaced by the dc converter and power switch combination previously mentioned. The design techniques used are generally conventional and are discussed in great detail in references 4, 5, and 8.

I. 6. 6 Transients

The broad definition of transients is the changing condition of a characteristic which goes beyond and returns to the steady-state limits within a specified time period. This characteristic may be frequency, voltage, current, etc. When considering a solid state transmission link, voltage and current transients become important in device selection, overload protection and circuit design.

I. 6. 6. 1 Transient Generation

Transients may be generated by the source or at the load. For example, when power is applied to a lamp load or a capacitive load, many times the steady-state current will flow for a short period. This surge of current may be considered as a current transient. The sudden increase in current may cause the supply voltage to decrease (depending upon load regulation characteristics of the supply), thereby generating a voltage transient. Consider any inductive loads which have been conducting and are switched off. Voltage transients will be generated by the loads which are, in general, equal to the rate of change of current through the inductive components multiplied by the inductance factor of the components. These voltage transients are unde-

sirable because they can produce the following: (1) breakdown of circuit insulation; (2) generation of radio interference noise; and (3) requirements for voltage ratings of circuit semiconductor devices which are disproportionate to the steady-state values needed for the circuit.

An an example of typical voltage transients, consider the voltage transient limits in aircraft electrical systems which are established by MIL-STD-704. In particular, the transients which may exist on the +28 vdc bus. Limit one of this specification is an 80 volt evaluated step function of 50 milliseconds duration decaying to 36 volts in 5 seconds. A transient of this magnitude would cause the current to more than double through the power switch if the switch were on; hence, more than four times the normal power (providing the saturation resistance remains constant) would be dissipated at the junction of a solid state device used as a power switch. Since 50 milliseconds must be considered a long term transient when compared with the thermal time constant of most power transistors, it becomes necessary to derate the maximum junction temperature considerably if a transient of this magnitude is to be handled without damaging the switch. If the power switch is off, its maximum voltage rating must be greater than 80 volts.

I. 6. 6. 2 Transient Protection

Since transients are undesirable and may cause equipment failure, an important part of the system design problem is transient protection. The reduction of voltage transients may be accomplished by using suppression devices. These cause the transient energy to be dissipated quickly at a low voltage level in the suppression device, rather than at a high voltage level in the functional components of the circuits. Transient suppression may be necessary not only to minimize the generation of radio frequency interference for the benefit of other electronic equipment, but also to prevent false triggering within the transmission link circuitry itself. All action possible should be taken to reduce transients at their point of origin. This applies throughout the system. It includes not only the distribution system, but the loads on all buses. All loads on the buses should receive adequate transient reduction and should be capable of withstanding the transients which may exist after reduction.

The transient problem can be divided into 2 categories. The first is for power switches that are on; the second is for power switches that are off. For the first category, transient suppressors may be useful. However, the current surges through the power switches due to the long-duration transients must be handled in one of 2 ways. Either the power switch must have sufficient thermal capacity to withstand the current surge, or cycling interruptive circuit breakers must be used to limit the surge. For the second category, a dual

approach may also be taken. Transient suppressors can be used for high voltage spikes of short duration; however, the power switches themselves should be selected with voltage ratings sufficient to withstand the long-duration (compared to the thermal time constant of semiconductor devices), lower-amplitude transients.

Some transients may be removed at their source by connecting a diode in shunt with any inductance present. The diode is connected in the reverse direction so that it will not conduct when the power switch is on; however, if the switch turns off, a reverse voltage is generated across the inductance and the diode now appears as a very low resistance, thereby damping the voltage transient. The maximum steady-state current flowing through the inductance is the maximum current which will flow through the diode.

The correct selection of a transient suppressor requires a knowledge of 4 factors:

(1) Maximum applied voltage;
(2) Maximum surge discharge current;
(3) Clamping voltage at maximum discharge current;
(4) Energy of the surge and the rate of repetition.

Various devices are available which can be used as transient suppressors. Zener diodes, special selenium rectifiers, spark gaps, and neon glow lamps all have the constant voltage characteristic necessary in a voltage transient suppressor. Some examples of these devices are the G.E. Thyrector diode, the International Rectifier Klip-Sel, and the Dale Surge Arresters. The Thyrector diode and the Klip-Sel are selenium rectifiers with a sharp, zener type reverse characteristic. They are available in a wide range of voltage and current ratings. When operated below their maximum ratings, they will exhibit long life, temperature stability, and no measurable time delay between the current through the device and the transient voltage. Some of the disadvantages are relatively low current ratings (as much as 12 ma leakage in the larger units) and a maximum operating cell temperature of 100°C to 130°C.

The Dale Surge Arresters are basically a variable air gap. When a voltage transient becomes greater than the breakdown voltage, an arc is formed; however, unlike a standard spark gap, the arc causes current to flow through a coil which creates a magnetic field. This field causes the arc to rotate down a spiral electrode. The spark is continually lengthened as it rotates and is extinguished before excess current flows. A primary advantage of this suppressor is the high resistance before breakdown; hence, it has very low leakage. Some of the disadvantages are: (1) shorter life than the selenium rectifier type; (2) a minimum voltage breakdown of 300

volts; (3) a changing breakdown point if transients occur frequently; and (4) some ionization time before breakdown occurs (1 microsecond).

I.6.7 References

The following references provide detailed data for the design of switching circuits.

(1) Rectifier Components Guide, General Electric Company, Auburn, New York, 1961

(2) A.I. Pressman, Design of Transistorized Circuits for Digital Computers, J.F. Rider, New York,1959

(3) J. Millman and H. Faub, Pulse and Digital Circuits, McGraw-Hill, New York, 1956

(4) K. Pullen, Handbook of Transistor Circuit Design, Prentice-Hall, Englewood Cliffs, New Jersey, 1961

(5) A Handbook of Selected Semiconductor Circuits, NAVSHIPS 93484, Bureau of Ships, Department of the Navy

(6) Handbook of Preferred Circuits, Volume II, Semiconductor Device Circuits, NAVWEPS 16-1-519-2, BuWeps, Department of the Navy, 1962

(7) Silicon Zener Diode and Rectifier Handbook, Motorola, Inc., Phoenix, Arizona, 1961

(8) Motorola Power Transistor Handbook, Motorola, Inc., Phoenix, Arizona, 1961

(9) Silicon Controlled Rectifier Manual, Second Edition, General Electric Company, Auburn, New York, 1961

(10) Transistor Manual, Sixth Edition, General Electric Company, Syracuse,, New York, 1962

(11) R. Riddle and Mr. Ristenblatt, Transistor Physics and Circuits, Prentice-Hall, Englewood Cliffs, New Jersey, 1958

I.7 RELIABILITY

The reliability of a component or system is the probability that it will give satisfactory performance for a specified period of time under specified operating conditions. Consider a typical system composed of three functional blocks: a sensor, amplifier, and power switch. Let us say that such a system would be considered reliable if it performed satisfactorily nine out of ten times. In other words, the system reliability was 90%. Since the reliability of the total system may be calculated by multiplying together the individual reliability factors of the functional blocks, the reliability required of each block is the cube root of 0.90 or 0.966 which is 96.6%. From this simple example we see that a complex system of many functional blocks will require a reliability greater than 99% for each block in order to achieve an overall system reliability of only 90%.

There are two basic concepts which form the foundations for all procedures concerning the numerical reliability prediction for electronic equipments and systems: (1) that equipments fail by performance degradation, and (2) that equipments become inoperative due to random catastrophic failures of the parts. Although a complete reliability analysis should consider both of these concepts, most degradation failures are usually eliminated as the result of conservative design, type testing, and maintenance practices. Therefore, equipment reliability is primarily determined by the number of catastrophic failures incurred as a function of time.

I.7.1 Component Reliability and Failure Rates

High quality components do not guarantee the reliability of the finished system but they do make a higher degree of reliability possible or achievable. In general, time and stress are the most significant factors in determining component reliability. Since this is usually true, the primary responsibility for increased reliability lies in the design techniques used by the circuit and system designers. Component stress may be controlled through intelligent, conservative design procedures which take into account worst case conditions both environmental and electrical. Two examples of conservative design procedure are the derating of h_{FE} from typical values to assure saturation of transistors under all conditions, and the maintenance of junction temperatures below the maximum ratings to reduce device thermal stress. A number of techniques such as redundancy may be used to compensate the shortcomings of components; however, all such schemes increase size or weight or power consumption or add undesirable complexities to the system.

The inherent reliability of any equipment is determined by: (1) calculating the failure rate for each part based upon the stresses to which it is subjected, and (2) summing the failure rates for all such parts employed in the equipment.

I.7.1.1 Semiconductor Devices

It is believed that failure rates for semiconductor devices are primarily a function of junction temperature. The philosophy used is to present failure rates as a function of ambient temperature and device power dissipation. Experience indicates that failure rate curves tend to have a flat portion at low temperature end and a rapidly rising portion. In the flat portion, temperature increases produce no perceptible increase in failure rate. In the rapidly rising portion, failure rates increase exponentially with temperature. Other factors such as overvoltage, vibration, radiation, and poor encapsulation contribute to the failure rate of semiconductor devices.

In general, failure rates for transistors when operating well within the manufacturer's specifications will fall between 0.02 and 0.2% per 1000 hours of operation. For example, the 2N2226 power transistor when operated at an ambient temperature of 80°C, a case temperature of +125°C, collector current of 5 amperes, has a predicted failure rate as per the methods of calculation presented in MIL-HDBK-217 of 0.025%/1000 hrs. Diodes have approximately 1/2 the failure rate of transistors; therefore, their failure rates will normally fall between 0.01 and .1% per 1000 hours.

Available test data for the solid state integrated circuits used in the Matrix program indicate a failure rate for these circuits of 0.13% per 1000 hours of operation at +85°C. The tests were performed per MIL-S-19500B plus even higher stress conditions in some cases. It should also be noted that this particular device is a new product (1961) and considerable improvement is possible as improved process controls are achieved along with higher manufacturing levels. Each network which was tested to provide this data was the equivalent of approximately 20 discrete components interconnected as one circuit.

I.7.1.2 Resistors

Resistor failure may be caused by a number of factors; temperature, electrical stress, humidity, shock and vibration, altitude, etc. The primary factors are temperature and electrical stress; and, resistor failure rates are based on these two factors. At +80°C, the failure rate for composition resistors varies from 0.004 to 0.04% per 1000 hours. The failure rate for film resistors at +80°C varies from 0.04 to 0.1% per 1000 hours and the failure rate for accurate wirewound resistors ranges from 0.1 to 0.2% per 1000 hours.

I. 7. 1. 3 Capacitors

One-half of all capacitor failures are caused by improper selection and application. Some of the primary causes of capacitor failure are: current and voltage overload, temperature, frequency effects, pressure, humidity, shock, and vibration. Overheating is one of the chief factors decreasing capacitor reliability. Whether incurred as a result of overload, high ambient temperatures, or high power factors combined with ac currents, high operating temperatures will introduce high failure rates. For a part temperature of +80°C, the failure rate for wet slug and foil tantalum capacitors is 0. 02 to 0. 1% per 1000 hours, for solid tantalum the failure rate ranges from 0. 04 to 0. 4% per 1000 hours.

I. 7. 1. 4 Inductors and Transformers

The reliability of inductors and transformers depend primarily upon type of insulation, ambient temperature, and electrical stress. Most failures consist of breakdown of the insulating material due to insulation embrittlement and degradation of insulation resistance. The causes of failure are excessive voltage or current, fluctuation of input frequency, and corona. Excessive voltage can puncture the insulation. Excessive current will cause overheating with a consequent weakening of the dielectric strength of the insulation, or open or short-circuited windings. Frequencies lower than the lower limit of design will result in higher than design currents; above the upper design limit, higher core losses will result. In either case, additional internal heat will be generated; hence, decreased dielectric strength of the insulation. As the temperature of a given insulation increases, its dielectric strength decreases. Corona occurs at points of high potential stress and causes accelerated aging of the insulation. This creates weak spots in the insulation and eventually leads to insulation breakdown. The failure rates for transformers and inductors suitable for operation at 80°C, range from 0. 07 to 0. 7% per 1000 hours.

I. 7. 2 System Reliability

It may be said that the reliability of any system can only be as good as the engineering ability of the people involved in device selection, circuit design, and system development. Therefore, engineering ability is the only guarantee of a reliable system. Reliability must be designed into a complex system.

Despite the precise appearance of equations used when predicting system reliability, the processes are almost entirely random. In fact, it is just this behavior which allows mathematical analysis. The basic assumption which is made in any analysis of system reliability is that the probability of a particular event is the same for any interval of time inde-

pendent of where this interval is situated and of the past history of the system. This means that the average failure rate is a constant, which is approximately correct if taken after the initial period of operation and before the equipment wears out. The failure rates are abnormally high during the initial "burn-in" period and the "wear-out" period.

Quite often, failure rates are more meaningful if converted into the reciprocal relationship, Mean Time Between Failures (MTBF). Therefore, for example, an equipment failure-rate summation of 200% per 1000 hours can be expressed as a MTBF of 500 hours. A MTBF figure is an attainable figure providing reasonable preventive maintenance practices are followed so that most deterioration-type failures can be anticipated and corrected before equipment failure occurs.

Equipment has a certain level of inherent reliability when it leaves a contractor's plant. This level of reliability assumes reasonable maintenance, proper installation, and operation in the specified environment. These desired conditions are not always met; hence, the level of reliability obtained in the field is usually less than the inherent reliability and is called operational reliability. A high maintenance rate indicates low operational reliability. From this it can be seen that the design and production of more reliable equipment are not the only objectives when attempting to increase the MTBF.

The principle of redundancy is an important method which may be used to increase the inherent reliability of an electronics system. Redundancy is the concept of providing duplicate functional units which allow continued performance if a failure should occur. In general, the following statements may be made concerning redundancy.

(1) Where redundancy is employed, systems will be larger, heavier, and usually require more power.

(2) A careful analysis should be undertaken to determine which circuits will benefit the most from redundancy.

(3) Since redundancy may conceal failures, testing procedures must be devised to check both circuit paths.

(4) Redundant techniques should only be applied to active elements since they have a lower survival probability than passive elements.

(5) Provide parallel redundancy for circuits where there is a high probability of open-circuitry and series redundancy for circuits where there is a high probability of short-circuiting.

(6) Incorporate adequate fusing and decoupling to permit the take-over by the redundant circuit if a failure occurs.

I.7.3 References

A more rigorous analysis of both component and system reliability may be obtained from the following references.

(1) "Reliability Stress and Failure Rate Data for Electronic Equipment," MIL-HDBK-217, 1962.

(2) "Solid Circuit Reliability Report First Quarter - 1962" Texas Instruments Incorporated.

(3) "How to Design for Transistor Reliability," Electronic Equipment Engineering, March, April, May, and June 1959.

(4) "Reliability of Military Electronic Equipment," MIL-STD-441, 20 June 1958.

I. 8 ENVIRONMENTAL EFFECTS

The environmental effects on solid state circuitry are many and varied. An electronic system may encounter variations in temperature, radiation (both nuclear and electromagnetic), shock, vibration, pressure, humidity, and fungus. For example, consider the environment of an electronic package in an aerospace vehicle. This environment includes launch vibration, high temperatures from propulsion combustion and re-entry, low temperatures from a cryogenic propellants, and radiation from clestial bodies and perhaps from on-board nuclear reactors. The electronic system must not only survive, but must function properly in this environment. Each factor of a complex environment must be considered if satisfactory operation is desired.

I. 8. 1 Temperature

Thermal effects are generally given primary consideration in solid state design since semiconductors are quite temperature sensitive. Transistor gain, maximum power dissipation, leakage current, and collector to emitter saturation voltage are all affected by temperature. When a transistor is used at high junction temperatures, it is possible for regenerative heating to occur which will result in thermal run-away and the possible destruction of the transistor. The maximum power dissipation of a semiconductor is primarily dependent upon the maximum junction temperature which may be maintained without destroying the junction. Since power dissipated at the junction causes a heat rise referenced to the ambient temperature, the maximum power dissipating capability of a transistor is dependent upon the ambient temperature of its environment. At low temperatures a major problem encountered in the operation of transistors is the reduction in both ac and dc current gain.

Thermal stress may also affect the mechanical structure of a semiconductor device. Expansion and contraction of materials with different coefficients of expansion can cause open electrical connections and broken seals, thereby exposing the semiconductor material to moisture. Two techniques may be used to combat the thermal effects on solid state circuits. A cooling system may be used to maintain a more constant temperature than the overall environment exhibits and/or conservative design practices may be followed which take into account the upper and lower temperatures which may be encountered. These upper and lower limits of temperature are primarily limited by the availability of active devices. If the thermal environment exceeds these limits a cooling system is required.

I. 8. 2 Radiation

A great deal of emphasis is now being placed upon nuclear radiation effects.

Both the natural electron and proton radiations of space and the neutron and gamma radiations introduced by nuclear power supplies are of critical interest to system designers engaged in space work. Missile systems must be able to operate despite atomic blasts from anti-missile missiles. Surface equipment must remain operational during and after an atomic blast. Sattelites must operate during intense radiation generated by solar flares and while passing through the Van Allen Belts. Therefore, radiation becomes an important environmental factor.

Semiconductor materials are affected by radiation in various ways, but the fundamental effect is the changing of minority-carrier lifetime. This causes transistors to exhibit a decrease in current gain when subjected to radiation. In a diode, the shortened lifetime resulting from radiation increases the forward voltage required to pass a particular current. It is interesting to note that contrary to what is usually assumed, germanium is 3 to 30 times more radiation resistant than silicon. Transistors can be expected to fail if subjected to radiation of the order of 10^{11} to 10^{14} nvt. Electrolytic capacitors are also susceptible to radiation damage and tend to fail below the radiation level of 10^{16} nvt.

Effects produced by purely electromagnetic radiation are not yet fully understood. Some semiconductor device types are sensitive while others are quite insensitive. However, it has been impossible to discern a pattern in the wide variation of results obtained from different device types.

I. 8. 3 Shock and Vibration

The mechanical integrity of an electronic system may be compromised if insufficient attention is paid to suddenly applied forces (shock) and periodic motion (vibration) which may be encountered. Electrical and mechanical connection can be broken causing failure of the system. The protection of an electronic system against the hazards of shock and vibration presents many varied problems to the designer. Unfortunately, there are no blanket rules solving these problems and each problem must be considered separately.

Vibration in aircraft can be expected to range from 1. 5 to 10, 000 cps and space applications can exceed this range. The electronic system designer usually must consider primarily the internal structure of the equipment and the method of mounting the system in the aircraft, space vehicle, etc. When considering the internal structure of the equipment, the positioning and arrangement of the component parts are of primary concern. Some general rules to follow for proper mechanical placement are:

1. locate heavy components on the corners of the chassis and as low as possible in order to keep the center of gravity of the equipment low,

2. do not align chassis holes so that the chassis is easily torn,

3. avoid long-lead lengths on components,

4. bind conductors into cables and clamp to the chassis, and

5. do not rely on solder for mechanical strength.

The method of mounting the system may be direct or with isolators. If at all possible, the equipment should be designed without shock and vibration isolators. However, equipment built for nonisolation must be rugged and able to withstand the shock and vibration environment. If isolators are used they serve two functions. One function is to isolate or attenuate vibration and the other is to control or establish the resonant frequency of the equipment. Unless both vibration attenuation and stability are accomplished, the isolating system is unsatisfactory.

I. 8. 4 Altitude-Pressurization

One of the effects of a pressure change is the accompanying change in the effectiveness of convection as a cooling technique. As pressure goes down the amount of heat transferred by convection decreases. Low ambient pressures present suitable conditions for corona formation and arc-over. Pressure variations also cause equipment "breathing" which results in moisture condensation. Metals that are somewhat unstable may sublime and condense on cold areas if exposed to the vacuum of space. Thereby, electrical short circuits could be formed.

The critical breakdown voltage of air decreases with altitude (pressure). For example, an air gap which breaks down at 10 kvdc at sea level, breaks down at 2 kvdc at 70,000 feet. Since the voltage gradient between two adjacent parts is influenced by the radius of curvature of each part, spherical or rounded terminals rather than sharp-edged shapes should be used when dealing with high voltages.

To avoid the effects of low air pressure, pressurized units are sometimes used to house electronic equipment. The advantage of enclosing the equipment in a pressurized container is that performance is independent of atmospheric pressure and humidity. The disadvantages are: (1) aggravation of heat transfer problem; (2) increased size and weight; (3) additional pressuring equipment is required.

I. 8. 5 Moisture

Moisture affects electronic equipment in many ways. Component parts may absorb moisture, thereby changing circuit constants. Mechanical fea-

tures may be altered by swelling, warping, or corrosion. The presence of moisture on the surface of a material reduces the surface resistance and may cause short circuits to develop. Changes in capacitance of a circuit due to moisture may change the frequency of a tuned circuit or the calibration of a variable-frequency circuit. Rapid cooling of the equipment results in condensation from humid air and possible freezing of the water which has been condensed.

Encapsulation of parts is one technique which may be used where the effects of moisture upon electronic equipment is a problem. Two different approaches are possible when considering the embedment of electronic assemblies: the embedment of the entire assembly, which has not proved too successful, and the embedding of certain components as a unit. Embedment also provides good protection against shock damage, eliminates the need for some mounting hardware, prevents unskilled tampering and adjustment in the field, and is relatively cheap. However, it adds electrical losses, multiplies stray capacitances, may present thermal problems, makes replacement of parts more difficult, and will add weight to the assembly. Therefore, the specific application of the equipment must determine whether or not encapsulation is advantagous.

I. 8. 6 References

The following references provide detailed information concerning environmental effects upon electronic equipment.

1. "Criteria for Environmental Analysis of Weapon Systems," C. Eiwen, D. Winer, WADD Tech. Report 60-627.

2. "Handbook of Instructions for Aircraft Designers," Vol. I, AFSCM 80-1.

3. "Design Factors for Aircraft Electronic Equipment, " WADC Tech. Report 56-148.

4. "Reactor Irradiation of Semiconductor Devices," L. Taylor, IRE Transactions on Nuclear Science, Vol. NS-9, No. 1, Jan. 1962.

5. "Nuclear-Radiation Circuitry Design and Test, " J. Perkins, same source as ref. 4 above.

6. "Electronics in Outer Space," J. McQuary, Electronics World, Oct. 1959.

7. "Cryogenic Testing of Electronic Components, " E. Clinger,

presented at the 17th Annual Meeting of the American Rocket Society, Los Angeles, California, Nov. 1962.

8. "Nuclear Blast Effects on Components and Equipment," L. Kaplan, R. Saelens, Electronic Industries, Oct. 1962.

I. 9 PACKAGING AND INSTALLATION

The packaging and installation of any particular system is usually a unique problem and each system must be handled differently. However, there are certain aspects of the problem where some general rules will apply.

I. 9. 1 Required Data

Such things as RFI and line voltage drop may determine the location of certain functional blocks of the system. Therefore, the basic layout becomes a preliminary step in packaging and installing the various parts of any system. Environmental effects on circuits may also determine location, since special mounts and shields may be necessary to minimize the effects of temperature, radiation, vibration, etc.

Semiconductor devices are inherently temperature sensitive; therefore, the heat sinks and cooling system play a large role in determining packaging and installation methods and techniques. In order to analyze the thermal problems which may be encountered in any particular installation, the primary sources of heat must be recognized; hence, data which will provide device power dissipation is necessary. For the same reason, the maximum allowable component temperatures must also be considered. The power requirements of any system should be determined, especially where line currents are large enough to cause significant line loss.

The combination of sensitive bistable devices and circuits handling high power pulses may create significant problems requiring extensive shielding of circuits and cables. In general, it is desirable to minimize lead length where high frequency, high level pulses are being transmitted and to separate any sensitive circuits from undesirable signal sources.

I. 9. 2 Cooling Techniques

Techniques for controlling temperature vary in nature from design features, such as the surface finish and color, to flight control of speed and path. The use of metal heat sinks, ablation surfaces, radiation, and transpiration cooling are employed for re-entry vehicles. By means of controls, a temperature range can be maintained within which equipment will operate efficiently. Every effort should be made to integrate the cooling requirements and provisions for all the electronic equipment installed in a vehicle in an effort to reduce the overall penalty on vehicle performance.

As long as power is being dissipated, it will be rejected in the form of heat; therefore, the purpose of any electronic cooling system is to provide a low thermal resistance path to a heat sink so that this waste heat will be

absorbed.

Miniaturization and high density packaging has led to ever increasing heat concentrations and has increased the complexity of cooling techniques. Effective cooling of electronic equipment is of prime importance in obtaining satisfactory life, reliability, and performance.

I. 9. 2. 1 Approach to Thermal Design

In order to define the thermal parameters, the rate of heat production in the system and the desired surrounding thermal environment must be determined. The dissipated power within the system elements can usually be measured or calculated. The cooling system must then be designed to maintain the desired thermal environment.

The three methods of heat transfer -- conduction, convection, and radiation -- may be used to achieve this desired thermal environment. The transfer of heat from a semiconductor device to its mounting bracket is primarily by conduction; therefore, the points of contact between the device and the mounting surface are of great importance. This thermal connection should be tight with as much surface to surface contact as possible. Preferably, no insulator should be used and a lubricant such as silicon grease will improve the thermal path from the device to the mounting bracket. Resistor lead lengths should be kept short and where possible, the body of the resistor should be clamped to a mounting surface. This mounting technique will provide the best thermal conduction path. In many applications conduction will be the only important heat-rejection method available. In the vacuum of space, convection is absent and conduction is the best means of cooling modules even though the equipment heat must ultimately be radiated.

Convection takes place from the surface of a solid to moving masses of fluids, either gaseous or liquid. For example, if a power dissipating device is mounted on a bracket with relatively large surface area when compared to the device surface area, convection will be important in transferring heat from the mounting bracket to the surrounding fluid. Convection currents will occur naturally from a temperature differential or may be caused by blowers or pumps. This latter case is called forced convection. Of prime importance in heat transfer by convection is fluid velocity, surface area, and temperature difference. Convection is also affected by fluid density. For example, in the case of air, free convection is only 50% as effective at 30, 000 feet as it is at sea level.

The third method of heat transfer is radiation. Bodies under thermal agitation emit electromagnetic waves ranging in wave length from the long infrared to the short ultraviolet. Major factors determining the rate of heat

transfer by radiation are surface area, temperature difference, and surface emittance. Surface emittance is dependent upon color, roughness, and material. The surface emittance of polished copper, for example, is 0.023, whereas that of oxidized cast iron may be as high as 0.95. Most materials used in electronic systems may be assumed as having a surface emittance from 0.5 to 0.8.

From the previous discussion, the thermal problem may be simplified by considering the mounting plate or bracket of a semiconductor device which is dissipating an appreciable amount of power as a heat source and the surrounding fluid as the ultimate heat sink.

I.9.2.2 Device Heat Sink Design

The design formulae contained herein are usually simplified approximations and are only presented here to provide a means to achieve a preliminary design.

In the practical situation, the ambient temperature is the uncontrolled variable and the junction temperature of a semiconductor device must be controlled by the thermal resistance, θ, from the source to the ultimate heat sink. The thermal resistance from the device heat sink to the surrounding fluid is dependent upon the type of material, shape, thickness, color, area, temperature, and air flow. The maximum allowable value of θ_{sink} to ambient (θ_{sa}) may be calculated from the following equation:

$$\text{Max } \theta_{sa} = \frac{T_j\,(max) - T_a}{P_{dis}} - \theta_{cs} = \theta_{jc};\ ^{\circ}C/W \qquad (28)$$

where

θ_{cs} is the thermal resistance from case to the device mounting sink,

θ_{jc} is the thermal resistance from junction to case.

θ_{jc} is usually provided by the device manufacturer (2N2226 transistor $\theta_{jc} = 0.5^{\circ}C/W$). θ_{cs} is determined by the method of mounting the device to the sink and may range from $0.1^{\circ}C/W$ with no insulator and silicon lubricant to $1.45^{\circ}C/W$ with a teflon insulator and no lubricant.

After the maximum θ_{sa} is known, the maximum heat sink temperature may be calculated from the following formula:

$$T_{sink}\,(max) = T_a\,(max) + \theta_{sa}\,P_{dis} \qquad (29)$$

The total heat transfer from sink to ambient can be expressed as follows:

$$P = (hr + hc)\, a' \eta\, \Delta T \qquad (30)$$

where

P = device dissipation (watts)
hr = radiation heat transfer coefficient (watts/in^2 $^\circ$C)
hc = convection (free or forced) heat transfer coefficient (watts/in^2 $^\circ$C)
A = total surface area of heat sink (in^2)
η = fin effectiveness factor
ΔT = temperature difference between hottest point on sink and ambient ($^\circ$C).

The radiation coefficient h_r may be determined from the following equation:

$$hr = 1.47 \times 10^{-10} \varepsilon \left(\frac{\Delta T}{2} + 273 \right)^3 ; \text{ watts/in}^2\ ^\circ\text{C} \qquad (31)$$

where

ε = the surface emittance.

The convection coefficient hc, in free air may be approximated at 4×10^{-3} watts/in^2 $^\circ$C. This value is actually for $\Delta T = 30^\circ$C and a vertical length of fin of 3 inches; however, the error will be small if there is not too great a deviation from this temperature difference and fin length. The fin effectiveness factor may be approximated at 0.8 for most normal fin configurations.

These approximations and assumptions have been made on the basis that any cooling problem of this type can best be solved by a short preliminary design to reach a rough approximation and then sufficient experimental data to achieve more optimum results.

I.9.2.3 Forced Air Cooling

Increasing the air velocity past a heat source results in a decreased resistance to heat transfer across the air film. This will result in heat transfer rates many times that of natural convection. The general heat transfer equation for a fluid flowing past a heated surface is:

$$q = hc\, A\, \Delta tm \qquad (32)$$

where: q is the heat rate (watts)
hc is the coefficient of convection (watts/in^2 °C)
A is the area of the heated surface (in^2)
Δtm is the mean temperature difference (°C)

The amount of thermal energy absorbed by air is given by:

$$q = wc\,\Delta t \qquad (33)$$

where: Q is the thermal energy absorbed by air (Btu/hr)
w is the airflow rate (lbs/hr)
c is the specific heat (Btu/(lb)(°F))
Δt is the air temperature rise (°F)

From this equation, we see that w is directly proportional to Q; however, any device used to increase air flow will add additional heat to the system. Hence, a point of diminishing returns may be reached where very little increase in heat transfer rate is noted with increasing w.

I. 9. 3 Packaging

The mechanical aspect of electronic equipment design is circuit packaging. Effective packaging provides more functions per cubic foot and per pound. The miniaturization of electronic parts is the primary method of increasing packing density.

I. 9. 3. 1 Miniaturization

The first basic requirement for miniaturization is that the reduction in size and weight shall not limit performance or service conditions. Miniaturization at the very least must retain the previous quality level.

Electronic-part miniaturization has been accomplished by both miniature discrete elements and integrated circuits. Miniaturization is commonly judged by element density and an element density of 60 components per cubic inch on the equipment level is usually considered miniaturized. Miniature discrete elements have the advantage of retaining adequate design flexibility and permitting component value changes. Microminiature capacitors, resistors, inductors, diodes, and transistors are available to the circuit designer. These components can be used to form conventional circuits and some increase in packing density will be achieved. However, this technique has the disadvantage of still requiring interconnections between parts which limits the degree of packing density achievable.

The integrated circuit permits increased packing density over the

microminiature component approach. Element-to-element connections are integral in the circuit; hence, less space is required for these connections. Each integrated circuit performs a conventional circuit function and can be represented by conventional circuit symbols although they also may be handled as blocks with only the inputs and outputs of concern to the equipment designer.

The uniform envelope lends itself to modular packaging and production tooling. These circuits may be packaged into planar assemblies or welded stacks. The stack configuration has the highest potential for element density and an element density of 20,000 parts per cubic inch is possible. The interconnections to the stacks are usually made by welding rather than soldering in that joints can be made closer to the body of the circuit and closer to other joints. Also, welded joints are more frequently self-supporting.

In the planar configuration, the circuit blocks are arranged in a geometry similar to that of printed circuit boards. The planar assembly features accessibility, easier assembly, predetermined conductor geometry, suitability to convection cooling, reduced inter-element capacitance, suitability to soldering, and easier maintainability. The planar approach is usually more compatible with hybrid systems. The size advantage of hybrid equipment over completely conventional equipment depends directly upon the percentage of the equipment suited to the integrated circuit approach. For example, a system having a 50% suitability can be reduced to 51% of the original volume.

It is commonly said that high packing density means high heat density; however, high density packaging offers a short thermal exit path which tends to somewhat compensate. Tests have been run which demonstrate the ability of encapsulated modules to reject heat by conduction through one face of the circuit block. The result is a combination of good thermal transfer of the integrated circuit case (ceramic), the fair conduction of the embedment compound, and the short thermal path.

I.9.3.2 Conventional Devices

Even though there is a great difference in possible packing density, between the previously mentioned microminiaturized components and circuits and more conventional components, there are still applications where the conventional devices should be used. The miniaturized components and integrated circuits are expensive and in some cases difficult to handle. Techniques and processes have long been in existence to handle conventional devices; hence, re-training and re-tooling are not required.

Microminiaturized components and circuits are low power level devices; therefore, conventional components must still be used in applications where high power signals are required. Therefore, combinational or hybrid systems

of both microminiaturized components and integrated circuits and conventional components seem to be the rule for the immediate future, at least until device manufacturers solve many of the problems which confront them today.

I.9.4 References

Further coverage of packaging and installation considerations is beyond the scope of this manual and more detailed discussions may be obtained from the following references:

1. "Guide Manual of Cooling Methods for Electronic Equipment," NAVSHIPS 900, 190.

2. "Aircooled Electronic Equipment, "AF Technical Report No. 6579.

3. "Packaging of Miniaturized Electronics," Ernest C. Singletory, a paper given at the Seventh Region Conference, I. R. E., 1962.

4. "Survey of Microminiaturization of Electronic Equipment," R. V. Horton, T. D. Smith, AFBMD-TR-60-57, STL/TR-59-000-09957.

5. "Techniques of Microminiaturization," D. H. Roberts, D. S. Campbell, presented at the convention on "Radio Techniques and Space Research" in Oxford, 1961.

6. "Applying Dot Components to Electronic Packaging," J. R. Goodykoontz, R. C. Frank, Electronic Industries, Oct. 1961.

7. "Maintainable Electronic Component Assemblies," H. Wasiele, Jr., presented at the Second International Packaging Symposium, Boulder, Colorado, 1961.

8. "A New Mechanical Approach for the Construction of Modular Electronic Equipments," R. C. Swengel, W. R. Evans, ASME, Aviation Conference, Los Angeles, Calif., 1961.