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Technical Reliability Study

MICROCIRCUIT SCREENING EFFECTIVENESS

RAC

1978

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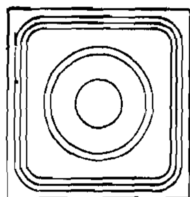

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Technical Reliability Study

MICROCIRCUIT SCREENING EFFECTIVENESS

1978

Prepared by:

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Under Contract to:

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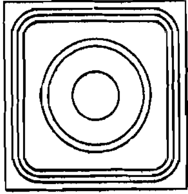

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Data are collected on a continuous basis from a broad range of sources including testing laboratories, device and equipment manufacturers, government laboratories, and equipment users, both government and nongovernment. Automatic distribution lists, voluntary data submittal, and field failure reporting systems supplement an intensive data solicitation program.

Reliability data documents covering most of the device types mentioned above are available annually from RAC. Also, RAC provides reliability consulting and technical and bibliographic inquiry services which are fully discussed at the end of this document.

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PREFACE

The purpose of this report is to broaden the readers awareness of the factors affecting the reliability of microelectronics through the application of screening techniques. The information compiled within this document should provide a valuable resource to those responsible for design, specification, testing and failure analysis of integrated circuits.

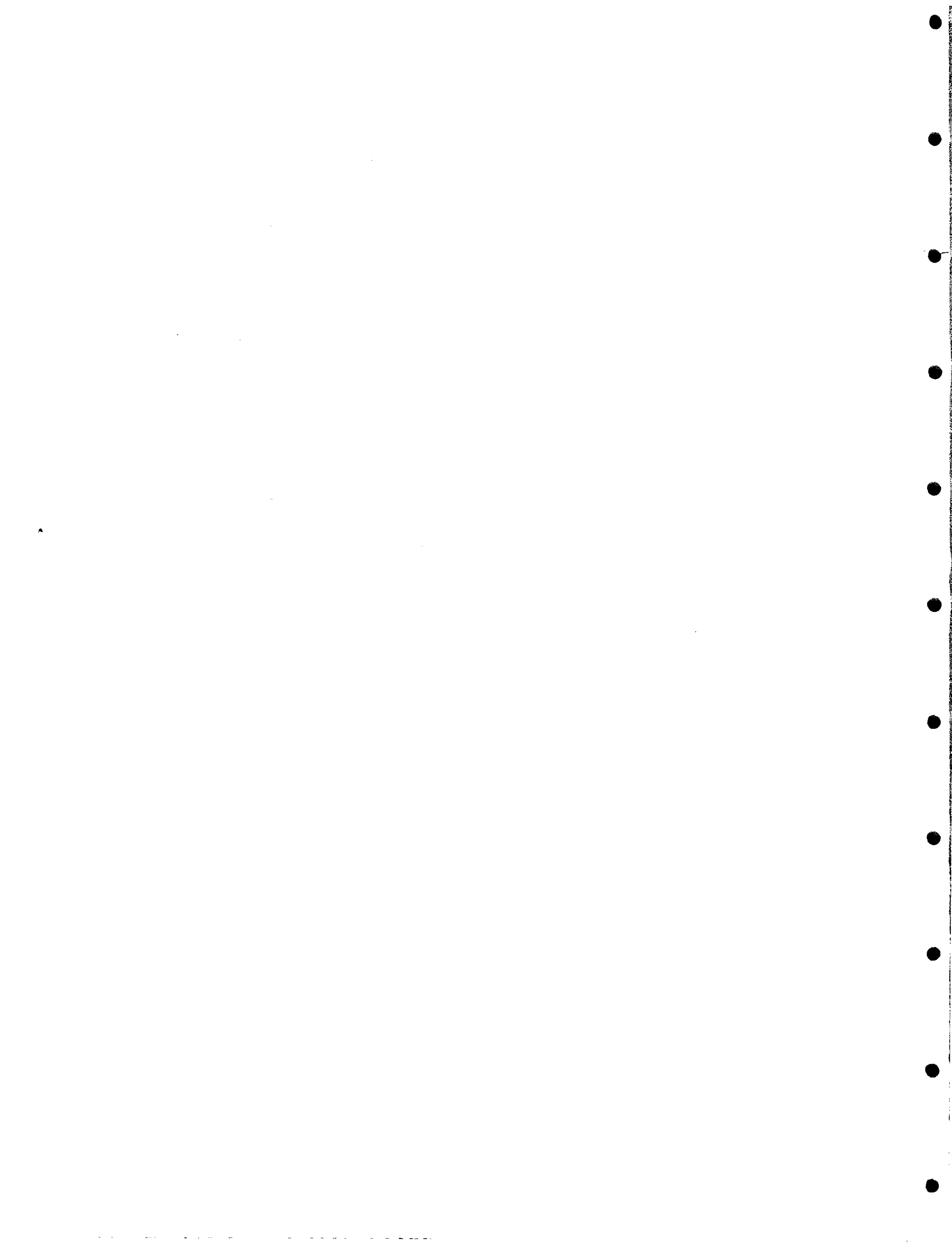
This document is prepared as part of the Reliability Analysis Center's (RAC) continued responsibility to provide new information on the reliability of electronic devices. The bulk of the information reported herein has been obtained through an active data solicitation program. The reliability data related to component screening in this document have also been, or will be, reported in the RAC Data Publication Series.

This report is one of a new series of documents being prepared by RAC treating topics of particular interest to the electronics industry. Other technical reports under preparation include:

Failure Mechanisms of Microcircuit Metallizations

Electrostatic Discharge Damage in Microcircuits

The primary responsibility for the compilation and accuracy of this document rests with Mr. H. C. Rickers and the Reliability Analysis Center staff. However, equal credit must be given to the many people who performed the tests and took the time and effort to document their results.



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INTRODUCTION

The advent of complex equipments incoporating large numbers of integrated circuits has further emphasized the importance of microcircuit reliability programs. Product reliability can only be realized by combining the proper uses of compatible materials, processes and design practices. While it is not possible to test reliability into a product, testing can be instrumental in identifying and eliminating potential failures while not adversely affecting good components.

Unfortunately, product reliability is often compromised by economic considerations. In some commercial applications the greatest profit may be achieved by producing equipment of the lowest quality level that will meet the required product specifications and warranty commitments. However, even this practice would require extensive knowledge of device quality, as well as the capability to predict the quality level throughout the warranty period.

A general approach for evaluating reliability involves concepts pertaining to failure rate as a function of age. In general, the total life of a large device population can be categorized into three distinct intervals defined as follows:

1. Infant mortality period - Initially, a population exhibits a high failure rate resulting primarily from device failures caused by process defects, marginal design and testing errors. The failure rate rapidly decreases, eventually stabilizing at some value at the end of this initial period.

2. Useful life - After the infant mortality period, the population failure rate remains relatively constant, characterized by random failures. This useful life period extends until the effects of wearout spawn an increase in the failure rate.

3. Wearout - The onset of the wearout period is characterized by a rapidly increasing failure rate resulting from the degenerative effects of fatigue and accumulated wear.

Optimizing product reliability involves special consideration applied to each of the three life intervals. Infant failures should be eliminated from the device population by controlled screening and burn-in procedures. Adequate derating factors and design guidelines should be employed to minimize stress-related failures during the normal operating lifetime of the product. Finally, the effects of component wearout should be eliminated by timely preventive maintenance.

To properly assess the reliability of devices in the early life period, the impact of manufacturing-process-induced defects and the efficiency of conventional inspection methods and reliability screening tests must be evaluated. Two major defect classifications are considered to be dominant in the infant mortality period: quality defects and latent defects.

A quality defect is one which may be found by employing normal quality control inspection equipment and procedures without stressing the component. A latent defect is one which will escape the normal quality control procedures and requires component stressing in order to be detected by inspection at the propagated failure level.

Conventional inspection methods utilizing visual observation and/or measurement rejection criteria are designed to segregate anomalous devices. Associated with every inspection is an efficiency factor whose value depends on the rigor of the inspection operation. A well-planned inspection station utilizing detailed criteria, proper instrumentation and trained personnel will exhibit a high inspection efficiency. However, no inspection is perfect; 100% efficiency is impossible to attain.

Similarly, there is also an efficiency factor associated with screening tests which represents the ability of the screen to convert latent defects to actual defects. These tests, based on time, stress type, and stress level, precipitate as failures the defects which can be removed by conventional detection methods.

The determination of the efficiency factors associated with conventional screen tests for various technologies is essential to the derivation of an optimal screening program. The most proficient method for determining representative efficiency factors for conventional screening tests, and subsequently an optimal screening effectiveness program, involves a five-step approach:

1. Determine the dominant failure modes experienced in each technology and package configuration, as well as the impact of variables such as device complexity on those failure mode distributions.

2. Investigate the types and magnitudes of stress which activate the various failure mechanisms and associated failure modes. Relate these stresses and stress magnitudes to those specified in conventional screens.

3. Examine screening data for each technology to establish the range and the average reject rates actually experienced in the conventional screen tests. When available, the information concerning the types of failure modes eliminated in each screen should be reviewed.

4. Analyze the field experience of screened devices to determine for each technology the screening escape rates and the types of failure modes which escape screening.

5. Combine all reliability information to formulate efficiency factors for individual screening tests for various technologies and package configurations. These efficiency factors can be merged with screening cost information to determine overall screening effectiveness.

This study is therefore devoted to reporting and assessing the screening fallout and failure mode and mechanisms information available for microcircuit devices. This information is utilized to determine efficiency factors of individual screens/tests and is then combined with cost information for the assessment of screening effectiveness. This type of analysis provides the proper guidance in determining the optimal screening program for any specific situation.

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Section 1

DESIGN FACTORS INFLUENCING MICROCIRCUIT RELIABILITY

One of the primary steps in evaluating screening effectiveness is the analysis of the various types of malfunctions experienced within each of the microcircuit technologies. The types of malfunctions experienced will be strongly influenced by those structural characteristics of a given device which may affect performance when the device is subjected to electrical and environmental stresses. As an introduction to the analysis of malfunction experiences, an investigation of the device defects and structural design factors and their influence on the microcircuit reliability is desirable.

Bulk Considerations

Bulk defects are those associated with the starting silicon materials and most commonly result from crystal imperfections introduced during the wafer processing. The types of defects associated with the bulk material include: dislocations, resistivity gradients, impurity diffusions, etch pits and precipitations.

Steep concentration gradients in the epitaxial layer introduce strains in the crystal lattice which are subsequently released by the formation of a dislocation fault plane which forms perpendicular to the concentration gradient and results in structural weaknesses in the chip. Bulk defects at these fault planes are often manifested by exposure to mechanical stresses.

Impurity diffusions, caused by variations in the epitaxial growth, introduce crystal lattice orientation fault planes which result in a reduced reverse breakdown voltage for epitaxial structures.

Lattice defects resulting from dislocations, concentration gradients, or diffusion defects can increase localized current density, causing "hot spot" formation, diffusion spikes, junction breakdown, and deviations in electrical characteristics.

Surface Considerations

Surface defects include contamination, foreign material, inversion layers, and mechanically induced surface damage.

Certain types of residue, when activated by moisture and temperature, can result in physical deformation of the circuit topography. Ionic contamination can create surface charges which result in charges of the opposite polarity in the underlying silicon. Surface contamination may result in either

physical damage, alteration of the electrical characteristics, or a combination of both. Although foreign particles such as loose conductive particles within the package are not defects directly related to the surface, they may cause failures when they interact with the die surface. Foreign material such as loose conductive particles are particularly of concern in devices which do not utilize a protective glass layer. The presence of such material can result in intermittent operation, electrical shorts, increased leakage currents, or reduced breakdown voltages.

Oxide Considerations

Oxide defects are those associated with the silicon dioxide or the surface passivation layer. Defects in this classification include oxide pinholes, oxide shorts, oxide faults and surface passivation defects.

The oxides are employed to provide insulation between the interconnect metallization and silicon circuit elements and also to serve as diffusion masks. Surface passivation provides protection from ambient gases and other surface contaminants. Defects associated with these constitutents may be classified as either structural or contaminative.

The most common structural oxide defect is the oxide pinhole. The pinholes most commonly originate during the fabrication processes. Pinhole-related failures generally occur as a short between the interconnect metallization and an underlying circuit element.

Oxide faults are also associated with fabrication process control anomalies. Faults such as nonuniform thickness or incomplete isolation result from poor process control; e.g., mask misalignments and incorrect etching procedures. These faults are susceptible to oxide breakdown and shorts when subjected to electrical stresses.

Diffusion Considerations

Diffusion defects are those associated with the device diffusions which are used to implement device junctions and isolation regions. Common diffusion defects include incomplete diffusions, diffusion spikes or piped junctions, and mask misalignment. These types of defects are most commonly incurred during the fabrication processes.

Metallization Considerations

The defect mechanisms associated with the metallization process are mechanical-, chemical- or design-related. Common metallization defects include corrosion/contamination, electromigration, microcracks, overalloying and smears/scratches.

Contamination under the metallization can be introduced by improper cleaning of the die prior to the deposition of the metal, improper vacuum during deposition, and by humidity or contaminants in the package atmosphere.

The electromigration phenomena is activated by high current densities in the metallization paths; e.g., greater than 2×10^5 A/cm^2 for aluminum. Process anomalies which introduce regions of reduced cross-sectional area can result in high current densities. The high current densities cause the metallization material to migrate and eventually can result in voids and discontinuities in metallization.

Microcracks or other types of open metallization conditions result from nonuniform deposition, improper coverage at oxide steps due to improper contouring of the step, and mask faults. While the majority of the microcrack problems are a result of process anomalies, it is also possible to create metallization discontinuities by mechanically stressing the chip, thus producing cracks and fissures.

Overalloying causes the metal in the contact region to migrate through the semiconductor junction, resulting in the short circuit of the junction. On the other hand, insufficient alloying produces intermittent contacts in the junction regions.

Wirebond Considerations

Defects in this category include all defects related to the electrical integrity of the bond and associated interconnect wire. Among the more common defects in this category are the separation of the wirebond from the bond pad, broken wirebond, broken interconnect wire, smeared or overbonded wirebond, misplaced bonds, and intermetallic compound formation.

The separation or the lifting of a wirebond from the bonding pad can be caused by insufficient temperature and/or pressure during bonding, improper metals or metal preparation, the presence of contamination, or oxidation of the bond pad prior to bonding.

Broken bonds and interconnect wires result from mechanical overstress and/or poor lead dress conditions.

Smearing, overbonding, and misplaced bonds result from poor process control. In many cases overbonding will also result in cracked or chipped dice.

Intermetallic compound formation can result from the interaction of two metals in a bond situation, such as gold-aluminum bonds. In this reaction the gold atoms diffuse faster than the aluminum atoms, producing voids which result in high-resistance contacts or weakened lifted bonds. Reliable bonds of this type

can be realized by minimizing both the total mass of aluminum available for diffusion and the cumulative time-temperature product experienced by the device during manufacturing and use.

Package Considerations

Defects attributable to the device package are related to its mechanical shock protection and environment isolation functions. Defects in this category include hermeticity, lead defects, external contaminations, and external cosmetic defects.

The dominant defect in this category is nonhermetic seals. In hermetic packages such as ceramic DIP packages, the lead frame is embedded in the sealing material sandwiched between the top and bottom of the package. Mechanically stressing the leads, therefore, will also mechanically stress the seal material and could, by introducing fractures in the seal material, result in the loss of hermeticity. This applies to any package where the lead egress is through some type of seal material.

Hermeticity problems may also be introduced by subjecting the devices to variations in ambient temperature. Temperature variations, especially in a cyclic manner, tend to aggravate any mismatch in the thermal expansion coefficients of the seal and lead material. This mismatch can initiate cracks or voids which would result in a loss of hermeticity.

External lead defects such as plating defects or broken leads may result from mechanical stressing or exposure to some type of hostile environment.

This is certainly not an exhaustive listing of all the device defects and structural design factors which can influence the reliability of a microcircuit. Some of these failures will occur only in infrequent, isolated cases. However, the above discussion represents the majority of the defects reported in the literature as the causes of microcircuit failure. The next section will discuss the malfunction experiences associated with these device defects and structural design factors.

Section 2

MICROCIRCUIT MALFUNCTION EXPERIENCES

To facilitate the data analysis in this study the malfunction experiences have been divided into two categories: die-related and package-related malfunctions. The die-related malfunction category is comprised of all anomalies associated with some portion of the device chip. These faults are considered to be technology-related defects; i.e., TTL, MOS, LINEAR. The package-related malfunction category consists of all defects related to the device package, lead frame, interconnect wires, wirebonds, and die bond.

Theoretically, the probability of occurrence of package-related malfunctions for any given package configuration is equal for all technologies. However, the package configuration may influence the relative occurrences of die-related malfunctions in certain technology families. Initially, in this study, the analysis will be presented considering these malfunction categories to be independent; subsequently, the appropriate factors will be developed to reflect the interactions.

Die-Related Malfunctions

The normalized distributions of die-related malfunctions experienced for digital technologies are presented in Tables 1-4. The information summarized in these tables was extracted from failure analysis reports performed at competent failure analysis facilities. The raw data were scrutinized to eliminate any lot- or manufacturer-dependent problems. The data presented represent a substantial cross section of both device functions and device manufacturers within each technology.

Tables 1-4 reflect the failure mode distributions as well as the dominant failure modes within each technology. In several technology families the availability of LSI device malfunction experiences allows for the determination of the device complexity impact on the failure mode distributions.

In the standard TTL family, increasing device complexity apparently shifts the failure mode distribution to overwhelming dominance by metallization and oxide defects. The distribution shift can readily be explained by considering the physical attributes of the LSI devices. Most of these complex devices incorporate narrow, closely-spaced, multi-level metallization systems which would increase the probability of experiencing metallization and oxide defects.

TABLE 1: NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS (PART ONE)

FAILURE MODE	TTL SSI/MSI %	TTL LSI %	STTL SSI/MSI %	STTL LSI %
SURFACE DEFECTS	(19.04)	(15.18)	(57.78)	(33.33)
Contamination/Leakage	12.60	11.39	31.11	19.35
Foreign Material/Particles	3.08	1.26	---	1.08
Inversion/Channeling	3.36	2.53	26.67	12.90
BULK DEFECTS	(8.40)	(1.26)	(2.22)	(1.08)
Crystal Imperfections	1.68	---	---	---
Cracked Die	6.72	1.26	2.22	1.08
OXIDE DEFECTS	(13.44)	(25.32)	(13.35)	(10.75)
Oxide Pinholes	3.92	15.19	4.44	---
Oxide Fault	6.16	3.80	---	---
Oxide Short/Breakdown	2.52	6.33	8.91	6.45
Passivation Defects	0.84	---	---	4.30
DIFFUSION DEFECTS	(9.52)	(3.79)	(6.66)	(9.67)
Diffusion Anomalies	3.92	---	---	1.08
Diffusion Spike	1.40	1.26	4.44	5.37
Isolation Defects	0.28	---	---	---
Mask Faults	3.92	2.53	2.22	3.22
METALLIZATION DEFECTS	(49.60)	(54.45)	(19.99)	(45.17)
Open				
At Oxide Step	0.56	6.33	---	1.08
At Contact Window	24.37	2.53	2.22	1.08
Not Specified	7.03	5.06	2.22	3.22
Short				
Inter-layer	4.20	11.39	2.22	3.22
Not Specified	10.36	22.81	13.33	34.41
Pitted/Corroded	1.40	3.80	---	1.08
Smeared/Scratched	1.40	2.53	---	1.08
Electromigration	0.28	---	---	---
Malfunction Reports	357	79	45	93

*Total distribution for the major defect categories.

TABLE 2: NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS (PART TWO)

FAILURE MODE	LTTL SSI/MSI %	HTTL SSI/MSI %	LSTTL SSI/MSI %	ECL SSI/MSI %
SURFACE DEFECTS	(40.12)	(14.16)	(35.13)	(15.09)
Contamination/Leakage	17.90	13.33	21.62	14.15
Foreign Material/Particles	10.49	0.83	---	---
Inversion/Channeling	11.73	---	13.51	0.94
BULK DEFECTS	(1.23)	(3.33)	(2.70)	(0.95)
Crystal Imperfections	1.23	2.50	---	0.24
Cracked Die	---	0.83	2.70	0.71
OXIDE DEFECTS	(15.46)	(54.17)	(16.21)	(44.56)
Oxide Pinholes	3.70	5.00	5.40	6.84
Oxide Fault	3.70	33.33	2.70	29.95
Oxide Short/Breakdown	0.62	11.67	8.11	1.18
Passivation Defects	7.44	4.17	---	6.59
DIFFUSION DEFECTS	(14.81)	(6.67)	(16.21)	(10.14)
Diffusion Anomalies	6.79	0.83	---	0.24
Diffusion Spike	1.23	1.67	10.81	0.47
Isolation Defects	---	---	---	---
Mask Faults	6.79	4.17	5.40	9.43
METALLIZATION DEFECTS	(28.38)	(21.67)	(29.75)	(29.26)
Open				
At Oxide Step	1.23	---	2.70	---
At Contact Window	14.81	3.33	---	---
Not Specified	4.32	3.33	16.24	3.54
Short				
Inter-layer	1.23	4.17	---	3.77
Not Specified	4.94	8.33	10.81	7.08
Pitted/Corroded	1.23	0.83	---	5.90
Smeared/Scratched	0.62	1.68	---	1.89
Electromigration	---	---	---	7.08
Malfunction Reports	162	120	37	424

*Total distribution for the major defect categories.

TABLE 3: NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS (PART THREE)

FAILURE MODE	CMOS SSI/MSI %	CMOS LSI %	PMOS SSI/MSI %	PMOS LSI %
SURFACE DEFECTS	(40.01)	(35.55)	(37.03)	(51.54)
Contamination/Leakage	34.71	31.11	26.85	46.15
Foreign Material/Particles	1.18	---	6.48	3.85
Inversion/Channeling	4.12	4.44	3.70	1.54
BULK DEFECTS	(7.64)	(---)	(0.93)	(0.77)
Crystal Imperfections	5.88	---	---	---
Cracked Die	1.76	---	0.93	0.77
OXIDE DEFECTS	(37.64)	(40.03)	(16.67)	(23.05)
Oxide Pinholes	8.23	13.37	4.63	13.82
Oxide Fault	1.76	6.66	0.93	0.77
Oxide Short/Breakdown	27.06	20.00	10.18	8.46
Passivation Defects	0.59	---	0.93	---
DIFFUSION DEFECTS	(8.24)	(11.10)	(15.74)	(8.47)
Diffusion Anomalies	2.35	4.44	8.33	2.31
Diffusion Spike	0.59	---	3.70	---
Isolation Defects	---	2.22	0.93	1.54
Mask Faults	5.30	4.44	2.78	4.62
METALLIZATION DEFECTS	(6.47)	(13.32)	(29.63)	(16.17)
Open				
At Oxide Step	1.18	---	4.63	1.54
At Contact Window	---	---	4.63	3.85
Not Specified	2.35	6.66	7.41	0.77
Short				
Inter-layer	---	2.22	0.93	3.08
Not Specified	0.59	4.44	5.55	2.31
Pitted/Corroded	---	---	2.78	4.62
Smeared/Scratched	2.35	---	3.70	---
Electromigration	---	---	---	---
Malfunction Reports	170	45	108	130

*Total distribution for the major defect categories.

TABLE 4: NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS (PART FOUR)

FAILURE MODE	NMOS	LINEAR	
	LSI %	OP AMPS %	GENERAL %
SURFACE DEFECTS	(57.42)	(62.70)	(17.54)
Contamination/Leakage	50.52	57.14	8.77
Foreign Material/Particles	4.31	1.19	5.26
Inversion/Channeling	2.59	4.37	3.51
BULK DEFECTS	(3.45)	(5.16)	(9.65)
Crystal Imperfections	---	0.79	3.51
Cracked Die	3.45	4.37	6.14
OXIDE DEFECTS	(24.49)	(11.90)	(10.52)
Oxide Pinholes	5.18	2.38	---
Oxide Fault	6.90	4.37	8.77
Oxide Short/Breakdown	11.55	1.98	1.75
Passivation Defects	0.86	3.17	---
DIFFUSION DEFECTS	(6.03)	(5.15)	(28.95)
Diffusion Anomalies	1.72	2.38	13.16
Diffusion Spike	---	0.79	11.40
Isolation Defects	1.72	---	---
Mask Faults	2.59	1.98	4.39
METALLIZATION DEFECTS	(8.61)	(15.09)	(33.34)
Open			
At Oxide Step	1.72	0.40	0.88
At Contact Window	---	2.38	3.51
Not Specified	1.72	1.59	10.52
Short			
Inter-layer	2.59	1.59	---
Not Specified	0.86	4.76	14.04
Pitted/Corroded	0.86	2.78	4.39
Smeared/Scratched	0.86	1.59	---
Electromigration	---	---	---
Malfunction Reports	116	252	114

*Total distribution for the major defect categories.

In the MOS technology families, the increasing complexity produces a failure distribution shift to a dominance by surface and oxide defects. This shift can be attributed to the increasing component density, resulting in increased susceptibility to these types of defects.

A high percentage of the malfunctions experienced in linear devices can be attributed to contamination. This high percentage can be explained by the sensitivity of critical electrical parameters to the effects of contamination. Ionic contamination and surface inversion or channeling caused by contamination may result in increased collector-to-base leakage current, shifts in the small signal current gain, and shifts in the junction breakdown voltages.

Package-Related Malfunctions

The normalized distributions of experienced package-related malfunctions for various package configurations are presented in Tables 5 and 6. As with the die-related malfunctions, the package-related malfunction information was extracted from failure analysis reports performed at competent failure analysis facilities. Again, all lot- and manufacturer-dependent problems have been eliminated.

Combining the malfunctions for a given technology with the package malfunctions presented in this section allows for the determination of a screening program which will be effective in eliminating the majority of the malfunctions experienced for any package-technology combination.

When considering differences in construction between plastic encapsulated and hermetic cavity packages, it appears obvious that different reliability characteristics will be exhibited. In plastic encapsulated devices, the lead frame and interconnect wires are embedded in the encapsulant material. It is this property which is responsible for most of the reliability characteristics of the plastic package. Since the interconnect wires and die are rigidly constrained, the encapsulated devices are much less susceptible to mechanical stresses than their hermetically packaged counterparts.

The lack of a true hermetic seal is one of the most important differences between plastic and hermetic packages with respect to reliability. All plastics are permeable to water, which can introduce contaminants into the package. Water can also be introduced into the package during temperature cycling of the encapsulated packages. Due to the mismatch of expansion coefficients of the materials, moisture can enter the package at the plastic-to-lead frame interface and travel toward the chip along the leads and bonding wires.

TABLE 5: NORMALIZED DISTRIBUTIONS OF EXPERIENCED PACKAGE-RELATED MALFUNCTIONS FOR ALL PACKAGE TYPES (PART ONE)

	DUAL-IN-LINE PACKAGES					
	UP TO 16 PINS			GREATER THAN 16 PINS		
FAILURE MODE	PLASTIC %	CERAMIC %	CER/MET %	PLASTIC %	CERAMIC %	CER/MET %
BOND DEFECTS	(67.21)	(20.45)	(50.01)	(76.92)	(9.72)	(49.29)
Broken Wirebond	24.59	6.82	11.76	19.23	1.77	25.00
Lifted Wirebond	26.23	3.03	20.59	30.77	2.65	4.29
Over-bonded	8.20	2.27	---	7.69	---	---
Misplaced Bond	---	2.27	---	---	---	1.43
Multiple Bond	---	---	---	15.38	---	0.71
Intermetallic Formation	4.92	3.03	---	---	0.88	---
Die-Attach Defect	3.27	3.03	17.66	3.85	4.42	17.86
INTERCONNECT DEFECTS	(31.15)	(11.37)	(11.76)	(23.08)	(4.44)	(3.57)
Broken Wire	13.11	0.76	2.94	11.54	0.88	3.57
Shorted Wire	9.84	3.03	2.94	---	---	---
Poor Lead Dress	1.64	6.82	5.88	---	3.56	---
Corroded Wire	6.56	0.76	---	11.54	---	---
PACKAGE DEFECTS	(1.64)	(68.18)	(38.23)	(---)	(85.84)	(47.14)
Nonhermetic Seal	---	61.36	29.41	---	83.19	36.43
Excessive Seal Material	---	1.52	2.94	---	0.88	0.71
External Lead Defect	1.64	5.30	5.88	---	1.77	10.00
Malfunction Reports	61	132	34	26	133	140

*Total distribution for the major defect categories.

TABLE 6: NORMALIZED DISTRIBUTIONS OF EXPERIENCED PACKAGE-RELATED MALFUNCTIONS FOR ALL PACKAGE TYPES (PART TWO)

	FLAT PACKS		CANS
FAILURE MODE	CERAMIC %	MET/GLASS %	METAL %
BOND DEFECTS	(18.85)	(60.00)	(56.34)
Broken Wirebond	7.25	6.15	14.08
Lifted Wirebond	2.90	4.62	16.90
Over-bonded	1.45	9.23	2.82
Misplaced Bond	---	6.15	2.82
Multiple Bond	1.45	---	1.41
Intermetallic Formation	---	---	1.41
Die-Attach Defect	5.80	33.85	16.90
INTERCONNECT DEFECTS	(4.35)	(9.23)	(9.86)
Broken Wire	4.35	6.15	7.04
Shorted Wire	---	---	---
Poor Lead Dress	---	3.08	---
Corroded Wire	---	---	2.82
PACKAGE DEFECTS	(76.80)	(30.77)	(33.80)
Nonhermetic Seal	50.72	23.08	28.17
Excessive Seal Material	13.04	---	---
External Lead Defect	13.04	7.69	5.63
Malfunction Reports	69	65	71

*Total distribution for the major defect categories.

These differences in thermal expansion can also cause relative motion among the encapsulant, wires and chip, which strains the interconnect wires and the wirebonds.

Hermetic seal defects are not applicable to plastic packages since all plastics are permeable to water. As expected, the overwhelming majority of package-related malfunctions experienced in plastic packages are associated with interconnect and wire-bond integrity.

The incidence of some die-related malfunctions is a function of the reliability aspects of the package construction. The frequency of contamination and surface-related defects is much greater for plastic packages than for hermetic packages. By the same token, the frequency of stray particles and defective die-attach bonds is less for plastic packages as compared to hermetic packages. Hermetic packages are more sensitive to mechanical shock environments than their plastic counterparts.

The values presented in Tables 1 through 6 are not intended to indicate the relative occurrences of failures among the technologies or package types, but rather the distributions of experienced failure modes within any technology or package configuration.

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Section 3

SCREENING TECHNIQUES FOR TECHNOLOGY-RELATED MALFUNCTIONS

In order to provide effective screening and testing techniques for integrated circuits, it is necessary to investigate the basic mechanisms associated with each of the experienced failure modes, as well as the types of stresses which will be most effective in accelerating those mechanisms. Certain types of failure mechanisms can be avoided by complying with proper design and fabrication procedures. However, a number of defects will escape even the most rigorous vendor quality-control program. These defects necessitate the implementation of screening procedures to assure that devices incorporated into systems and equipments are virtually defect free. This section is devoted to the device technology and the screening and test techniques which are effective in accelerating the associated mechanisms. The screens and tests recommended for various die-related failure modes are presented in Table 7.

Surface Defects

Contamination is the basic mechanism associated with several surface defect failure modes. The contaminants may be present from the residue of materials used during the fabrication and trapped in the package at final seal, or they might be introduced due to a package seal failure.

In many cases, the presence of surface contamination does not result in any detrimental effect until a combination of heat and bias causes migration of ions toward a critical area. Contaminants in critical areas can cause threshold shifts, excessive leakage currents, and erroneous circuit operation. A high-temperature storage condition actually tends to disperse the contaminants evenly on the surface. This process might cause contaminants to migrate from a harmless region to a more critical region or, conversely, in the other direction, which could improve device performance. While the prediction of the effects of high-temperature storage is difficult, it can be useful as a means of identifying the presence of contaminants.

Contamination, along with other anomalies, may also be introduced by particles or foreign materials. Although device manufacturing facilities employ clean room environments to minimize the occurrence of particles, certain types of particles can be introduced during the device fabrication. These particles, which are often electrically conductive, are generated by the materials used in the device fabrication. Fragments of a gold or aluminum bonding wire, die attach material, solder, or even silicon particles can cause catastrophic

TABLE 7: RECOMMENDED SCREENS/TESTS FOR VARIOUS DIE-RELATED FAILURE MODES

Constituent Failure Mode	Stabilization Bake	Temp Cycle/ Thermal Shock	Const Accel/ Mech Shock	Reverse Bias and Temp	Dynamic Op and Temp	X-ray
Surface Contamination/ Leakage	●			●	●	
Foreign Material/Particles			●			●
Inversion/Channeling	●			●		
Crystal Imperfections	●	●			●	
Cracked Die		●	●		●	
Oxide Pinholes		●		●	●	
Oxide Faults		●			●	
Oxide Short/Breakdown		●		●	●	
Passivation Defects		●			●	
Diffusion Anomaly				●	●	
Diffusion Spikes				●	●	
Mask Faults					●	
Open Metallization (excluding corrosion)		●		●	●	
Metallization Shorts		●		●	●	
Electromigration					●	

failure or intermittent operation in cavity type packages. Initially, at the internal visual inspection prior to final seal, the device may appear to be void of any particles or foreign material. However, after exposure to mechanical stress environments, particles may result from the fragmenting of materials at structural imperfections. Such particles are particularly of concern in more complex devices where component spacing is minimal.

Many devices employ a glassivation layer as protection against bridging-type shorts which can be caused by conductive particles. Electrical measurements are extremely limited in facilitating the detection of stray particles since the electrical parameters will only be affected when the particles are located in such a way as to cause electrical shorts. Radiographic inspection is an effective method for detecting particles but it should be performed after all mechanical stress testing has been completed.

The accumulation of surface ionic contamination often results in inversion or channeling conditions. Biasing a junction in the reverse direction causes an inversion layer to form near the surface of the oxide. As with other types of contamination, subjecting devices to a high temperature (200°C to 300°C) bake for intervals of a few hours causes dispersion of the ions to harmless locations. This phenomenon also makes the stabilization bake a useful tool in the failure analysis procedures. Also, an elevated temperature combined with a biased condition results in a "preferential drift" of the mobile ions into critical areas. Therefore, high-temperature life testing with bias applied is an effective method for detecting inversion or channeling conditions.

Bulk Defects

Crystal lattice defects are created during the crystal growing process and the wafer processing steps, such as epitaxial growth, diffusion, oxidation, and alloying. Crystal imperfections can result in excessive leakage, reduced breakdown voltage, or fractured and chipped dice.

Crystal defects such as impurity diffusion, precipitations, and steep concentration gradients can result in strains in the crystal lattice. These lattice strains are subsequently released by the formation of dislocation structures, which results in structural weaknesses. Bulk failures often occur when these weaknesses are mechanically or thermally stressed.

Bulk failures such as crystal imperfections and cracks in the die do not necessarily result in infant mortality failures. Cracks through active elements can degrade device performance but do not necessarily cause a catastrophic failure.

Dislocations in the crystal lattice which introduce structural weaknesses or cracks in the chip can be detected by thermal stresses such as thermal shock and temperature cycling, or by mechanical stresses such as constant acceleration and vibration fatigue.

Oxide Defects

Oxide defects are most commonly detected as electrical shorts or increased leakage currents. Oxide layers between conductors or between a conductor and an active region are subjected to electrical stresses during operation. The thickness of the oxide layers is designed to be sufficient to withstand the anticipated electrical potentials experienced during normal operation. However, defects present in the oxide could reduce the dielectric strength to the point where breakdown could occur during normal operation. Oxide breakdown, which is a time-temperature-dependent process, is often accompanied by the migration of the metallization through the defect site to the underlying conductor or active region, producing an electrical short.

The oxide breakdown process can be accelerated by the application of either electrical or thermomechanical stresses. Temperature cycling is useful in inducing mechanical stresses in the oxide. Life tests, such as high-temperature reverse bias or dynamic operation at elevated temperatures, are effective in electrically stressing oxide imperfections.

Diffusion Defects

The physical dimensions, as well as the positions of the diffusions, are critical in the determination of the device electrical characteristics. The diffusion depth, width, length, and doping profile are all important characteristics. Variations in any of these attributes will alter the characteristics of a junction region. Diffusion defects are commonly introduced by crystal imperfections or masking faults.

Crystal defects in the bulk material can hinder the diffusion processes, leading to diffusion anomalies or spikes. Other faults, including discontinuous isolation diffusions and irregular diffusion shapes and edges, can result from dust particles on the masks.

Initial electrical measurements will easily detect conspicuous diffusion faults such as missing or misplaced diffusions. The detection of degraded or marginal diffusion problems is more subtle. Electrical stresses induced during operation at elevated temperatures are effective in eliminating marginal diffusion problems.

Metallization Defects

The metallization pattern on a device electrically connects the various elements, and also provides for the functional inputs and outputs of the circuit. Metallization defects can be grossly categorized as either open or short conditions. Metallization defects can be attributed to mechanical, electrical or chemical phenomena.

Mechanical metallization defects are induced during the device fabrication. Mechanically induced defects, such as scratches, can range from the complete severing of the stripe or reduced metallization cross sections, to smearing of the metal to adjacent conductors, forming a short circuit. A thorough pre-seal internal visual inspection is an effective method for detecting and rejecting devices exhibiting severe cases of these types of faults.

The metallization etching process is also responsible for the creation of defects. Insufficient etching can result in extraneous metal which could cause metallization shorts. Over etching results in opens or reduced cross-sectional area runs which could melt open or experience electromigration under the current densities experienced during operation. An internal visual inspection is effective in eliminating the obvious etching defects. The more subtle defects, such as reduced cross-sectional area, can be often detected by a dynamic life test at high temperature, or by temperature cycling.

Metal coverage at oxide steps is a major concern in the integrity of metallization systems. Insufficient coverage and microcracks are frequently responsible for open metallization at oxide steps. The thin metal in the step region is mechanically stressed by the thermal mismatches, causing the cracks and intermittent operation. Temperature cycling and dynamic operation at elevated temperatures are commonly employed to detect these faults.

Open conditions have also been attributed to increased resistance of metal to silicon contacts. Contacts which are initially inadequate can be detected by initial electrical measurements. Contacts which become degraded can be restored by realloying the devices at high temperatures for short durations. These degraded contacts can be detected by dynamic life tests at elevated temperatures and by temperature cycling procedures.

Lifted metallization, usually bonding pads, results from poor adhesion to the oxide layer. The metallization will not adhere properly to oxide which is contaminated. This type of defect is detected in internal visual inspections. Lifted bond pads are subjected to the mechanical stress sequences designed for the interconnect wires and bonds. The thin-film metallizations will not withstand these stresses and will typically be

separated from the principal metallization system.

Interlevel-metallization shorts are particularly of concern in high-complexity devices which employ multi-level metallization systems. These conductors are typically separated by thin oxide layers. A breakdown of this oxide layer, as discussed in the oxide defect section, can cause a short between the two levels of metallization. Temperature cycling and dynamic life tests at elevated temperatures are again employed as detection methods.

Electromigration is the physical transport of the conductor material by ion migration resulting from the passage of a direct current. It occurs when electrons or holes flowing in a material exert sufficient force on the stationary atoms of the conductor, in a momentum exchange, to cause the atoms to move. The ion rate of movement is exponential and is proportional to the cross-sectional area of the conductor and the square of the current density. Circuit failures occur where the cross section of the metallization is the smallest or the current density is the largest. Electromigration results in open metallization conditions or degraded junction characteristics. Electromigration is accelerated by high current densities. High-temperature dynamic life tests are useful in accelerating the transport mechanisms. However, the time required to manifest electromigration failures, even at high temperatures, makes it impractical to screen for these defects. Long-term life tests on a device population sample are useful in identifying potential electromigration problems.

Section 4

SCREENING TECHNIQUES FOR PACKAGE-RELATED MALFUNCTIONS

Integrated circuit packages are responsible for providing both protection from hostile environments and electrical connections for the device die. In order to assure long life for the device, it is necessary to investigate the reliability aspects of the integrated circuit packages and develop screening techniques which are directed toward the elimination of package-related malfunctions. This section is devoted to the analysis of the failure modes experienced with each package type and to the screening and test techniques applied. The screens and tests for various package-related failure modes are presented in Table 8.

Wirebond Defects

Every integrated circuit employs some type of interconnect system from the die to the external leads. These interconnect systems are usually comprised of a series of wires bonded at both the die pads and the package lead posts. The integrity of these bonds is essential to the operation of the device. Any degradation of the conductive properties of the bonds could cause a device malfunction.

Wirebond defects can be introduced either during the device fabrication or during the operation of the device. Overbonding, or smeared bonds, results from excessive bonding pressure during the bonding process. These types of defects can result in several kinds of anomalies. The smeared metal may result in shorts if smeared to adjacent metallization. The excessive pressure could result in damage to the underlying substrate. In all cases overbonding produces a mechanically weak bond. This weakness can be attributed to the reduced cross sections of the foot and heel of the ultrasonic bonds and the increased diameter of the thermocompression bonds. Bond weakness can be detected by applications of mechanical stresses.

In encapsulated packages, where the interconnect wires are embedded in the package material, temperature cycling produces mechanical stresses due to the difference in thermal expansion coefficients of the materials involved. The difference in the expansion coefficient between the plastic and wire introduces tension forces on the wire which can stretch the thin bond heel until it breaks.

In packages with internal cavities, where a gaseous atmosphere surrounds the die, wires, and bonds, the wires are free to move within the package cavity. Subjecting these devices to temperature cycling can introduce "wireflex" failures.

TABLE 8: RECOMMENDED SCREENS/TESTS FOR VARIOUS PACKAGE-RELATED FAILURE MODES

Constituent Failure Mode	Stabilization Bake	Temp Cycle/ Thermal Shock	Const Accel/ Mech Shock	Seal Test	Reverse Bias and Temp	Dynamic Op and Temp	X-ray	External Visual
Broken Wirebond		●			●	●		
Lifted Wirebond		●			●	●		
Overbonded		●				●		
Misplaced Bond					●	●		
Multiple Bond			●					
Intermetallic Formation	●	●				●		
Die-Attach Defect		●	●			●	●	
Broken Wire		●			●	●		
Shorted Wire					●	●		
Poor Lead Dress		●	●					
Corroded Wire		●			●	●		
Nonhermetic Seal		●	●	●				
Excessive Seal Material								●
External Lead Defect								●

As the device changes temperature, the wires respond by expanding or contracting. Changes in the wire length cause variance in the angle at which the wire contacts the bond. Eventually, the heel of the bond will become "work hardened," brittle and fractured. Generally, the fracture occurs at the thinnest region of the heel of the bond. Wireflex failures occur primarily with aluminum wires. Gold wires are generally more ductile and resist "work hardening." The susceptibility to wireflex failures is also related to the physical dimensions of the wire loop. A tight wire condition would represent the worst case while large loops would tend to expand along the loop and create very little flexing.

Underbonding introduces lifted wirebond conditions which often result in intermittent operation. The lifted wirebond condition is aggravated by the compression and tension of the interconnect wire during temperature cycling. Enough residual spring is usually present in the wire to displace the bond from the pad or post with minimal exposure to mechanical stresses. Temperature cycling is commonly employed to eliminate lifted wirebonds in most package configurations.

The bonding of any dissimilar metals which have electrochemical differences can result in electrolytic action, a phase change, or chemical reactions. In the common gold-aluminum bond system, a chemical phase change occurs in a ternary gold-aluminum-silicon system at temperatures above $300^{\circ}C$. The silicon tends to catalyze the formation of Al-Au compounds. Even though the intermetallic formation material is hard and brittle, it is a good conductor and will not affect bond integrity unless fractured. Subjecting these bonds to repeated thermal cycling causes microcracks in the intermetallic formation. These microcracks can develop into Kirkendall voids, resulting in intermittent operation or hard opens. High-temperature storage conditions which accelerate the formation of intermetallics, followed by temperature cycling, are an effective method for producing fractures in the formation. Such fractures can be detected by electrical measurements.

Die-attach defects are not necessarily limited to the catastrophic separation of the die from the package structure. Certain anomalies, such as voids, in the die-attach material can introduce subtle problems. Voids in the attach material cause an increase in the junction-to-case thermal resistance which can result in increased junction temperatures and localized heating. These voids are most commonly detected by X-ray examination. The application of mechanical stresses or temperature cycling to a defective die bond could result in the separation of the die from the package. If this condition occurs, the die is then supported solely by the interconnect wires.

Interconnect Defects

Interconnect defects include all anomalies associated with the interconnect wires. Open wires frequently occur due to damage experienced during bonding. The necking down or nicking of lead wires often result in latent failures which are manifested by various mechanical stresses. The necking down and nicks also reduce the cross section of the wire, which can cause localized heating or aluminum migration.

Temperature cycling of encapsulated devices, where the wires are embedded in the package material, subjects the wires to high stresses due to the difference in the thermal expansion coefficients of the wires and the encapsulant material, causing excessive grain growth to occur across the wire. Eventually the wire would fracture along the grain boundary.

Poor lead dress is sometimes responsible for interconnection shorts. Tight wires can inadvertently come into contact with the edge of the die, producing a short. Loops with excessive wire length can sag or droop, forming shorts with other wires.

Generally, interconnect defects can be detected by electrical measurements. For encapsulated devices, temperature cycling should be used to elicit interconnect defects. In the case of cavity packages, monitored vibration is useful in accelerating the mechanisms associated with interconnect defects.

Package Defects

It is meaningless to discuss the hermeticity of plastic encapsulated packages because all plastics are susceptible to moisture penetration. However, the integrity of the seal of the hermetic package is critical since it protects the internal components from hostile environments. Seal defects in hermetic packages provide an effective vehicle by which moisture and contaminants can penetrate the package. Seal leaks may result from process anomalies or from the aggravation of thermal expansion coefficient mismatches. Hermeticity failures can be easily detected in fine and gross leak tests which should be performed after thermal and mechanical screen sequences.

The balance of the package-related defects, such as excessive sealant or external lead defects, should be detected by screens such as external visual, or by final electrical measurements.

Section 5

SCREENING PROGRAM EVALUATION

Since no individual screening techniques are effective against all the possible failure modes which can be experienced in a given package-technology combination, a comprehensive screening sequence must be developed for each specific case under consideration. In such a program each of the screens should be selected to complement the other screens. While the highest screening efficiency would be realized in a sequence comprised of all possible screens, this sequence is seldom feasible economically. It is the cost-effectiveness criterion which compels us to evaluate the merit of each of the individual screens for various situations.

As a preliminary step in examining the value of each of the individual screens it would be beneficial to distinguish between activator and detector screens/tests. Screens or tests which, through applied stresses, convert latent defects into actual anomalies are classified as activators. Detectors are those screens or tests which actually identify failures, usually employing some type of measurement or visual criteria. Screens or tests which fall into the detector category include: hermeticity tests, electrical measurements, radiographic and visual examinations.

Screening sequences are often arranged in groups of consecutive activators with detectors inserted in the appropriate positions to identify the rejects from the various activator groups. It is the characteristic inability of activators to segregate anomalous devices which introduces difficulty in the direct assessment of individual screen efficiencies.

To determine screening program efficiency, the approach of this study will be to combine the evaluation of actual screening experiences with the theoretical analysis provided by the physics-of-failure approach to screening.

The analysis of actual screening experiences is fundamental to forming a basis for determining screening efficiencies. Only data obtained from device users and independent test facilities were considered in this study. This was done to eliminate any data which might be biased in nature. To ensure that the information generated in this study is representative of current vintage devices, only data on devices of 1975 or later vintage were considered.

It should be realized from the onset that actual experienced reject rates for any given technology-package combination in a

given screening sequence will be both lot- and manufacturer-dependent. The average fallouts, as well as the distributions of those fallouts, will give an indication of the magnitudes of reject rates which can be anticipated for the various technologies, complexities, and package combinations. The average reject rates for a screening sequence consisting of initial inspection, environmental screen, burn-in, and final inspection are summarized for each technology and complexity group in Table 9. The median reject rate value is also given for each entry to indicate the distribution of the reject rates for each category. The actual distributions for each group are graphically illustrated in Appendix A.

The average reject rate values presented in Table 9 represent the total observed reject rates, a combination of package- and die-related defects, for each group. To determine the contributions of package- and die-related defects to the total reject rates experienced, it is necessary to analyze the failure mode distributions. The analysis was performed on standard TTL, SSI/MSI devices since the largest quantity of data was available in this category.

The results of this analysis, which reveals the failure mode distributions of TTL and SSI/MSI devices in both plastic and hermetic packages, are presented in Figure 1. These pie charts do not necessarily reflect the frequency of occurrence of various modes in hermetic and plastic packaged devices, but rather the distribution of failure modes experienced within each package type. The distributions presented in this figure indicate that the failure mode contribution attributable to package defects was 47% for plastic encapsulated devices and 35% for devices in hermetic packages. Using these values, and the detailed screening results obtained in the TTL SSI/MSI category, it is possible to develop a package-related and die- or technology-related reject rate for each technology category.

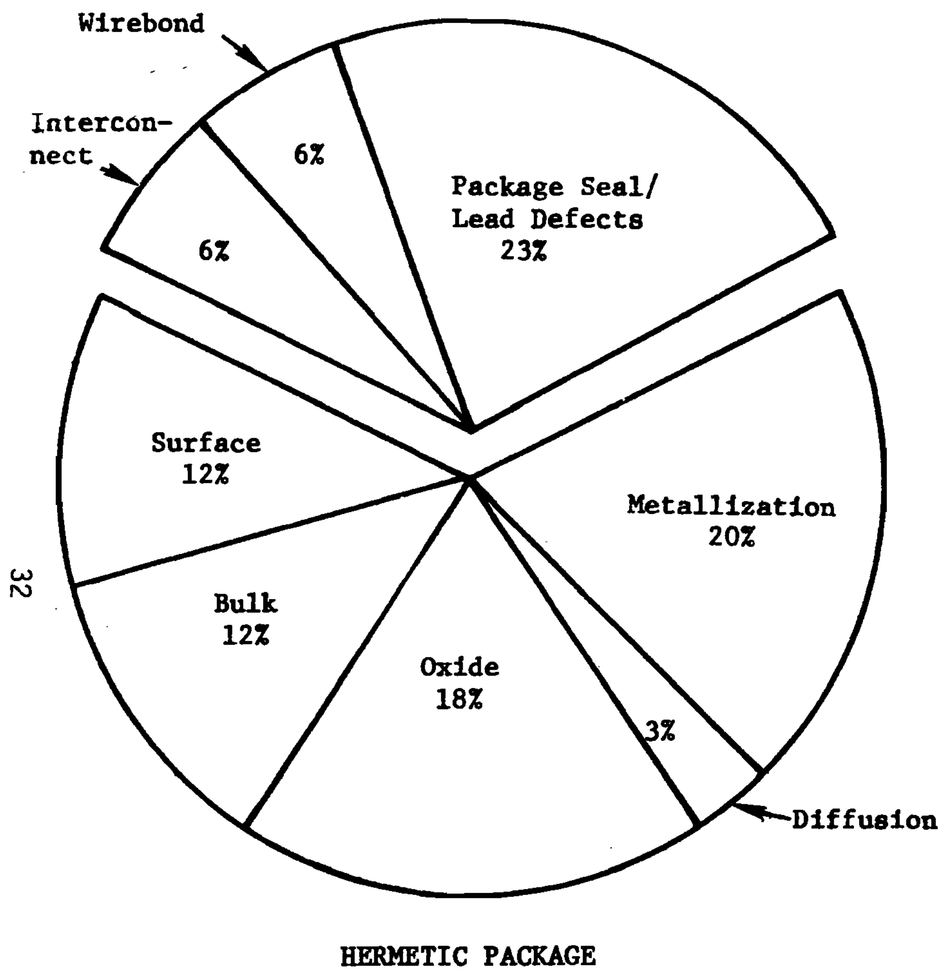
It can be assumed that the frequency of occurrence of package-related defects for any given package configuration is constant, regardless of the technology of the device contained within. This assumption is valid since the frequency of occurrence of package-related defects is determined by the physical characteristics of the package construction and materials.

The failure mode contribution attributable to package defects was determined for LSI devices by using the same technique: performing the analysis on TTL LSI screening data. This analysis indicated that the percentages of experienced defects attributable to package-related defects were 40% and 42% for plastic encapsulated and hermetic packaged devices, respectively.

TABLE 9: MICROCIRCUIT SCREENING RESULTS, GENERIC
(INCLUDES ALL PACKAGE TYPES)

TECHNOLOGY	COMPLEXITY	NUMBER SCREENED*	NUMBER REJECTED	AVERAGE % DEFECTIVE	NUMBER OF ENTRIES	MEDIAN % DEFECTIVE
TTL	SSI/MSI	5,353,442	69,308	1.30%	2670	0.98
	LSI	61,583	2,261	3.67	79	3.21
STTL	SSI/MSI	183,992	3,676	2.00	216	1.47
	LSI	22,701	719	3.17	58	1.00
LTTL	SSI/MSI	186,918	3,601	1.93	133	1.86
	LSI	23,352	530	2.27	12	3.10
HTTL	SSI/MSI	192,743	2,912	1.51	196	0.51
LSTTL	SSI/MSI	276,794	4,331	1.57	206	0.96
ECL	SSI/MSI	132,284	3,161	2.39	106	1.74
CMOS	SSI/MSI	1,049,802	26,994	2.57	843	2.41
	LSI	54,656	3,404	6.23	67	4.45
PMOS	SSI/MSI	101,254	2,579	2.55	82	2.11
	LSI	189,019	6,041	3.20	184	1.02
NMOS	LSI	117,982	3,695	3.13	97	2.68
OP AMPS		383,503	17,455	4.55	135	3.98
LINEAR, GENERAL		346,305	15,392	4.44	175	4.20
INTERFACE		181,409	5,696	3.14	104	1.88

*Screen consisting of initial inspection, environment screen, burn-in, and final EM.



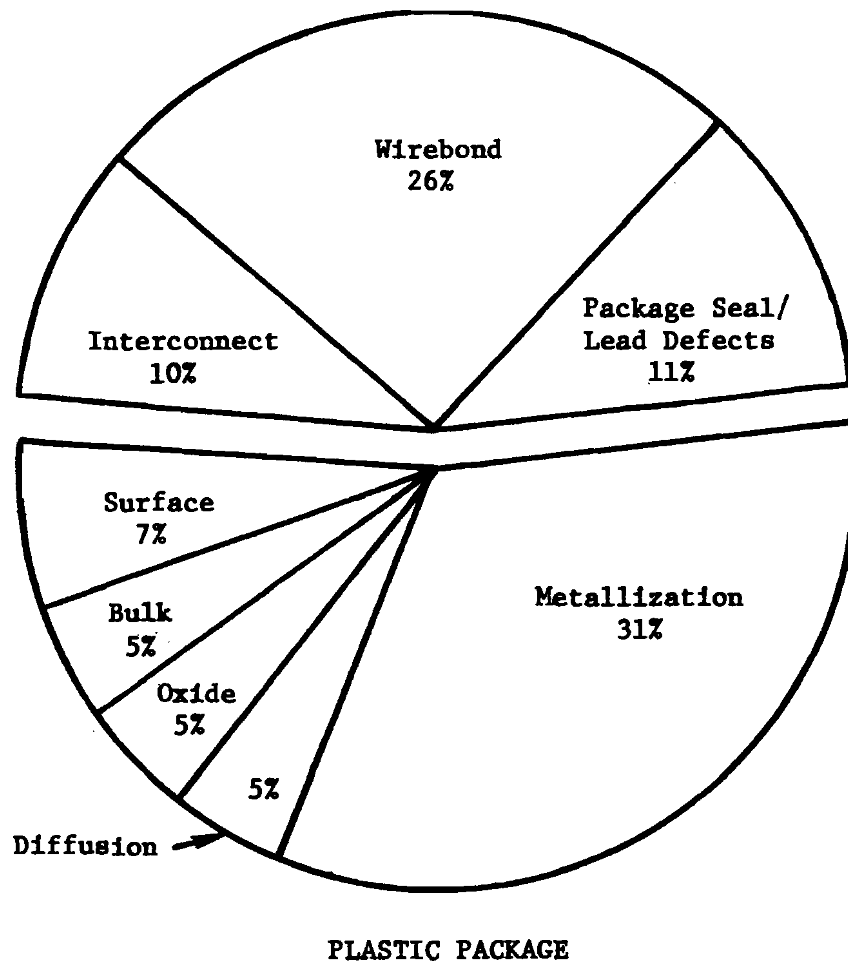


Figure 1: Failure Mode Distributions For TTL SSI/MSI Devices In Hermetic And Plastic Packages

Using the data available in the TTL category, the appropriate reject rates attributable to package defects can be determined for each of the various package types. At the same time, the corresponding reject rates due to technology-related defects can be derived. The values of technology-related reject rates are presented in Tables 10 and 11 for devices in plastic and hermetic packages, respectively. Accordingly, the package-related reject rates are presented in Table 12.

To ascertain the average percent-defective reject rate for a given technology-package combination and for a given screening sequence, merely add the reject rates for the technology defects from the appropriate screen types in either Table 10 or 11, to the reject rates for the package defects in the same screen types as displayed in Table 12.

The numbers developed in these tables will be used in conjunction with screening cost information to evaluate screening cost-effectiveness later in Section 8.

TABLE 10: AVERAGE DIE-RELATED REJECT RATES IN VARIOUS SCREENS, PLASTIC ENCAPSULATED DEVICES (% DEFECTIVE)

TECHNOLOGY	COMPLEXITY	SCREENING REJECTS	INITIAL REJECTS	ENVIRONMENTAL REJECTS	BURN-IN REJECTS	FINAL REJECTS
TTL	SSI/MSI	0.81	0.40	0.17	0.18	0.06
	LSI	2.33	0.98	0.59	0.68	0.08
STTL	SSI/MSI	1.48	0.45	0.49	0.51	0.03
	LSI	1.86	0.68	0.52	0.61	0.05
LTTL	SSI/MSI	1.54	0.93	0.21	0.25	0.15
	LSI	1.57	0.96	0.11	0.41	0.09
HTTL	SSI/MSI	0.96	0.08	0.42	0.44	0.02
LSTTL	SSI/MSI	1.34	0.84	0.16	0.24	0.10
ECL	SSI/MSI	1.85	0.72	0.46	0.53	0.14
CMOS	SSI/MSI	2.31	1.05	0.48	0.70	0.08
	LSI	4.58	1.62	0.91	2.03	0.02
PMOS	SSI/MSI	2.14	0.58	0.83	0.57	0.16
	LSI	2.18	0.66	0.73	0.69	0.10
NMOS	LSI	2.21	0.59	0.68	0.86	0.08
OP AMPS		3.95	1.60	0.64	1.45	0.26
LINEAR, GENERAL		3.75	1.64	0.71	1.22	0.18
INTERFACE		2.78	1.11	0.59	0.92	0.16

TABLE 11: AVERAGE DIE-RELATED REJECT RATES IN VARIOUS SCREENS, HERMETIC PACKAGED DEVICES (% DEFECTIVE)

TECHNOLOGY	COMPLEXITY	SCREENING REJECTS	INITIAL REJECTS	ENVIRONMENTAL REJECTS	BURN-IN REJECTS	FINAL REJECTS
TTL	SSI/MSI	0.79	0.40	0.16	0.17	0.06
	LSI	1.98	0.84	0.50	0.58	0.06
STTL	SSI/MSI	1.45	0.44	0.48	0.49	0.04
	LSI	1.72	0.62	0.47	0.58	0.05
LTTL	SSI/MSI	1.31	0.68	0.24	0.25	0.14
	LSI	1.34	0.74	0.12	0.40	0.08
HTTL	SSI/MSI	0.93	0.06	0.41	0.44	0.02
LSTTL	SSI/MSI	0.98	0.42	0.21	0.28	0.07
ECL	SSI/MSI	1.85	0.72	0.46	0.53	0.14
CMOS	SSI/MSI	1.98	1.00	0.31	0.60	0.07
	LSI	3.86	1.40	0.70	1.74	0.02
PMOS	SSI/MSI	1.92	0.58	0.65	0.55	0.14
	LSI	2.00	0.46	0.74	0.71	0.09
NMOS	LSI	1.87	0.46	0.49	0.84	0.07
OP AMPS		3.82	1.58	0.64	1.35	0.25
LINEAR, GENERAL		3.53	1.47	0.69	1.20	0.17
INTERFACE		2.59	0.98	0.57	0.89	0.15

TABLE 12: AVERAGE PACKAGE-RELATED DEFECT REJECT RATES FOR VARIOUS SCREEN TYPES (% DEFECTIVE)

PACKAGE TYPE	SCREENING REJECTS	INITIAL REJECTS	ENV SEQ/SEAL REJECTS	BURN-IN REJECTS	FINAL INSP REJECTS
SSI/MSI*					
DIP - PLASTIC	0.72	0.31	0.24	0.13	0.04
CERAMIC	0.45	0.14	0.21	0.06	0.04
CER/MET	0.35	0.06	0.17	0.04	0.08
FPK - CERAMIC	0.41	0.10	0.21	0.08	0.02
MET/GLASS	0.34	0.12	0.10	0.02	0.10
CAN - METAL	0.29	0.06	0.14	0.03	0.06
LSI					
DIP - PLASTIC	1.55	0.55	0.82	0.12	0.06
CERAMIC	1.77	0.57	0.97	0.11	0.12
CER/MET	1.11	0.25	0.46	0.08	0.32

*SSI/MSI packages have 16 pins or less.

Section 6

THERMAL/MECHANICAL STRESS ANALYSIS

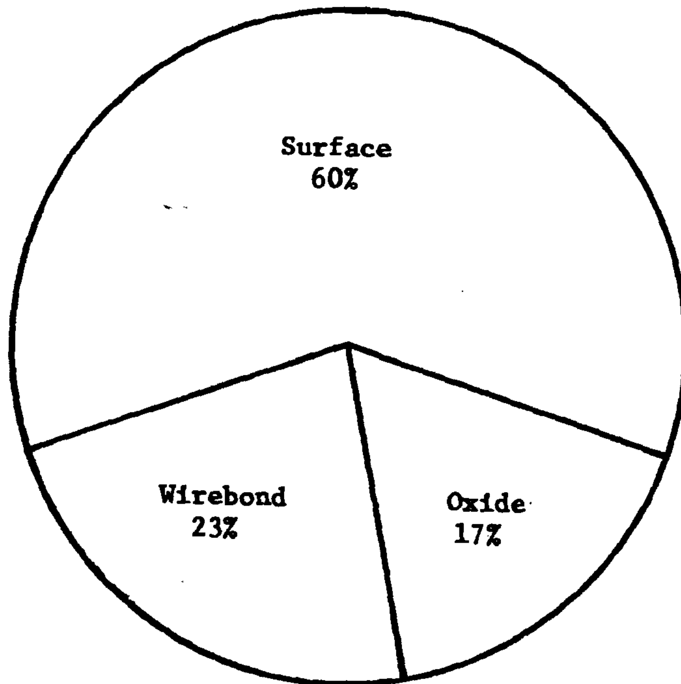
Thermal and mechanical stresses have long been considered to be effective tools in the evaluation and screening of integrated circuits. In order to properly assess the efficiency of thermal and mechanical screens, it is necessary to investigate the failure mechanisms which are activated upon the application of stresses and the degrees to which the mechanisms are actually activated. This section will present a discussion of the stresses associated with each of the major screens and of the types of defects which they are useful in activating.

Stabilization Bake

The stabilization bake involves, as the name implies, storing devices at an elevated ambient temperature for a specified time. At the end of the specified time the device may be subjected to electrical measurements or transferred directly to the next screen in the sequence.

This stabilization bake is commonly employed to evaluate the effect of storage at elevated temperatures without electrical stress applied on microelectronic devices. This technique is primarily used during preconditioning to stabilize the electrical characteristics of the device. Theoretically, the thermal stress applied during the stabilization bake should be useful in accelerating failures attributable to contamination, oxide, and wirebonding defects. The actual failure mode distributions for plastic and hermetic devices experienced in the stabilization bake are shown in Figure 2. The distributions are very similar for devices utilizing either package type, with surface defects, wirebond defects and oxide defects being the failure mode contributors.

The surface defects experienced in the stabilization bake were predominately contamination/leakage problems with an occasional inversion/channeling problem. While contamination problems are the largest contributor to the experienced failure mode distribution, the stabilization bake is not particularly efficient in activating these types of defects. High temperatures present during the bake mobilize ionic charges, thus allowing them to freely drift on the surface of the chip. This could allow contaminants to drift from a criticial area to some non-critical portion of the chip, actually improving the device's electrical characteristics. A more efficient method for activating contamination problems involves the application of an electrical stress (bias) to provide preferential drift of the ionic contaminants. This more realistically represents the



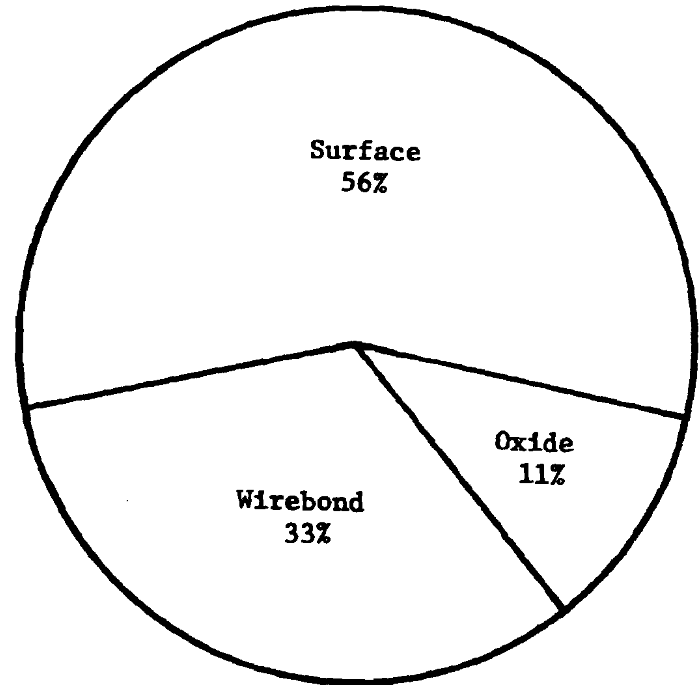


Figure 2: Failure Mode Distributions For Stabilization Bake Screens

actual operating conditions of the device and will tend to identify parts susceptible to these types of failures.

The wirebond defects, activated during the stabilization bake, are predominantly intermetallic compound-formation defects. Extended exposure at elevated temperatures accelerates the diffusion of gold atoms in the gold-aluminum bond system and results in a brittle intermetallic formation in the bond structure. However, this brittle intermetallic is a good conductor and it will not affect the bond integrity unless fractured. The thermal expansion stresses provided by the stabilization bake are normally not sufficient to cause a fracturing of the intermetallic, so many of the defects go undetected until subjected to sufficient stresses such as those exhibited in temperature cycling. The intermetallic failures detected during stabilization bakes commonly reflect bonds with abnormally low bond strengths.

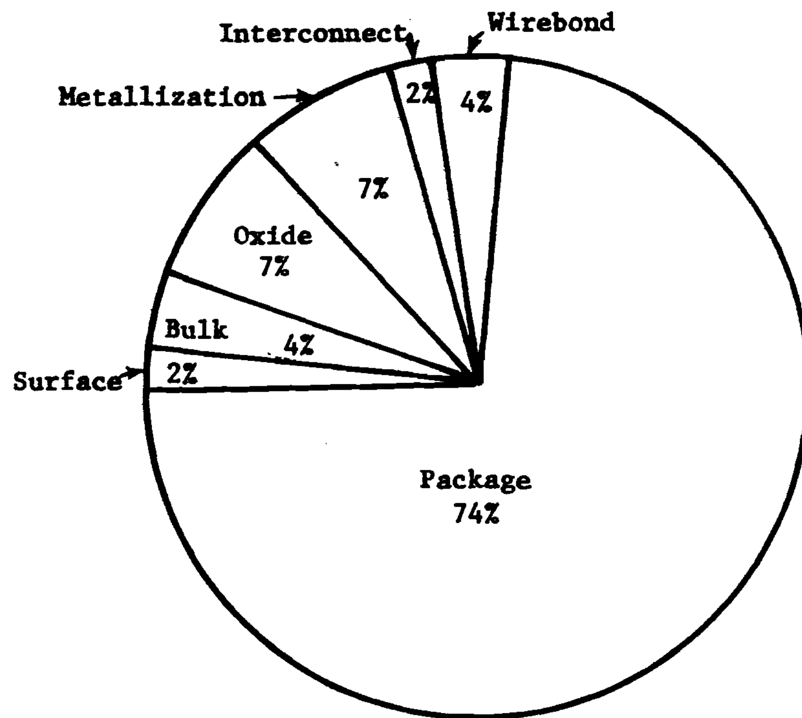
The stresses exhibited in a stabilization bake can be directly correlated to the time-temperature product. The basic philosphy associated with the stabilization bake, as with all screens, is to simulate a long interval of actual life in a short period of laboratory time. In most situations the duration of the bake is limited to a maximum of 168 hours. The ambient temperature is typically in the range of 125°C to 150°C. The ambient temperature for plastic encapsulated devices should be maintained below the glass transition point (~150°C) to avoid any undesirable, detrimental effects.

Temperature Cycling/Thermal Shock

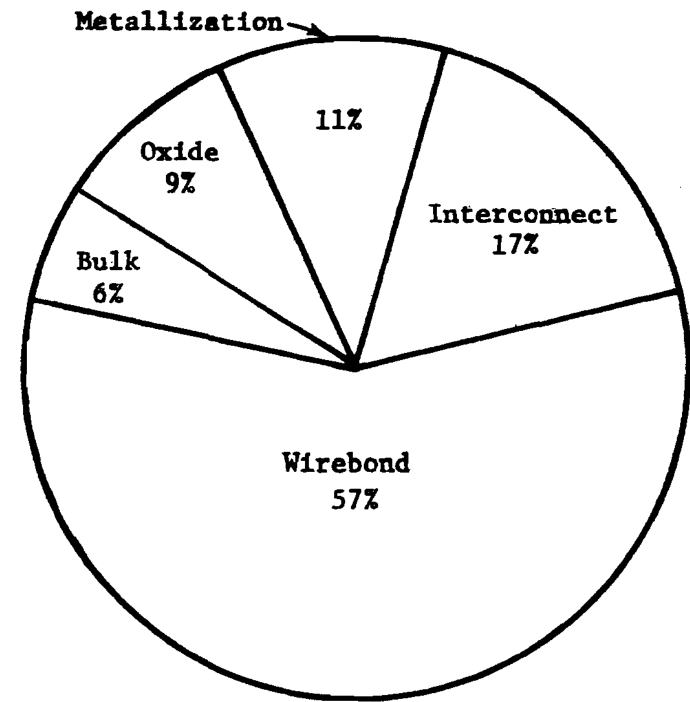
Temperature cycling and thermal shock screens are designed to determine the resistance of a device to exposure at high- and low-temperature extremes, and the effects of alternate exposures to these extremes. In addition, the thermal shock technique employs short transition times between the extremes to determine the resistance to rapid changes in temperature.

Both of these techniques derive their stresses from the thermal expansion coefficient mismatches of the constituent materials. These stresses are most critical at the material interfaces and especially critical at defect sites in the materials. The application of these stresses at defect sites propagates cracks, ruptures, or fracture materials at the defect sites, and results in fatigue-type failures upon repeated application of the stresses. The distributions of failure modes experienced during temperature cycling/thermal shock screens for devices in both plastic and hermetic packages are shown in Figure 3.

The actual distribution of failure modes experienced in thermal shock and temperature cycling, as well as the reject



HERMETIC PACKAGES



PLASTIC PACKAGES

Figure 3: Failure Mode Distributions For Thermal Shock And Temperature Cycling Screen Fallout

rates experienced, vary between the two techniques. To determine which is responsible for these variations, it is necessary to investigate the parameters associated with each technique.

The temperature cycling techniques, as defined by MIL-STD-883, Method 1010, is comprised of alternate exposures to hot and cold air or dry nitrogen in a confined chamber, remaining a minimum of 10 minutes at each extreme after the stabilization of the test chamber temperature. The transition time between the temperature extremes may vary from an instantaneous transfer to a 5 minute transfer interval. While the device experiences rapidly changing temperatures, the temperature distribution within the device is fairly uniform, resulting in only small temperature gradients.

The thermal shock technique, as defined by MIL-STD-883, Method 1011, specifies alternate immersions in hot and cold liquids, with each immersion lasting 5 minutes. The transition time for this technique is specified to be less than 10 seconds. This rapid transition between temperature extremes introduces large thermal gradients within the device. The mechanical stresses resulting from the thermal gradients may exceed the strength of the materials, causing deformation and actually inducing failures.

To realistically evaluate the potential of temperature cycling and thermal shock as screening techniques, it is necessary to analyze actual data obtained in these two test types. Numerous studies* have been directed toward the comparison and analysis of thermal/mechanical stress testing techniques. The information presented in these studies, supplemented by additional data, will be later discussed in detail.

Since the response to various thermal/mechanical stresses will obviously be dependent upon the package materials and configuration, the information presented below has been organized by package categories, hermetic and plastic encapsulated.

<u>Plastic Encapsulated Devices</u>

As shown in Figure 3, the majority of the failure modes experienced in temperature cycling the thermal shock for plastic encapsulated devices are associated with interconnect and wirebond integrity. The distribution of experienced failure modes can be explained by considering the physical characteristics of plastic device construction.

The temperature variations experienced in these thermal stress techniques cause the expansion and contraction of the constituent materials within the device. The interconnect wires, which are embedded in the encapsulant, and the encapsulant

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*See Bibliography (entry numbers 5, 12, 14).

material exhibit different thermal expansion coefficients. The different coefficients of thermal expansion of the constituent materials produce stresses between the materials. The induced stresses have the most pronounced effect at defect sites or at the weakest portion of the system, which is typically a bond or grain boundary in the interconnect wire. Upon repeated application, the stresses propagate cracks or fractures resulting in lifted or broken bonds or broken wires.

The thermal stresses also activate metallization-, oxide-, and bulk-related defects. However, the occurences of these types of failures are more closely related to the device technology rather than the package configuration.

Detailed failure data for plastic encapsulated devices subjected to temperature cycling or thermal shock screens are presented in Table 13.

The response of the plastic packages to thermal stresses varies dramatically between manufacturers and is clearly influenced by the type of encapsulant and the size of the interconnect wires.

The performance of plastic packages in thermal stress screening can be correlated to the glass transition points for the encapsulant materials. During conditions where the temperature exceeds 125°C, phenolic packages performed better than epoxy packages since the glass transition point for phenolic (200°C) is considerably higher than that of epoxy (150°C). For plastic packages, a temperature excursion above the glass transition point is not immediately destructive, but it is not recommended.

A second factor which impacts the performance of plastic packages in thermal screening is the diameter of the interconnect wires. Increased wire diameter improves performance in temperature cycling and thermal shock tests.

The highest reject rates in thermal screens were observed for a package with the lowest glass transition point and smallest diameter wires. The majority of the data presented in Table 13 reflects the characteristics of Epoxy "B" packages containing 1.0 mil wires. It appears from the analysis of the data that the experienced reject rates are related to the magnitude of the high-temperature extreme rather than to the delta temperature interval.

Hermetic Packaged Devices

The response of hermetic packaged devices to thermal stres screening differs drastically from that of plastic encapsulated

TABLE 13: DETAILED TEMPERATURE CYCLING/THERMAL SHOCK SCREENING DATA FOR PLASTIC ENCAPSULATED DEVICES

Screen Type	Low Temp (^{o}C)	High Temp (^{o}C)	ΔT (^{o}C)	Number Tested	Number Failed	% Defective
Temperature Cycling 10 Cycles $\geq$ 15 min/cycle	0	100	100	3125	24	0.77
	-40	70	110	12478	14	0.11
	-55	85	140	33745	283	0.84
	-55	125	180	3098	29	0.94
	-65	125	190	4025	35	0.87
	-55	150	205	1087	8	0.74
	-65	150	215	7714	89	1.15
Thermal Shock 10 Cycles $\geq$ 5 min/cycle	0	100	100	21392	30	0.14
	-55	125	180	21496	47	0.22
	-65	150	215	1847	7	0.38

devices. The major hermetic package defects which are activated in the thermal stressing are related to the integrity of the package seal. The performance of the various types of hermetic packages in thermal stresses is dependent on the physical characteristics of the package.

The common ceramic dual-in-line package (DIP) is comprised of a die mounted on a lead frame, surrounded by a glass preform, and sandwiched between a ceramic base and lid. In this package, it is the glass seal which establishes the package hermeticity. With the lead egress through the sealing glass, all lead-forming and handling operations performed after the sealing of the package stress the seal material. This characteristic explains the susceptibility of the package to hermeticity problems. It is the same condition, the lead egress through the seal material, which is aggravated with the application of thermal stresses. Because the lead frame and sealing glass possess different thermal expansion coefficients, induced stresses and possible cracks will result during thermal screening.

The detailed data for hermetic packaged devices are presented in Table 14. In examining the data for ceramic packages, one sees a dramatic increase in the average reject rates experienced during thermal shock testing as opposed to those experienced during temperature cycling. The package performance will obviously be influenced by the manufacturer, type of sealing glass, and bonding techniques. However, the data in Table 14 reflect the experiences of a wide cross section of manufacturers and should not be biased by any one of these factors.

The phenomenon experienced can be explained by considering the types of defects activated in each condition. Thermal shock affects package seal integrity while temperature cycling affects interconnects and wirebonds. Since the sealing glass has been identified as the weakest and most vulnerable material in the structure, it would be reasonable to expect that the majority of the defects would occur in the seal material and would be activated by thermal shock stressing.

A detailed investigation into the effects of thermal shock testing* has concluded that thermal shock, MIL-STD-883, Method 1011, Condition A, will cause fine leak failures in as few as 15 cycles and appears to be destructive to the integrity of the package. The recommendation was made that thermal shock should not be used as a 100% screen. MIL-STD-883A, Notice 2, has eliminated thermal shock from the screening sequence for Class A devices. However, the temperature cycling can be replaced by thermal shock Method 1011, Condition A, minimum, for Class B and C devices.

While temperature cycling stresses activate seal and certain

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*Banks, S. B. (Texas Instruments, Incorporated, Dallas, TX). Investigation of Microcircuit Seal Testing, RADC-TR-75-89, April 1975.

TABLE 14: DETAILED TEMPERATURE CYCLING/THERMAL SHOCK SCREENING DATA FOR HERMETIC PACKAGE DEVICES

Screen Type	Low Temp (°C)	High Temp (°C)	ΔT (°C)	Package Type	Number Tested	Number Failed	% Defective
Temperature Cycling 10 cycles ≥ 15 min/cycle	-55	85	140	Ceramic	3122	13	0.42
	-55	125	180	Ceramic	5417	33	0.61
	-55	125	180	Cer/Met	1021	6	0.59
	-65	150	215	Ceramic	3692	23	0.62
	-65	150	215	Cer/Met	976	7	0.72
	-65	150	215	Metal Can	7654	39	0.51
Thermal Shock 10 cycles ≥ 5 min/cycle	-55	125	180	Ceramic	14724	193	1.31
	-55	125	180	Cer/Met	3271	8	0.25
	-55	125	180	Metal Can	4787	47	0.98

die defects in ceramic packages, the greatest effect is observed with the interconnects and wirebonds. In ceramic packages, as with most hermetic packages, the interconnect wires are suspended in the package cavity and are relatively unconstrained in their movement. The application of thermal stresses causes the wires to expand and contract along the geometry of the wire. This flexing action introduces failures at the bond or at weak points of the wires. Common defects include lifted bonds, broken bonds, or broken wires.

The experienced reject rates will be influenced by the wire material, the type of bonding system, and the bonding technique. Thermally-cycled wedgebonds fail sooner than ball bonds. The gold-aluminum bond system will fail sooner than an aluminum-aluminum bond system. Devices employing an up-bonding technique experience 94% of their failures with their first bond, the one on the die. Devices using a down-bonding technique experience 85% of their failures with their first bond, the one on the post.

The thermal stress experiences with ceramic/metal packages are extremely similar to those of ceramic packages, with the exception of package hermeticity. The typical ceramic/metal dual-in-line package employs a thin-film conductor system sandwiched between two thin layers of ceramic rather than a lead frame as in a ceramic DIP. The package hermeticity is established by solder sealing or by welding a Kovar lid to the package. This package offers the advantages of a reduced seal perimeter and the replacement of a weak glass seal with a more durable solder seal.

The ceramic/metal package exhibits the best performance of all DIP's in temperature cycling and thermal shock. Hermeticity defects account for only a small portion of the experienced malfunctions in thermal stress testing. Wirebond problems accounted for the majority of the experienced defects. The majority of the wirebond problems involved weak post bonds which had resulted from the down-bonding technique employed and the intermetallics which developed in the gold-aluminum bonding system.

While the lids of metal can packages are commonly welded to the header, the leads protruding through the base are surrounded by glass to provide insulation from the base material. The difference in the thermal expansion coefficients of the glass and the wire introduces hermeticity problems. However, these problems do not approach the magnitude of the problems with ceramic devices.

In addition to hermeticity problems, devices in metal can packages also experienced interconnect and wirebond problems, as did the other hermetic packages. The detailed results of thermal stress tests for devices in metal can packages are also presented in Table 14.

Data obtained in extended temperature cycling and thermal shock tests have been collected and graphically presented in Figures 4 through 9. These figures reflect, for the various package configurations, the fatigue effects associated with extended exposure to temperature cycling and thermal shock environments.

Mechanical Shock/Constant Acceleration

The mechanical shock and constant acceleration screens, as originally conceived, were intended to identify structural and mechanical weaknesses in the devices. Since all the constituent materials in a plastic encapsulated device are constrained by the encapsulant material, mechanical stress testing will not be effective in activating and eliminating structural defects. In hermetic package devices the constituent materials are not constrained, as in plastic devices, and therefore mechanical stresses can cause cracking and fracturing of various structural weaknesses. The distribution of failure modes experienced in mechanical shock and constant acceleration are presented in Figure 10.

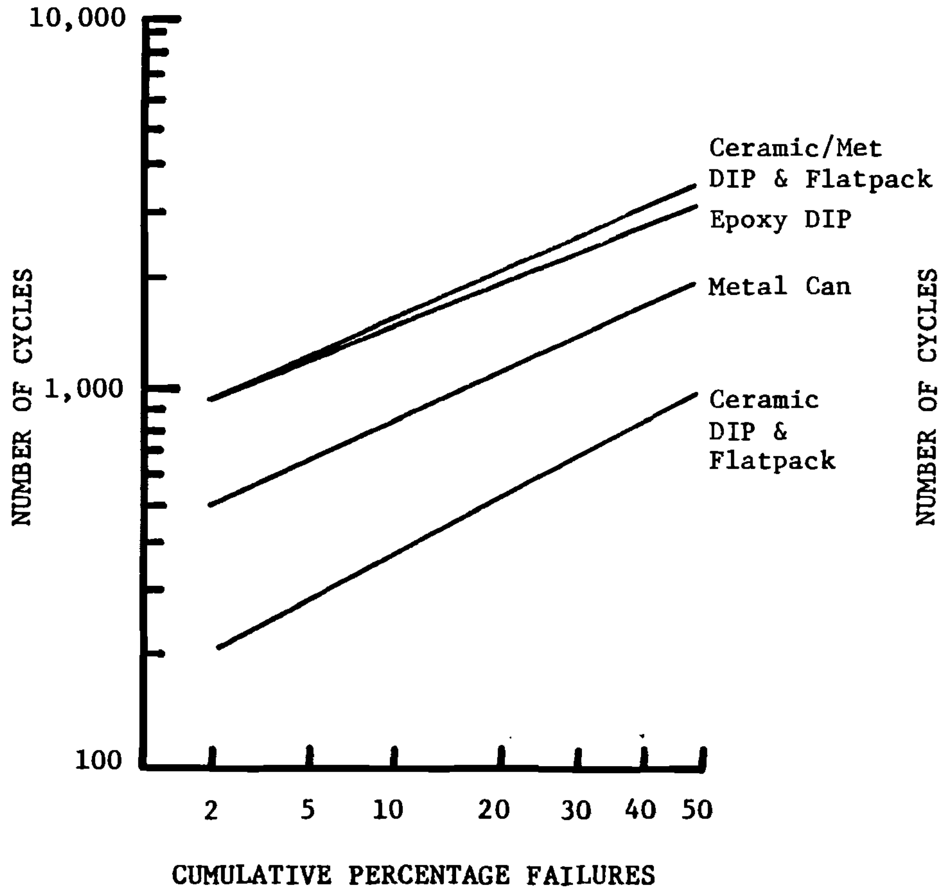

Figure 4: Package Response To Extended Temperature Cycling; Air-to-Air, $\geq$ 15 min/cycle, -65°C to 150°C

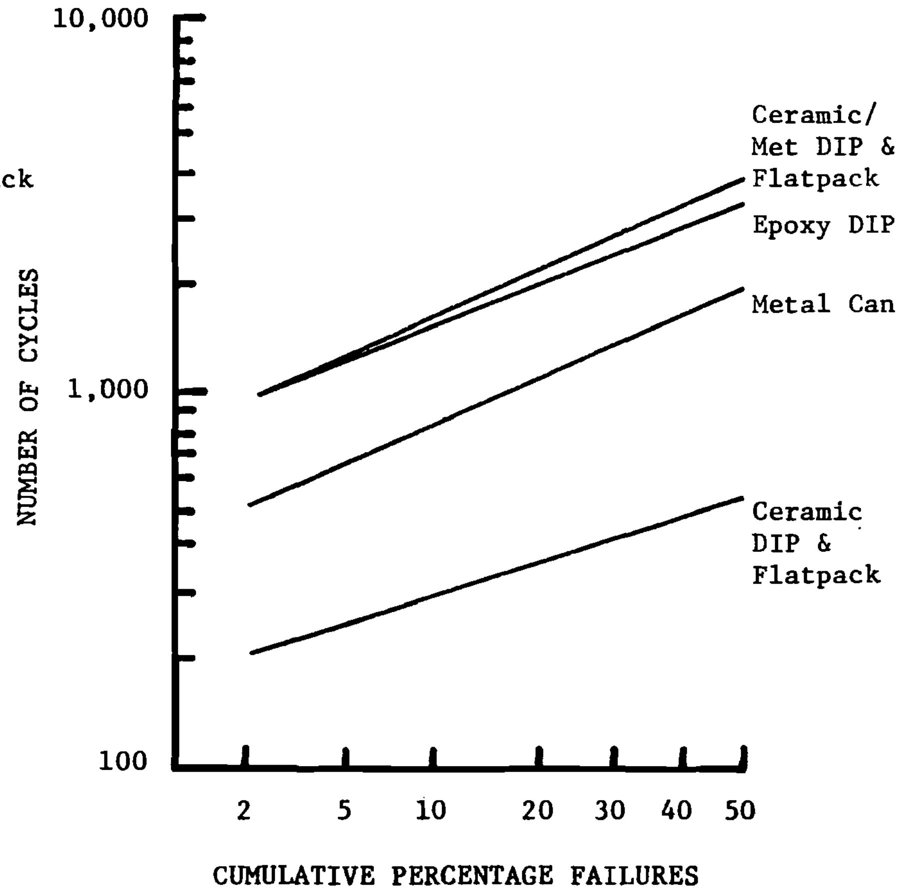

Figure 5: Package Response To Extended Thermal Shock; Liquid-to-Liquid, $\geq$ 5 min/cycle, -65°C to 150°C

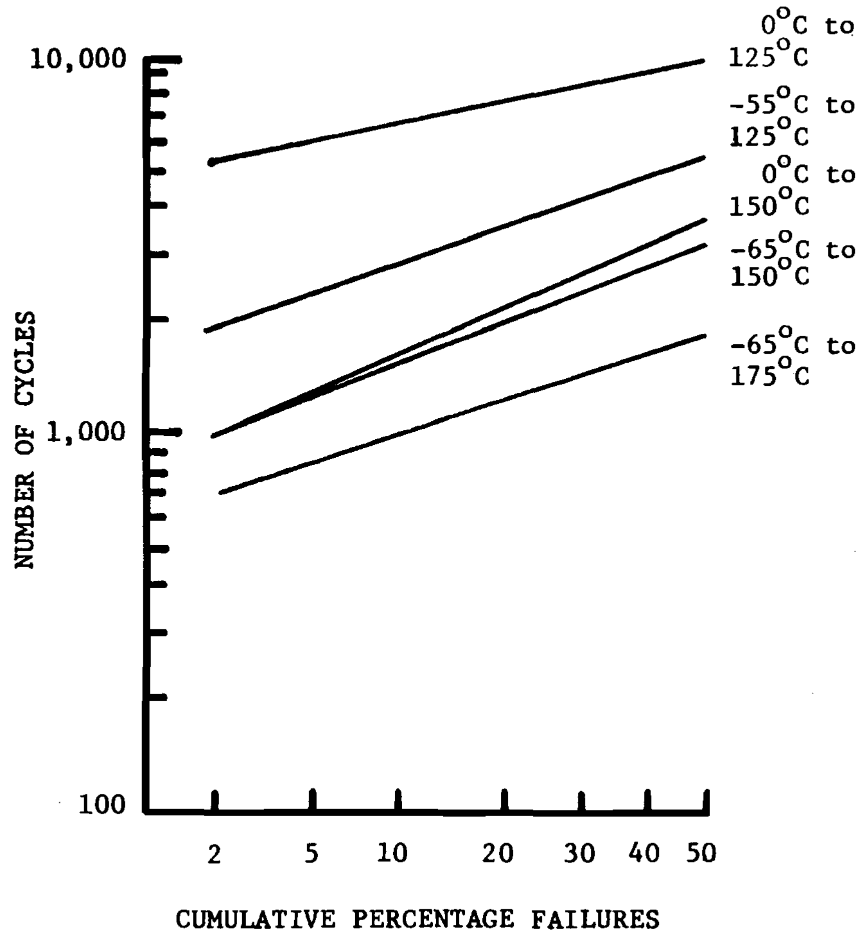

Figure 6: Epoxy DIP - Extended Temperature Cycles; Air-to-Air, $\geq$ 15 min/cycle

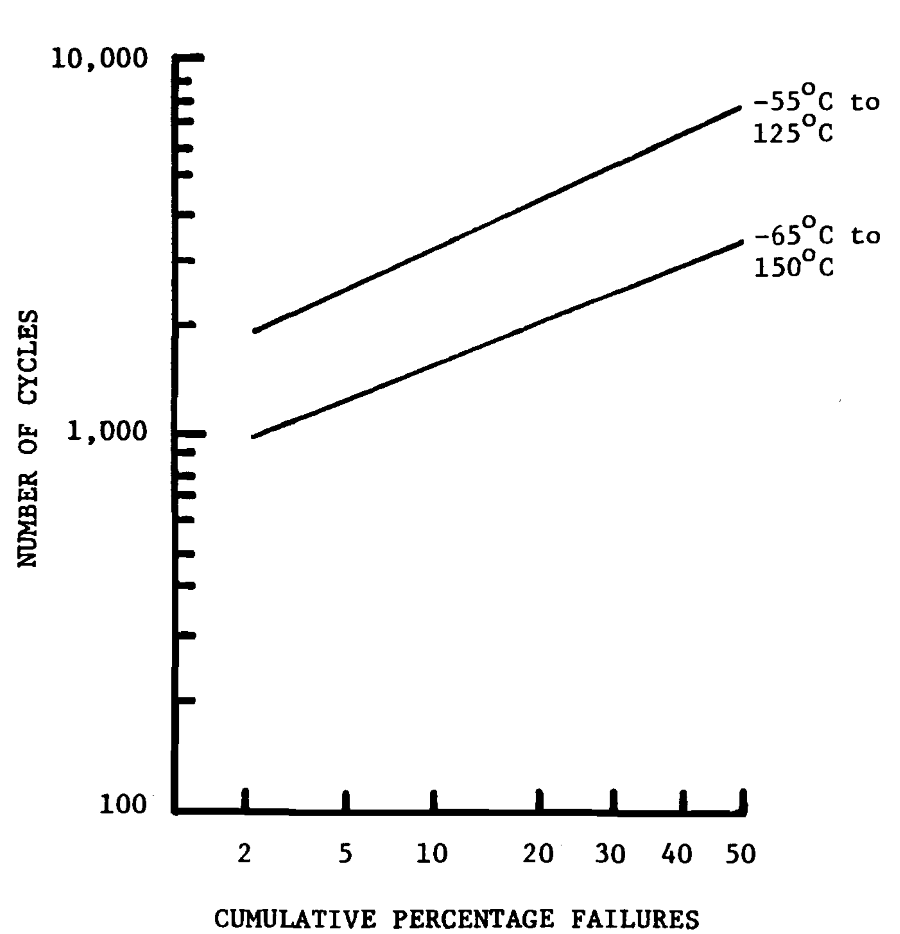

Figure 7: Epoxy DIP - Extended Thermal Shock; Liquid-to-Liquid, $\geq$ 5 min/cycle

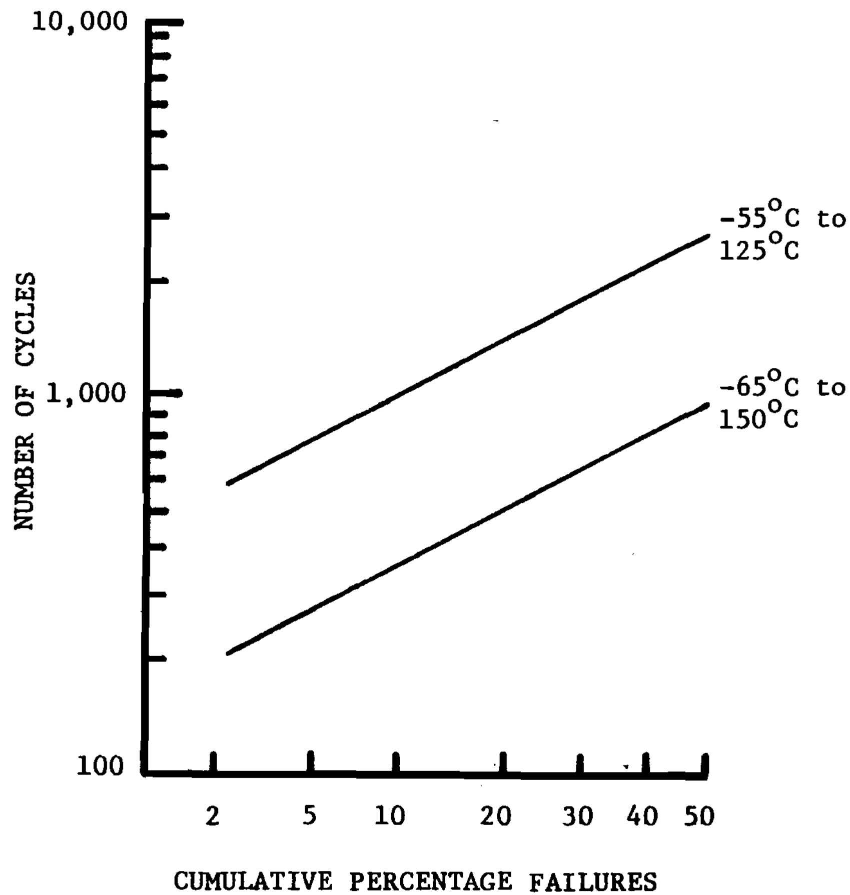

Figure 8: Ceramic DIP & FPK - Extended Temperature Cycles; Air-to-Air, ≥ 15 min/cycle

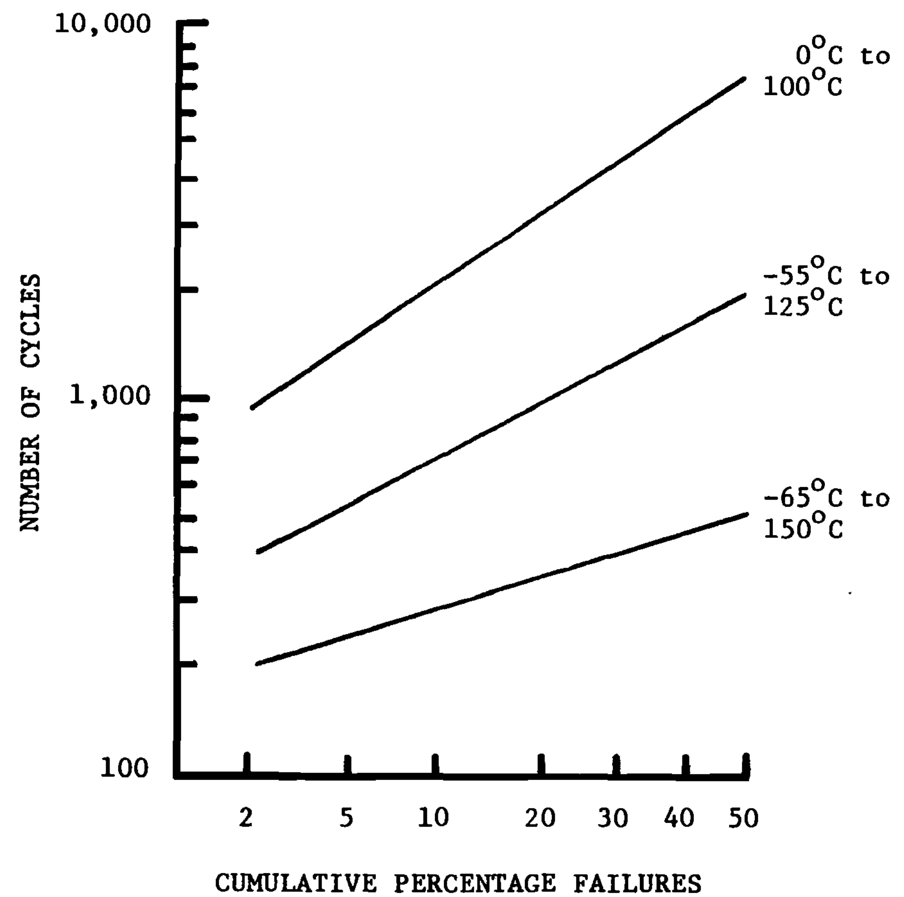

Figure 9: Ceramic DIP & FPK - Extended Thermal Shock; Liquid-to-Liquid, ≥ 5 min/cycle

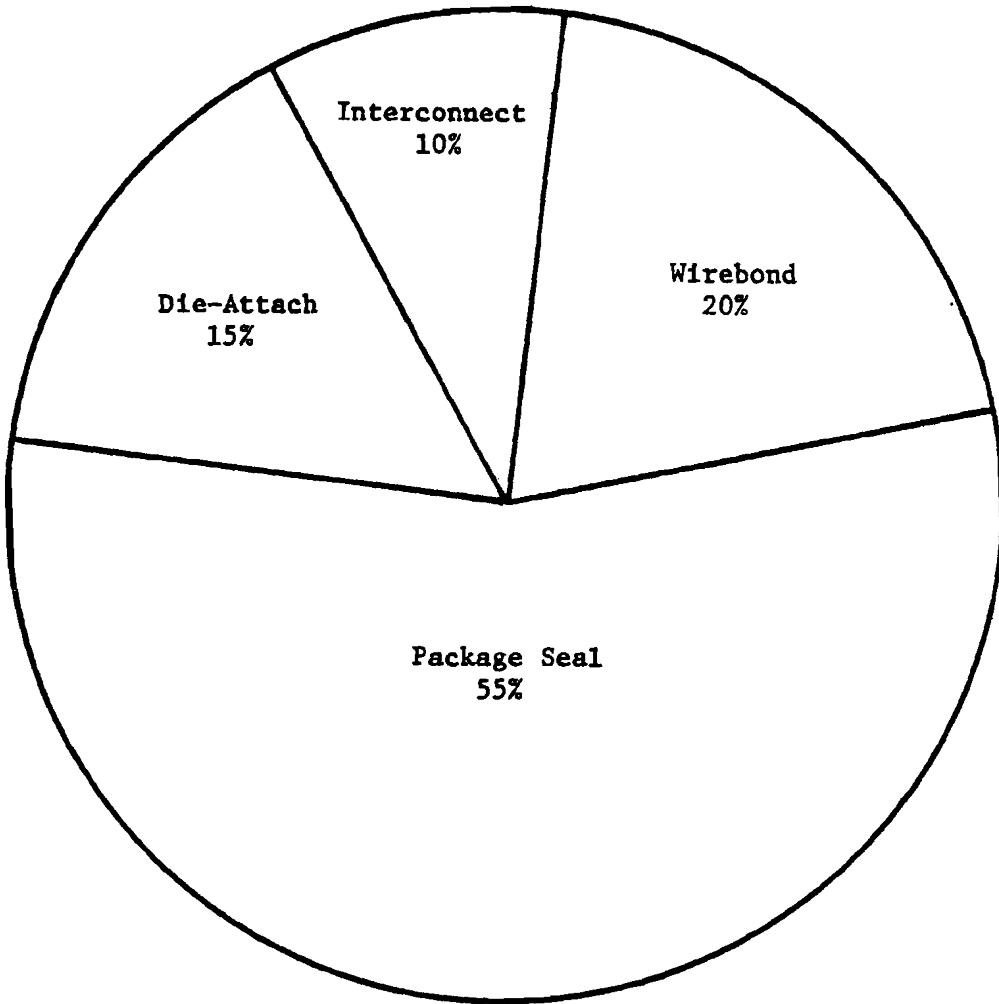

Figure 10: Failure Mode Distribution For Mechanical Shock And Constant Acceleration Screens (Hermetic Packages)

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Section 7

BURN-IN STRESS ANALYSIS

As previously discussed, screening is employed to eliminate infant mortality defects and to convert latent reliability defects into actual failures which can be identified by conventional detection methods. Subjecting a device population to screening stresses does not merely provide a time displacement along the continuous function "bathtub curve," but actually results in a hazard rate at the beginning of the useful life segment lower than that indicated by the continuous function curve [see Figure 11(a)].

This lower hazard rate can be explained by considering that the continuous function hazard rate curve is actually comprised of many underlying distributions. An example of this is shown in Fig. 11(b). The irregular underlying distributions arise from the stress-dependency variations of the multitude of failure mechanisms exhibited by the device population. The activating stresses which are typically experienced during the device lifetime include temperature, mechanical stress and strain, and electrical bias, all of which affect the positioning and shapes of these underlying distributions.

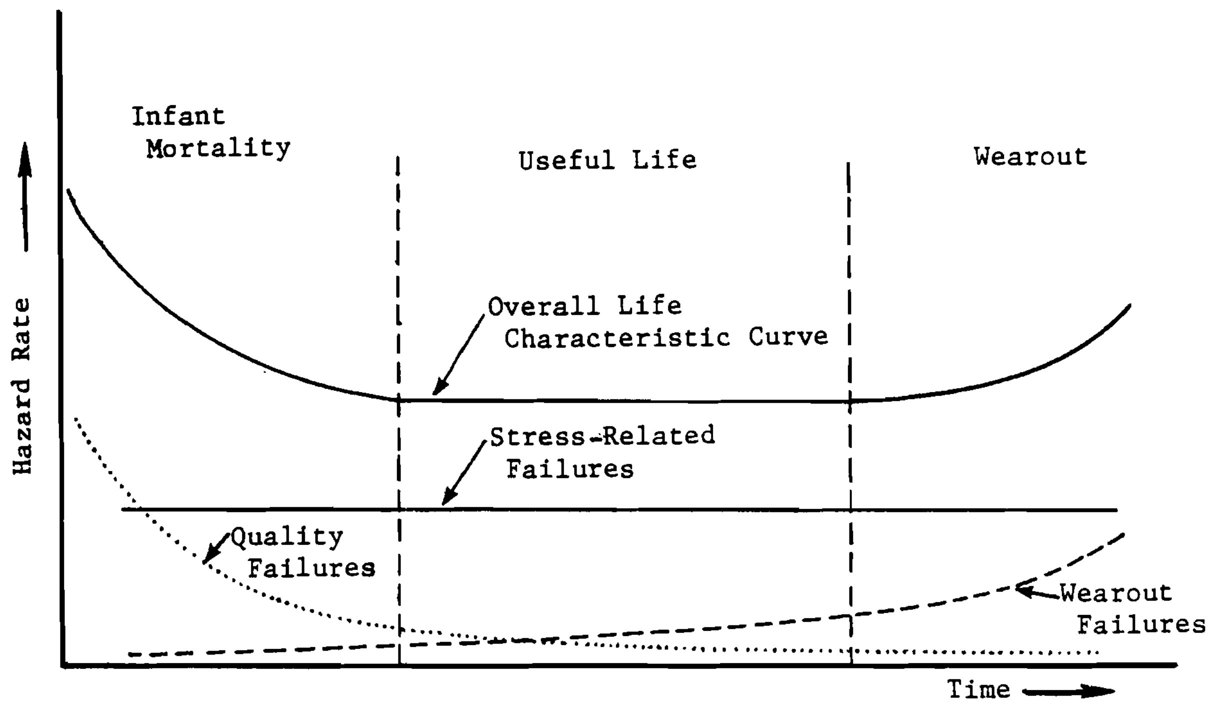
Temperature is considered to be the primary activating stress since it has the most pronounced effect upon a substantial number of failure mechanisms experienced in microcircuit devices. Associated with each of the underlying distributions is an activation energy which reflects the temperature dependence of a particular failure mechanism or group of mechanisms.

Several models have been developed to characterize failure mechanism temperature dependence and to provide an approximation of the relationship between stress (electrical and thermal), time, and failure rate. One model which is commonly used to depict the temperature relationships is the Arrhenius model. The Arrhenius model takes the following general form:

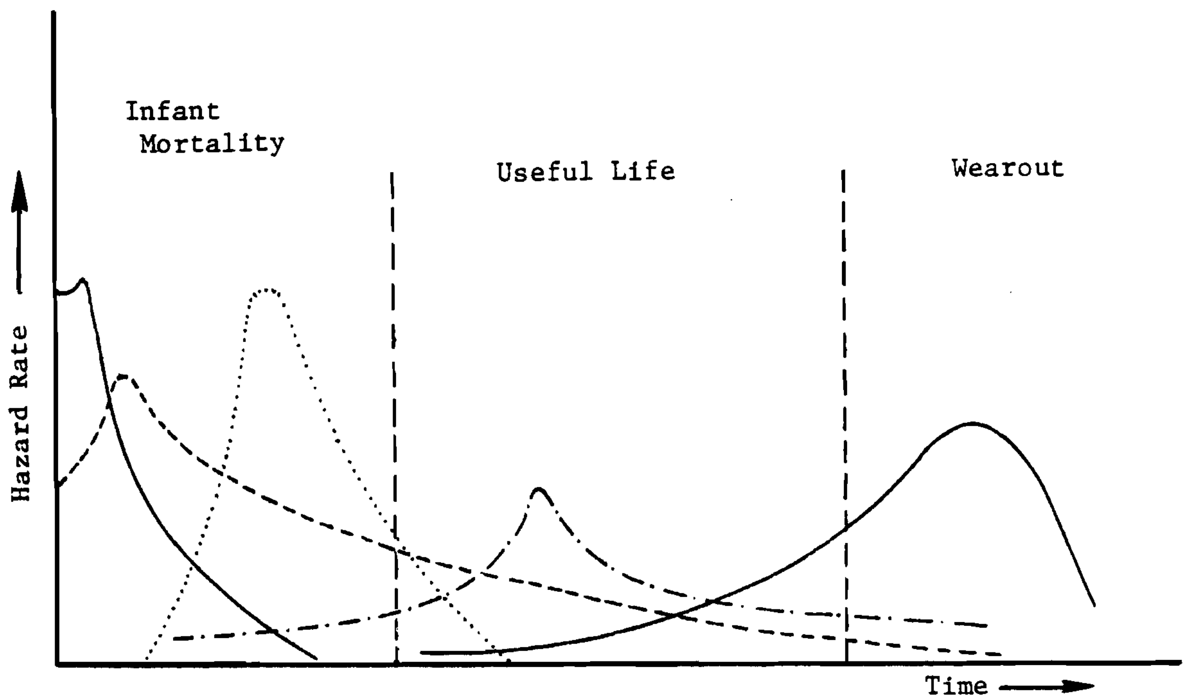
$$\lambda(T) = C_1 \exp\left(\frac{-E_a}{KT}\right)$$

where:

$\lambda(T)$ = part failure rate (temperature-dependent)
T = absolute temperature (^oK)
K = Boltzman's constant (8.63×10^{-5} eV/^oK)
E_a = the activation energy of the individual part failure mechanisms (eV)
C_1 = a constant



(a) Typical Model



(b) Possible Underlying Distributions

Figure 11: Modeling of Component Life Periods

The identification of the activation energies associated with each of the known integrated circuit failure mechanisms would permit accurate failure predictions and timely preventive maintenance actions. However, determining a realistic activation energy for any given failure mechanism is impractical since it is extremely difficult to isolate failure occurrences precipitated by any single mechanism. Therefore, it is more reasonable to consider representative activation energies associated with generic failure mode categories; i.e., surface defects, oxide defects, metallization defects, etc., or device technology categories, such as CMOS, NMOS, TTL, etc.

The experimental determination of activation energies requires extensive life testing at various temperatures and comprehensive failure analysis of all component failures. These techniques and their results are discussed in many of the documents listed in the BIBLIOGRAPHY.

To assure satisfactory reliability of a component population during the early and useful life period, it is necessary to eliminate those underlying failure distributions whose activation energies place them within these two life periods. This can be best accomplished, prior to the early life period, by accelerating to the point of detection those mechanisms associated with each of these underlying distributions. This is the primary objective of a screening program.

Component burn-in is considered to be one of the most effective methods for adequately screening a significant portion of the defects experienced in microcircuit devices. Burn-in screens often combine temperature with power and bias stresses which, in many cases, simulate worst-case operating conditions. The accelerated stress test conditions are intended to activate the time-temperature-dependent failure mechanisms to the point of detection in a relatively short period of time. The burn-in stresses may activate early life failures which have been only partially activated by previous screens or have been totally unaffected previously.

There are several popular test configurations, each of which results in a variation in the burn-in stresses created. These various techniques can be grossly categorized as being either static or dynamic. Static burn-in configurations commonly consist of a DC bias applied to the device at an elevated temperature. The bias is applied in a manner predetermined to either forward bias or reverse bias as many junctions as possible within the device. The direction in which the bias is applied will influence the power dissipation and consequently the junction temperature of the device. However, in complex devices there is very little distinction between the stresses resulting from the two biasing methods since it becomes increasingly difficult to implement a clear-cut version of either option.

In the dynamic burn-in configurations the devices are actually operated at an elevated temperature. The burn-in technique provides both voltage and power stressing. The two most common types of dynamic burn-in configurations are parallel excitation, where all devices are connected in parallel and driven by the same source, and ring counter excitation, where the devices are connected in series with the output of one device driving the input of the next.

To determine which configuration is more appropriate for a given technology package configuration, it is necessary to examine the types of defects and the extent to which these defects are activated by the various techniques. The failure mode distributions experienced during the static and dynamic burn-in configurations are shown graphically in Figure 12. The distributions in Figure 12 are not intended to indicate the relative frequency of occurrence of various failure modes between static and dynamic burn-in, but rather the distributions of failure modes experienced within each of these test configurations.

The distribution for the static burn-in is dominated by the surface-, oxide-, and metallization-defect categories. The majority of these experienced defects resulted from some type of contamination or corrosion mechanism. The static burn-in condition is useful in the detection of defects caused by corrosives and contaminants since the elevated temperatures make the contaminants more mobile, and the electric field created by the bias causes preferential drift of the ions into critical areas.

Other defects in the static burn-in distribution include wirebond problems resulting from intermetallic formation and oxide breakdown anomalies. The intermetallic compound formation is a time-temperature-dependent failure mechanism. The temperature present in the static configuration is effective in accelerating to the point of detection intermetallic defects which are in a fairly advanced state. The electric fields created by the bias in the static burn-in stress defective oxides or oxides of insufficient dielectric strength, and thereby cause breakdown at weak points.

The distribution of experienced failure modes for the dynamic burn-in indicates more uniform contributions by the various failure mode categories than is shown in the static burn-in distribution. The different stresses created by the dynamic and static configurations result in a variation in the effectiveness of activating the assorted failure mechanisms.

While dynamic burn-in is typically performed at high temperatures, its effectiveness in screening contamination defects is impaired by the lack of a constant electric field to provide preferential drift of ionic contaminants. The dynamic

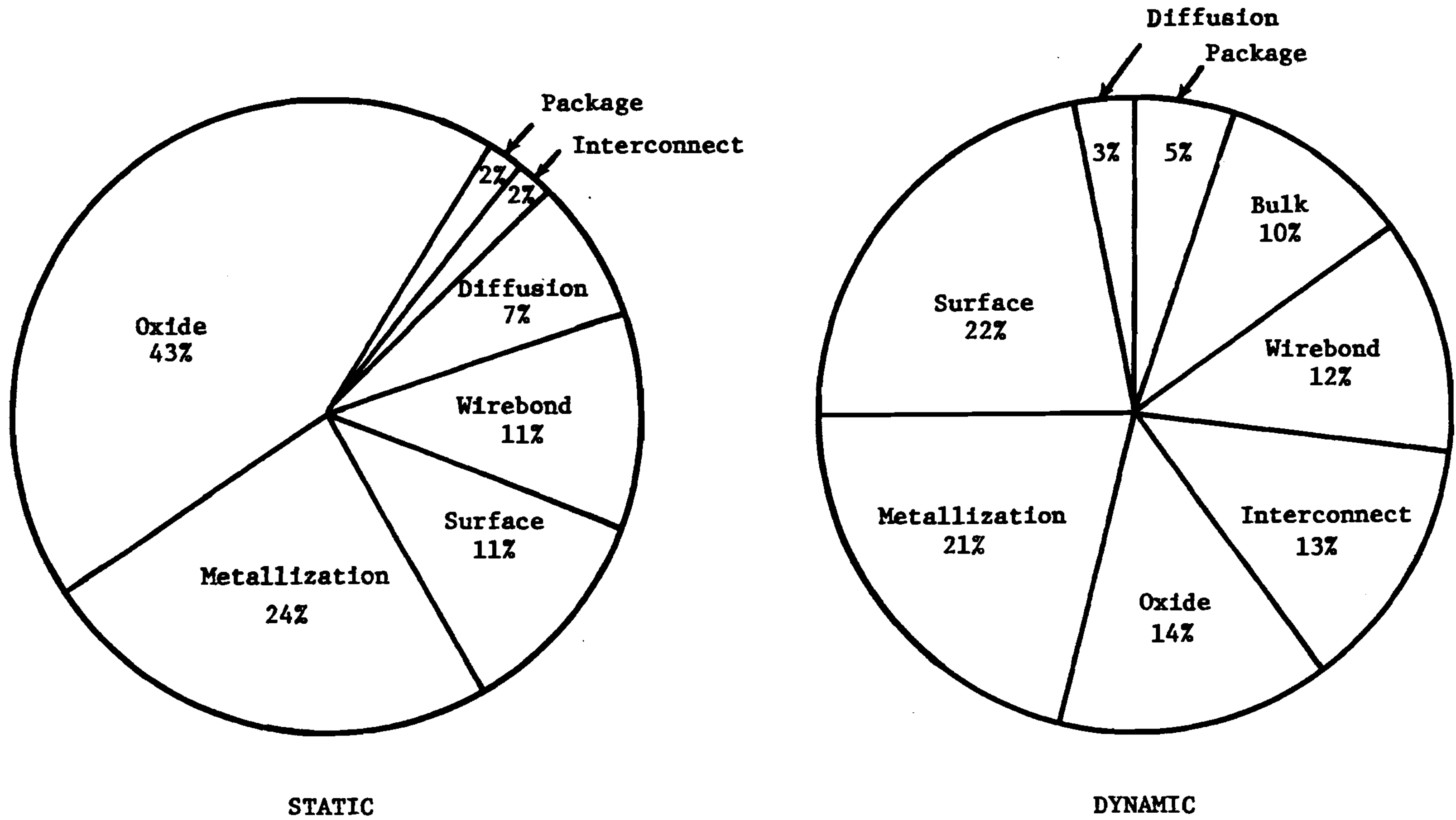


Figure 12: Failure Mode Distributions For Burn-in Screens (All Package Types)

operation causes the electric fields to constantly change with the electrical bias. These changing electric fields could actually cause ionic contaminants to drift to a noncritical area on the device allowing for "screening escapes."

Dynamic operation results in higher power dissipation, current densities and chip temperature than the static burn-in configuration. Increased current densities stress defects such as epitaxial and crystal imperfections, metallization, oxide and junction anomalies. Many of these defects require localized thermal stresses to provide activation for the associated failure mechanisms.

As a general overview, it can be noted that the dynamic burn-in configuration exhibits moderate-to-good efficiency in screening the majority of all experienced microcircuit defects, while the static burn-in is very efficient in screening only a limited number of experienced microcircuit defects.

The determination of the most cost-efficient burn-in requires the evaluation of the test temperature and duration in addition to the types of configuration. Low-temperature, short-duration burn-in tests offer obvious economic advantages in that they require the minimum amount of sophisticated equipment and increase the device throughput in testing. However, whether or not the burn-in efficiency is seriously compromised in the pursuit of economic benefits should be determined. The best approach to evaluate the relationship between burn-in temperature, duration, and efficiency is to examine actual burn-in data.

A summary of actual burn-in experiences for the various technology categories is presented in Table 15. The test type, temperature, duration and percent defective are indicated for each entry in this table. The results summarized in this table represent the reject rates of burn-in tests performed in a sequence of screens typically preceded by initial measurements and some type of environmental screening sequence. The reject rates experienced in burn-in tests performed independently will probably be slightly higher.

The burn-in results are displayed graphically in Figures 13, 14 and 15 for Bipolar, MOS, and Linear Devices, respectively. The time-temperature products for the various entries were determined by multiplying the test duration (hours) and device junction temperature (^{o}C). The junction temperatures for the devices in each of the entries may be approximated by employing the following equation:

$$T_j = T_A + \Delta T$$

where:

T_j = the junction temperatue

T_A = the ambient temperature

ΔT may be obtained from the table on page 59.

Test Type	Technology	Complexity	ΔT (°C)
Static	MOS	SSI/MSI	5
		LSI	10
	BIPOLAR	SSI/MSI	8
		LSI	15
	LINEAR		12
Dynamic	MOS	SSI/MSI	15
		LSI	20
	BIPOLAR	SSI/MSI	18
		LSI	25
	LINEAR		24

The junction temperature rise above ambient values indicated above were considered to be realistic average values determined from actual data.

The 60% confidence-interval percent-defective and point-estimate percent-defective values are illustrated in the summary figures. An examination of the data points displayed in the summary figures yields the general observation that burn-in percent-defective increases with increasing time-temperature product. This observation is true regardless of technology family, burn-in test, or device complexity.

General Burn-in Summary

There are several observations and recommendations which can be made from a detailed analysis of the various burn-in results.

Observations based upon the burn-in results show that the dynamic configuration yields an appreciably higher reject rate than the static configuration for LSI devices. Comparing the static versus dynamic burn-in reject rates shown in Table 15 for SSI/MSI devices, at 168 hours and 125°C, for Bipolar (entries 4 and 9), MOS (entries 16 and 19) and Linear (entries 27 and 29) technologies, it can be seen that the values are very similar in all cases. While the dynamic burn-in resulted in slightly higher reject rates in each case, the difference would not be sufficient to justify the increased cost for most applications.

A high-temperature reverse-bias configuration is the more effective screen for Linear and MOS devices, especially devices encapsulated in plastic packages. This screen is useful in activating and identifying contamination and surface anomalies, which are the dominant defects experienced with these device types.

TABLE 15: SUMMARY OF BURN-IN RESULTS FOR VARIOUS TECHNOLOGY FAMILIES

Technology	Complexity	Test Type	Test Temperature (°C)	Test Duration (Hrs)	Number Tested	Number Failed	% Defective	Number Test Records	Entry Number*
BIPOLAR	SSI/MSI	STATIC	100	96	647,452	2,666	0.41	181	1
			100	168	34,800	311	0.89	3	2
			125	48	12,253	30	0.24	46	3
			125	168	1,045,623	6,901	0.66	399	4
			150	48	473	4	0.85	3	5
			150	96	74,713	709	0.95	24	6
		DYNAMIC	125	72	2,323	6	0.26	13	7
			125	96	188,744	654	0.35	445	8
			125	168	7,891	55	0.70	7	9
	LSI	STATIC	100	168	4,969	44	0.82	2	10
			125	160	16,105	135	0.84	50	11
		DYNAMIC	125	96	817	6	0.73	2	12
			125	168	24,133	288	1.20	15	13
			175	168	573	8	1.40	4	14

*Entry numbers correspond to data graphically presented in Figures 13-15.

TABLE 15: SUMMARY OF BURN-IN RESULTS FOR VARIOUS TECHNOLOGY FAMILIES (Cont'd)

Technology	Complexity	Test Type	Test Temperature (°C)	Test Duration (Hrs)	Number Tested	Number Failed	% Defective	Number Test Records	Entry Number*
MOS	SSI/MSI	STATIC	125	48	18,741	52	0.28	11	15
			125	168	29,874	281	0.94	64	16
			150	48	9,765	38	0.39	2	17
			125	96	11,492	80	0.70	29	18
		DYNAMIC	125	168	54,326	554	1.00	35	19
	LSI	STATIC	125	96	194	1	0.51	1	20
			125	160	1,085	13	1.20	7	21
		DYNAMIC	70	48	3,776	16	0.42	11	22
			125	96	33,973	373	1.10	21	23
			125	168	32,857	525	1.60	41	24
LINEAR	ALL TYPES	STATIC	100	168	4,812	26	0.54	1	25
			125	96	376	2	0.53	1	26
			125	160	259,438	4,971	1.90	165	27
		DYNAMIC	125	96	5,490	88	1.60	45	28
			125	168	27,837	556	2.00	8	29

*Entry numbers correspond to data graphically presented in Figures 13-15.

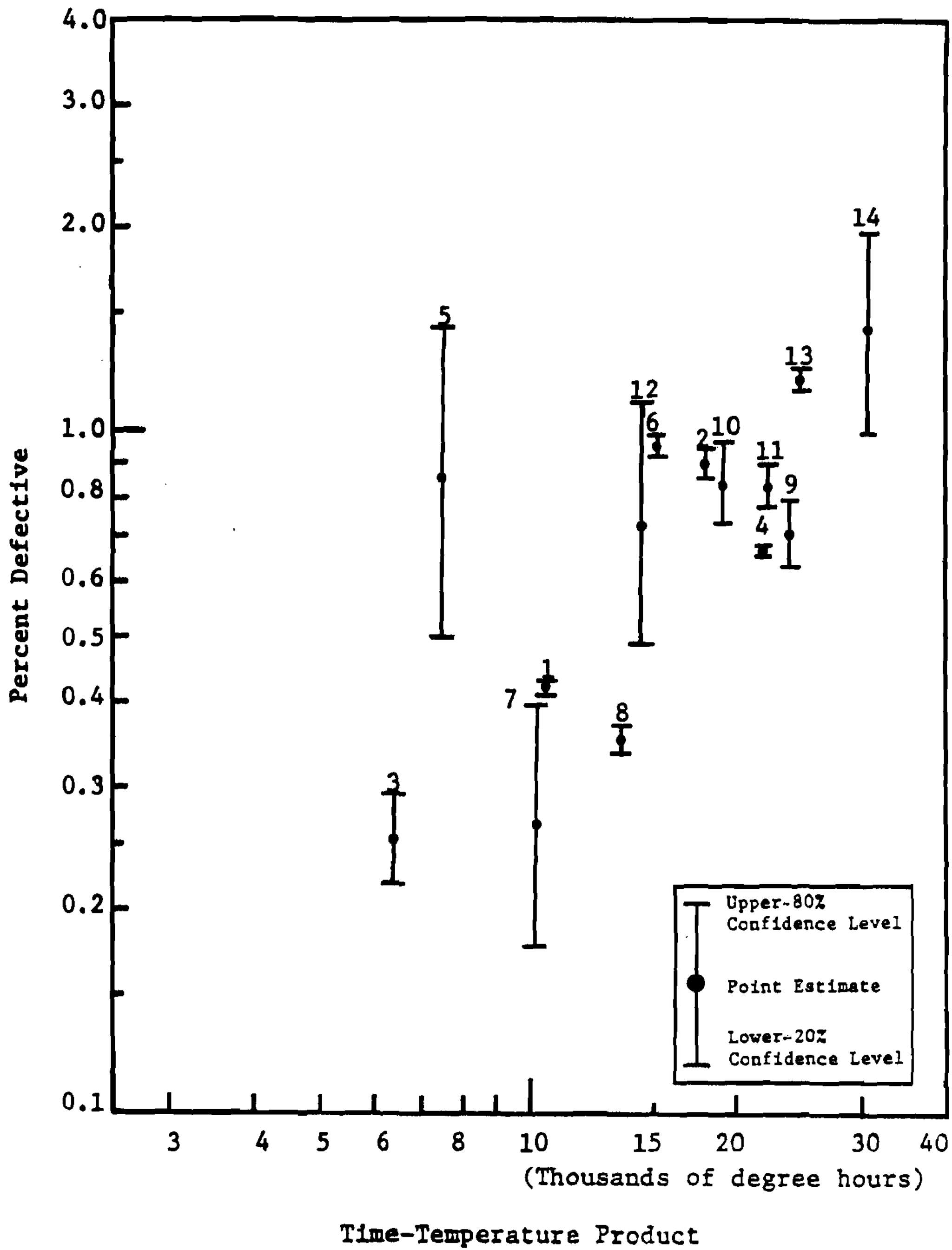


Figure 13: Burn-in Results for Bipolar Devices

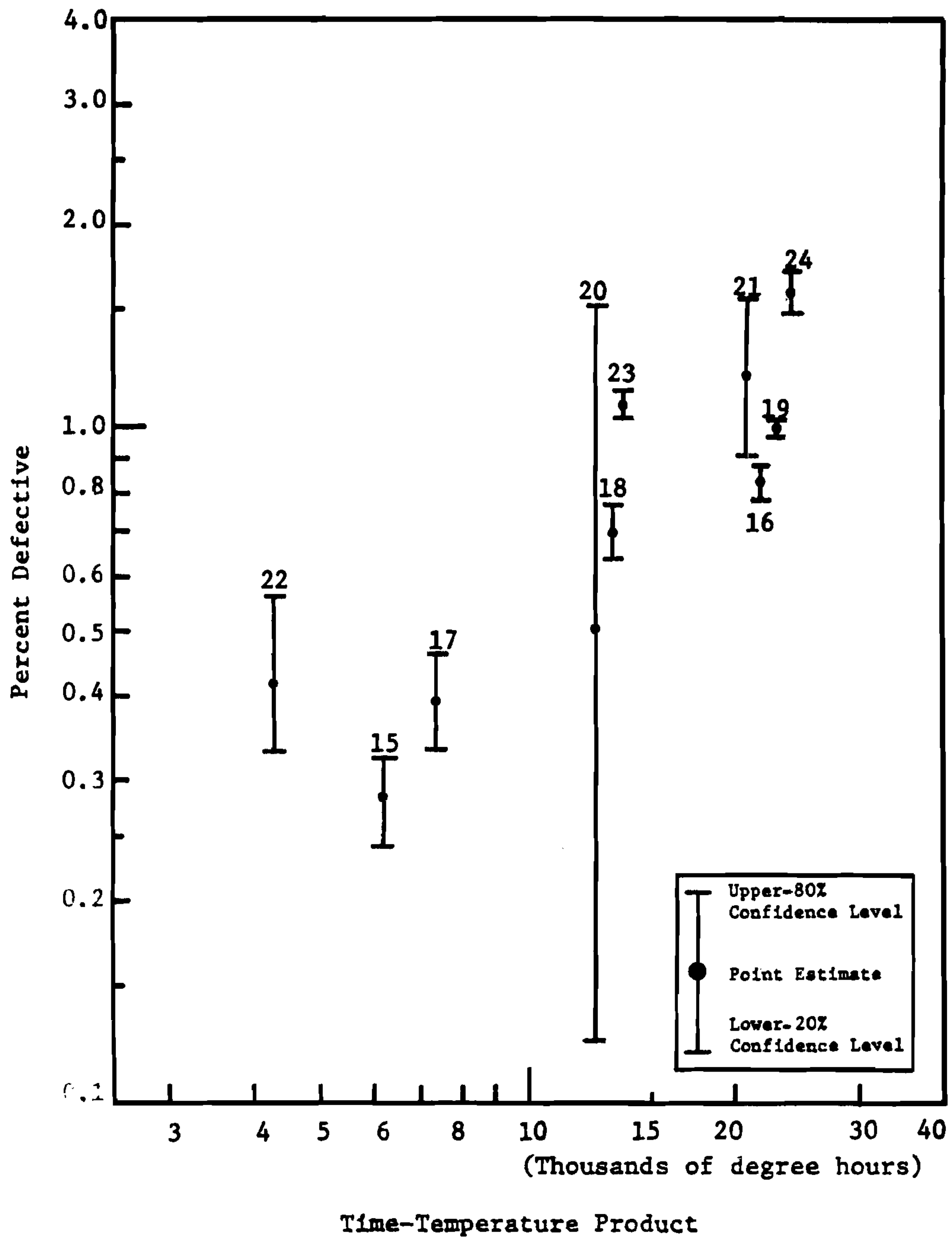


Figure 14: Burn-in Results for MOS Devices

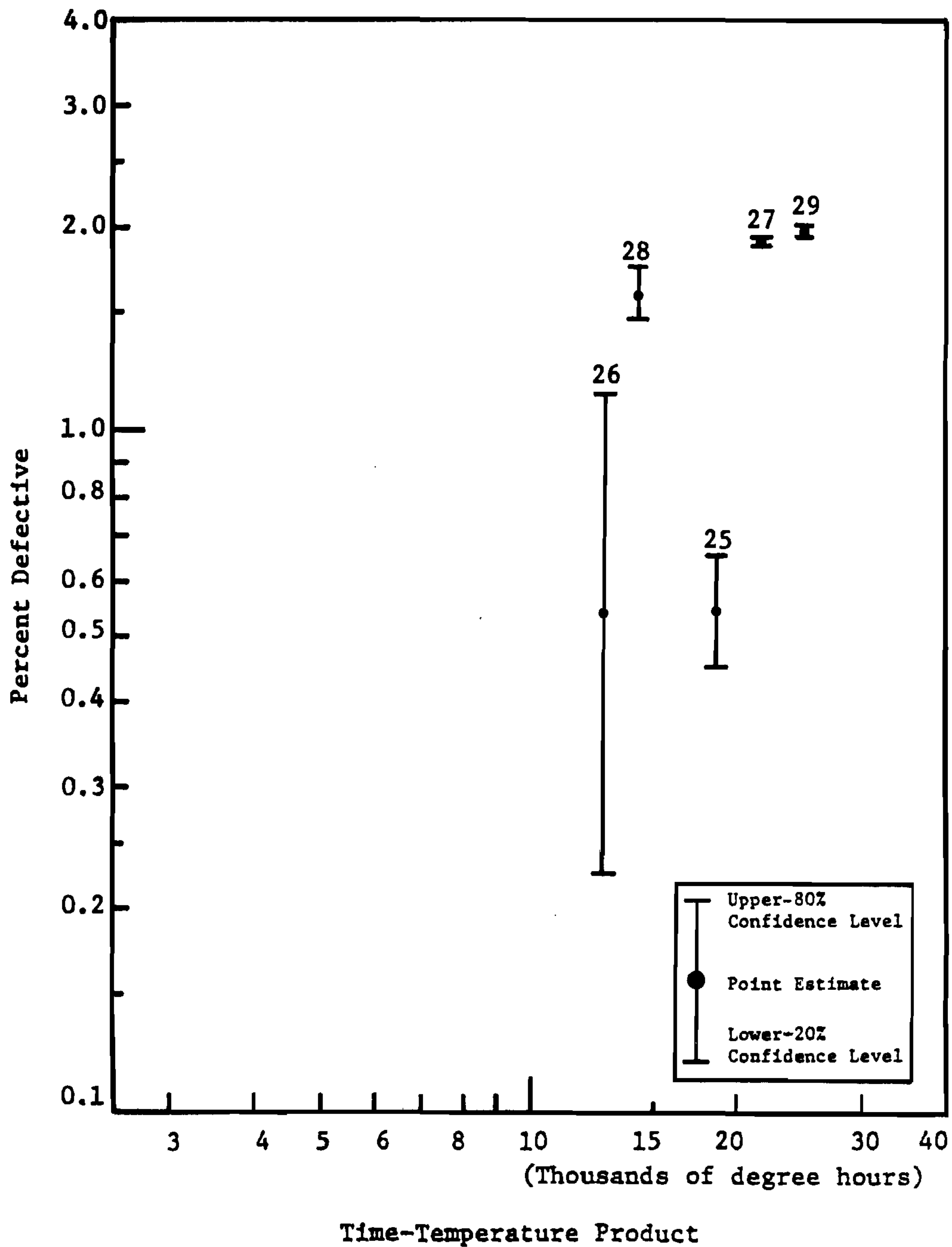


Figure 15: Burn-in Results for Linear Devices

The dynamic burn-in configuration should be employed with all LSI devices. The static configuration provides stress only to the input and output circuitry of complex LSI devices without providing stress to the interior nodes of the circuit.

All burn-in screens should be performed at 125°C. Greater temperatures may well result in increased reject rates. However, caution should be exercised to determine that no new failure mechanisms are introduced as a result of the increased temperature. Temperatures below 125°C do not provide adequate thermal stress to activate most microcircuit failure mechanisms during the typical burn-in duration. An exception to the minimum 125°C burn-in temperature might arise in a dynamic configuration for certain devices where the resulting junction temperature produced would be above the maximum rated value. In these cases the test temperature should be set sufficiently low to allow the operating junction temperature to remain below the rated maximum.

Burn-in duration is probably the most critical of all of the burn-in parameters. For most technologies the burn-in reject rate is greatest during the initial period and will continually decrease throughout the burn-in period. The high initial reject rate may result from the detection of defects which have been activated in previous stresses. A burn-in of less than 48-hour duration does not normally allow activation of thermal failure mechanisms but it is useful in identifying the defects activated in the previous screens.

In most cases the burn-in duration should be dictated by the intended application. Hi-Rel applications require burn-in conditions of a minimum of 168 hours. The failure mode experiences for a given technology or manufacturer may be employed in determining a realistic activation energy and the optimum burn-in duration. When an activation energy cannot be derived, the burn-in duration should be determined according to the warranty commitments.

Figure 16 presents the failure rate curves for 4K NMOS dynamic RAMs, incorporated in computer-type equipments, which had been burned-in for 48 hours and 96 hours at 125°C. One curve represents the reliability of several groups of devices which received only 48-hour dynamic burn-in at 125°C, and the second curve 96-hour dynamic burn-in at 125°C (approximately 8000 devices per group). Even though the devices were operated in the same equipments and under identical stress conditions, the 48-hour burn-in group, as compared to the 96-hour burn-in group, initially exhibited a higher failure rate and continued to exhibit a substantially higher failure rate throughout the first 1000 hours of equipment operation. In this case the additional 48 hours of burn-in resulted in a failure rate which was an order of magnitude lower at the end of the first

thousand hours of operation, effectively reducing warranty repair activities.

In most applications, a duration of 96 hours or slightly longer will result in the optimal cost-effective burn-in.

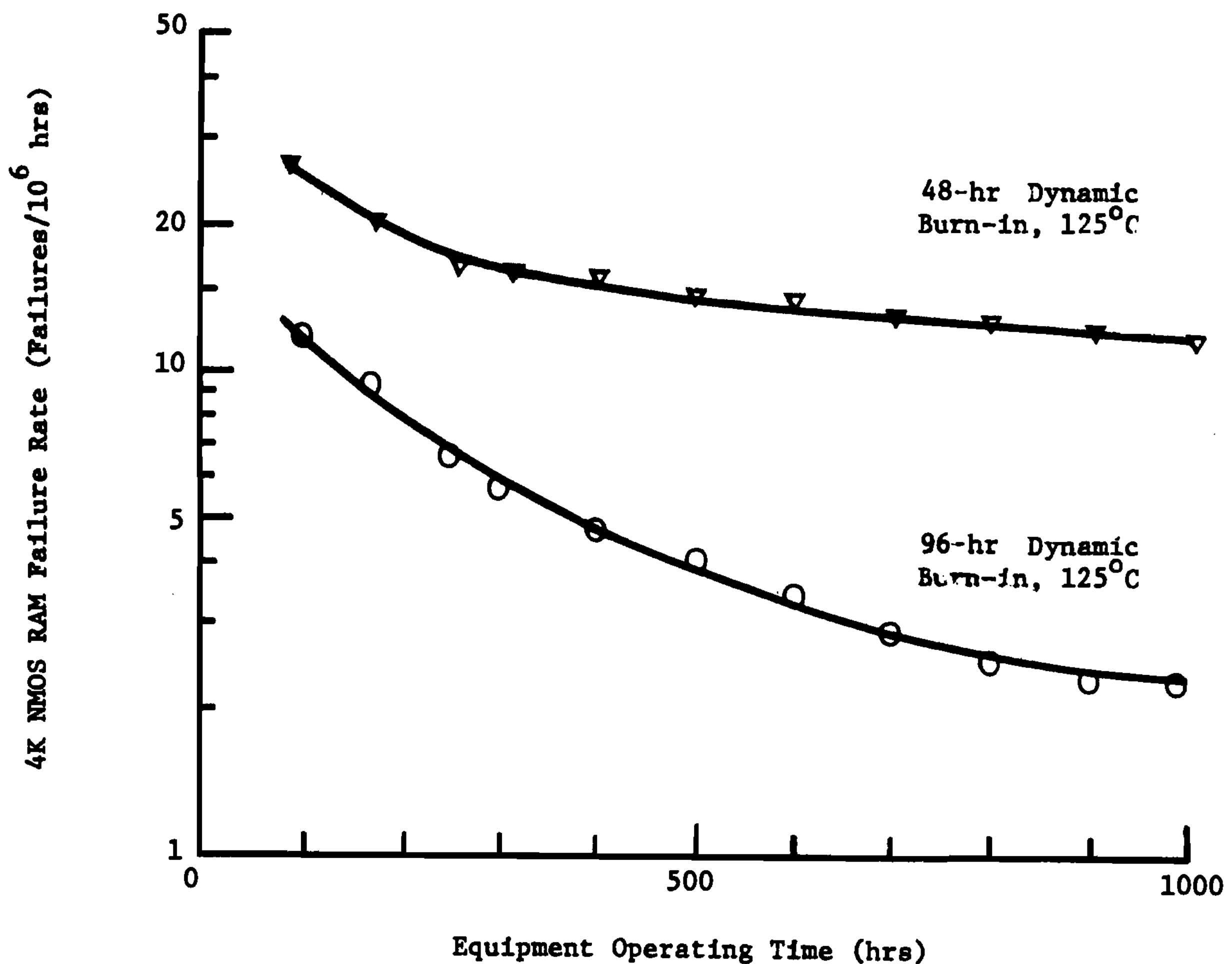


Figure 16: Failure Rates for 4K NMOS RAMs Operating in Equipment, 25° Ambient Temperature

Section 8

SCREENING COST-EFFECTIVENESS MODELING

Where maximum reliability is not essential, the foremost consideration in determining the optimal screening program is the cost-effectiveness or the savings which can be derived from the implementation of such a program.

Savings introduced by screening can be realized in several manners. Removing potential field defects prior to production will reduce field repair costs and equipment down time, and will thereby not only effectively reduce warranty commitment costs, but improve customer relations at the same time. The concept of screening cost-effectiveness can be interpreted, in a somewhat simplified fashion, as: the attempt to justify the initial investment in screening by considering both the ultimate gains incurred and the screening level at which the maximum investment return is realized.

To properly assess screening cost-effectiveness, a model can be developed based upon actual screening experiences previously summarized in this study. Screening costs will vary as a function of the quantity of devices screened, the level of screening, and the organization performing the screening. Estimates of screen costs per device are presented in Table 16. These values are considered to be representative of average values and are useful in determining program effectiveness. A screening cost-effectiveness model should be flexible enough to allow adjusting the actual costs to accommodate unique circumstances.

Several investigators who have addressed the topic of screening cost-effectiveness have previously suggested that the cost-per-reject is a worthy figure of merit. However, the use of this figure of merit as the sole criteria for evaluating screening cost-effectiveness is difficult to support considering that a screen which is destructive in nature would yield the lowest cost-per-reject figure obtainable. Therefore, the cost-per-reject is obviously inadequate as a sole figure of merit and must be evaluated in conjunction with other criteria to determine realistic cost-effectiveness figures for screening programs.

In order to develop a valid model for evaluating screening cost-effectiveness, it is necessary to consider the factors which will influence the ultimate investment return. For example, if an organization is responsible for the design, production and maintenance, over a fixed-interval warranty period, of a quantity of electronic equipments (the production and material costs are

TABLE 16: ESTIMATES OF SCREEN COSTS

DESCRIPTION	APPROXIMATE COST/DEVICE		
	LOW	MEDIUM	HIGH
High-Temperature Bake (24 hrs, 150°C)	0.005	0.0075	0.01
Temperature Cycle (10 cycles, -40°C to 125°C)	0.01	0.015	0.02
Thermal Shock (10 cycles, 0°C to 100°C liquid)	0.01	0.014	0.02
Acceleration (30 KG's, Y1 Axis, 1 min)	0.05	0.11	0.15
Fine & Gross Leak (to 10^{-8} cc/sec)	0.10	0.19	0.25
Radiographic	0.10	0.16	0.20
Visual Exam	0.02	0.03	0.04
Dynamic Burn-in (125°C)	0.08	0.16	0.20
HTRB Burn-in (125°C, 168 hrs)	0.06	0.10	0.15
Continuity (100°C, opens & shorts)	0.02	0.04	0.05
Electrical Test (functional, dc parameters, @ ambient)			
SSI/MSI	0.02	0.035	0.05
LSI	0.05	0.18	0.30

essentially fixed and will not be considered in this analysis), the factors which will have the most obvious impact upon the overall equipment cost are the repair and warranty considerations.

Equipment repairs can be categorized into two major classifications: board/equipment level in-plant repairs and equipment field repairs. Obviously, any repair action in either category adds to the total equipment cost and reduces the overall profit. Therefore, it is desirable to decrease the number of repair actions to reduce the maintenance costs.

A reduction in the number of warranty repairs can be realized by utilizing strict derating guidelines during the equipment design phase or by incorporating higher-quality devices in the equipments. The use of derating guidelines in the design of the equipment assures that all components will be operated well within the recommended stress limits. This technique will reduce the probability of equipment-induced failures and will allow the components to realize the full extent of their inherent reliability.

Assuming that the proper derating guidelines have been employed during the equipment design, the principal factor limiting the ultimate equipment reliability will be the component quality level.

An improvement in component quality can be obtained by adopting a rigorous screening program. Although a screening program does not actually improve device reliability, it is an effective technique for identifying and eliminating anomalous devices within a given population, and will thereby improve the reliability of that population. If unscreened microcircuit devices were incorporated into an equipment, failures would occur during both production testing and the field warranty period. Obviously, there are costs associated with the repair activities both in-house and in the field which should be minimized to realize the best economic benefits. Device screening effectively reduces the number of board and equipment level repairs by removing anomalous devices prior to their incorporation into equipments.

To evaluate the reliability improvement which is actually derived from a screening program, it is necessary to determine the number of potential device failures (those actually removed from a device population prior to being incorporated into the equipment) which would necessitate warranty repairs. This information, when combined with screening and repair cost information, would form the basis for evaluating screening cost-effectiveness.

To understand how economic benefits are derived from screening programs, consider the following grossly simplified mathematical expressions:

The total screening cost (S) is:

$$S = C \times N \qquad (1)$$

where:

C - Screening costs per device (represents combined costs of all screens/tests performed in the sequence; refer to Table 16)

N - Total number of devices

The total maintenance cost savings (M) is given by:

$$M = N \, \Sigma R_i \, \{(DP \times P) + (DF \times F)\} \qquad (2)$$

where:

ΣR_i - Summation of the average reject rates experienced in the various screens. (A combination of both package and technology reject rates obtained from Tables 10 thru 12.)

DP - Percentage of screened defects which would have failed in-plant

DF - Percentage of screened defects which would have failed in the field during warranty

P - Average cost of in-plant repair

F - Average cost of field repair

Therefore the savings can be represented as:

$$\text{Savings} = M - S \qquad (3)$$

where:

M - Total maintenance-cost savings (calculated by Equation 2)

S - Total screening costs (calculated by Equation 1)

Most of the information required to utilize these extremely simplified equations can be found in the various tables in this document. However, the model user must supply certain parameters, including the average costs for in-plant and field repairs, to reflect his particular situation. A survey of the literature indicates that realistic average values would be $15 to $20 for in-plant repair and $100 to $125 for field repair. These values, however, will vary from equipment to equipment and from user to user.

The equations also require information on the relative percent distributions of in-plant and field operation rejects but (unfortunately) before this type of information can be compiled decisions concerning the type of screening program to be employed must be made. It has been determined that up to 60% of the screened rejects would fail during production testing with the remainder failing during field operation. These numbers are based on limited data and may assist in screening program evaluation if better estimates are not available. This distribution will vary, however, according to the screening sequence, the type of production testing, and the length of the warranty period.

When used in conjunction with the screening data summarized in this report, the equations presented here can be instrumental in the assessment and comparative analysis of various screening programs. Moreover, the costs and savings connected to these screening programs, and the achievable reliabilities the programs may ultimately produce, can be determined by employing the information presented in this report. An example of such an analysis follows:

Company "A" is employing TTL SSI/MSI devices in Cerdip packages. In the development of their quality program of 10,000 devices they wish to determine the cost-effectiveness of their proposed screening sequence, especially the Final Inspection. The proposed program consists of the following screens and tests, chosen so that the highest efficiences would be realized:

Initial Electrical and Visual Examination
Temperature Cycling
Fine and Gross Leak Tests
HTRB Burn-in
Final Electrical and Continuity Measurements

The expected reject rates and cost-per-device for these screens, as determined from Tables 11, 12 and 16, follow:

	Reject Rate	Cost-per-Device
Initial Inspection	0.54%	0.065
Environmental/Seal Tests	0.37%	0.205
Burn-in	0.23%	0.100
Final Inspection	0.10%	0.075

Based upon a lot size of 10,000 TTL SSI/MSI devices, the economics of performing all screens and tests in the proposed sequence will be determined as follows:

Total screening costs: $S = C \times N$

$C = 0.065 + 0.205 + 0.100 + 0.075 = \$0.445$ per device

$N = 10{,}000$ devices

$S = \$4450$

Total maintenance cost savings: $M = N\Sigma R_i \{(DP \times P) + (DF \times F)\}$

$N = 10{,}000$ devices

ΣR_i = Summation of screen reject rates

$= 0.54 + 0.37 + 0.23 + 0.10$

$= 1.24\%$

DP = Percentage of screened defects which would have failed in-plant

= 0.60 (assumed, see text)

DF = Percentage of screened defects which would have failed in the field

= 0.40 (assumed, see text)

P = Average cost of in-plant repair

= \$20 per pair

F = Average cost of field repair

= \$125 per repair

$M = (10{,}000)\ (0.0124)\ \{(0.60)\ (20) + (0.40)\ (125)\}$

$= \$7688$

Savings = M - S

= 7683 - 4450

Savings = \$3238

This calculation shows that by subjecting the 10,000 TTL SSI/MSI devices to the entire proposed screening program a maintenance cost savings of \$3238 would be realized, as compared to the maintenance costs which would be incurred if the integrated circuits were used without any screening or testing.

The cost-effectiveness of the final inspection can be determined through the same calculations by leaving out the final inspection.

Total Screening Costs: $S = C \times N$

$C = 0.065 + 0.205 + 0.100 = \$0.370$

$N = 10{,}000$ devices

$S = \$3700$

$M = N\Sigma R_i \{(DP \times P) + (DF \times F)\}$

$N = 10{,}000$ devices

$\Sigma R_i = 0.54 + 0.37 + 0.23$

$\Sigma R_i = 1.14\%$

$DP = 0.60$

$DF = 0.40$

$P = \$20$ per repair

$F = \$125$ per repair

$M = (10{,}000)\ (0.0114)\ \{(0.60)\ (20) + (0.40)\ (125)\}$

$M = \$7068$

$\text{Savings} = M - S$

$= \$7068 - 3700$

$\text{Savings} = \$3368$

As can be seen from this calculation, the savings realized by screening the 10,000 integrated circuits to the proposed screening program, without the final inspection, are $130 greater than the savings realized in screening the integrated circuits to the entire proposed screening sequence. It could be therefore concluded for this example that, based upon the foregoing analysis, the inclusion of the final inspection in the screening sequence for 10,000 TTL SSI/MSI devices in Cerdip packages is not cost-effective and should be deleted from the screening sequence.

Similar analyses can be performed by utilizing these cost-effectiveness equations and the tabulated information presented in this report.

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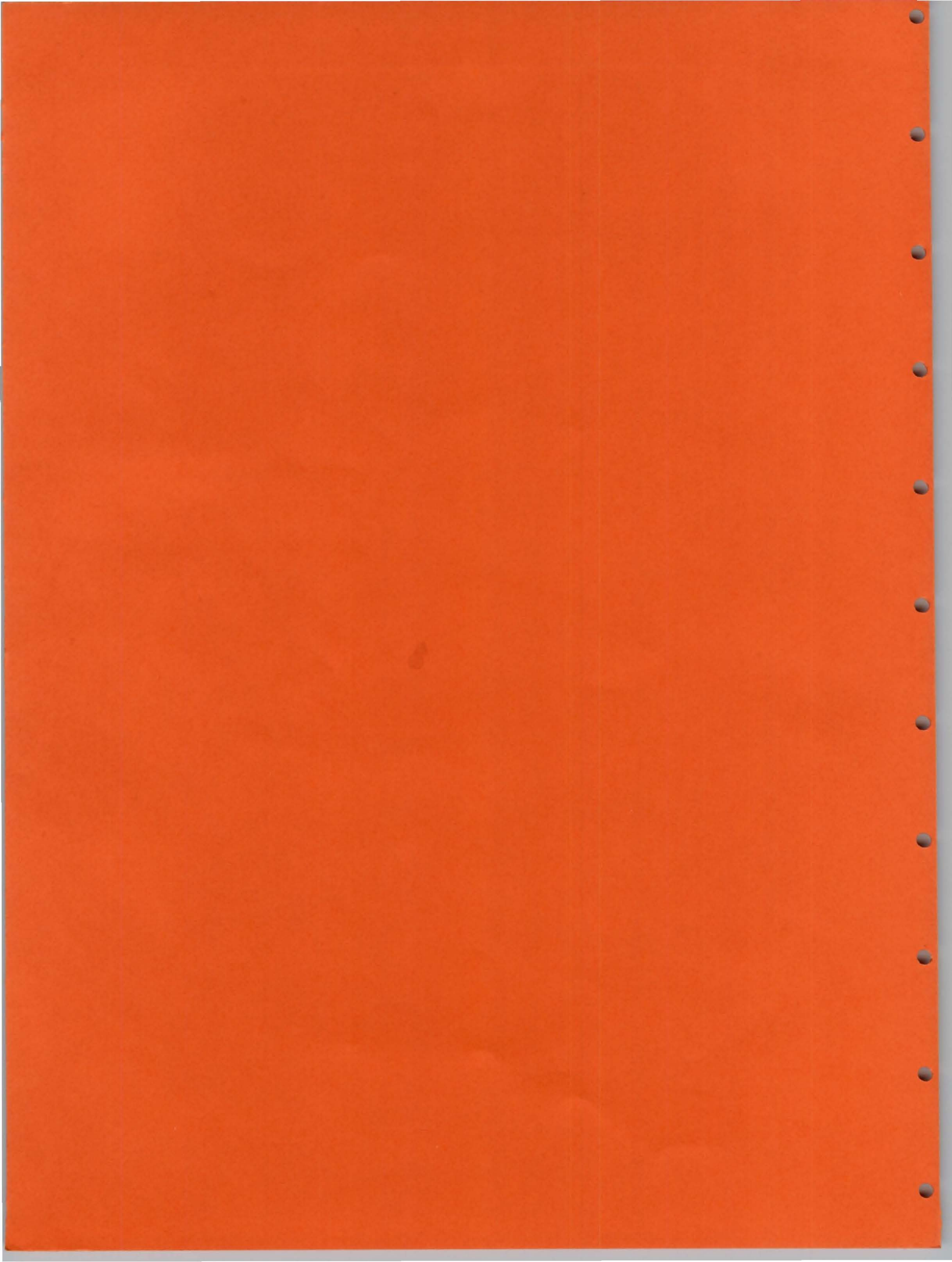
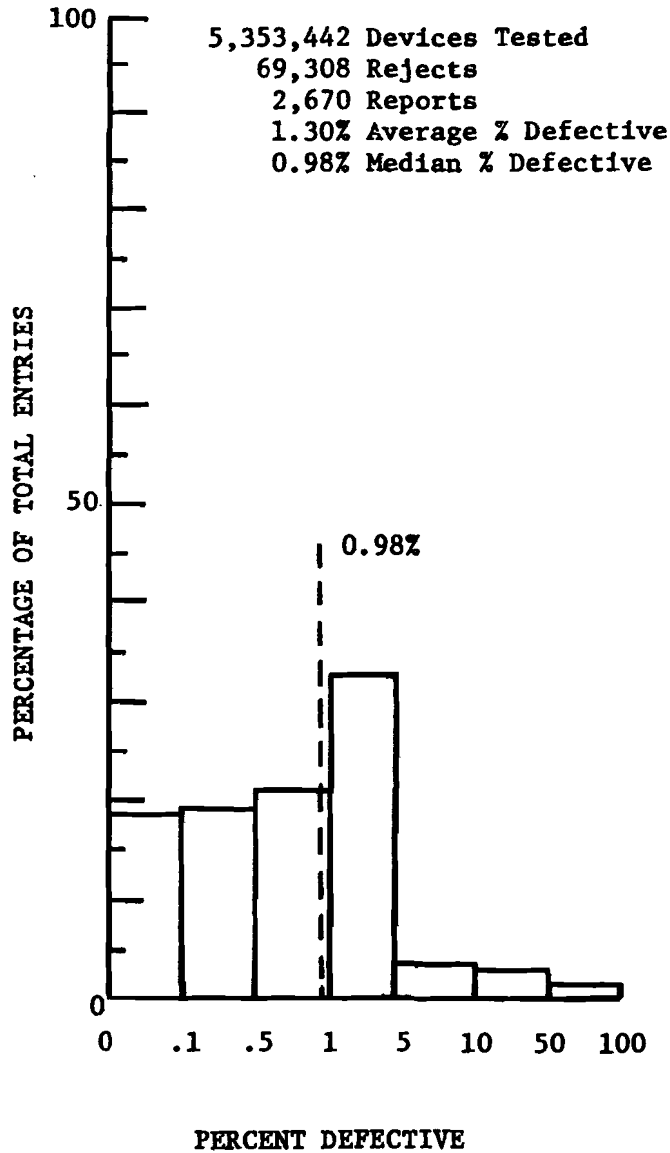
APPENDIXES



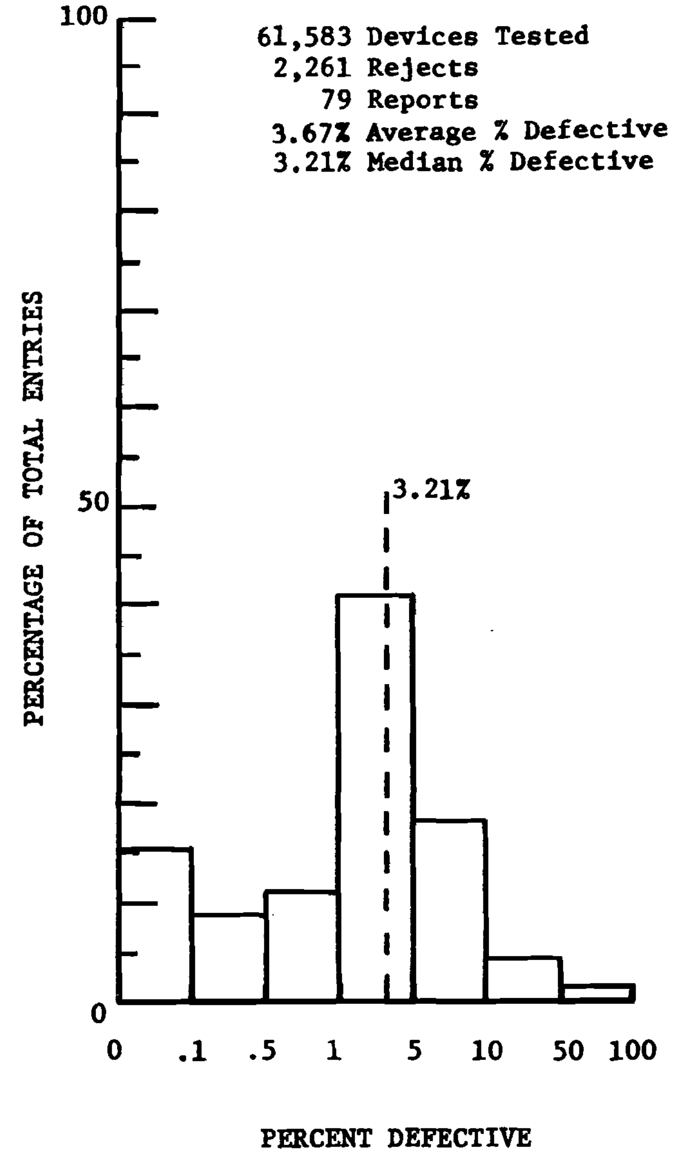
Appendix A

SCREENING REJECT RATE DISTRIBUTIONS

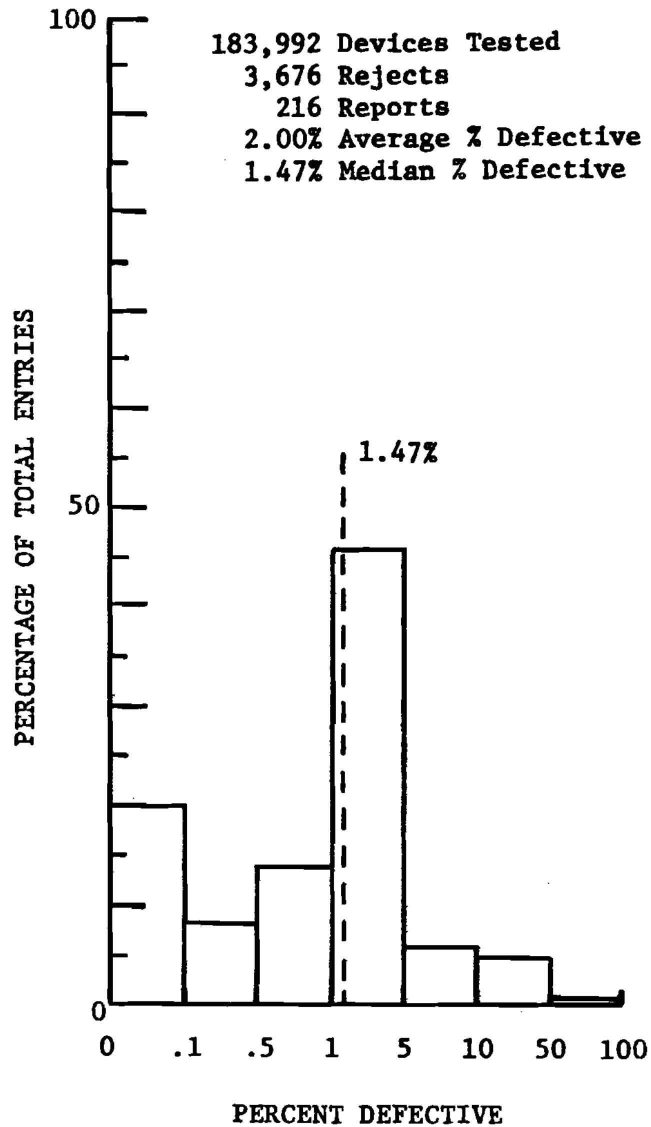
The graphs presented in this appendix illustrate the distributions of average reject rates experienced for various devices subjected to a screen consisting of initial inspection, environmental screen, burn-in and final inspection. Data on devices of 1975-or-later vintage were considered so that the graphs would reflect the current reliability characteristics of the various device types. The data presented here were obtained from device users and independent test facilities only.

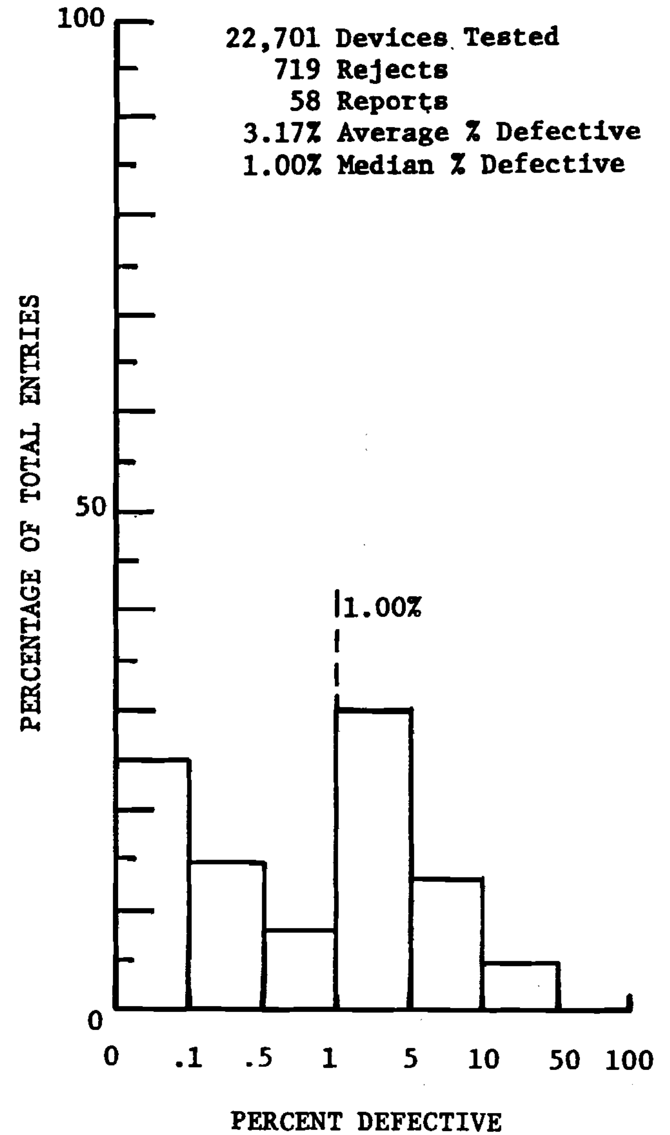


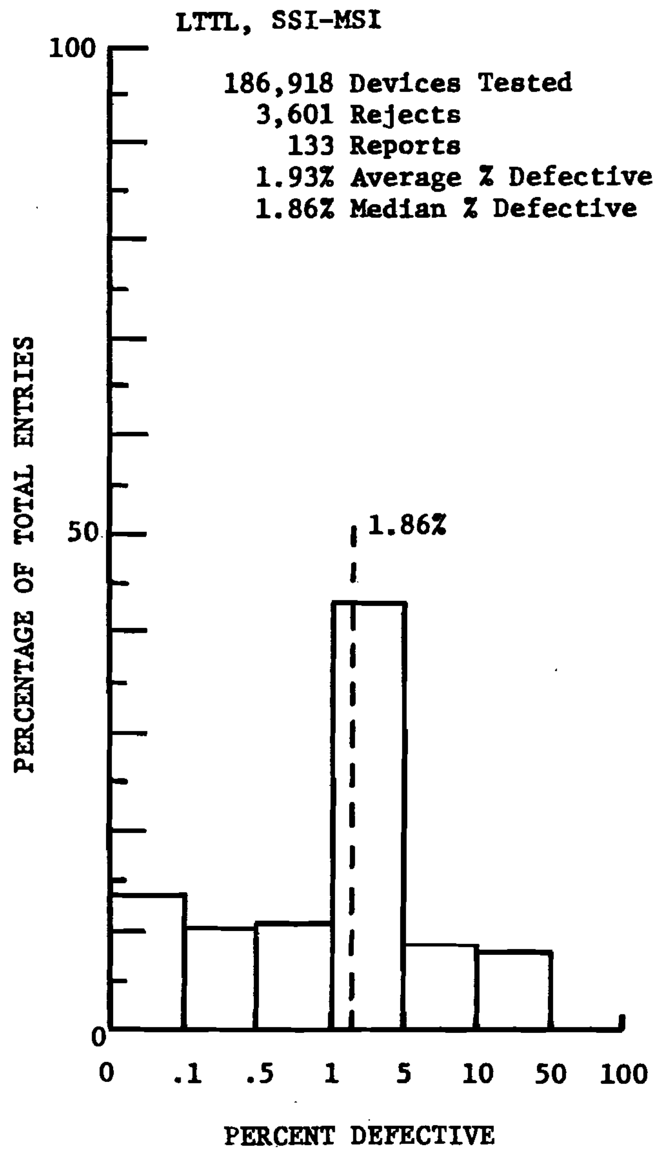
TTL, SSI-MSI
5,353,442 Devices Tested
69,308 Rejects
2,670 Reports
1.30% Average % Defective
0.98% Median % Defective
100
50
0
0.98%
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE



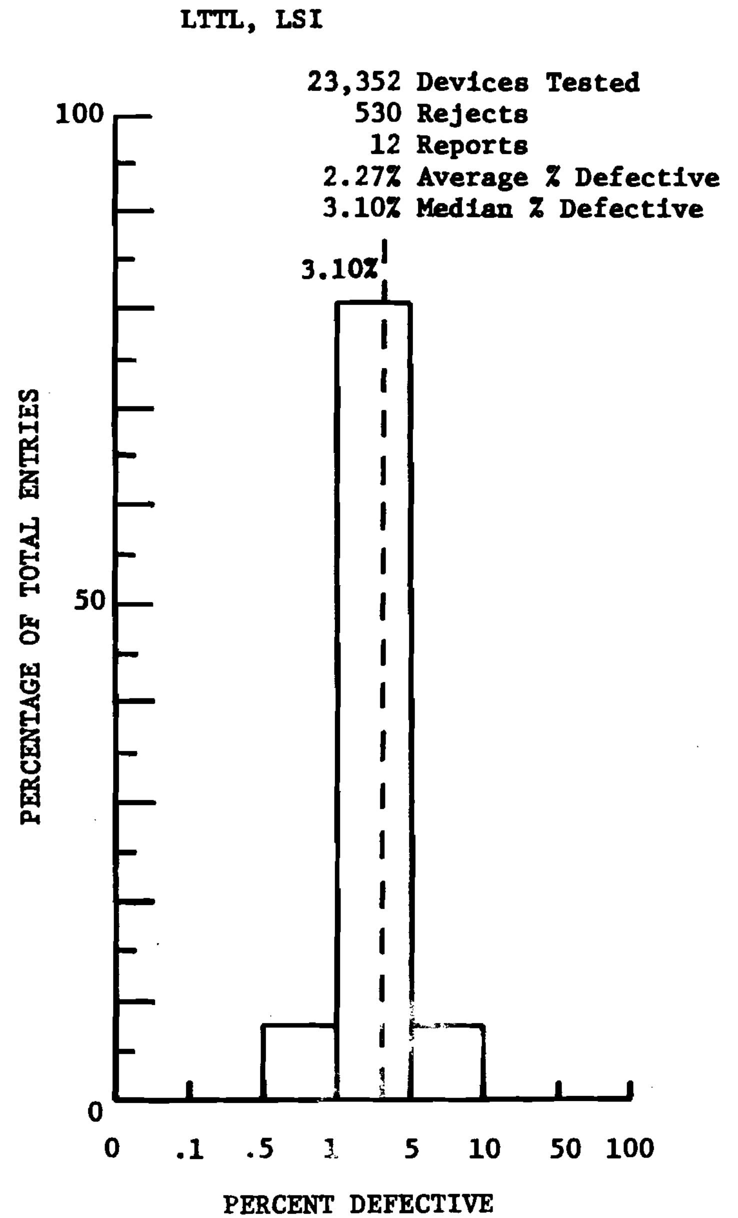
TTL, LSI
61,583 Devices Tested
2,261 Rejects
79 Reports
3.67% Average % Defective
3.21% Median % Defective
100
50
0
3.21%
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE


STTL, SSI-MSI
183,992 Devices Tested
3,676 Rejects
216 Reports
2.00% Average % Defective
1.47% Median % Defective
1.47%
100
50
0
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

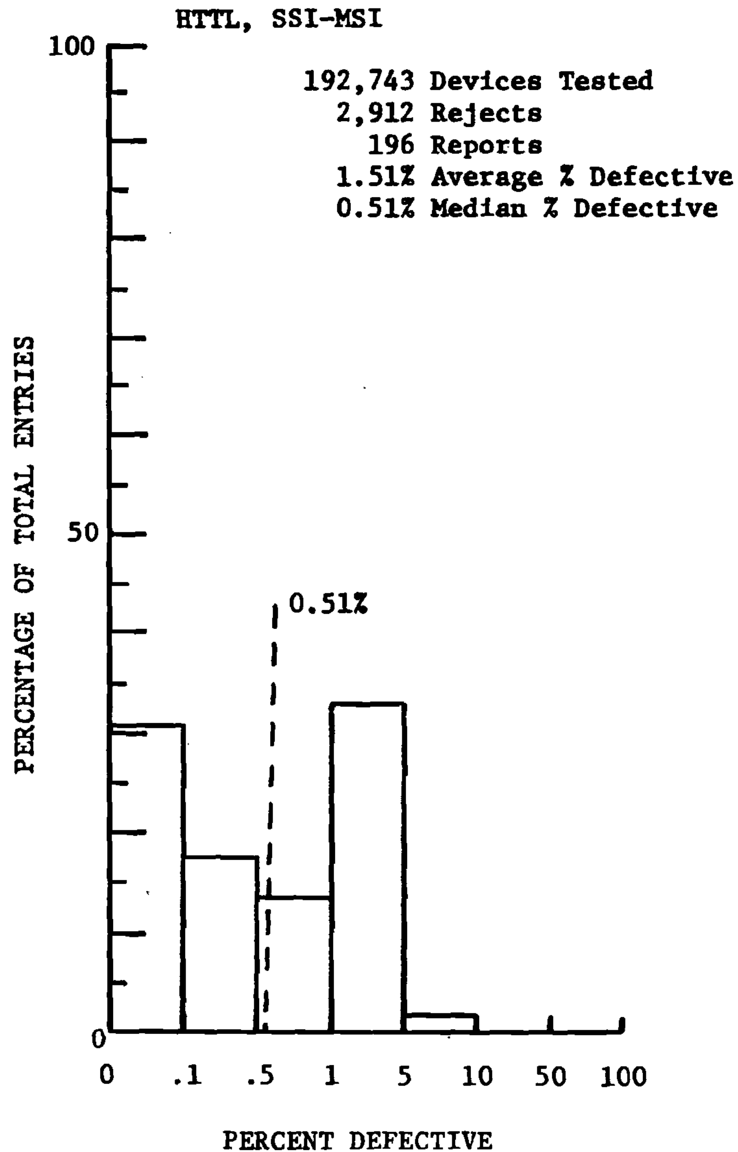

STTL, LSI
22,701 Devices Tested
719 Rejects
58 Reports
3.17% Average % Defective
1.00% Median % Defective
1.00%
100
50
0
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

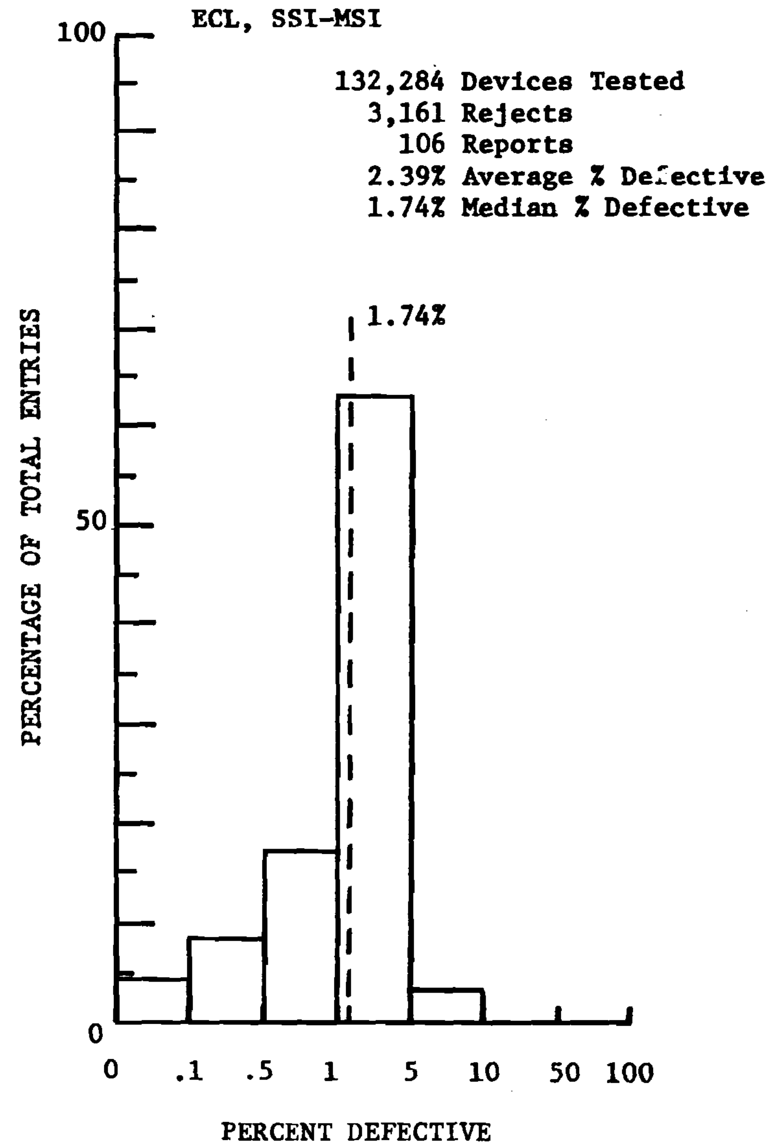


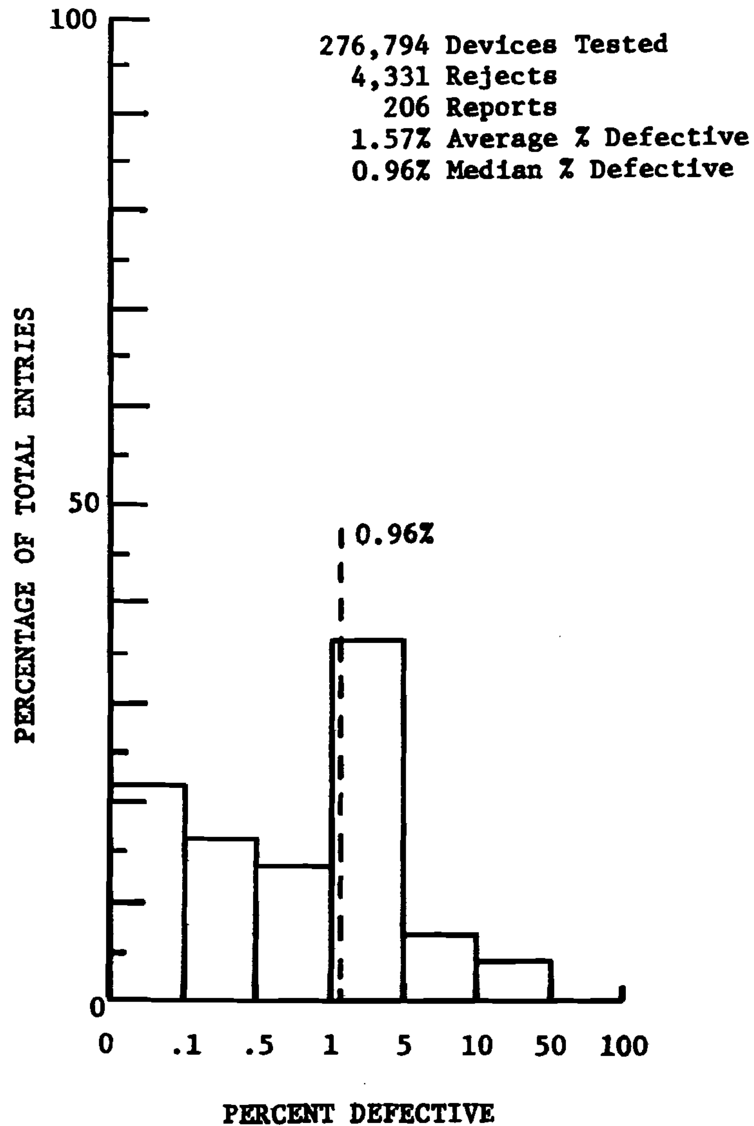
LTTL, SSI-MSI
186,918 Devices Tested
3,601 Rejects
133 Reports
1.93% Average % Defective
1.86% Median % Defective
1.86%
100
50
0
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

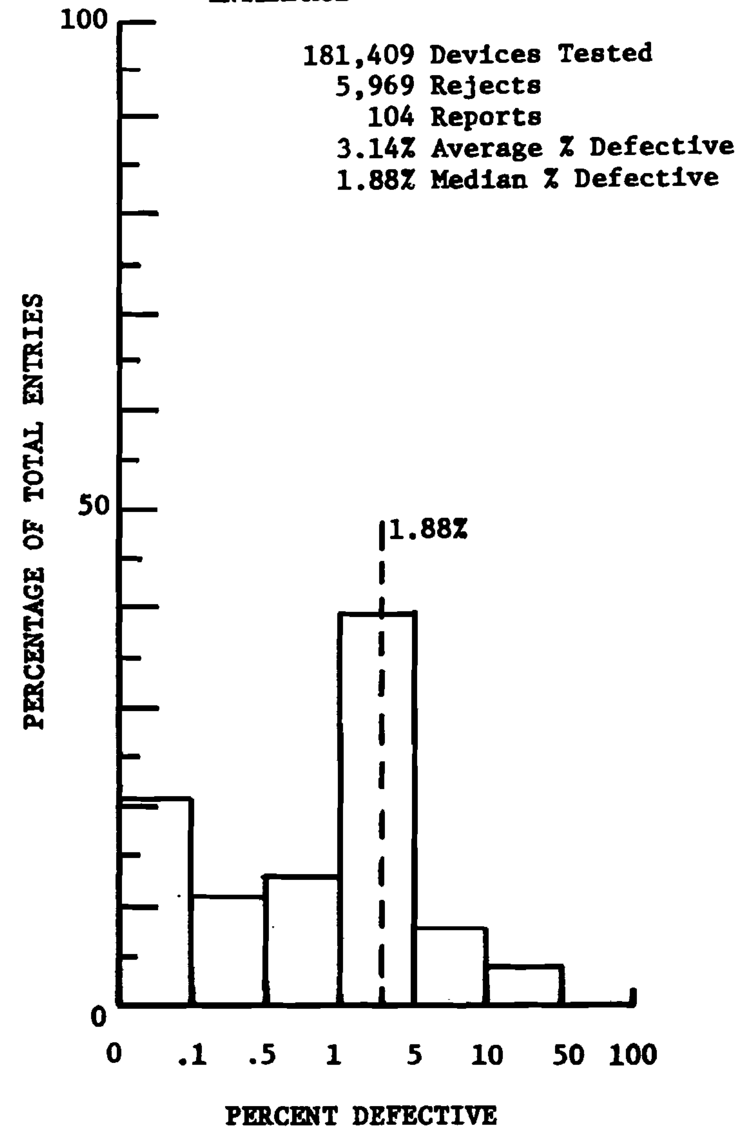


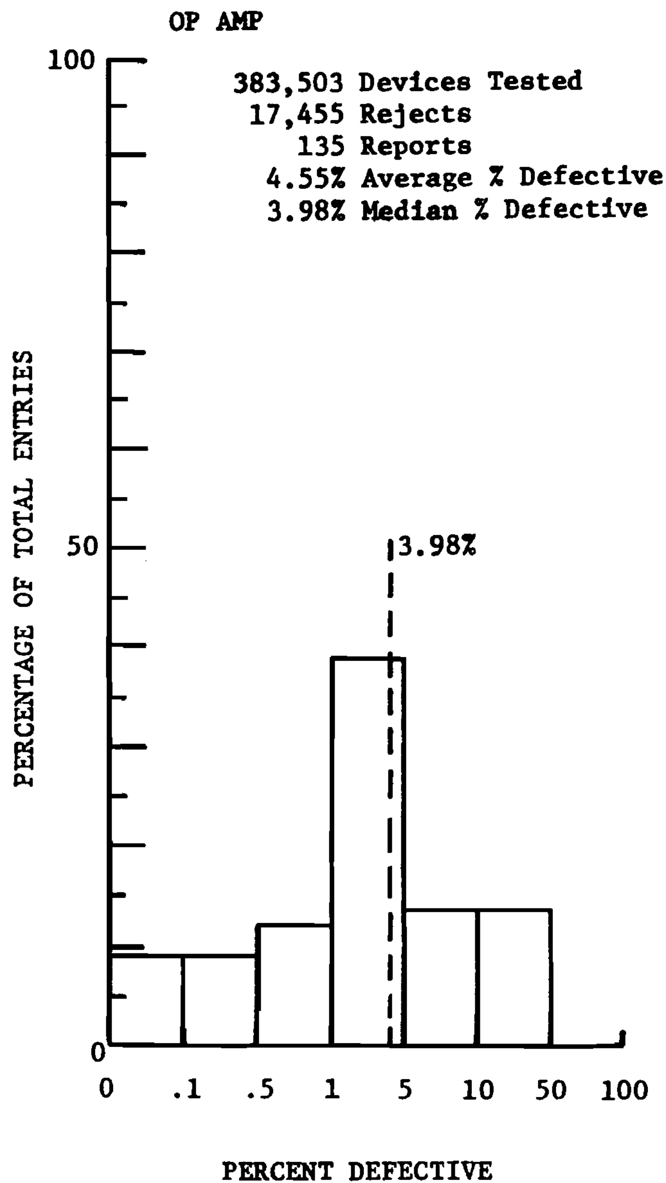
LTTL, LSI
23,352 Devices Tested
530 Rejects
12 Reports
2.27% Average % Defective
3.10% Median % Defective
3.10%
100
50
0
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

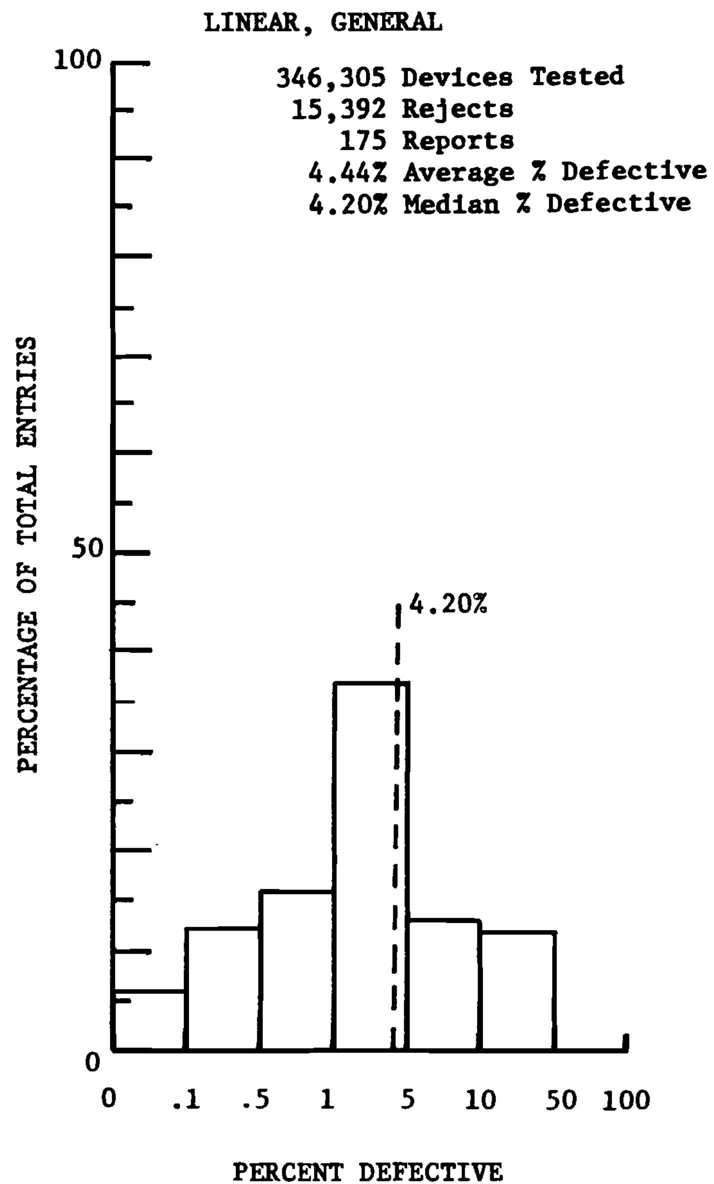

HTTL, SSI-MSI
192,743 Devices Tested
2,912 Rejects
196 Reports
1.51% Average % Defective
0.51% Median % Defective
0.51%
100
50
0
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

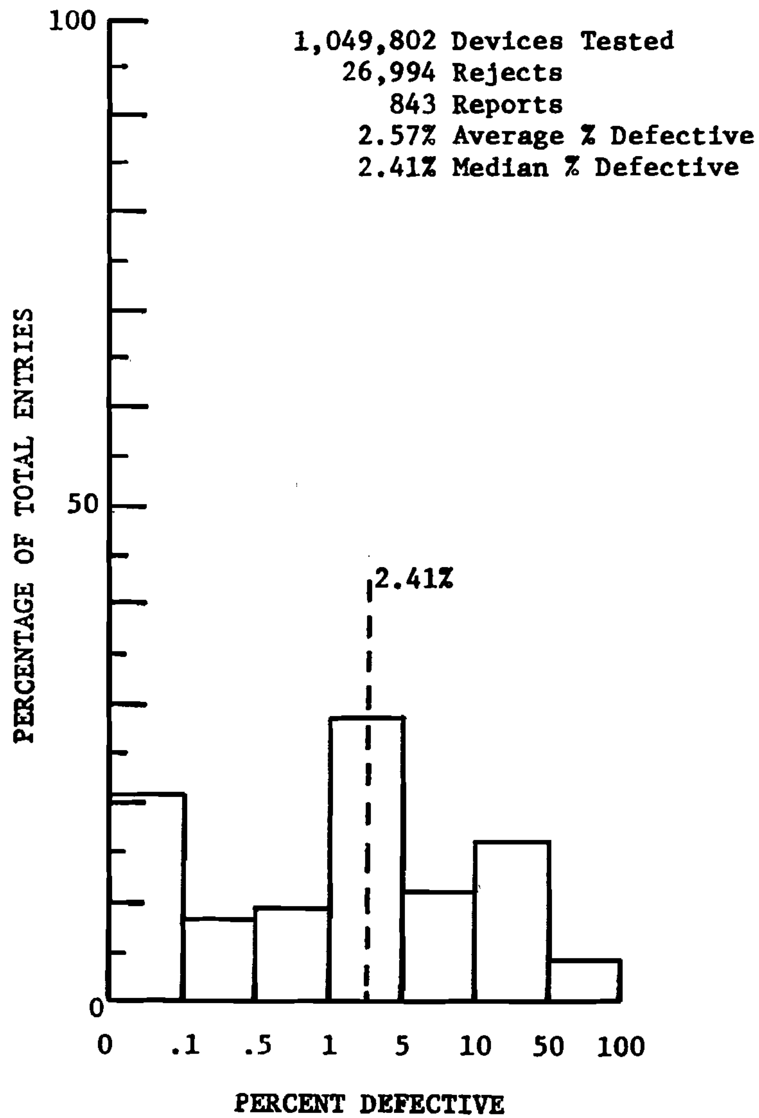

ECL, SSI-MSI
132,284 Devices Tested
3,161 Rejects
106 Reports
2.39% Average % Defective
1.74% Median % Defective
1.74%
100
50
0
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

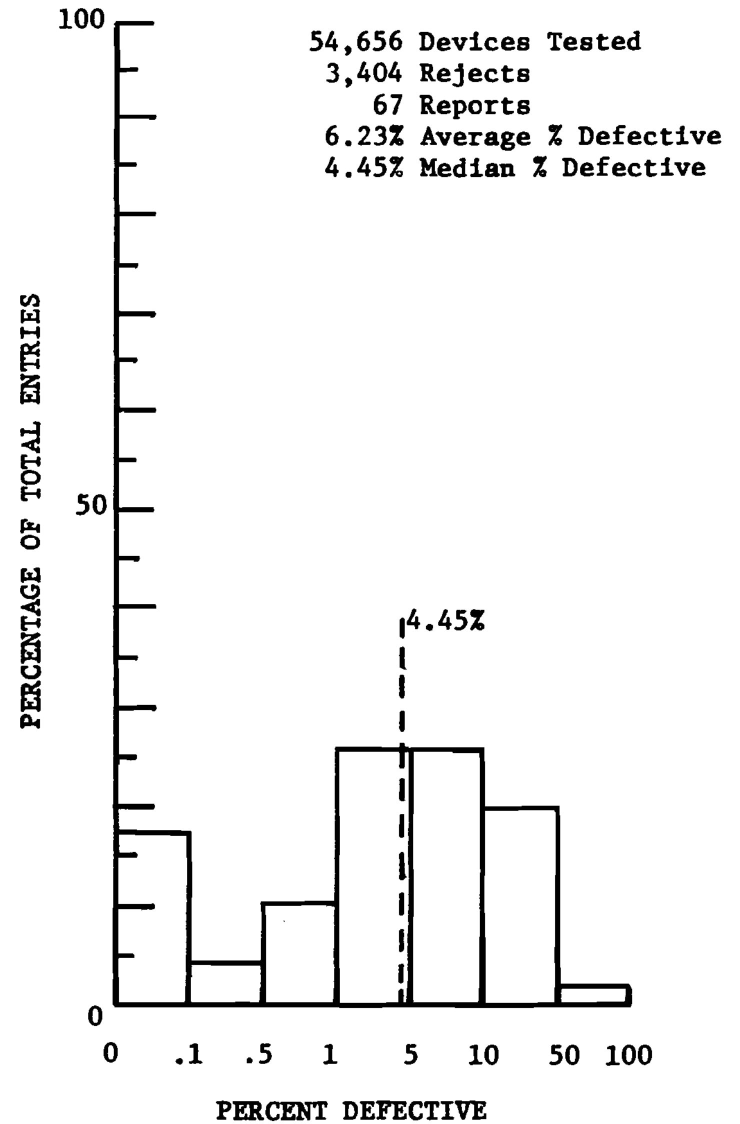

LSTTL, SSI-MSI
276,794 Devices Tested
4,331 Rejects
206 Reports
1.57% Average % Defective
0.96% Median % Defective
0.96%
PERCENTAGE OF TOTAL ENTRIES
100
50
0
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

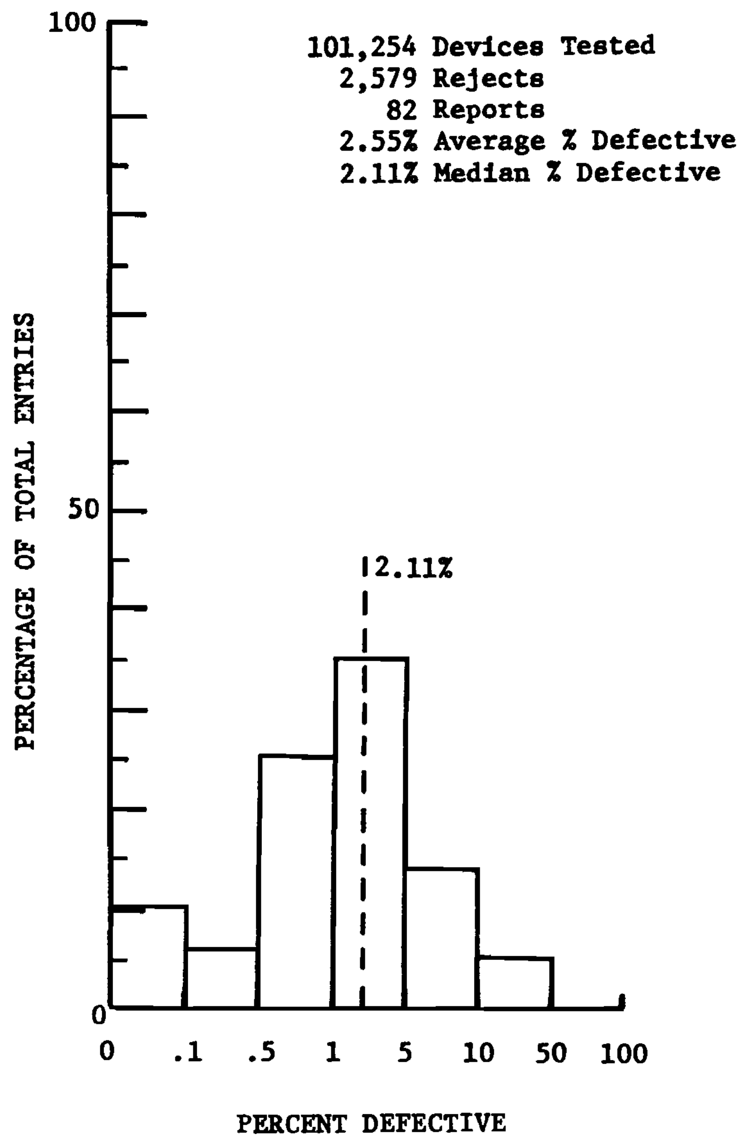

INTERFACE
181,409 Devices Tested
5,969 Rejects
104 Reports
3.14% Average % Defective
1.88% Median % Defective
1.88%
PERCENTAGE OF TOTAL ENTRIES
100
50
0
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

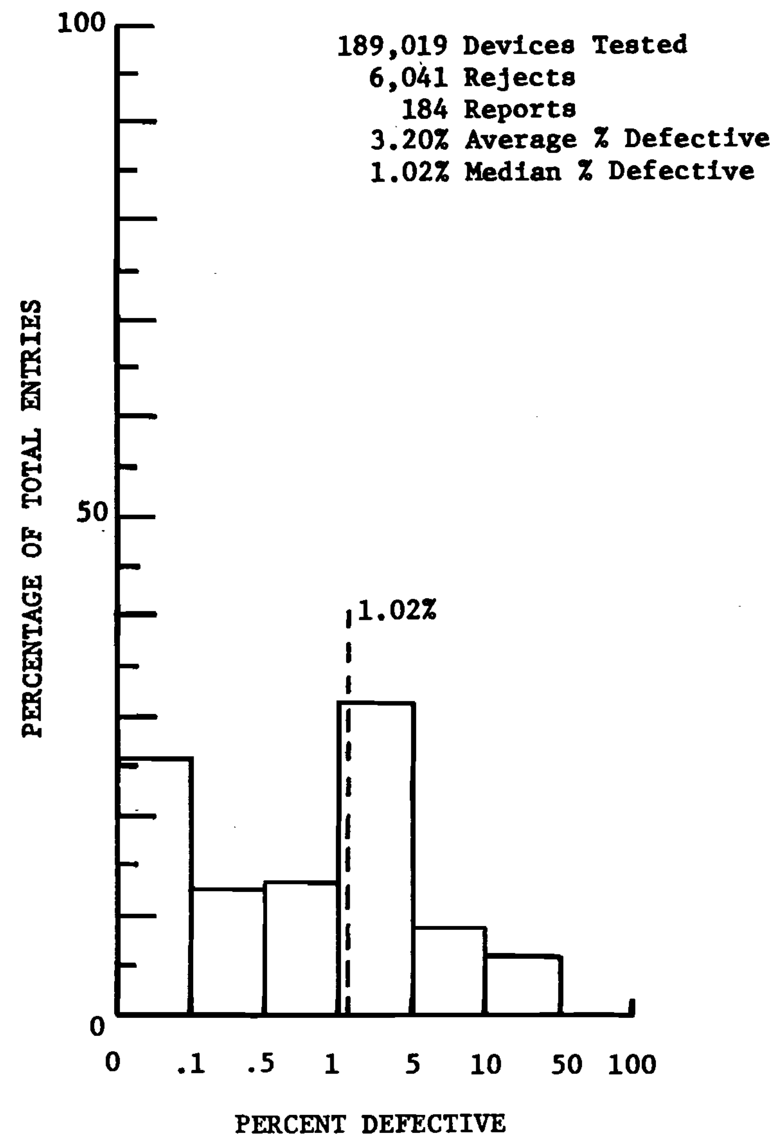

OP AMP
383,503 Devices Tested
17,455 Rejects
135 Reports
4.55% Average % Defective
3.98% Median % Defective
3.98%
PERCENTAGE OF TOTAL ENTRIES
100
50
0
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

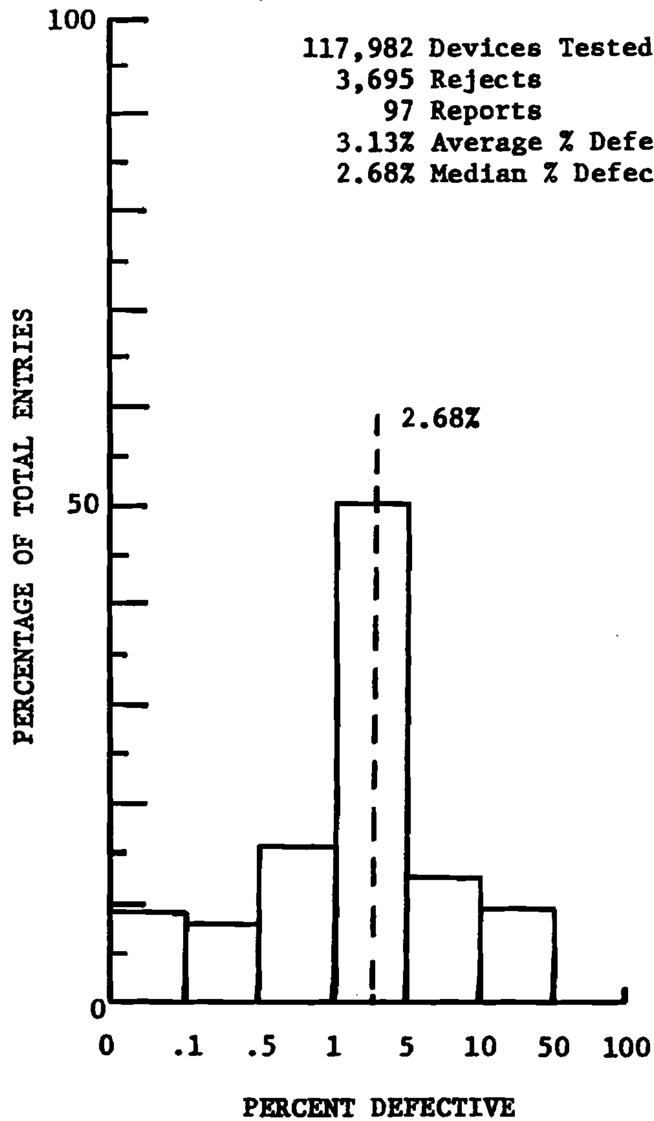

LINEAR, GENERAL
346,305 Devices Tested
15,392 Rejects
175 Reports
4.44% Average % Defective
4.20% Median % Defective
4.20%
PERCENTAGE OF TOTAL ENTRIES
100
50
0
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE


CMOS, SSI-MSI
1,049,802 Devices Tested
26,994 Rejects
843 Reports
2.57% Average % Defective
2.41% Median % Defective
100
50
0
PERCENTAGE OF TOTAL ENTRIES
2.41%
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE


CMOS, LSI
54,656 Devices Tested
3,404 Rejects
67 Reports
6.23% Average % Defective
4.45% Median % Defective
100
50
0
PERCENTAGE OF TOTAL ENTRIES
4.45%
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE


PMOS, SSI-MSI
101,254 Devices Tested
2,579 Rejects
82 Reports
2.55% Average % Defective
2.11% Median % Defective
2.11%
PERCENTAGE OF TOTAL ENTRIES
100
50
0
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE


PMOS, LSI
189,019 Devices Tested
6,041 Rejects
184 Reports
3.20% Average % Defective
1.02% Median % Defective
1.02%
PERCENTAGE OF TOTAL ENTRIES
100
50
0
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE


NMOS, LSI
117,982 Devices Tested
3,695 Rejects
97 Reports
3.13% Average % Defective
2.68% Median % Defective
2.68%
100
50
0
PERCENTAGE OF TOTAL ENTRIES
0
.1
.5
1
5
10
50
100
PERCENT DEFECTIVE

Appendix B

SCREENING DATA SOURCES

All screening data summarized in this report were collected from device users and independent screening labs. Device manufacturers' data were not considered since they would reflect obvious quality biases.

Only information adequately describing all details pertaining to the device technology, package configuration, screening sequence, and stress levels was considered in this study.

All data are of a post-1975 vintage and only lots of 100 devices or greater were considered.

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Appendix C

INDEPENDENT SCREENING LABS

This appendix contains an alphabetical listing of several independent reliability laboratories which offer screening services. Other screening labs may be identified by consulting periodic literature.

INDEPENDENT SCREENING LABS

1. American Electronic Laboratories, Inc.
   P. O. Box 552
   Lansdale, PA 19446

2. Associated Testing Laboratories, Inc.
   23 Vincent Street
   Wayne, NJ 07470

3. Continental Testing Laboratories, Inc.
   763 U. S. Highway 17-92
   Fern Park, FL 32730

4. DCA Reliability Laboratory, Inc.
   975 Benica Ave.
   Sunnyvale, CA 95086 (and other locations)

5. Electronic Test Center
   2200 Walsh Ave.
   Santa Clara, CA 95050 (and other locations)

6. Microelectronic Testing Laboratories
   17312 Gillette Ave.
   Santa Ana, CA 92705 (and other locations)

7. Micro-Test Systems Inc.
   743 Pastoria Ave.
   Sunnyvale, CA 94086

8. Pacific Reliability Corporation
   765 N. Mary Ave.
   Sunnyvale, CA 94086

9. Reliability Inc.
   P. O. Box 37409
   Houston, TX 77039

10. Semiconductor Reliability Laboratories
    1961 Wright Circle
    Anaheim, CA 92806

11. Solid State Testing, Inc.
    56 Middlesex Turnpike
    Burlington, MA 01802 (and other locations)

12. STL Electronics
    2821 Ladybird Lane
    Dallas, TX 75220

INDEPENDENT SCREENING LABS (Cont'd)

13. Stryco Electronics Corp.
    150 Charles Street
    Malden, MA 02148

14. Trio-Tech Testing Laboratory
    1400 Stierlin Road
    Mountin View, CA 94043

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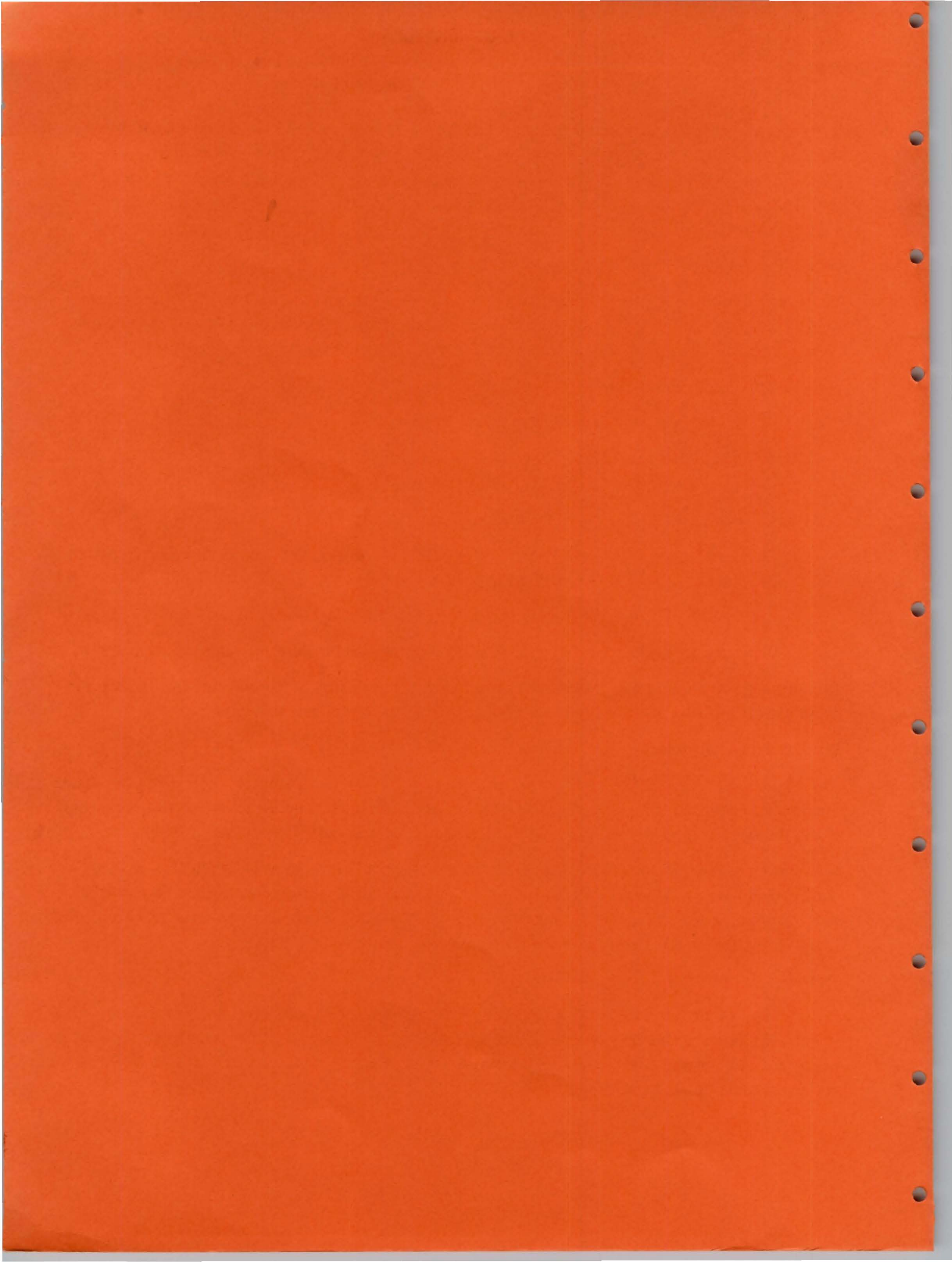

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12. Sponsoring Organization Name and Address Rome Air Development Center Griffiss Air Force Base, NY 13441	13. Type of Report & Period Covered N/A 14.

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Microcircuit Reliability
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Thermal Shock
Burn-in, Microcircuit

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