DEVELOPMENT OF A SOLID-STATE DISPLAY SYSTEM

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FOREWORD

This report presents the results achieved in one of a series of investigations aimed at advancing capabilities and knowledge necessary for the employment of the electroluminescent phenomenon in the generation of displays. The work was performed under Air Force Task 619009, "Advanced Display Generation Techniques," for which Captain B. M. Bertram served as Task Engineer. This task is an element of Project 6190 for which Mr. John H. Kearns serves as Project Engineer.

The objective of the program was to develop an experimental solid state display system utilizing the most advanced solid state logic, control circuitry, and electroluminescent display techniques to provide an extremely flexible display system. The electroluminescent displays were to be packaged in compact forms to provide minimum weight, size and volume.

This report, describing the effort for the Air Force Flight Dynamics Laboratory, Directorate of Laboratories, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio, covers work conducted from March 1967 to February 1968 under Contract F33615-67-C-1541 by ITT Federal Laboratories. The primary investigators were D. R. Howe, A. L. Fisher and P. R. Decker.

This report was submitted by the authors in August 1968.

This report has been reviewed and is approved.

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ABSTRACT

A research and development program to design a reliable and inexpensive solid-state display control and logic circuit integrated with advanced electroluminescent displays capable of withstanding flight test evaluation is described. The basic system displays capable of withstanding flight test evaluation is described. The basic system utilized a diode, resistor, electroluminescent cell integrated array. A control scheme incorporated an x, y switching arrangement with switches capable of operating at 800 volts peak at 400 hz. This array was backed up by integrated circuit logic and memory capabilities to provide a compact and efficient display package. Advanced techniques were employed in fabricating printed circuit boards and the multilayer assembly. A power change-over circuit was developed which permitted operation from 115 volts ac, 400 hz or 28 volts dc. A bar graph type electroluminescent panel, gapless display, was to be used with nine display packages and four numeric panels with five display blocks to make up the system along with a master control matrix.

This abstract has been approved for public release and sale; its distribution is unlimited.

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INTRODUCTION

Solid-state electroluminescent (EL) display systems, suitable for use in aircraft environmental conditions require highly reliable circuits. In addition the control circuits must be relatively inexpensive and applicable to large arrays of elements. Other requirements of individual unit data memory, small in size, gapless display, and manual or automatic intensity control further complicates the fabrication of a usable unit.

The objective of this program was to design, fabricate and package arrays of solid state display control and logic circuitry capable of withstanding flight test evaluation. Each unit utilizes flip-flop memory for continuous display of information derived from parallel entered binary data. Each unit is self contained, compact, has low power dissipation and has a minimum of hard wire input circuits. In addition, all units are common to the control unit output lines.

On a prior contract AF33(615)-3852 a control circuit was developed which was applicable to large arrays and provided high reliability. Since this circuit was a proven development, further investigation of the diode-resistor EL switching circuit was limited to optimizing and selection of components which would permit packaging within the desired space limitations. However, other approaches were not discounted without some consideration.

A major portion of unit and system packaging was devoted to advanced fabrication techniques of a diode-resistor switching matrix and a multilayer printed circuit assembly. Each display unit will function independently and will require only d-c voltages, data and address, inputs, and a clock input. The data/address inputs are used only to update the displayed information.

Input electronics were developed which were capable of accepting parallel binary data inputs, whether time shared or of a continuous nature when addressed to a particular unit. Each unit's self contained memory, permits a continuous display of the latest data entered. Each unit memory is to be reset by the correct address and presence of data or by the reset capabilities of the master control unit.

An identical 160 line EL display unit is used with the bar graph, line graph, and rate field presentations. Thus the primary difference is in the control logic. An XY matrix control is used to minimize the number of discrete components.

The capability of switching input power sources was developed and incorporated in the main control unit. The prime power source is 115 volts ac and 400 hz and the secondary source is 28 volts dc.

Two modes of intensity control for the EL display were developed, and incorporated, manual and automatic. In the automatic mode the EL intensity was directly proportional to the ambient light. In the manual mode the operator has full control from minimum to maximum intensity.

Figure 1 is a photograph of an artist's sketch of the proposed system. The panel on top of the control chassis was intended as a means to secure the bar graph type panels and numeric panels for demonstration purposes. Individual units could be removed and relocated as desired by the means of an extension cable.

Figure 2 is a photograph of the actual control unit with some changes in the front panel layout. The basic control concept remains the same. The main difference is found in the size of the A/D converter/multiplexer which is now located on the logic subchassis.

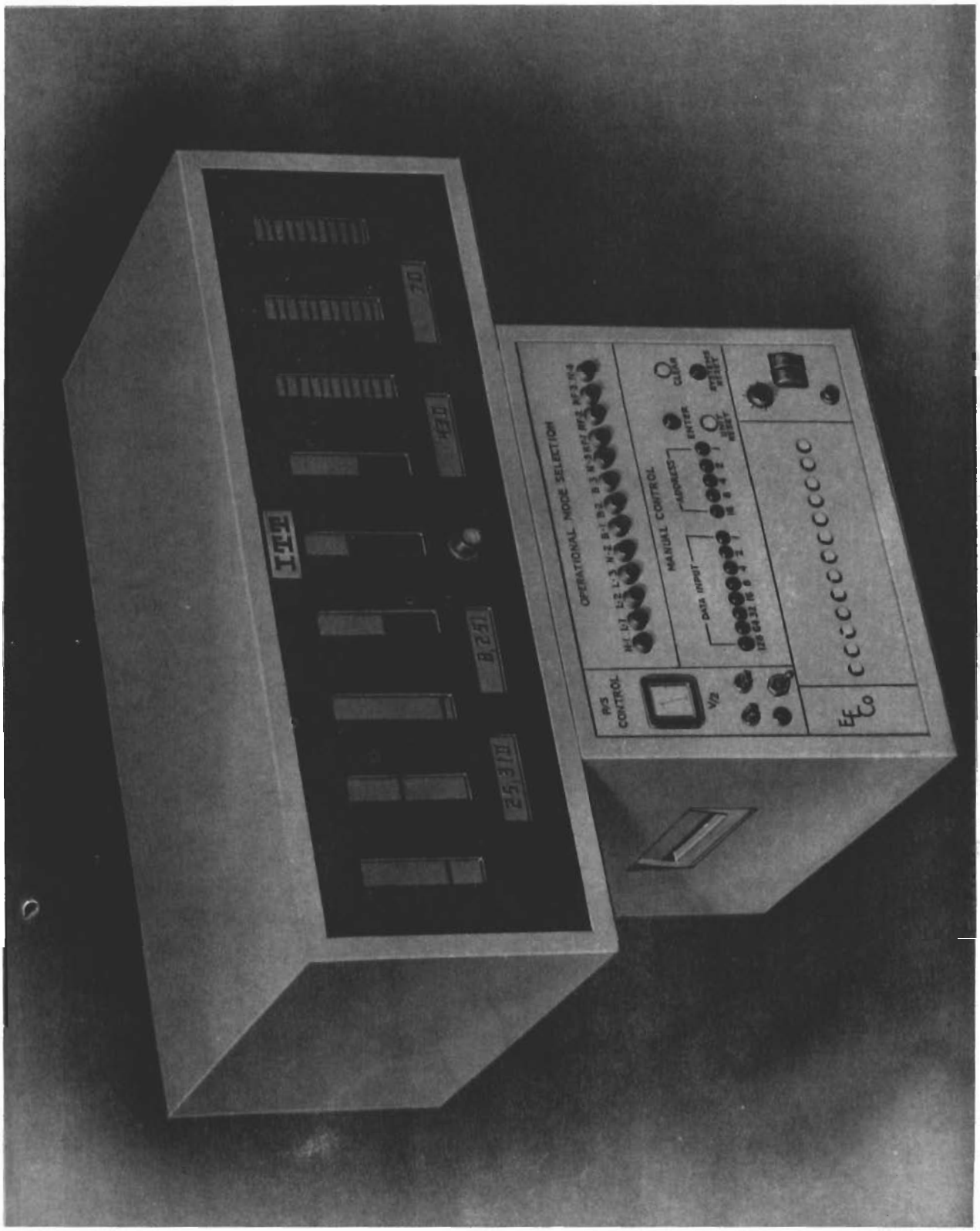


Figure 1 Proposed Display Unit

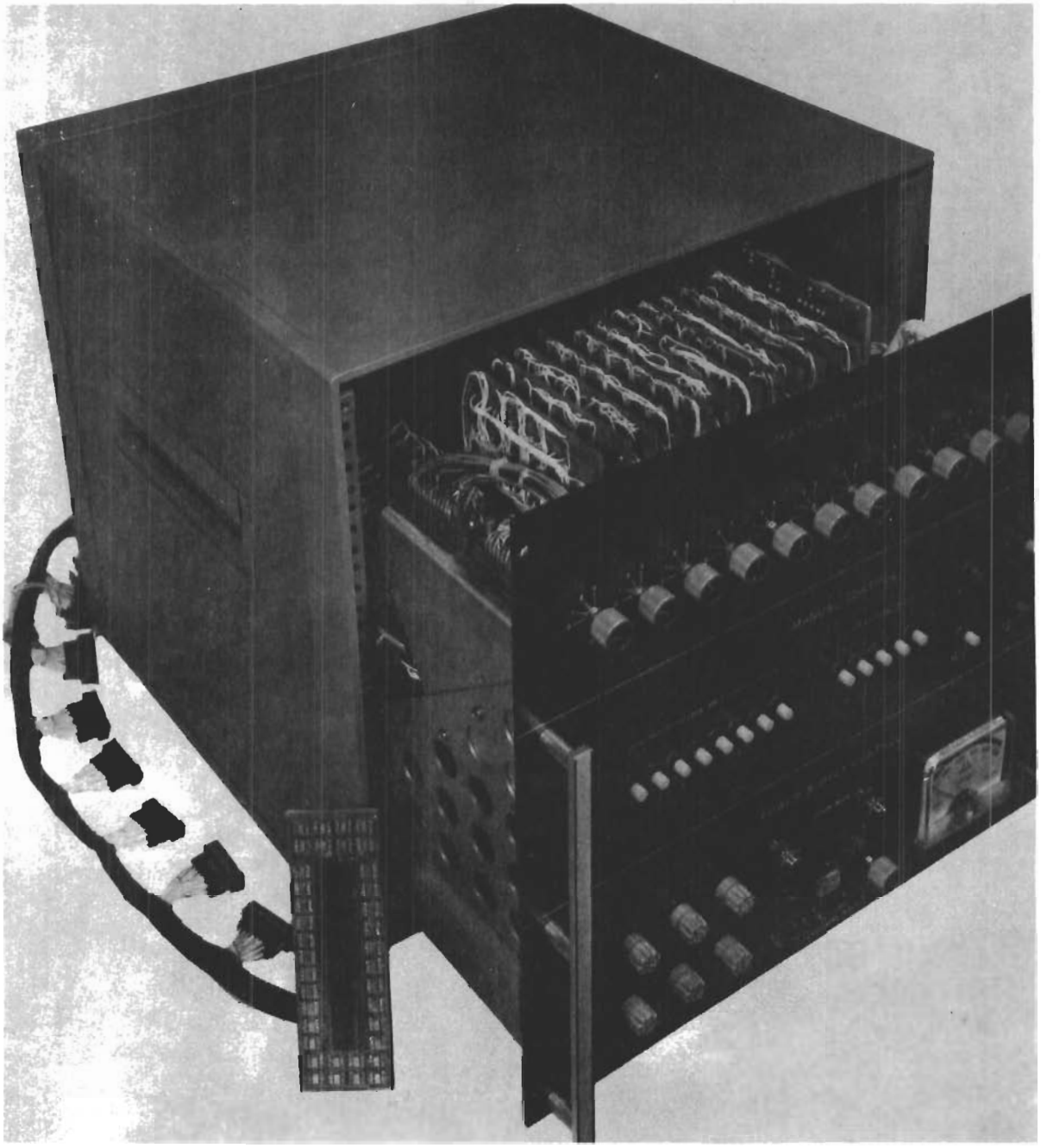


Figure 2 Control Unit

SECTION II

BASIC CONCEPTS

2.1 General

In order to achieve the design objective of developing and fabricating display units capable of withstanding flight test evaluation, certain design constraints were observed.

Only proven components were used in the system. Analog properties of semiconductors, such as switching voltage or leakage currents, are not used to provide circuit functions. Thus temperature sensitivity is minimized and maximum reliability was realized.

The EL element control is based on the use of a diode-resistor and an electroluminescent cell in an integrated array system. This array when backed up by integrated circuit logic and memory, provides compact and efficient display packages which are capable of independent or time-shared operation from common control lines. This approach was chosen because of its applicability to medium size arrays of elements, reliability and small package potential. Knowledge gained in prior research delving into this and other switching techniques, indicated the resistor-diode approach would satisfy the requirement of controlling an EL display.

A basic component for EL element control is a high voltage transistor switch. A minimum requirement of these switches is obtained by using an X and Y matrix approach. Compact integrated circuits are used to control the EL switches and to provide data memory and refresh capability.

The gapless display requires alternate line intensity control which maintains the correct differential throughout the range of over-all display intensity control. Individual lines within an activated area should not be discernible. Two brightness control modes, manual and automatic, were incorporated to provide the desired brightness under varying ambient lighting conditions.

The system will accept data at any speed presented, from computer data bursts at megacycle rates to the occasional updates of slowly changing display data. It will also accept combinations of continuously available analog and continuously available signal information.

The individual display units may be separately controlled and channeled to one of three data sources for display information without interference to or from other units. A four position hard contact switch provides a choice of display unit assignment: OFF, ANALOG DATA, ALWAYS AVAILABLE DATA, and MANUAL DATA.

The individual unit must be impervious to outside interference, yet completely under the operator's control if so desired.

The master control unit will automatically switch input power sources in the event of primary power (115 volts 400 hz) failure.

It had been anticipated that the major problem would not be one of EL element control, rather it would be one of packaging the EL switching control and logic circuits. Therefore, considerable effort was spent searching for smaller components, reliable high voltage switching transistors, improved integrated circuits, deposition of high value resistors, multilayer printed circuitry and reducing the logic to a minimum and yet providing adequate control for the display unit.

2.2 Electroluminescent Element Control

The development of the switching concept employed for this display is presented in report AFFDL-TR-67-169, "Development of Solid State Display Control Circuitry".

Representation of a 3 X 3 matrix is shown in Figure 3. It is noted that in using this technique, a d-c voltage is the power source for the display system.

The refresh rate is fixed at 400 hz and the pulse width nominally 30 μsec. The intensity of the EL panel is controlled by pulse amplitude.

The X and Y switches shown in Figure 3, must be operated in a cyclic manner in order to cause a continuous waveform on the EL segments.

Assuming that in Figure 3, EL 11, EL 22, EL 31, and EL 33 are to emit light, the X and Y switches must function as shown in Figure 4, matrix timing. Thus, the refresh method, shown in Figure 4, is for a line at a time. All elements (with X switches closed) in a horizontal row, are refreshed simultaneously by the Y switch.

The 160 segment (or line) display panel used in this program is now a simple X-Y array as shown in Figure 3. To accomplish the switching technique as if in an X-Y array, a block and line switching method was devised as shown in Figure 5.

Each block has a transparent front electrode and is electrically isolated from the adjacent blocks. Each EL line is an electrically isolated segment on the back of the phosphor. The physical arrangement of a typical bar graph display unit is shown in Figure 6. Techniques which provide the gapless display are not shown. In Figure 6, each EL segment is shown as a capacitor. This arrangement lends itself to double level switching as shown in Figure 3, where block and line nomenclature is substituted for X and Y.

2.3 Display Timing

When a particular block of the bar graph type display panel is enabled, the number of lines, or area of illumination, is dependent upon the type of display selected. The three types available are:

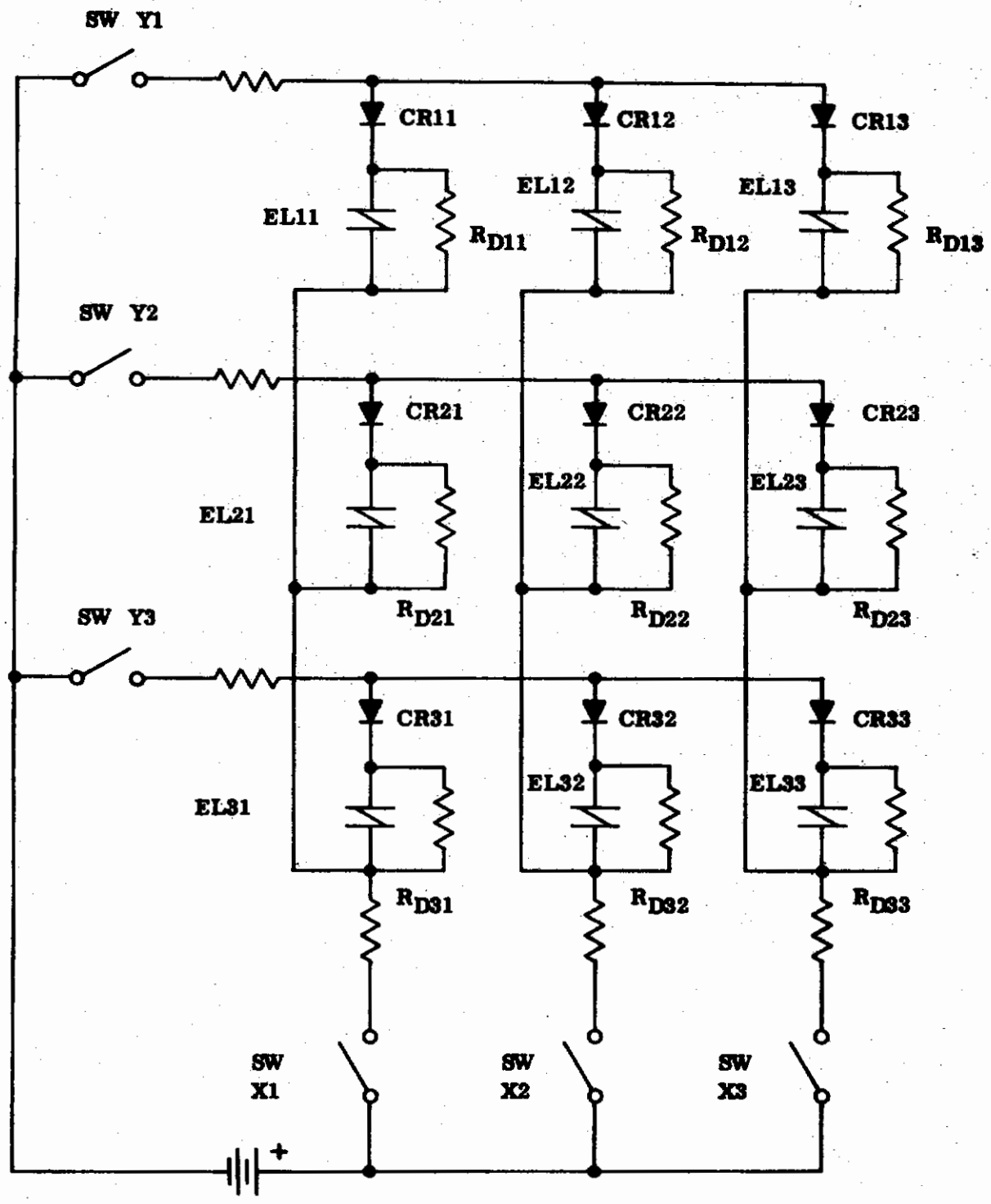


Figure 3 Matrix Switching Circuit

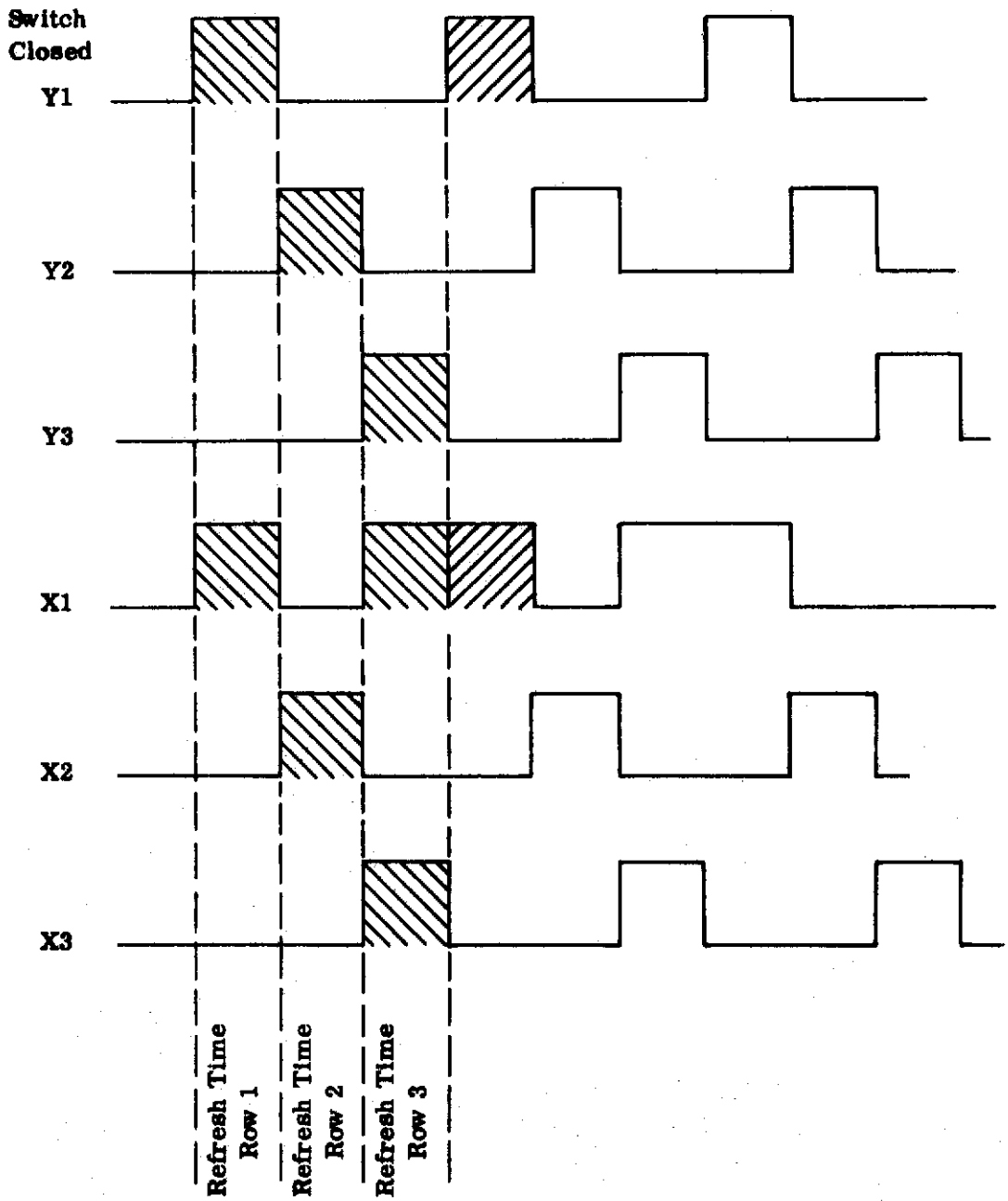


Figure 4 Matrix Timing

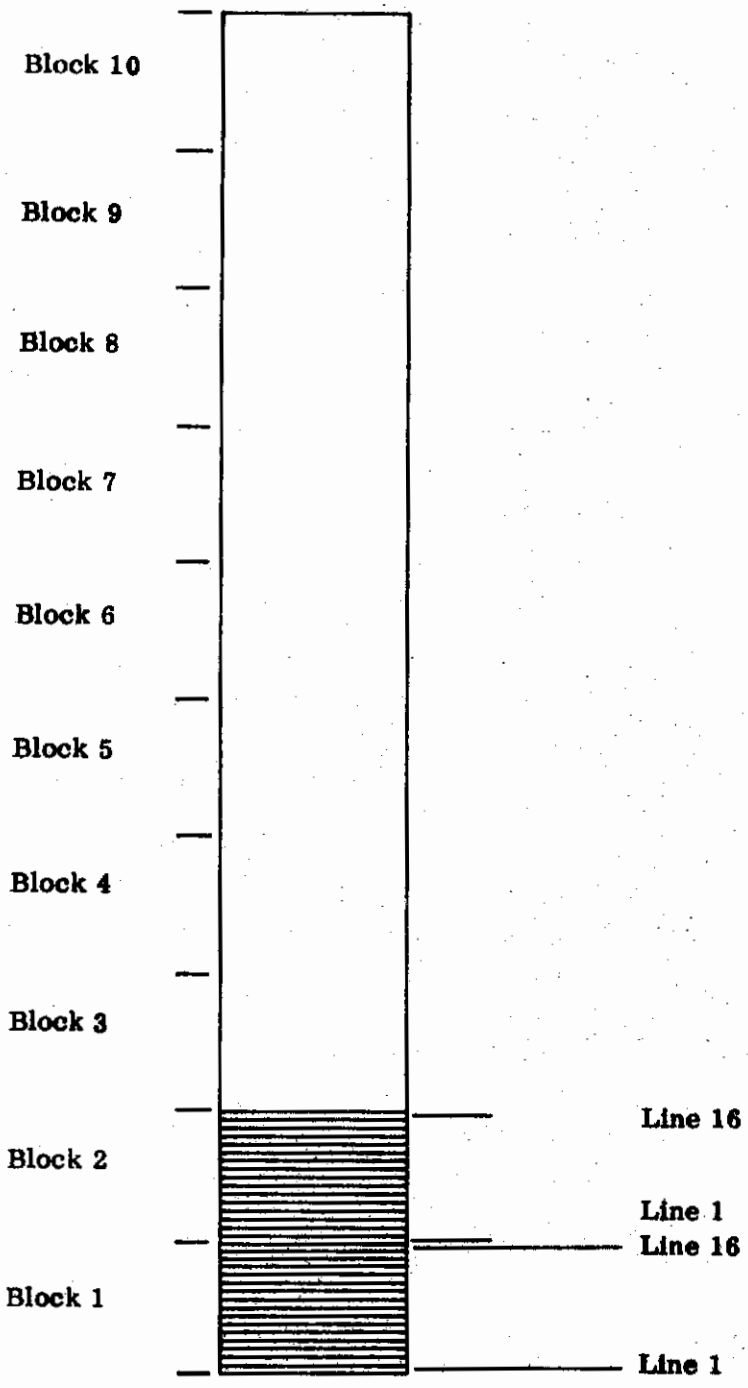


Figure 5 Bar Graph Matrix System

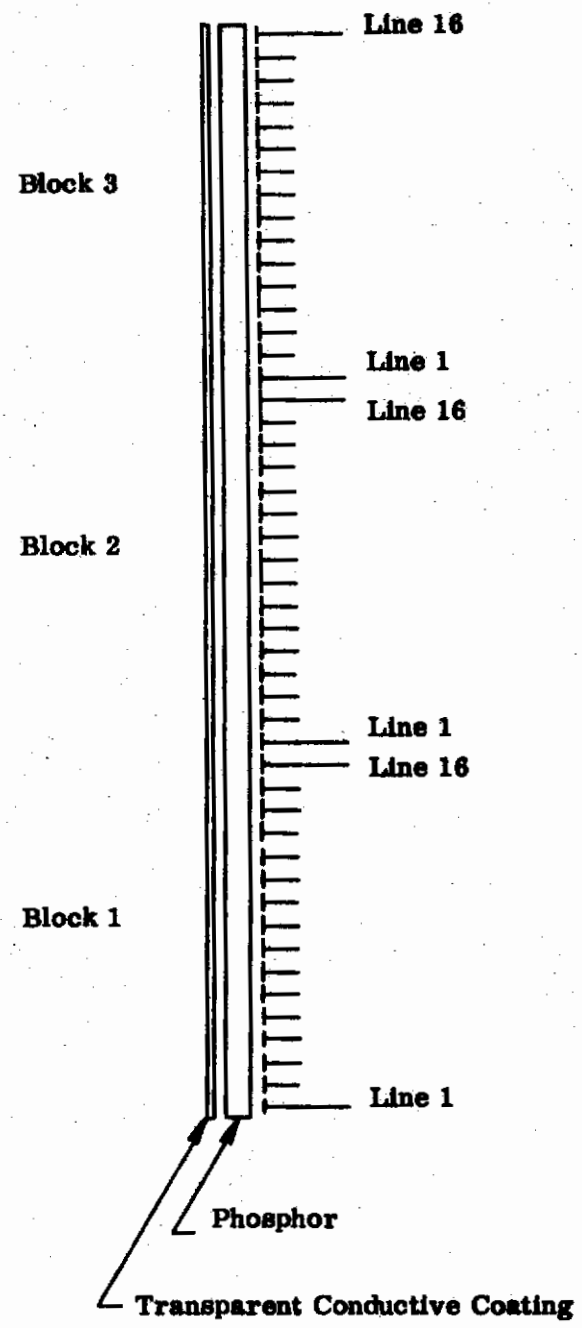


Figure 6 Physical Arrangement of Bar Graph Matrix

1. Bar graph display unit

2. Line graph display unit

3. Rate field display unit

In a bar graph display, all of the line segments below a particular selected point are activated and this area is illuminated.

In a line graph display, the particular line selected is activated, with the two adjacent lines and this area is illuminated.

In a rate field display, the particular line selected in the first block area, is also selected in all other block areas and all are activated. The area under these lines is illuminated. Each selected line will have the adjacent line activated and this area is also illuminated. It should be noted that the individual line width of the bar graph type display is 0.033 and when the combined adjacent lines are incorporated, this additional illumination will give a line width of 0.1.

The bar graph and line graph display may be considered somewhat of the static display, where the displayed information does not normally change rapidly. The rate field display could be considered a dynamic display responding instantly to a changing input source. The speed rate and direction of slew is determined by the source.

Since the selected refresh rate for all display units is 400 hz, this allows 2.5 msec for complete block and line selection. This time period is further divided to provide adequate block and line selection for all types of displays.

The numeric display panel is composed of 5 numeric blocks and each block has nine segments. The second block from the left has a comma, or a 10th segment which is illuminated when a number greater than 999 is to be presented. Each numeric block functions in an X-Y manner such as the bar graph type of display and only the particular lines desired are selected and illuminated to present numbers "0" through "9". All of the numeric blocks in each display panel can be refreshed in any given 2.5 msec time period. When all blocks in a numeric display group are illuminated, the line switches are pulsed 5 times as opposed to one pulse for each block in the 2.5 msec time period.

Figure 7 illustrates a fixed display of the bar graph type displays.

Figure 8 is a numeric panel display unit.

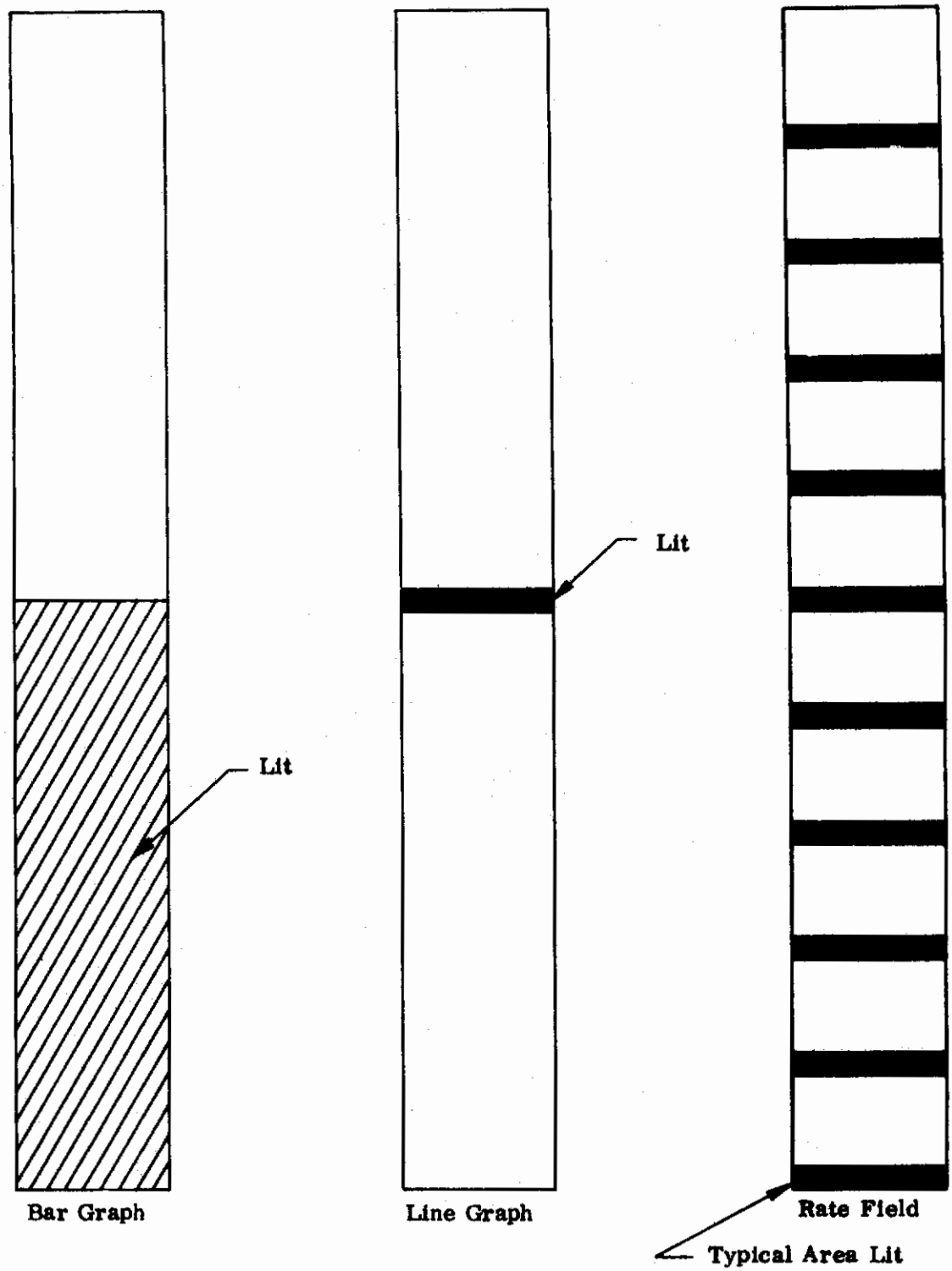


Figure 7 Bar Graph, Line Graph and Rate Field Displays

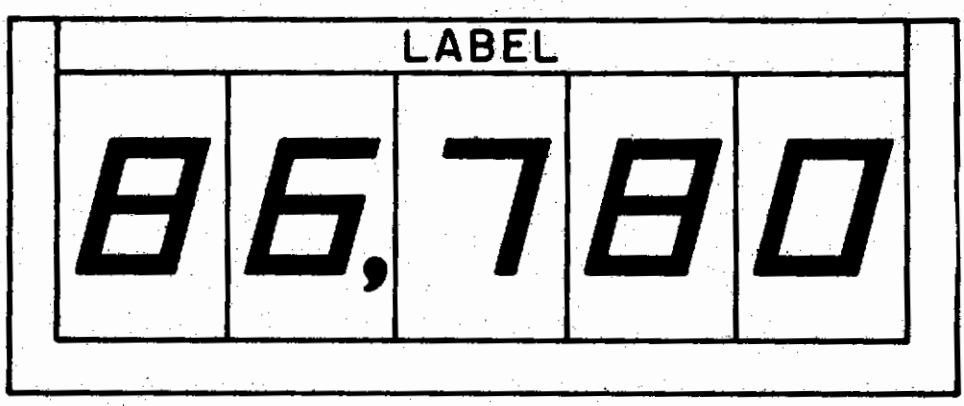


Figure 8 Numeric Display

SECTION III

INVESTIGATIVE EFFORTS

3.1 General

During the earlier part of the program an extensive investigation was conducted to extend the block and line switch operation level to 800 volts dc, to improve the switch operation and reliability. Considerable effort was expended in reducing the discrete component count and size.

Prior efforts indicated a potential diode which satisfied the peak reverse voltage, recovery time, leakages and size requirements. However, additional effort was expended in determining the best possible unit, body configuration and mounting tabs.

The initial concept of using a ceramic board for deposition of certain thick film circuits required many vendor contacts and visits. It was determined that the required tolerance for the diode holes in the substrate could not be held and furthermore the allowable area for the thick film circuitry was not sufficient to provide the minimum resistance desired in the switching circuits.

To determine the thick film resistive material, means of deposition, maximum resistive ability, the size limitation required long hours of experimentation. A portion of the data included in the investigative efforts was derived from a concurrent development program outlined in Technical Report AFFDL-TR-67-169 written by George Bagnall and Don Howe. It was used to verify the results of previous approaches and to gain assurance that the method selected was the best one for this application.

3.2 Switching Circuit Investigation

It was determined that if maximum light intensity was to be realized from the EL panel, the switches must operate with voltages equal to +800 volts dc and the transistors must have collector-to-emitter and collector-to-base breakdown voltage in excess of 800 volts if any degree of reliability was to be attained. Space consideration was also a determining factor in the transistor selection.

Previous effort in the development of EL switching circuits had resulted in several possible configurations. Each type offered certain advantages. These various configurations were evaluated with respect to this application. As a result, the circuit of Figure 9 was selected. This circuit had been used previously with excellent results.

The original circuit used two transistors in series to give the desired breakdown voltage protection. This is shown in Figure 9. Placing V/2 on the base of the upper transistor prevents the collector-to-base or collector-to-emitter voltage on either the upper or lower transistor from exceeding its breakdown voltage.

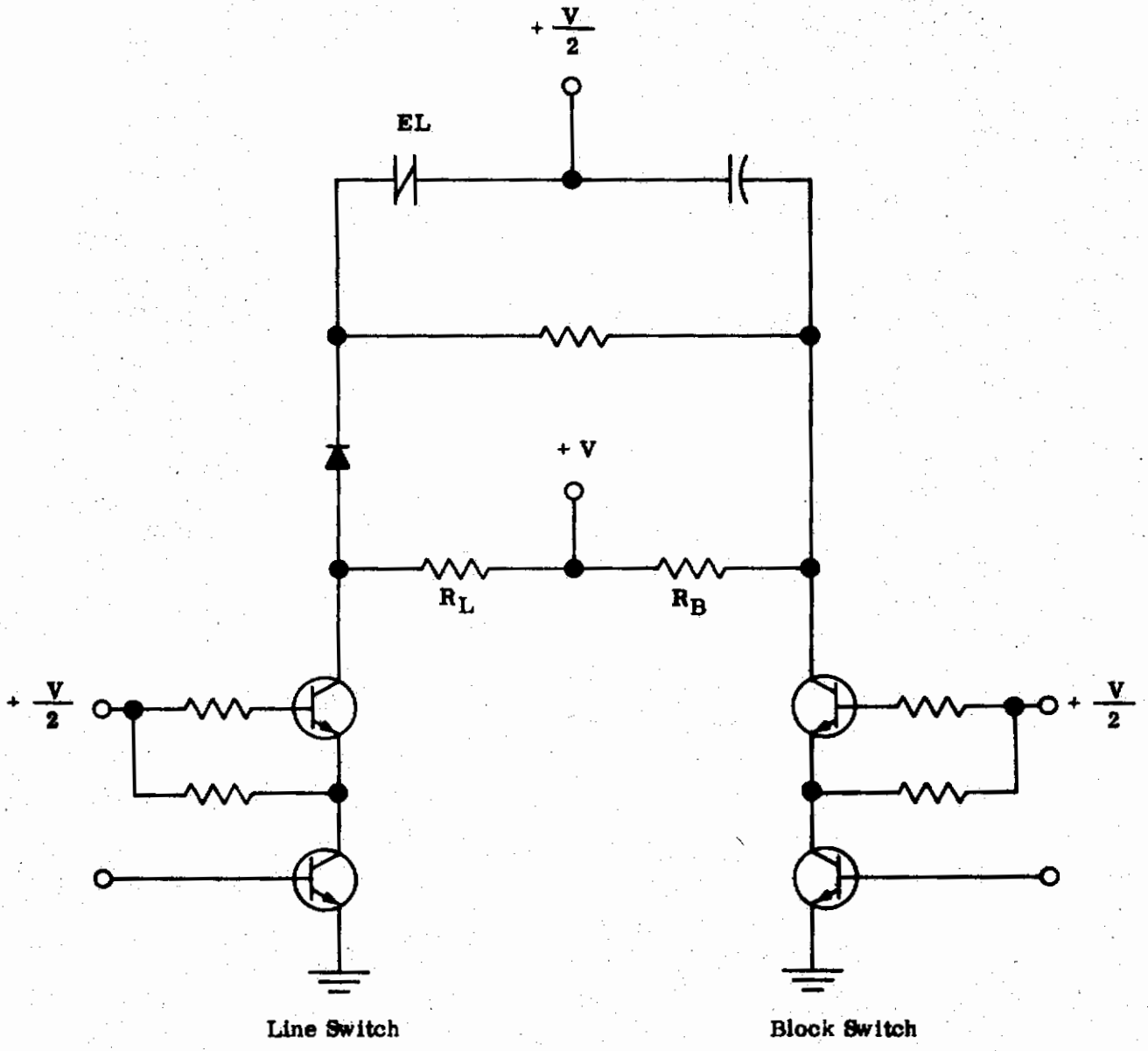


Figure 9 800 Volt Switching Circuit

A series of tests on breadboard EL panels indicated that this switch would suffice as the line-and-block switch. There are some features of this switch that are undesirable if a very large matrix of EL segments were to be controlled. These drawbacks are:

1. The light output of the EL segment is a function of input pulse width to the line and block switches in the 1 to 50 μsec range. If each illuminated element in an X-Y display is to be refreshed at a 400 hz rate and the elements are refreshed a line at a time, then as the number of lines increases, the time interval per line decreases. For example in a 10 x 10 display, each line must be refreshed at a 2.5 msec time interval for a 400 hz rate. Therefore, each of the 10 horizontal lines must be refreshed in a 250 μsec interval. This means the switch serving the vertical elements has 250 μsec in which to operate. If the 10 x 10 display matrix was increased by a factor of ten, the switch time operation would be decreased by the same factor for a time interval of 25 μsec. Extension to a 1000 x 1000 matrix limits the switch interval to 2.5 μsec. Operation of the circuit in Figure 9 at this speed causes a noticeable decrease in light output.

2. Recovery time of the switch becomes a major problem as the matrix size is increased.

3. The inhibit nature of the circuit complicates the logic and wastes power. In the normal refresh cycle, as each block is selected, all the lines in that block that should be ON will be selected and illuminated simultaneously. The lines that are not to be ON must be kept off by application of an inhibit signal. (Block selected-line not selected). In the specific case of a line graph, the worst case condition would be when one line is illuminated in any particular block. In order to accomplish this, inhibit signals must be applied for 15 lines. The worst case condition of the bar graph is also 15 lines and for the rate field, it is 13 lines. When the inhibit signal is applied current will flow to ground causing wasted power which could be considerable in a large array.

4. A large percentage of the charge on the EL is lost because the series diode does not recover fast enough.

Additional effort was then spent in attempting to improve the basic circuit by reducing the size and quantity of components. This was necessary in order to obtain the desired packaging size.

From the basic design, the circuit of Figure 10 was derived. This reduced the transistor and the resistor requirements by two for each X-Y circuit. Considerable vendor contact was made in the selection of the transistor. A possibility existed that one could be obtained in a TO-46 header which would be highly desirable in reducing package size. However, the version was not developed to the point where it would be available within a reasonable time.

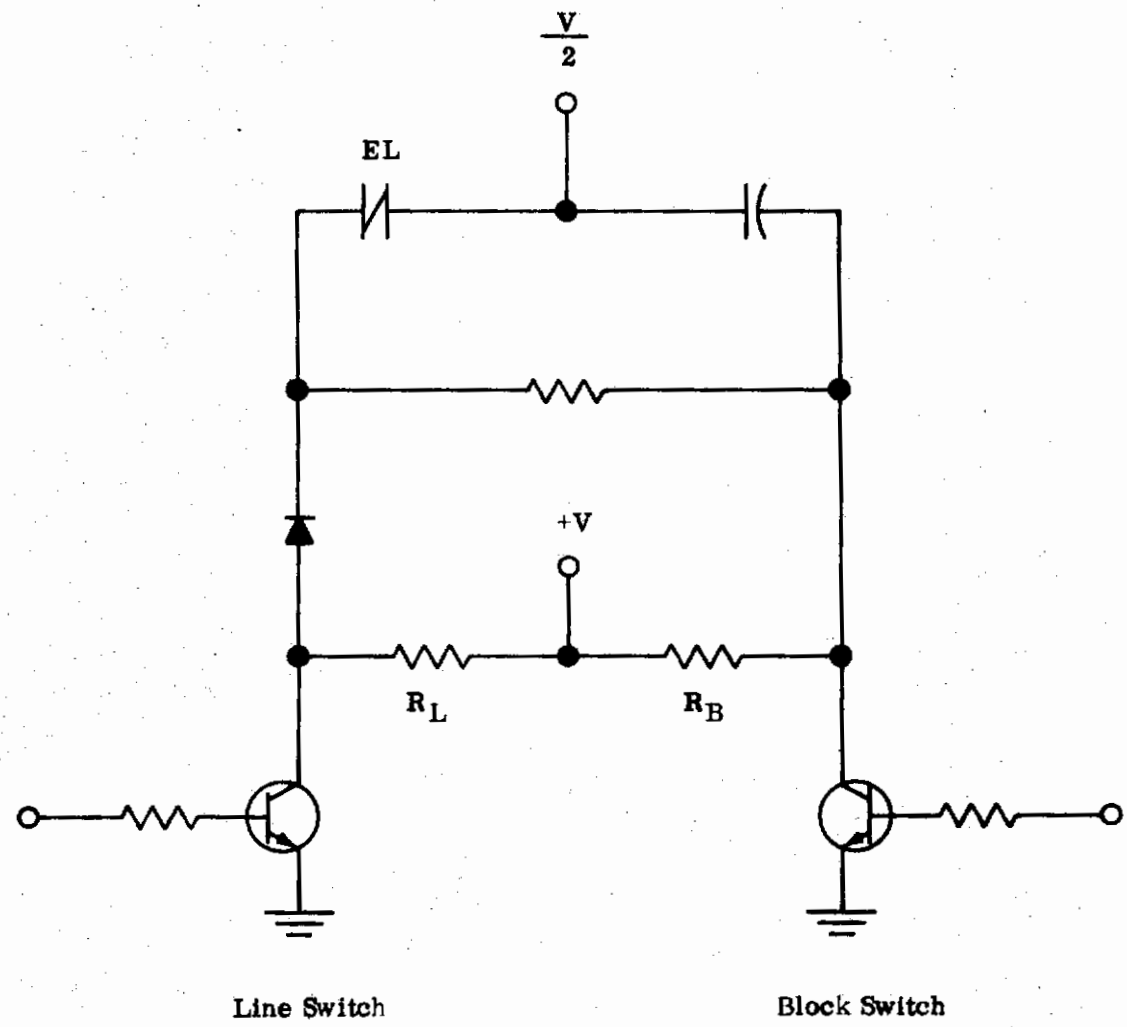


Figure 10 Simplified Switching Circuit

The transistor selected is a special 2N5013 manufactured by M. S. Transistor Corporation. It is mounted in a standard TO5 header with a pancake case and has a minimum collector-emitter and collector-base breakdown voltage of 825 volts. The pancake case permitted an assembly within the desired package depth.

Minimum average circuit power consumption was obtained by reducing the switch on-time of each transistor, thus permitting a size reduction for the collector resistors.

Various diodes were evaluated by inserting them into the switching circuit and observing the waveform as it would appear across the EL element. The type of waveform observed is illustrated in Figure 11. In order to obtain optimum circuit operation, it is necessary to minimize the voltage drop caused by the diode characteristics. This drop is shown in Figure 11. This drop also increases as the input pulse becomes narrower with a resultant decrease in light emitted by the EL.

Of primary importance in the selection of the diode is also the configuration. The diode should be as small as possible and permit relatively easy assembly as well as provide the necessary electrical characteristics. With these factors in mind, the MC 4025 diode in a pellet configuration was chosen.

3.3 Substrate Materials

Several types of materials were evaluated for use as a substrate for a resistor-conductor pattern. Conclusions drawn from a lengthy study of these materials, which included many contacts with the vendors, indicated another approach must be taken if there were to be any hope of maintaining the required diode hole spacing tolerances. It is in this area that 160 pressure contacts are made to the 5 inch EL bar graph type panel.

Since the use of a ceramic material as a substrate for the resistor-conductor pattern was dictated by the firing temperature requirement of thick film printed resistor networks, (it was this additional temperature cycle that caused deformation) a search was made to find a suitable resistive compound having a lower curing temperature.

A paint type resistive material was located which cured at room temperature or at a recommended 250 degrees F for a faster rate. The lower curing temperature permits the use of a standard fiber base glass substrate used in printed circuit work. This permitted the desired hole spacing tolerance to be attained and it is far more economical than the ceramic materials approach. Additional discussion of this area is contained in Section V.

3.4 Control Logic

The control logic was based upon utilizing readily available microminiature logic circuits of the "flatpack" type. This package lends itself to the particular configuration required by the display panel design. Because of the stringent packaging requirements, minimization of the control circuitry assumed great importance and considerable effort was expended in this area to decrease component requirement without sacrificing function or reliability.

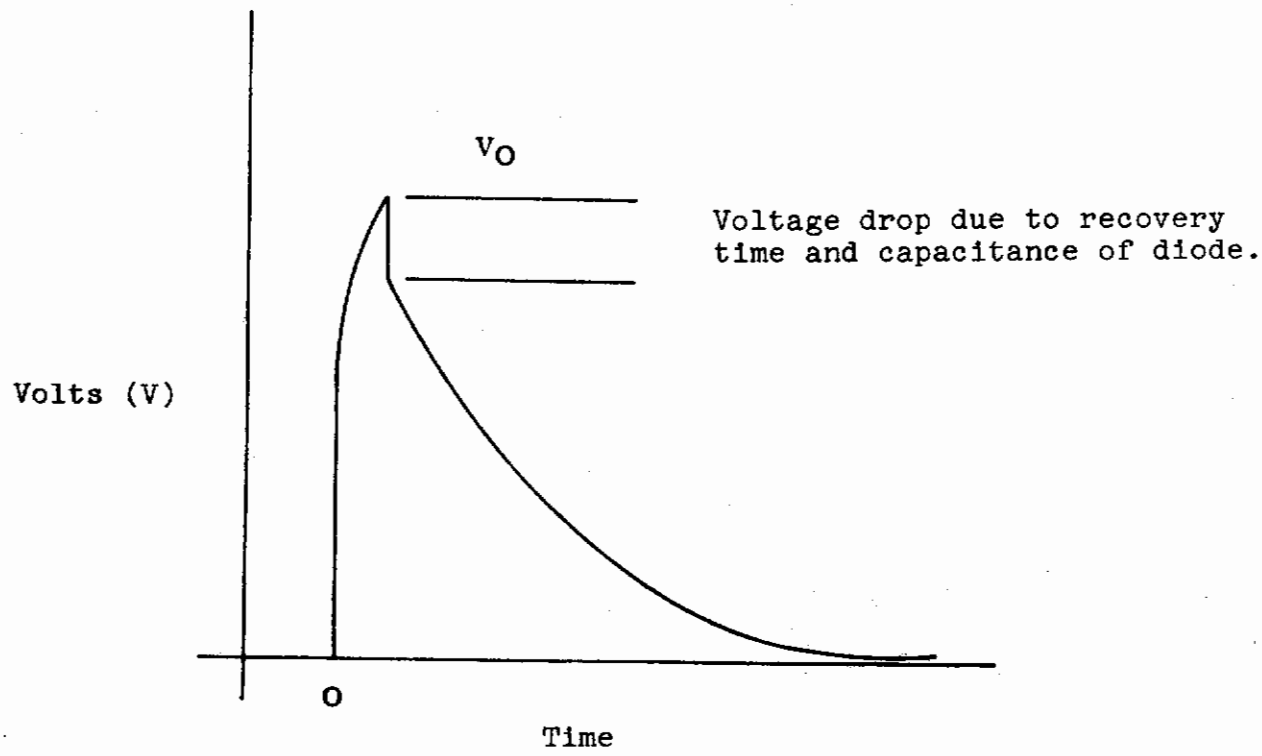


Figure 11 EL Waveform for Diode Investigation

3.5 Display Unit Packaging

The bar graph, line graph, and rate field instrument package size design goal was 2 inches wide by 7 inches long, and 0.5 inch thick. Because of the vast amount of logics interconnection the width and length was increased by 0.25 inch. The depth remained constant. The packaging approach utilized multilayer (Figures 12, 13, 14) printed circuit boards, thick film hybrid circuits and a standard printed circuit component board. The completed package (Figures 15, 16, 17) was the result of a combination of several advanced packaging techniques using each to the best advantage to gain a maximum function for the least volume.

The numeric display unit construction was based upon the same technique used for the other display units. The packaging problems of this unit were greater than anticipated, since a memory must be incorporated for each of the five addressable areas within one display unit.

3.6 Common Control Unit

The common control unit is housed in a commercial type cabinet and will accept a standard 19 inch wide by 17-1/2 inch high front panel and a 17-1/2 inch deep chassis. (See Figure 2).

The master control matrix within this unit will accept data from the A/D converters, always available data (binary and BCD), and manually generated data and place it on the common control lines with the correct address.

Connectors mounted on the rear door provide for data inputs and outputs, also the power input lines.

The front panel controls provide the following functions:

1. Thirteen four-position rotary switches permit the assignment of a particular display panel to the desired data source.

2. For a manual data generation, 8 data, 5 address, and 1 enter control buttons are provided. A CLEAR control is provided to reset the front panel when desired. The master reset clears all display panels. The unit functions only with an address permitting individual panel reset.

3. An OFF-ON switch provides input power control. Two jewel lights indicate the source of input power.

Figure 12 Display Unit Assembly

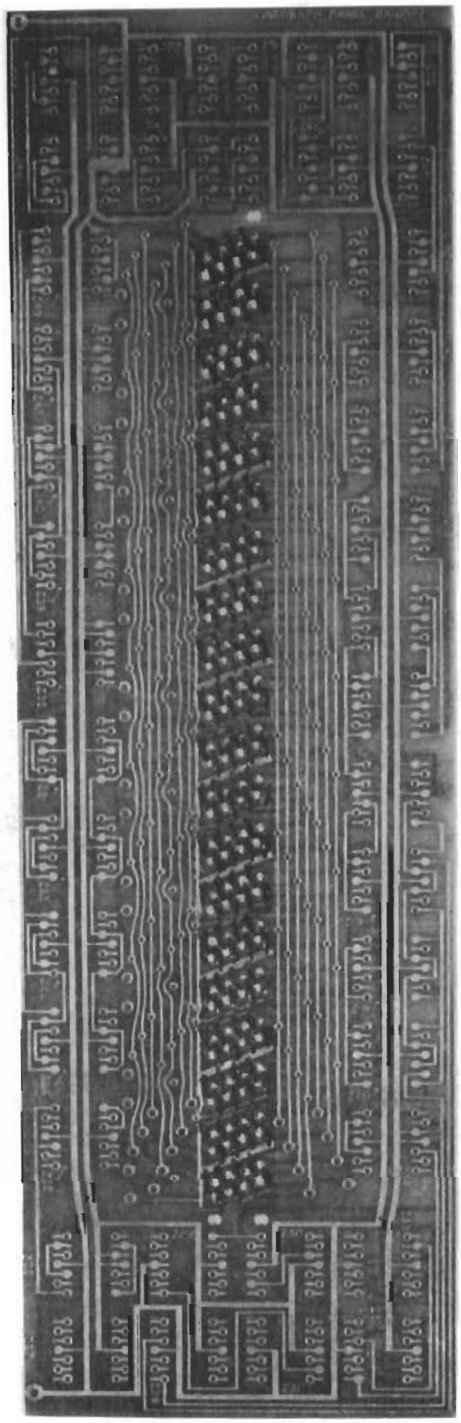


Figure 13 Thin Film Resistor - Diode Assembly - Front View

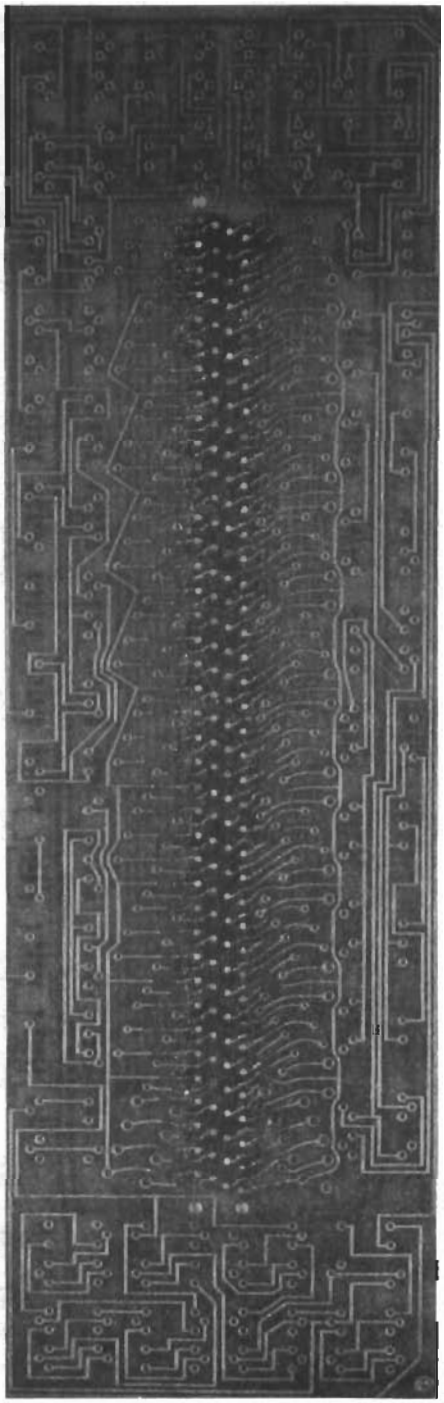


Figure 14 Thin Film Resistor - Diode Assembly - Rear View

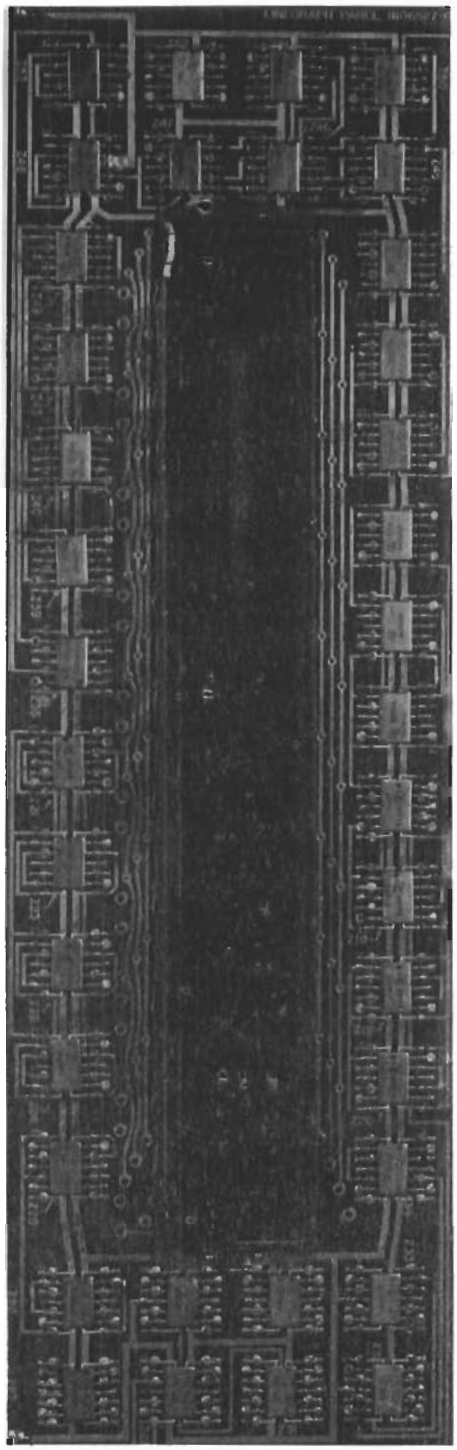


Figure 15 Assembled Display Unit - Front View

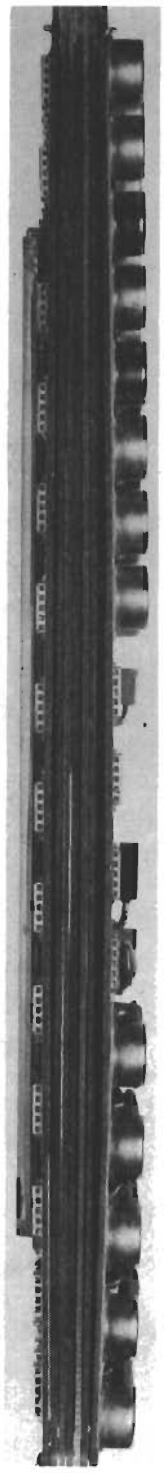


Figure 16 Assembled Display Unit - Side View

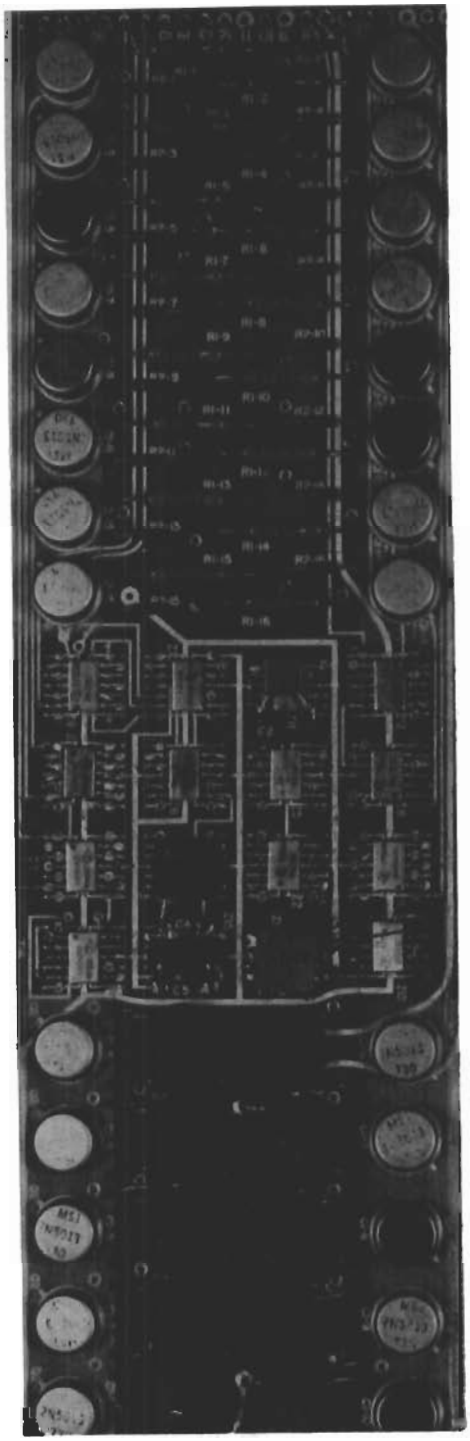


Figure 17 Assembled Display Unit - Rear View

4. A switch coded MANUAL-AUTOMATIC controls the d-c voltage to the EL switching circuits thereby controlling the display panel intensity. The meter registers half voltage at all times and has a transparent color coded operating range overlaying the meter scale. The operator has full control in the manual mode. In the automatic mode the ambient light controls the level of dc to the EL panels, a higher ambient light provides a higher dc voltage.

The over-all weight of this unit has increased from a design goal of less than 70 pounds to 100 pounds. It was discovered that the power supply change-over feature required transformers of heavier current capabilities which increased the over-all weight. The power change-over feature further complicated the design of the high voltage power supply in that the original approach was not compatible with an ordinary dc to ac inverter. A unique approach was developed which permitted operation from either mode with only a small variation in d-c voltage to the EL panels.

An A/D converter multiplexer was located which replaced the original planned unit. This resulted in considerable space and weight savings without sacrificing the required function of the A/D converter. A substantial reduction in cost helped to offset increased component cost elsewhere. The new A/D converter was mounted on the logic chassis in the upper part of the control unit.

SECTION IV

CIRCUIT DESCRIPTION

4.1 General

Descriptions of individual display unit control and logic flow for the system is outlined in the following paragraphs.

4.2 Manual Controls

Front panel controls (Figure 19) provides complete operator control in assigning a display unit to a remote data source or to locally generated data. Figure 1 shows the typical display of all thirteen panels. Each panel accepts data for display only when properly addressed. The available display panels, each with a fixed address are:

1. Three Bar Graph panels (address 14, 15 and 16)

2. Three Line Graph panels (address 6, 7 and 8)

3. Three Rate Field panels (address 22, 23 and 24)

4. Four Numeric panels (address 1, 2, 3, 4 and 5
   9, 10, 11, 12, and 13
   17, 18, 19, 20, and 21
   25, 26, 27, 28 and 29)

Figure 19 shows the various front panel controls available to the operator. The function of each starting with the lower section, is as follows:

ON-OFF Switch

Two jewel lights are associated with the power control to identify the power source. If the unit is operating from the d-c source and the 115 volts 400 hz is available, change over is accomplished by placing the power control switch in the OFF position for a minimum of 3 seconds before returning it to ON.

MANUAL-AUTOMATIC Switch

This switch selects the mode of display intensity control. In the MANUAL position, the operator controls the intensity by rotating the adjacent BRIGHTNESS control. A dc, half-voltage meter, is associated with the intensity control for monitoring purposes. In the AUTOMATIC position the intensity is controlled by the ambient light sensed by a light sensitive device.

Fuses

The control unit and display packages have overload protection in the form of three fuses located in the lower left section and by a circuit breaker accessible by the rear door.

Manual Data Generation

The center section of the front panel provides the means to generate data, address, and enter data to a particular unit. A CLEAR feature permits resetting of data and address flip-flops prior to depressing the ENTER button. Unit reset is possible only when an address is present and the ENTER button is activated. System reset does not require an address and will reset all units. Each device in this section contains an indicator light for status indication. A high level is indicated by a lighted unit.

Operation Mode Selection

The upper section contains thirteen, four-position, rotary switches for control of the individual display unit. The four positions are coded as follows:

"0" Off Line From All Data Inputs

"1" Analog to Digital Converter

"2" Always Available Data

"3" Manual Data

The display units may be assigned to any position desired without interference with another unit.

4.3 Data Input Output Connectors

Figure 18 shows the input and output connectors mounted on the hinged rear door. The binary and BCD data inputs are separated by individual connectors permitting a maximum flexibility in display panel use.

4.4 Logic

The logic is divided into four unique display units and a master control unit. For simplicity, block diagrams will be used mainly to indicate logic flow and control.

4.4.1 Master Control Unit Logic

A logics nest located just back of the front panel (Figure 20) contains a 24 volt control card, a clock card, twelve logic cards, and the A/D converter multiplexer.

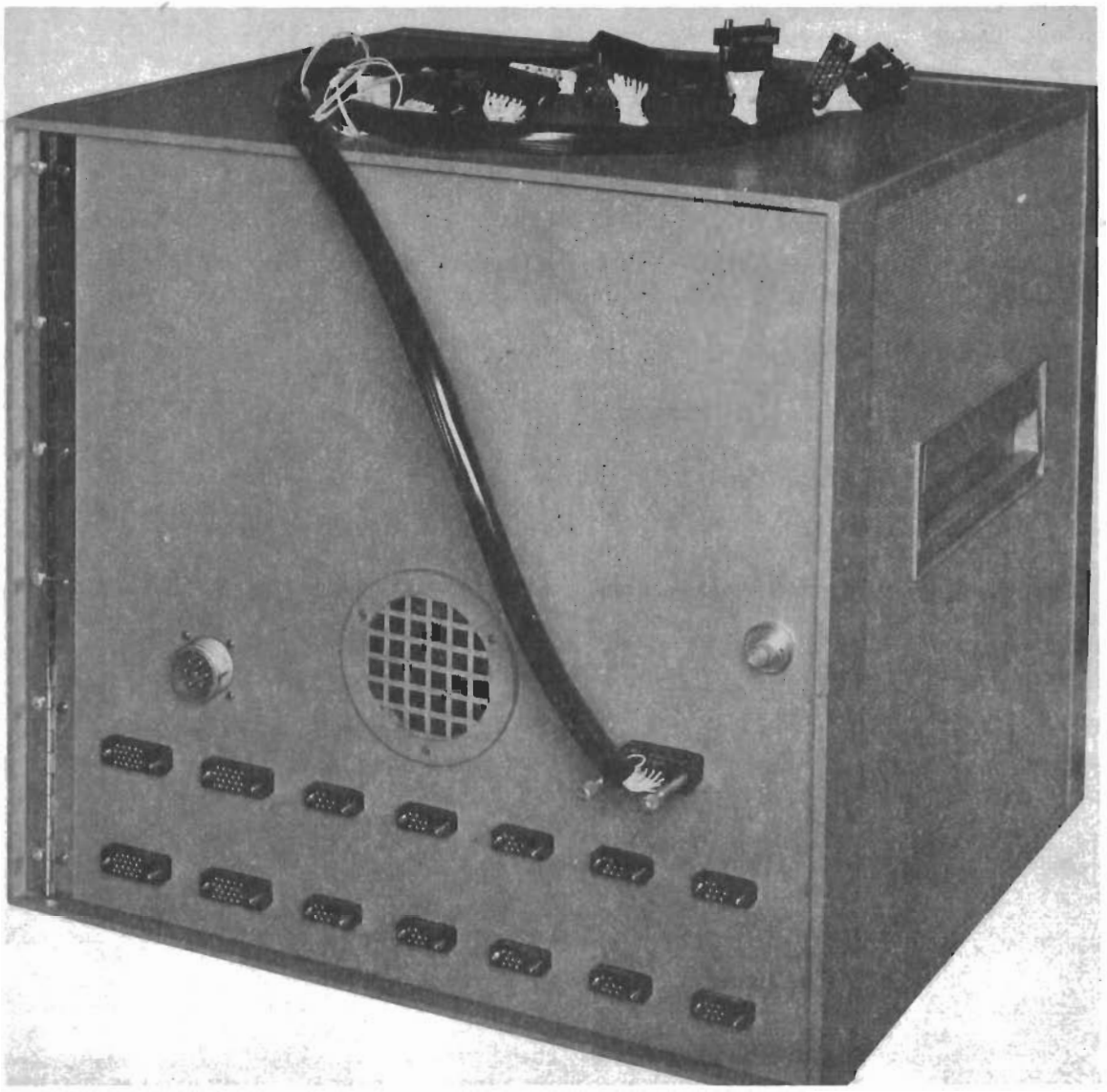


Figure 18 Rear Door of Control Unit

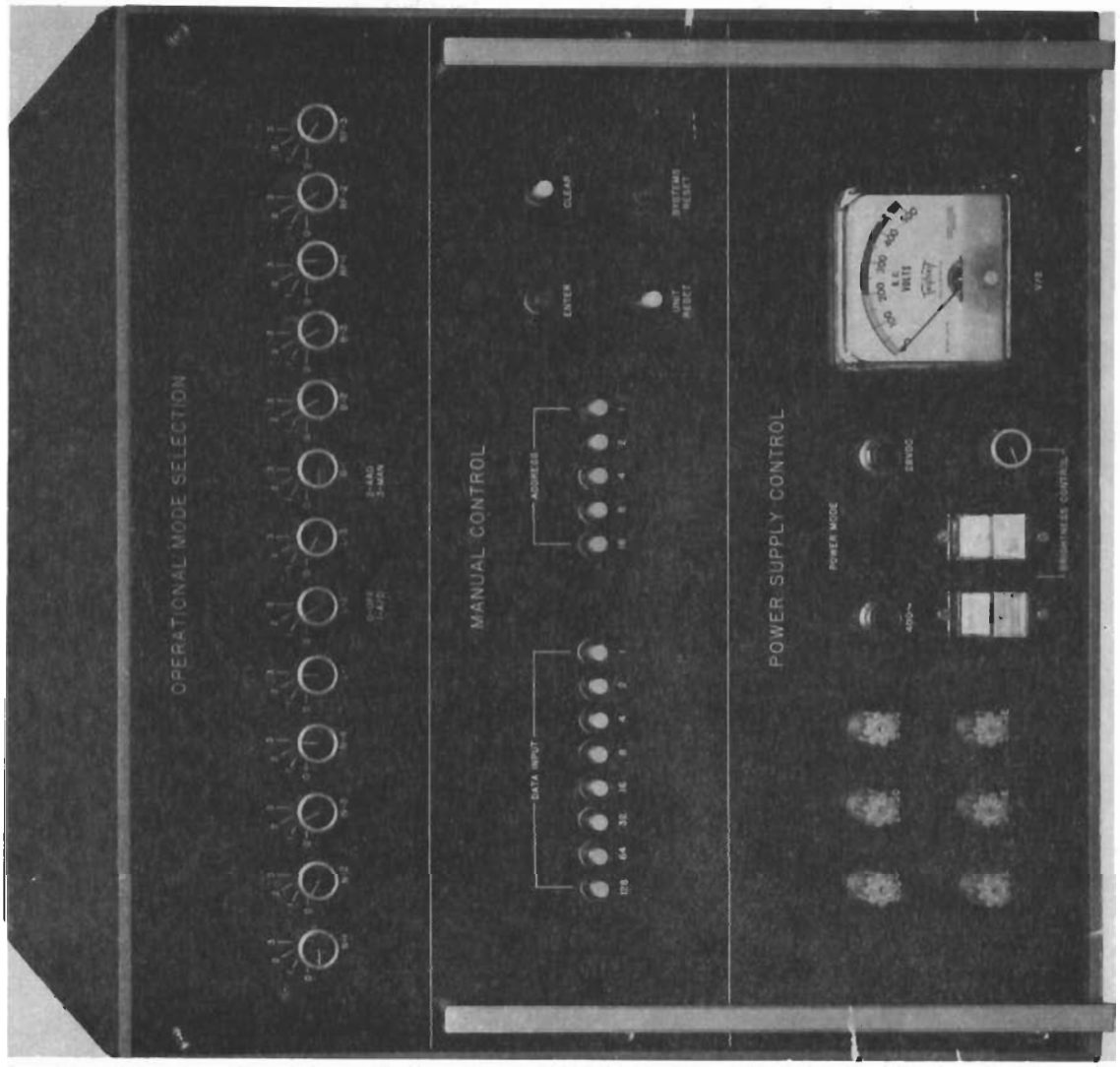


Figure 19 Control Unit Chassis - Front View

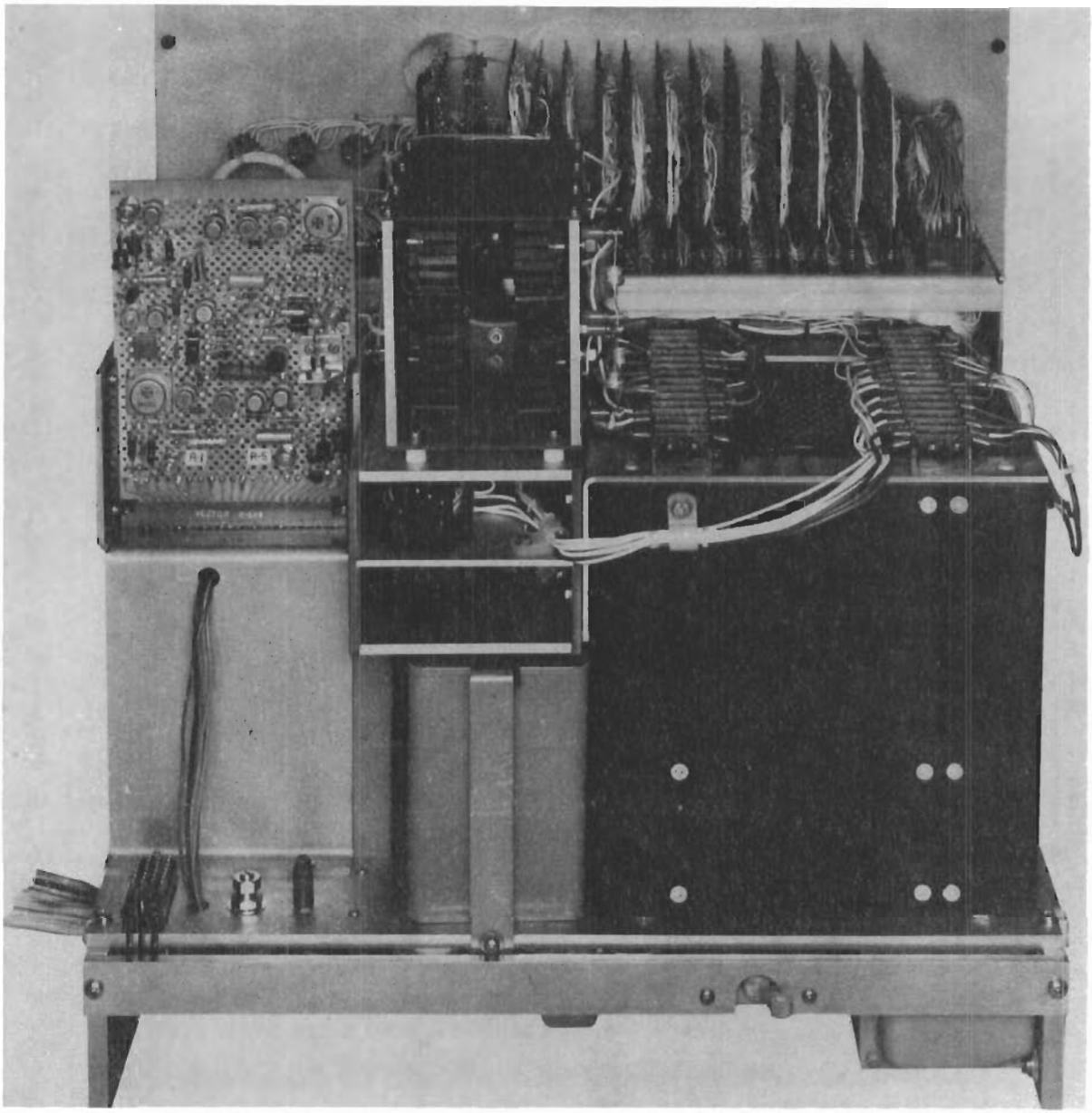


Figure 20 Control Unit Chassis - Rear View

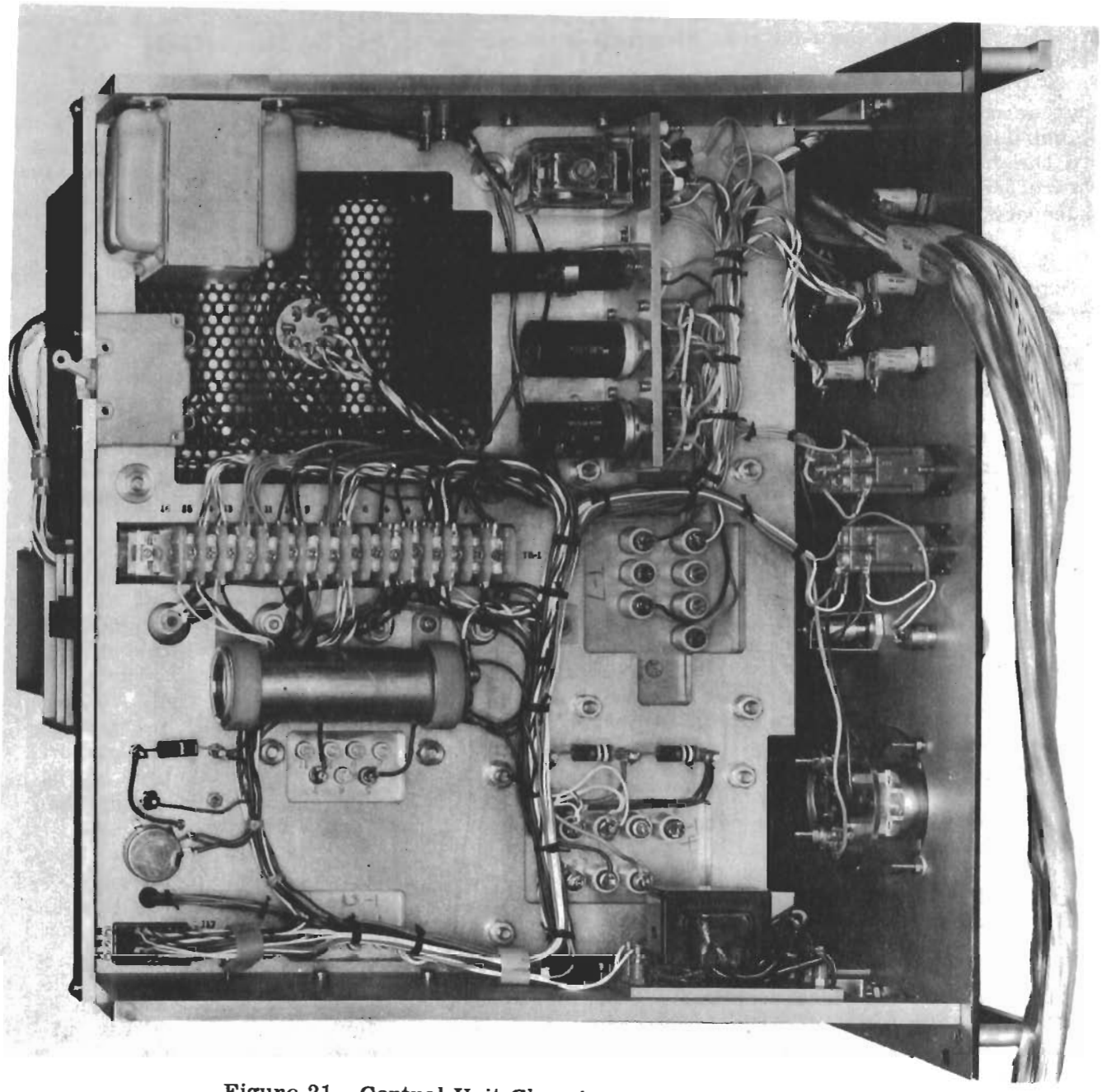


Figure 21 Control Unit Chassis - Bottom View

Figure 22 is a block diagram of the master control unit logic. With reference to the circled numbers on this diagram, each section is quickly identified.

System timing and refresh capabilities are derived from a 2 khz clock identified by the number 2. The output of this clock is fed to all display units by a common clock line for refresh timing. The output is also gated to a five-stage counter and to the data multiplexer for reset purposes. The 2 khz clock is a symmetrical multivibrator controlled by a unijunction transistor with frequency and pulse width controls. Adequate stability is obtained by controlling Vcc.

The Counter/Address decoder (3) driven by the 2 khz clock signal, provides binary data to the display address data and unit address decoder. The counter consists of five flip-flops wired as a ring counter. All output lines are set to "0" on the 32nd clock pulse giving a potential update for each unit every 16 milliseconds. The unit address decoder provides 29 separate addresses to the display mode selector, always available data gate, and to the manual control gate.

The Display Mode Selector (4) in conjunction with the "Mode Selector Switches" on the front panel routes the gated address to the mode data register. The mode register consists of three flip-flops that are set by the desired address. These flip-flops are reset by the negative going clock pulse, thus a flip-flop will follow sequentially all addresses gated into the register.

The "Manual Control Data/Address Generator" (5) contains a number of flip-flops and gates to generate binary information for updating the display units assigned to the manual mode. The data and address flip-flops are set by the control buttons on the front panel. A high level signal back to the control buttons turns on the indicator lamp indicating a set of conditions of the flip-flops. When the data and address is set, the enter button is depressed causing a flip-flop to set and provide one of two gate signals required to send the data to the "Display" data multiplexer. The second gate signal occurs when manually selected address is coincident with the address from the address decoder. When data is gated out and it is accepted by the display data multiplexer, a data accept pulse resets the manual data and address flip-flops.

The "Always Available Data" (6) gates, routes 9 groups of 8 binary inputs, (72 inputs) when properly addressed, to the data multiplexer (1). Also, 20 groups of BCD inputs (80 lines) are routed to the data multiplexer.

The A/D converter control (7) provides the controlling pulses for the A/D converter. The A/D control will gate data from the A/D converter to the data multiplexer upon receipt of the correct address. The A/D converter operates in a sequential mode. Each start pulse causes it to move to the next channel. Address one will reset the A/D converter. Address six will move the A/D converter from Channel "0" to Channel "1", if display unit 6 (line graph) is not assigned to the A/D operational mode, data will not be gated out to the data multiplexer.

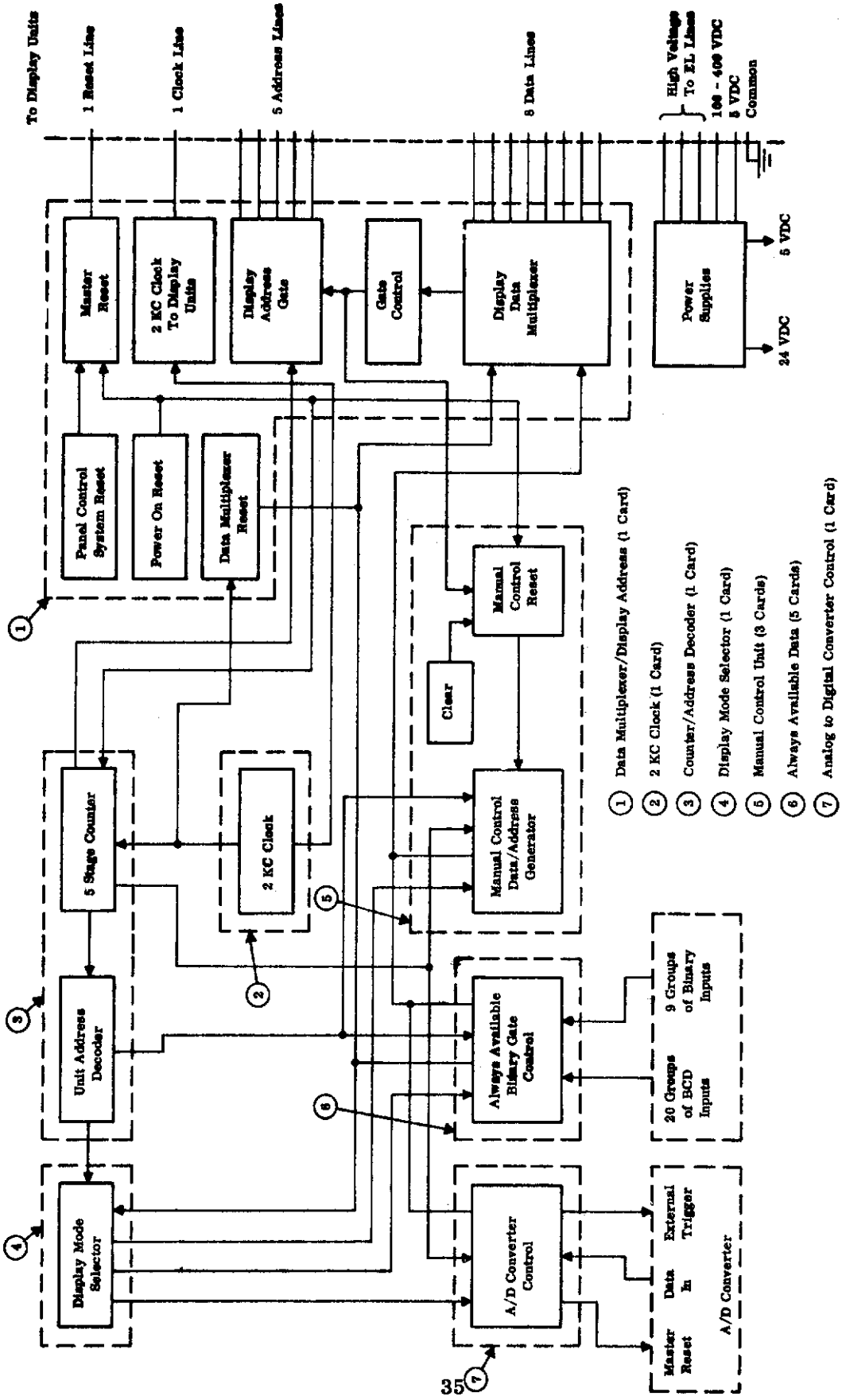


Figure 22 Block Diagram - Master Control Unit

The "Display Data Multiplexer" (1) accepts data from all active sources and places the data on common lines to all display units. The register is reset by the negative going clock pulse. Binary data from address information is gated out to the display units only when data is present in the register, then the data and address information is routed to the addressed display unit.

4.4.2 Line Graph Logic

Figure 23 is a block diagram of the line graph panel. The three line graph panels are identical except for the address gates. Each panel has a pig-tail connection for ease of removal from the common control lines or to use extended lines for remote applications.

A clock signal is applied to a pulse counter which is reset after the fifth positive going clock pulse. The output of the counter is coupled to the line enable, block enable and block count up chain. Only two pulses, identified as 1 and 3, are required. When an address is accepted by the address decoder gate, a 5 usec reset pulse is applied to the pulse counter and both memory blocks. When the reset pulse is removed, high levels on the data lines are gated to the memory registers. Data contained in the lower register is decoded as line information and data in the upper register provides block information. When a line enable gate is activated, the upper and lower adjacent lines are also activated to provide a line width of 0.1 inch for display. The correct block selection is determined by the total data in the memory register. Lines 1 through 16 is block one, lines 17 through 32 is block two, etc., for a total of 10 blocks or 160 lines. When all three of the segments which make up one line appear in one block, only pulse one is used, if one or two of the segments appear in the adjacent block, both pulses are used. For example, line (or segment) 17 is activated by data in the memory register, the two lines adjacent chain will activate lines 18 and 16. Line 16 located in block one is illuminated by pulse one, and lines 17 and 18 are in block two and are illuminated by pulse three. Figure 24 shows the pulses for one 400 hz (2.5 msec) time period which is the panel refresh rate. Gate pulse width of one and three is approximately 45 μsec and the enable pulse is approximately 30 μsec in width. On the count of the first positive going clock pulse, a one-shot multivibrator provides the gate pulse to line and block gates and to the enable one shot multivibrator. After a 10 μsec delay (to allow for gate activation) the enable pulse is applied to the display unit for segment illumination. The third positive going clock pulse provides gate levels and drives the one shot multigate and enable unit when required. Thus a display line (made of three smaller lines or segments) may have two separate enable pulses, however, it is not discernible because of the 400 hz refresh rate.

The line graph panel unit will interpret and display the data contained in its memory register for an indefinite period.

The gate pulse and enable pulse are kept to a minimum width to reduce the total power dissipation and wide enough to provide maximum illumination of the panel.

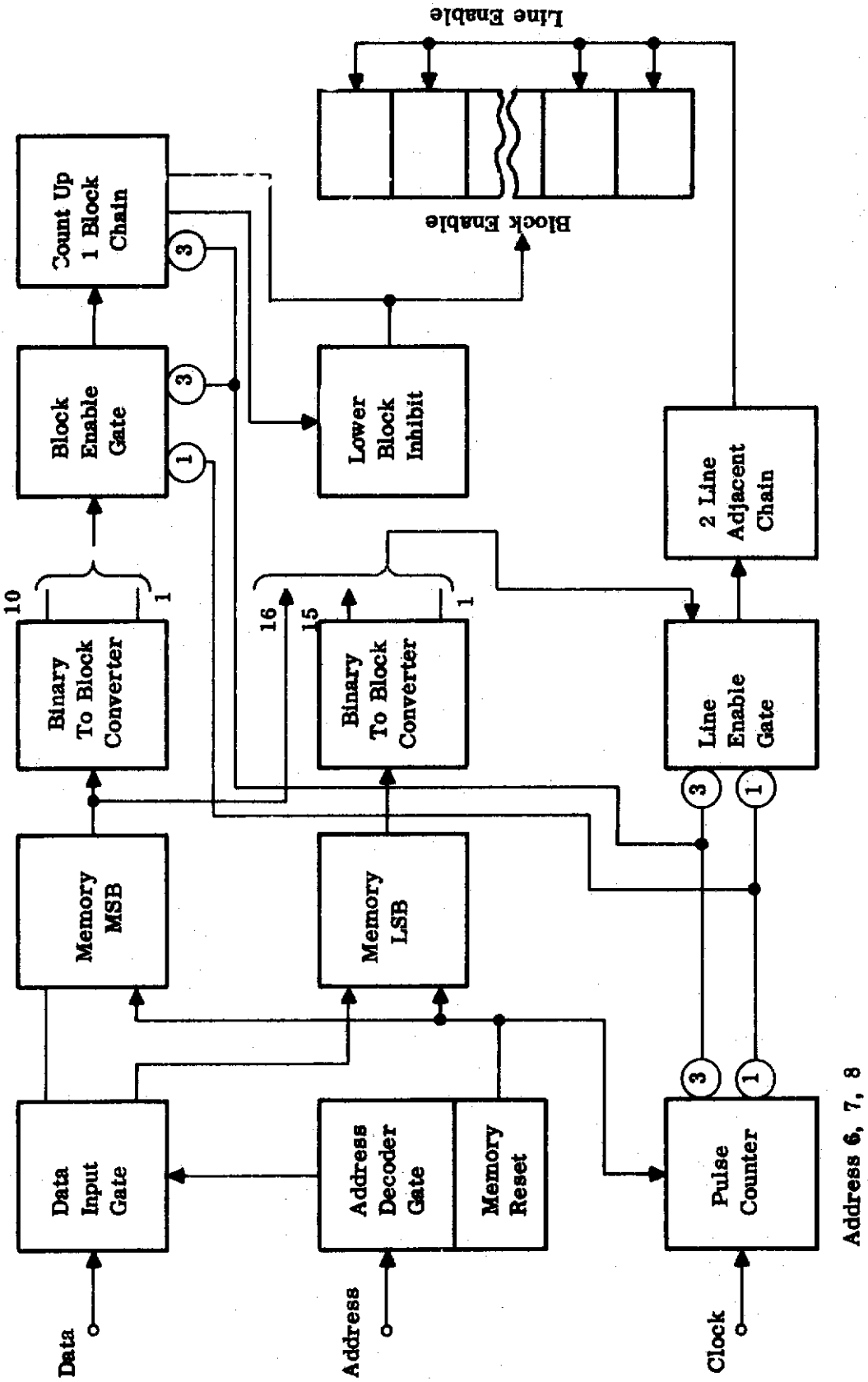
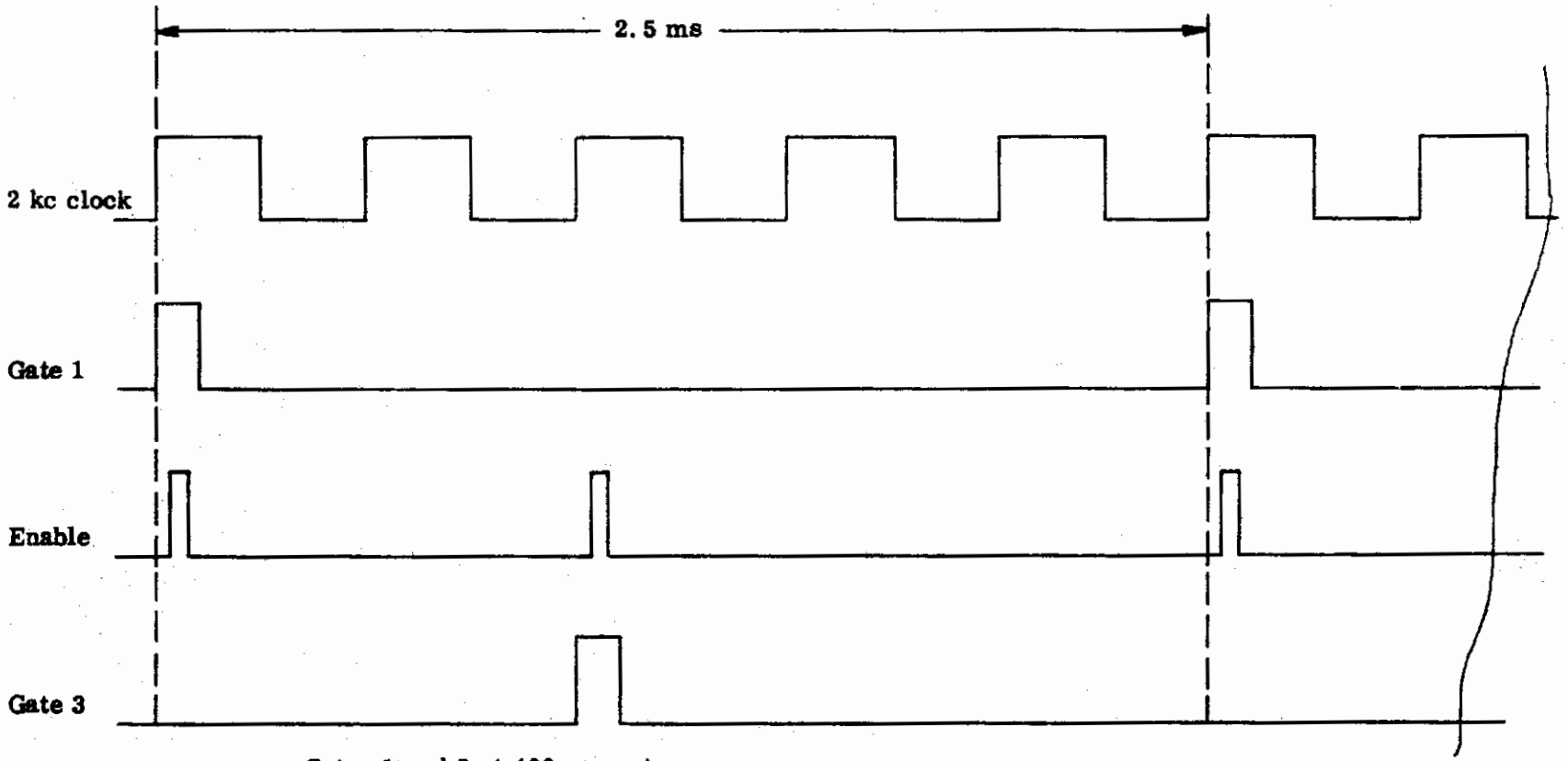


Figure 23 Block Diagram - Line Graph Panel



Gates 1 and 3 at 400 pps rate
Pulse width 50 μsec

Enable pulse delayed 10 μsec
Pulse duration 30 μsec
Enable Pulse Activated by both gate pulses

Figure 24 Timing Diagram Line Graph Panel

4.4.3 Bar Graph Logic

Figure 25 is a block diagram of the bar graph panel. The three bar graph panels are identical except for the address gates. The basic construction of the bar graph panel is the same as the line graph panel. The input logic is the same as used in the line graph panel except for block and line control. In a bar graph arrangement, all lines below and including the line number stored in the registers are illuminated. If the line selected represents a partial block, that block is illuminated by pulse one (Figure 26) and all lower blocks are illuminated by pulse three. The line block division is the same as in the line graph panel and the refresh rate is the same. The display changes only when new data is entered in the memory unit.

4.4.4 Rate Field Logic

Figure 27 is a block diagram of the rate field panel. The three rate field panels are identical except for the address gates. The basic construction is the same as used for the line graph panels. The logic for the rate field is not as complex as for the line graph or bar graph panel. In the rate field display one line width (three combined segments as in the line graph panel) per block is illuminated in all block separations. A total of 10 lines is illuminated at any given time. The spacing between illuminated lines is always 13 lines. The direction and rate of field movement is dependent only upon the data entered into the memory unit. Since a change could occur every 16 milliseconds, the display could appear as a full panel bar graph to a slower input change which would show as roll-drift, or would be relatively stable. This panel requires only one gate and enable pulse and one memory unit capable of storing four binary data. The gate and enable pulse width is shown in Figure 28. Individual address gates are connected to accept 22, 23, and 24.

4.4.5 Numeric Panel Logic

Figure 29 is a block diagram of the numeric panel logic. The four numeric panels are identical except for the address gates. Each numeric panel has five display blocks, therefore, each panel requires five separate addresses. Panel address is:

Panel one, 1-2-3-4-5

Panel two, 9-10-11-12-13

Panel three, 17-18-19-20-21

Panel four, 25-26-27-28-29

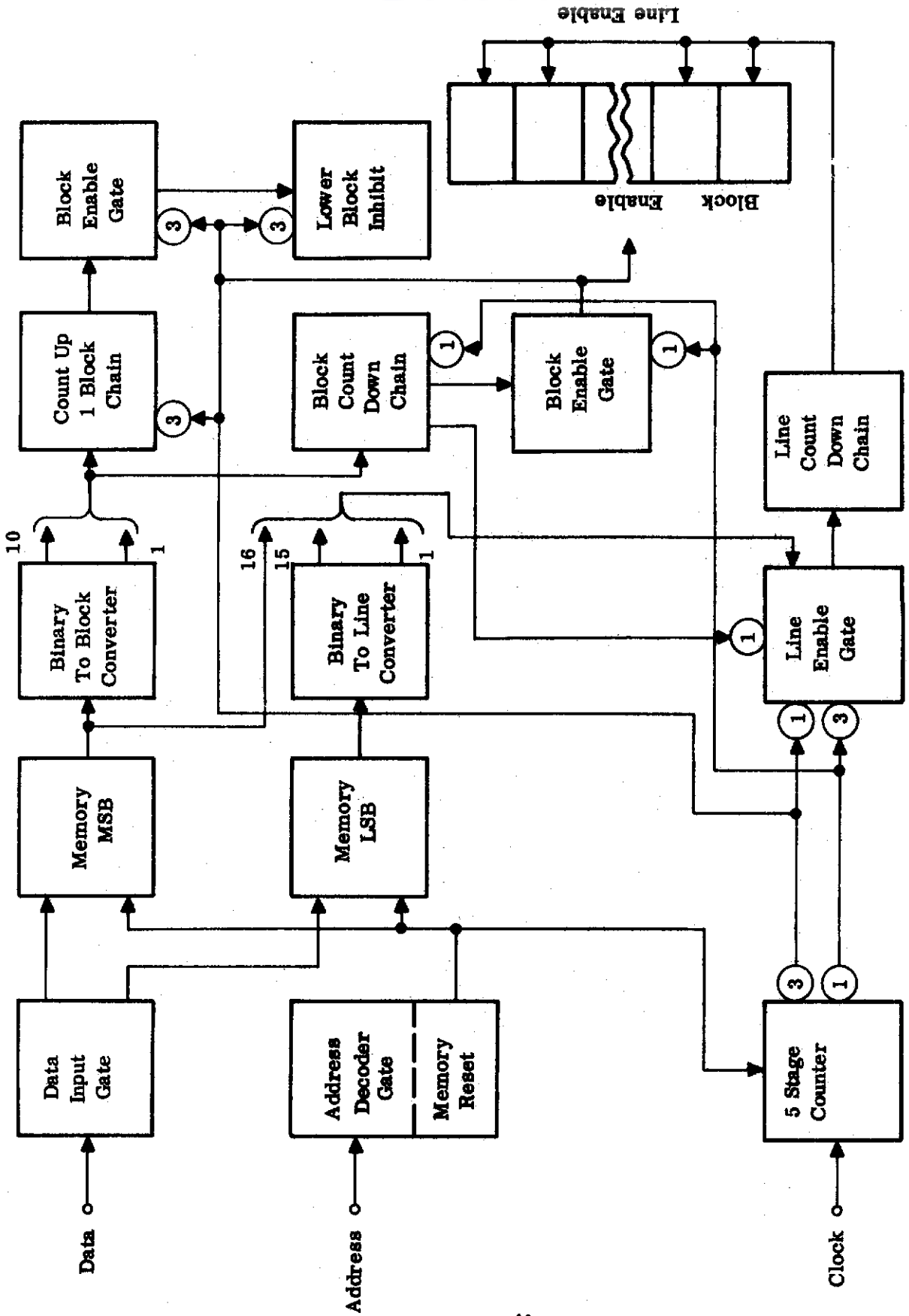


Figure 25 Block Diagram - Bar Graph Panel

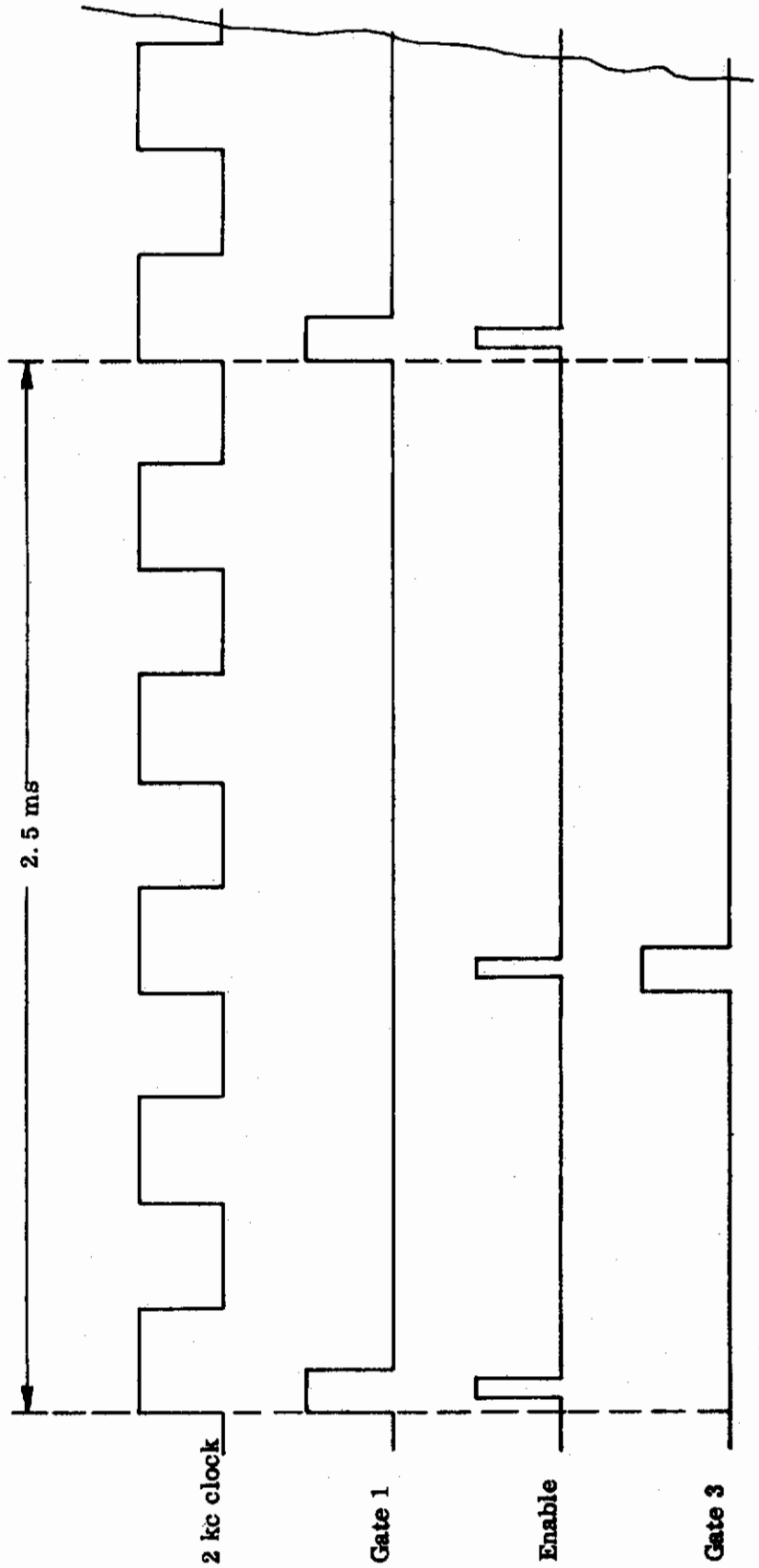


Figure 26 Timing Diagram Bar Graph Panel

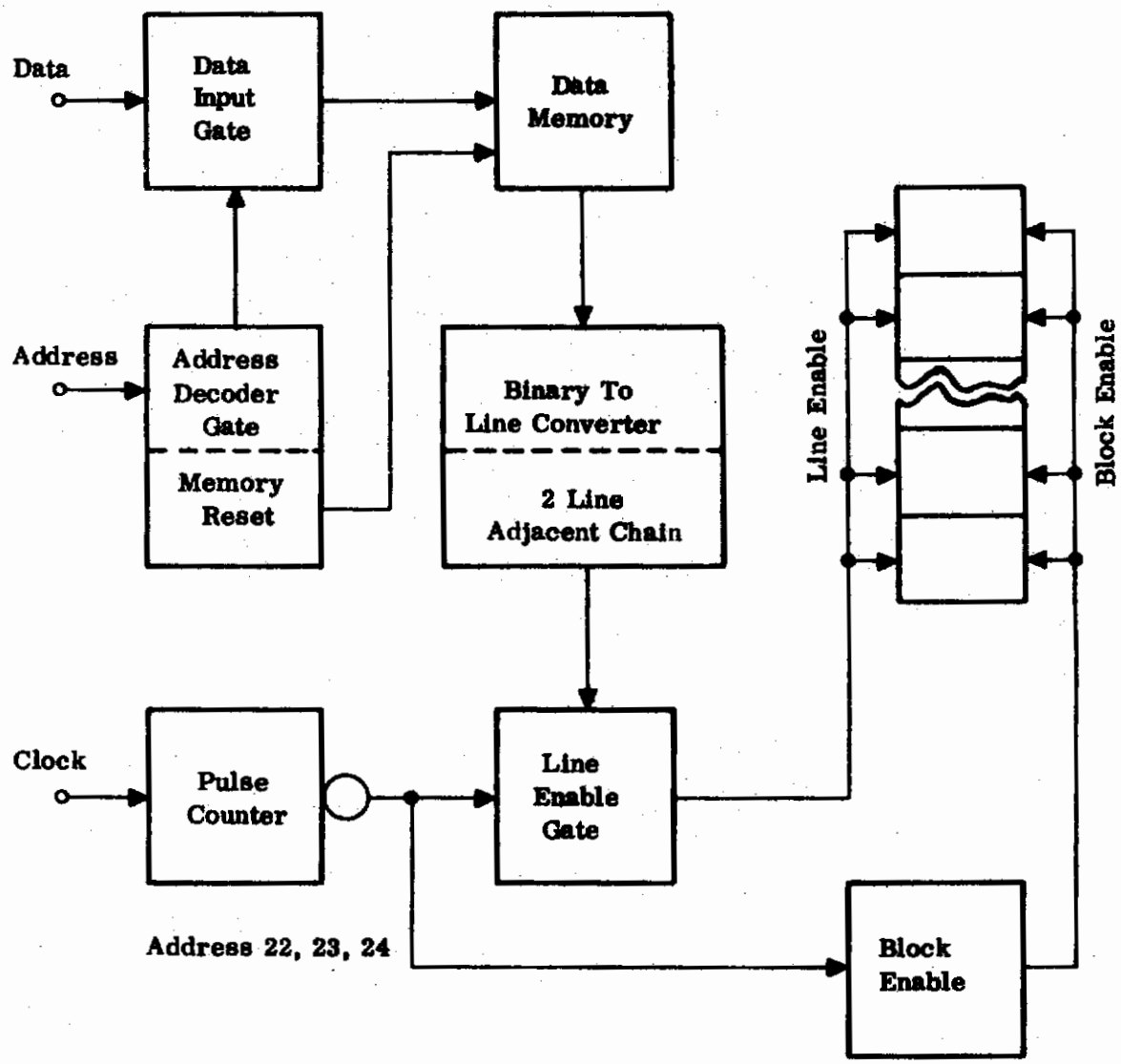
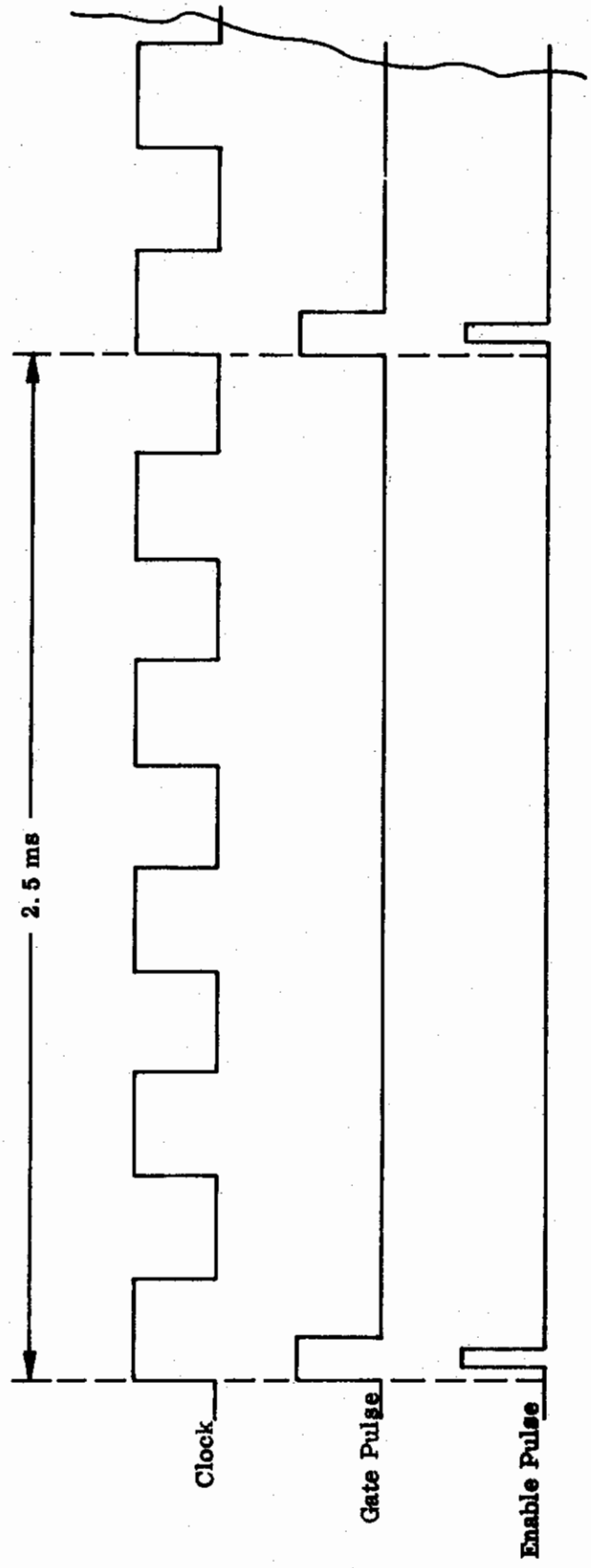


Figure 27 Block Diagram - Rate Field Panel



Gate pulse at 400 pps rate. Pulse duration 50 μsec.
Enable pulse at 400 pps rate. Delayed 10 μsec, pulse duration 30 μsec.

Figure 28 Rate Field Timing

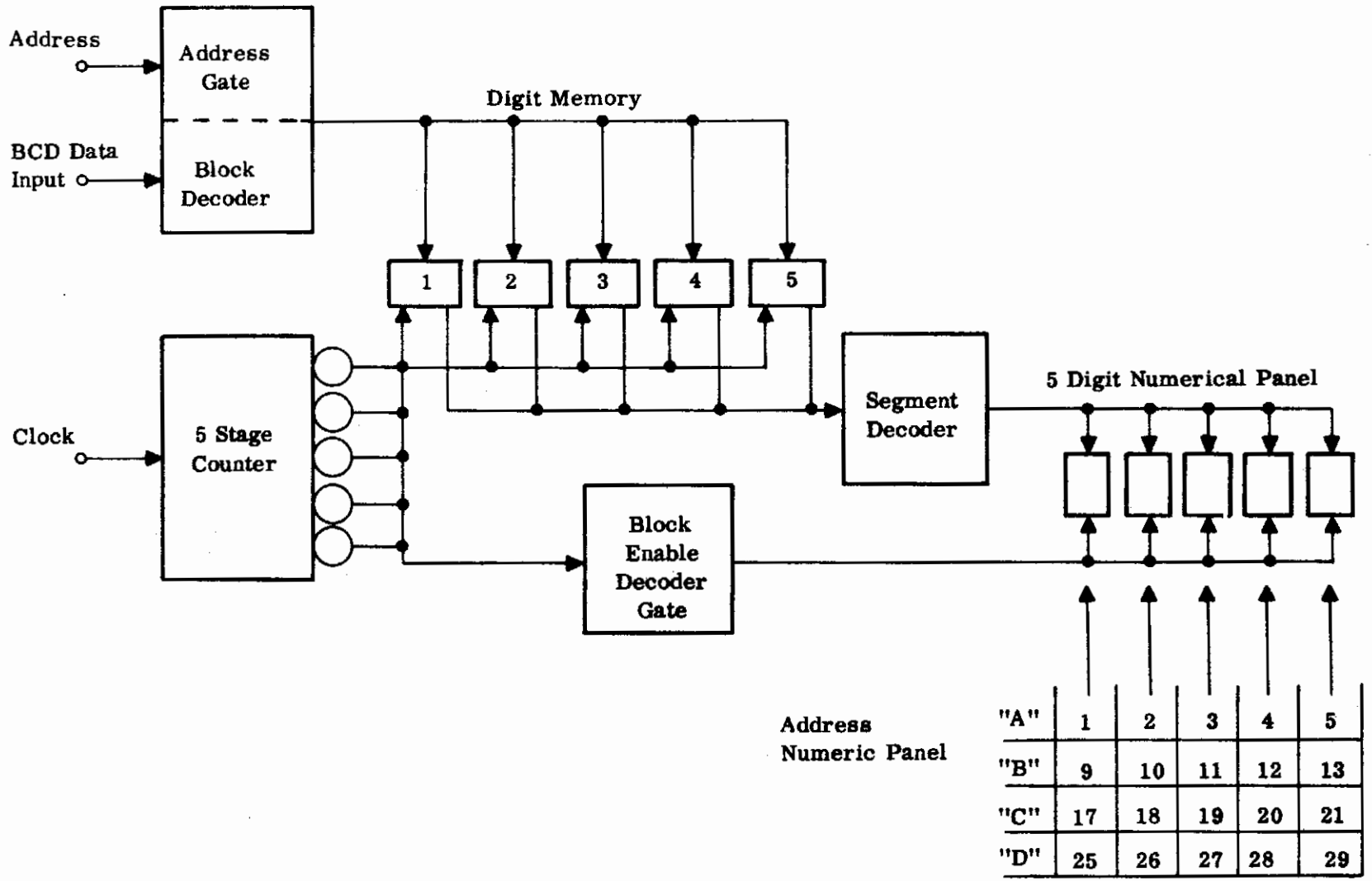
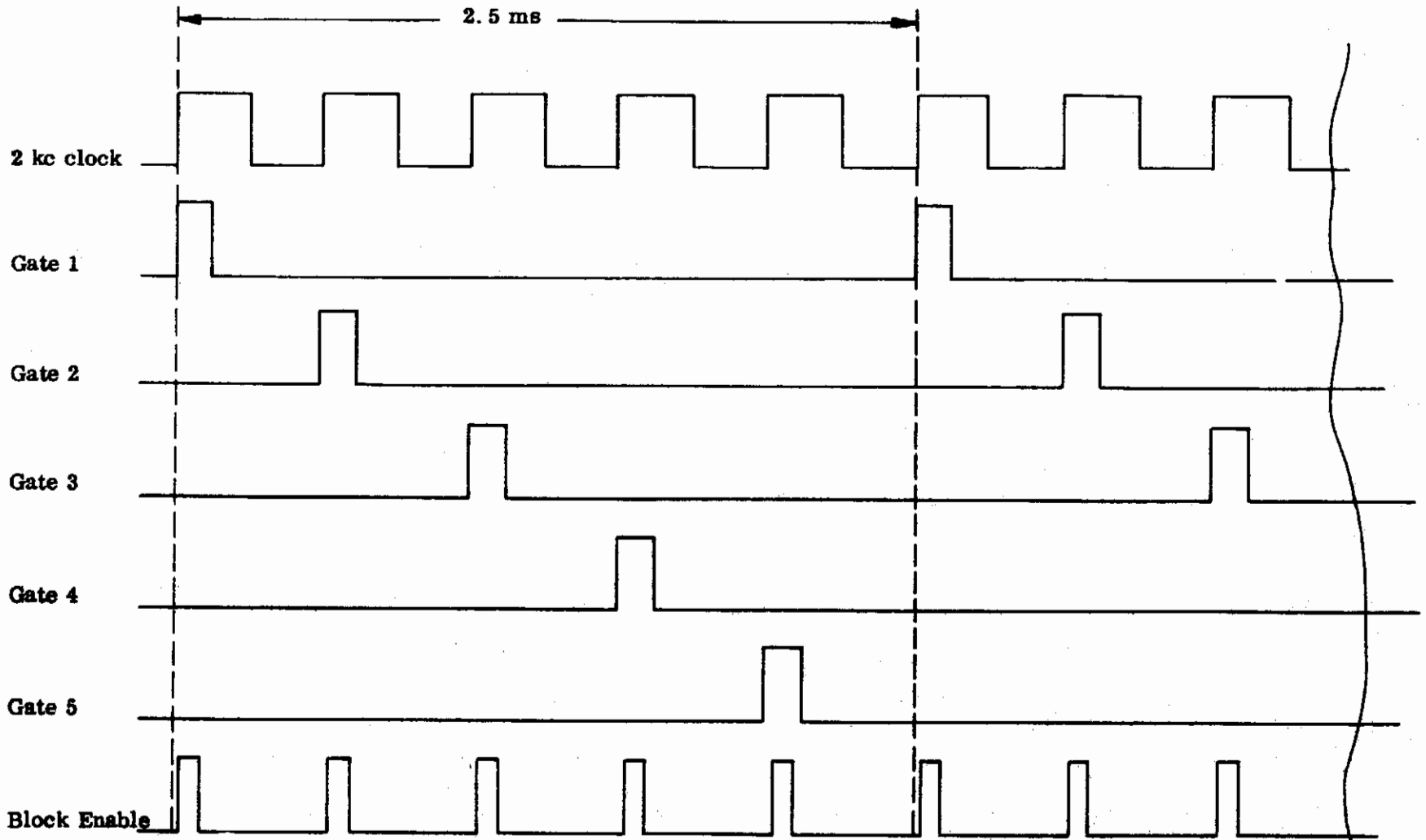


Figure 29 Block Diagram Numeric Panel

Five memory units are required for each display panel and five gate and enable pulses per each 2.5 msec time period. If data is available for a particular numeric panel, it is gated into the appropriate memory. During the first 5 μsec of this 250 μsec time period, data to the segment decoder is inhibited and then it is gated to the decoder for the desired display. The memory units are sequentially sampled and data, if present, is gated to the decoder/display section. Figure 30 is representative of the gate and enable pulses in one 2.5 msec time period.



Gate pulses at 400 pps rate, pulse width 50 μsec.
Enable pulse triggered by gate pulse. Delayed 10 μsec. Pulse width 30 μsec.

Figure 30 Numeric Panel Timing Diagram

SECTION V

MECHANICAL CONSIDERATIONS

The mechanical effort and accomplishments can be categorized under two primary headings; (1) the EL electronics and (2) the EL control unit. Mechanical effort was initially directed toward the EL electronics since it more nearly involved state of the art problems and the EL control unit was merely a packaging task. This being the case, the EL electronics packaging will be discussed first. At the very outset of the program a key decision was made regarding techniques and materials to be used. EL unit space limitations dictated that printed resistors be used in conjunction with the MC4025 diode to make the switching circuit for EL element control. At this point a search was made to obtain the best printed resistor technique available. With the space available for printed resistor patterns, it was apparent from the initial board layouts that a resistance material having approximately 0.3 megohm/square/0.001 thickness would be needed. The Dupont printed resistor material seemed to be the most effective choice. The Dupont line of printed resistor material did not have a high enough resistance range to suit the resistance requirements of this project but it was felt that by adding additional glass frit to the mixture, the resistance range could be increased. This has been done successfully by ITTFL in Nutley, New Jersey. The Dupont material is dependent upon high temperature firing to diffuse and harden the compound; therefore, a ceramic or lava type board was required as a substrate. After many vendor contacts, it was found that the design complexity of the substrate board was such that the hole pattern accuracies could not be held within reasonable limits for the over-all size of board needed. The vendors contacted were the pioneers and leaders in the ceramic and lava substrate field. They all agreed that the hole patterns should be put in the substrate in the "green" state prior to firing for ease of drilling. During the high firing process, the substrate begins to shrink and/or expand thereby losing the required dimensional tolerances. The hole patterns could be drilled ultrasonically after firing to eliminate the expansion and contraction factors but the material then is very hard and time consuming to drill. The cost using the ultrasonic drilling method is extremely high and prohibitive for use on this project for that reason. Since the only reason for using ceramic was the high temperature requirement for firing the resistor material, a new resistor material was sought.

A resistive paint having the required resistance/square value was found and subsequently tried. This formulation was produced by Micro Circuits, Inc., New Buffalo, Michigan and could be baked out at 250 degrees F for 1 hour or air dried at ambient for 8 hours. A sample of the paint was tried with successful results. A line resistor was drawn on G-10 general purpose epoxy glass board, baked out at 250 degrees F and 1 hour and actually connected into a typical EL element switching circuit. After 4 hours of EL operation, the resistance value was found to be the same as the initial value and the performance indicated acceptable stability. The G-10 material and Micro Circuits resistor paint was selected after many laboratory tests indicated successful results.

The completed EL display assembly consists of one EL unit, an interface diode-resistor printed circuit board, two intermediate crossover and jumped printed circuit boards and the back component board. These boards when assembled form a manual multilayer stack up. An insulator sheet of glass epoxy was placed between each printed circuit board to keep the circuits from shorting out. The design of these boards posed no particular problem except the time consuming trial and error artwork layout to obtain the most efficient use of board space versus interconnection complexity front to back. Were these assemblies to go into production, the artwork interconnection and optimum component placement should be diagnosed by computer programming to reduce the congestion on the boards and probably the size of the boards also. The manufacture of the printed circuit and insulator boards was no particular problem since the ITTFL printed circuit facility is well versed in microcircuitry boards production. The hole patterns were drilled using photoetched and drilled, tool steel templates (not hardened).

Assembly of the IC's and discrete components on the front and back followed normal assembly processes. Assembly of the MC4025 diodes; however, proved to be somewhat of a problem because of the diode configuration and the fact that the diode was being placed in a hole in the printed circuit board with anode and cathode connections being on opposite sides of the board. The first method tried was to remove the lead from the cathode end of the diode and solder the anode lead to its appropriate printed circuit pad with the body of the diode pressed into the hole, cathode end up. The connection was then made from the cathode printed circuit pad to the cathode end of the diode (with the lead removed) by means of a solder jumper. This connection proved to be too difficult to make and a high percentage of diodes were shorting out. To remedy this, the anode and cathode printed circuit board pads were changed to rectangular lands and moved back away from the diode hole. The diode was placed in the hole with the leads extending vertically out of the holes and on opposite sides of the printed circuit board from each other. See Figure 31. This technique completely eliminated the shorting problem and with both leads of the diode now available for solder bonding, it eliminated the marginal solder jumper contact to a leadless cathode.

Several different methods of applying the printed resistors were tried. The ideal process would be to silk screen the entire 160 resistors per board at one time with little or no trimming to value. Contact with the resistor compound manufacturer indicated that a 120 mesh stainless screen could and has been used successfully by other companies. A quantity of stainless cloth of different meshes was procured and made into screens in an attempt to find the optimum mesh gauge for the resistor paint application. It is necessary to understand at this point what the consistency and make-up of the resistor compound is. When the compound is thoroughly stirred and shaken, it has the consistency and appearance of a dykum ink and can be used in inking tools if used quickly before the fluid coagulates. After drying, a line resistor appears to be uniformly granular. Further tests disclosed that the smaller and more homogeneous the granules, the higher the resistance value. The heavier the line, the larger the granules appear and the less the resistance value. It is therefore necessary to obtain the proper balance and granule consistency in the dried resistor to get the proper and consistent resistance value without tailoring.

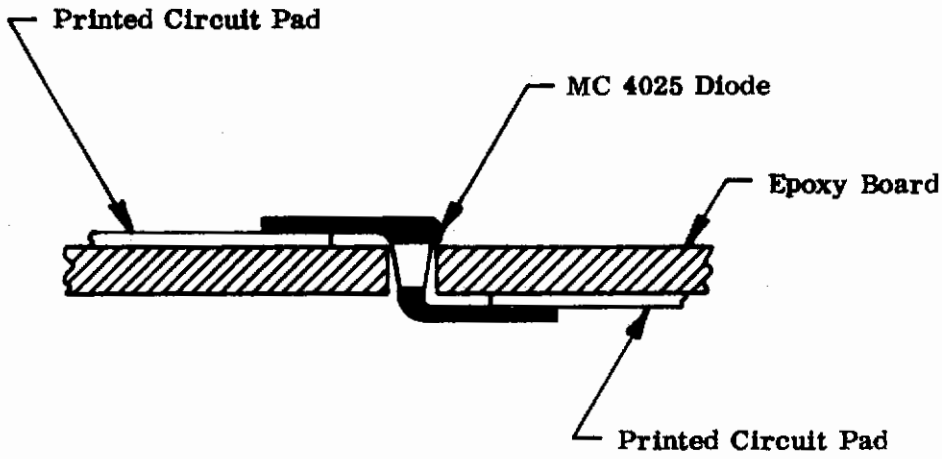


Figure 31 Diode Printed Circuit Assembly

When the various mesh screens were used to deposit the resistor paint on to an epoxy board, it was found that a screen mesh on the porous end of the range let the large granules pass through adequately but allowed too much of the fine granule fluid pass through thereby underflooding the epoxy board. Using a mesh screen on the fine end of the range eliminated the flooding and produced a well defined resistor, but it screened out the larger conductive granules and the total resistance value of the resultant resistor was much too high. All attempts at finding a correct screen mesh wound up in final or at best with inconclusive results. Other problems became apparent with a screening type process also; namely, the fast drying time of the resistor paint. Approximately 30 seconds is all the time available for pouring, screening, and screen clean-up before it coagulates to the point where it would be most difficult to clean up the screen. All of the completed printed circuit resistor-diode boards were made using "one-at-a-time" drawing tool techniques. The resistors can be produced this way surprisingly fast and accurately even though this method is certainly not the most desirable for production. For resultant low value resistors, they can be tailored up in value by narrowing the resistor line by scraping or reducing the thickness of the line, or a combination of both. Additional resistance paint can be added to a resistor line whose value is too high. To use this type of compound for thick film resistors, a wide tolerance is needed to accommodate the many variables involved. In the case of this particular switching circuit resistance, the parameters were set at 1.5 megohms while using 0.33 megohm/square/0.001 thickness formulation.

Another primary problem apparent at the beginning of the program was that of making contacts from the resistor-diode junction on the printed circuit board to the EL unit contacts. The problem was solved by using miniature compressible stainless steel wool balls. These tiny contactors were secured to the resistor side of the diode by means of a small amount of conductive adhesive. The insulating epoxy board separates the printed circuit junction and the EL contact side and has an oversize hole pattern identical to the placement of the miniature contactor balls. When the EL insulating layer and printed circuit board are registered and compressed, the oversize holes in the sandwiched insulating layer form small expansion chambers for the contactor balls to expand laterally as they are compressed longitudinally by the EL pads. The insulating layer holes also serve to isolate each of the contactor balls from each other thereby nullifying the possibility of 800 volt arcing.

The second category of mechanical effort was for the design and packaging of the control unit. This unit is housed in a standard 19 inch wide by 18 inch high by 18 inch deep cabinet.

The power supplies, logics nest, power switching network, voltmeter, panel switches and controls, along with the circuit breaker, A/D converter, and cabinet cooling fans are housed in this cabinet. Basic power is 120 volts ac-400 hz. All cabinet in and out connections are accessible from the rear. The original intent was to package the necessary electronics in the cabinet so as to have excess space for air movement inside the cabinet. As the circuitry evolved and became more complex and bulky, the inside space available lessened and the density and weight increased. From the start of the program, no effort was made to miniaturize any portion of the control unit since this was not a requirement.

SECTION VI

EL PANEL DEVELOPMENT

Because of the specialized nature of the program, it was necessary to have special EL panels built. This effort was undertaken by Hartman Systems Company.

It was determined that two basic configurations would be required, the bar graph and the numeric. One panel type could be used for the bar graphs, line graphs and the rate field displays.

The bar graph panels would require a total of 160 lines with a resolution of 32 lines per inch. The transparent conductor would be divided into ten segments with 16 lines associated with each. The display could then be driven as a 10 x 16 matrix. In addition, the panels were to be of gapless construction, use high-contrast techniques, have an anti-reflective coating, and provide the desired mechanical and contact configuration to permit ready replacement.

The major problem encountered during panel fabrication consisted of developing a suitable sealing technique in conjunction with the requirement for 170 exposed contact areas. This required considerable effort and many experiments.

Another problem concerned itself with the gapless technique. It was found that a large differential in brightness existed between the alternate EL lines due to the voltage drop across the insulating material used in the gapless construction. Experiments were then conducted to determine a suitable material possessing the required insulating capability and a more desirable dielectric constant.

Although not completed prior to the conclusion of the contract, the final EL panel configuration consisted of a glass substrate on which the desired pattern in the transparent conductive coating was accomplished by scribing the lines on a Pratt and Whitney Coordinate Measuring Machine. The high-contrast filter used was a HSC development. Sealing of the lamp employed the use of a solid plastic with the rear contacts consisting of copper tabs connected to the lamp by means of conductive epoxy.

Further refinement in the lamp construction was required before the final lamps could have been completed.

SECTION VII

CONCLUSIONS AND RECOMMENDATIONS

Although this program was not carried to completion, most of the original objectives have been accomplished. Effort progressed to the point of being able to attain a packaging configuration for the display panels which would permit decoding, memory, switching and EL panels to be contained within the required one-half inch depth. Methods were developed for the assembly of the diode dice and deposited resistors which made this depth possible.

On the basis of the progress made to date, several areas of further development would be desirable. Completion of the final assembly would provide the necessary evaluation of the system. During the program it became apparent that additional effort is required in the area of electroluminescent panel fabrication in order that all of the desired features (gapless, brightness, contrast) may be incorporated into one panel. Many additional applications are also suggested as a result of attaining the small display volume. The EL panel could be mounted on one edge of the multilayer assembly for use where panel space must be kept to a minimum. Another area of investigation would be that of developing a standard panel similar to the bar graph display and have interchangeable sensor-interface modules which plug into the display unit.

The ability to operate the display units from a common digital buss also lends itself to applications where the same type of data must be viewed at several different locations.

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13. ABSTRACT

A research and development program to design a reliable and inexpensive solid-state display control and logic circuit integrated with advanced electroluminescent displays capable of withstanding flight test evaluation is described. A basic system utilized a diode, resistor, electroluminescent cell integrated array. A control scheme incorporated an x, y switching arrangement with switches capable of operating at 800 volts peak at 400 hz. This array was backed up by integrated circuit logic and memory capabilities to provide a compact and efficient display package. Advanced techniques were employed in fabricating printed circuit boards and the multilayer assembly. A power change-over circuit was developed which permitted operation from 115 volts ac, 400 hz or 28 volts dc. A bar graph type electroluminescent panel, gapless display, was to be used with nine display packages and four numeric panels with five display blocks to make up the system along with a master control matrix.

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Electroluminescent Elements						
Aircraft Displays						
Display Systems						
Electroluminescent Control						

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(PAGE 2)

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