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CATHODE RAY TUBE CENTERED HSI

By

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FOREWORD

This report was prepared by Astronautics Corporation of America, Milwaukee, Wisconsin, under Air Force Contract F33(615)-57-C-1316, on "Modified Horizontal Situation Indicator". See last page.

The studies presented herein were begun in December 1966, and were completed in February 1968.

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This technical report has been reviewed and is approved.

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ABSTRACT

The contract study demonstrated that the electro-mechanical elements in the center section of a Horizontal Situation Indicator (HSI) could be successfully replaced by electronically generated symbols on a cathode ray tube, thus allowing the HSI to be used as a multi-mode display for future requirements of the Air Force.

The course pointer, vertical deviation bar, horizontal deviation bar, and the TO/FROM indications were generated by digitally programming an UP/DOWN counter for both the X and Y axis. The outputs were converted to CRT sweep voltages by a digital to analog converter. The generated symbol set was rotated with respect to aircraft heading by resolving the X,Y sweep voltages.

A flyable prototype was successfully constructed and delivered to the Air Force Flight Dynamics Laboratory.

This abstract has been approved for public release; its distribution is unlimited.

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CHAPTER I

INTRODUCTION

Display Requirements - Current Horizontal Situation Indicators (HSI) provide the display shown in Fig. 1. The center section is constructed of a complex arrangement of mechanically driven parts and meter movements. The entire card assembly inside the heading numerals (A) is mechanically driven by the aircraft heading reference servo. The horizontal deviation bar (B) is driven left/right by the output of the omni/localizer radio receiver which detects the difference between the aircraft's actual position compared to the selected course set-in (C). This bar is mechanized as a simple DC meter movement. The TO/FROM indicator (D) is driven by a phase detector in the omni/localizer receiver which detects when the aircraft has crossed a line that is perpendicular to the course line selected, and which passes through the ground transmitter. This is indicated using a DC meter movement with a mask between the two states. The vertical deviation bar (E) is driven up/down by the output of the glide slope radio receiver which detects the difference between the aircraft's actual position and the glide slope defined by the ground-based radio transmitter. This bar is also a simple DC meter movement.

The problems associated with this mechanization are:

a. The entire center section must be servo driven.

Figure 1 - AQU-4/A Horizontal Situation Indicator (Modified)

Since the mass is large, a strong servo is needed with a resultant increase in system weight, power consumption and heat.

b. Since the center section rotates, both deviation bars and the TO/FROM indicator will experience gravity and aircraft vibration accelerations in all possible axis. Thus, an almost impossibly perfect counter-weight balancing is required to prevent objectionable oscillation of the meter movement.

c. The package density prohibits any additional functions without major redesign of the entire instrument.

The solution to these problems defined in this paper is to replace the center section with a three inch diameter cathode ray tube and generate the symbols electronically. In this way, large rotating masses and meter movements are eliminated. The potential for providing many addition functions such as destination or threat symbology, and missile TV modes is inherent in the display design.

The form of the electronically generated symbols is defined in Fig. 2. The various portions are labeled to correspond to the parts that they replace in Fig. 1. It should be noted that the heading pointer (A) has a 60^{o} generation angle, so that it can readily be distinguished from the 45^{o} angle of the TO/FROM indication (D). Also, the vertical deviation bar is generated with a smaller length than the horizontal deviation bar. This makes it easier to distinguish the two at the various rotated positions. The vertical and horizontal bars are blanked to provide two dots on either side of center. These are required to advise

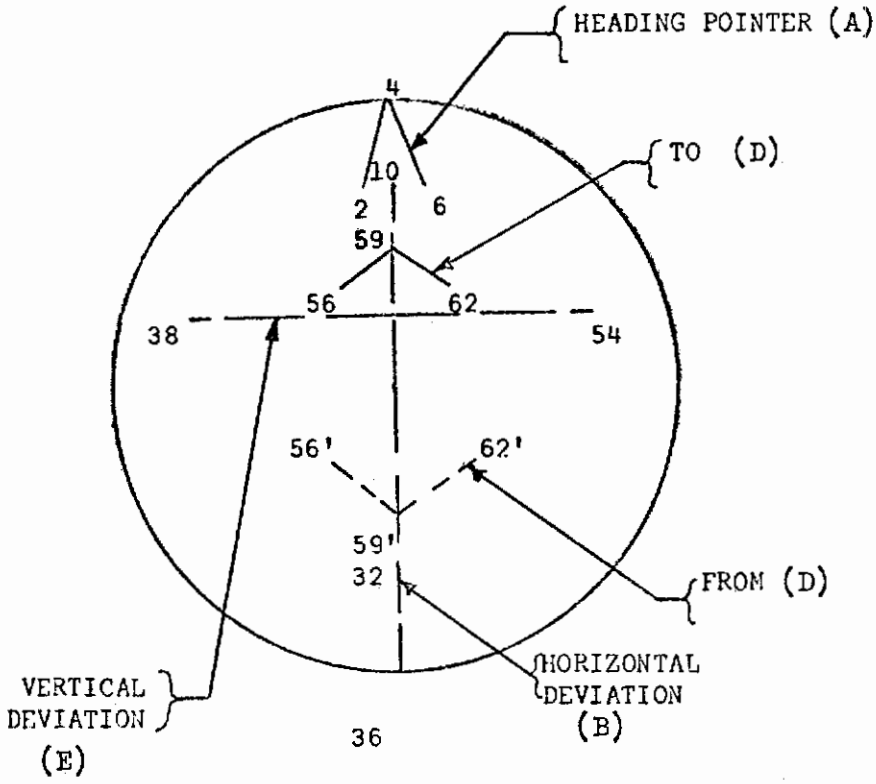


FIG. 2 - CRT - HSI DISPLAY

the pilot as to the extent of deviation from the required flight path; for in the later stages of an instrument approach, it will be impossible for the aircraft to reach the runway if the aircraft has strayed more than one dot from center. Since the deviation bars are quite sensitive, the system must be designed to limit the display of deviation to just past the two dot indication; otherwise they would be driven off scale in the early stages of the instrument approach.

Possible Standard Approaches - Previous approaches to generating symbols on CRT indicators resolve into two major classes: Blanked TV Raster or Blanked X-Y Deflection systems. The oldest and most widely used TV Raster system is the monoscope technique (1). The general operation is defined in Fig. 3. The monoscope is basically a small CRT (1" dia x 3" long), in which the phosphor is replaced by a mask over a coating that provides secondary emission electrons. The operation of the system is to provide a TV sweep in synchronism with the X-Y TV raster on the display CRT tube. Typically, the monoscope symbol provides only a small portion of the total raster, thus the X'-Y' coordinates of the monoscope are generated only around the X_c and Y_c command inputs. The concept can be shown for the heading pointer (A). In Fig. 3 it is noted that $X_c = 0$, $Y_c = 1.5$ inches. Thus, as the overall X, Y raster sweeps through the dashed area, unblanking video pulses will be generated to display the cursor at the

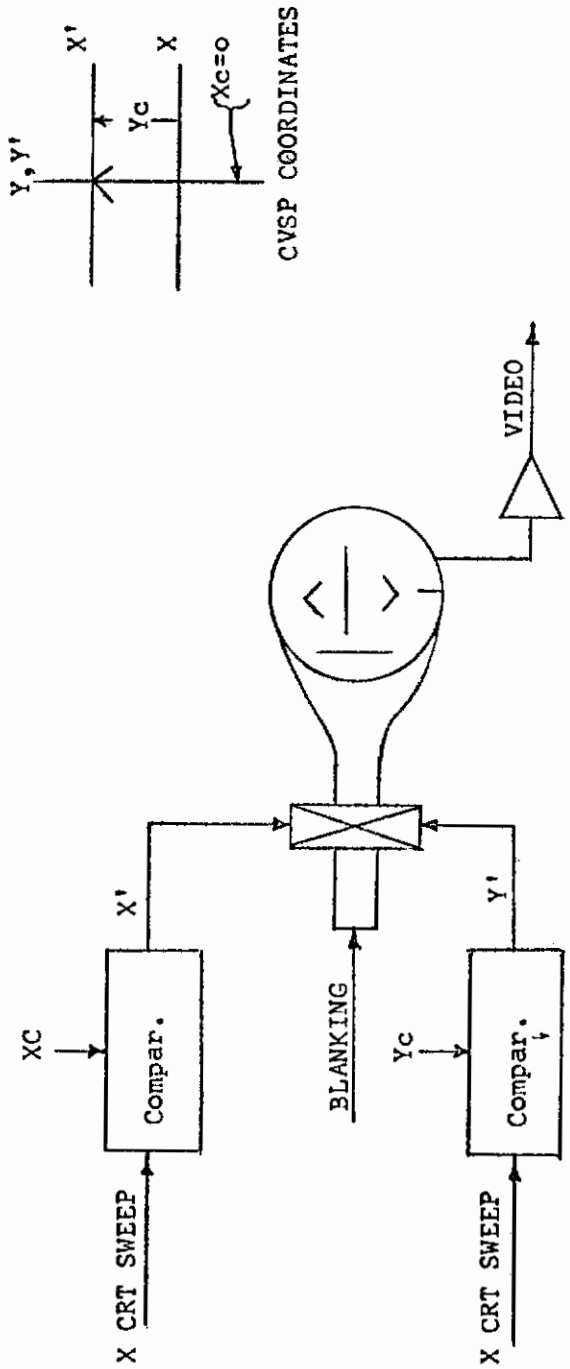


FIG. 3 - MONOSCOPE SYMBOL GENERATION TECHNIQUE

desired X_c, Y_c screen positions. In order to display the desired HSI symbology, the monoscope technique would require five symbols to be etched on the screen, and a separate symbol generator for each to define the X_c and Y_c coordinates and to define the X' and Y' area of generation scan. This would result in a bulky and complex symbol generator. Also, scan accuracy of approximately 1% on the monoscope would provide unbearable inaccuracies, when added to 1% in the display CRT. For these reasons, the monoscope technique was not chosen.

The accuracy problem was overcome by the Norden Division of United Aircraft, and the Federal Aviation Agency (2,3) where the monoscope is repla ced by a digitally programmed symbol generator. In this scheme, the basic X,Y coordinate system is defined by the system clock and binary counters. The X_c and Y_c command coordinates are converted to X' and Y' as before, and are converted into a displayed symbol, blanking pulses by use of a digitally programmed symbol matrix, composed of the desired intersections of X' and Y' coordinates. Besides requiring a separate symbol generator for each of the five symbols, this technique has a drawback that human eye resolution of 0.01 inch on the CRT would require operation at clock rates in excess of 5 M Hz. At these frequencies T^2L mirologic must be used, and great care in matching logic level delays to avoid mismatching timing into logic elements. For these reasons, the digital scheme was not used.

The most common X-Y Deflection system in use is the Stroke Generator technique (4), defined in Fig. 4. In this scheme the symbol to be generated is broken into all the possible straight-line strokes. A typical set is the sixteen strokes that are required to generate any letter or number as shown in Fig. 5. The desired symbol digital input is decoded into a gate that sums all the strokes required for that symbol. It can be seen that a 16 stroke sequence for X = 1, 2, 10, 14, 3, 4; and Y = 6, 8 will produce a 5 . In this example, the strokes are applied to a character deflection coil; however, some high speed units are connected to electrostatic deflection plates. The stroke generator technique obtains the X_c, Y_c position by applying this information directly to a second set of deflection coils. The stroke generation is normally accomplished by use of constant current capacitor charging. Although this is a simple technique, difficulty is found in obtaining long term linearity and scaling stability of the ramps. Also, since separate deflection systems are used for symbol and position, difficulty is experienced of matching scaling of the two systems. For these reasons, this technique was not used.

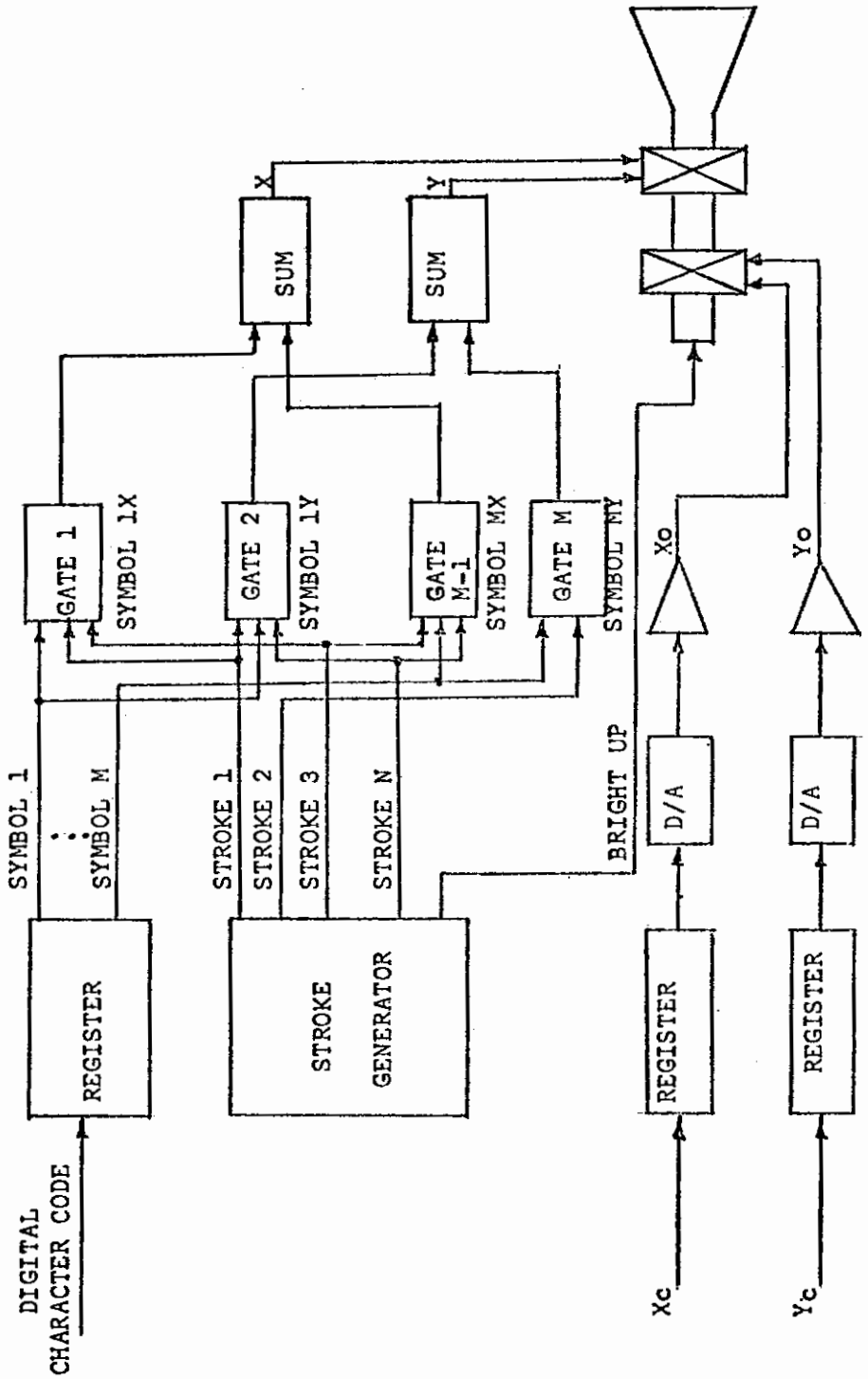


FIG. 4 - STROKE GENERATOR SYMBOL GENERATION

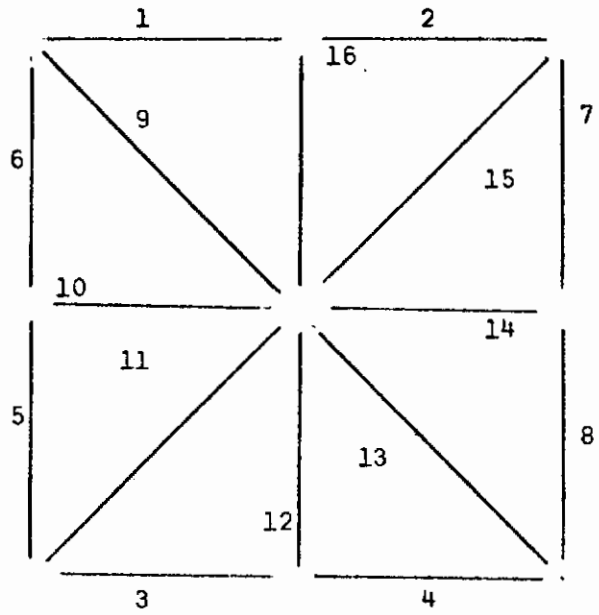


FIG. 5 - LETTER - NUMBER STROKE DEFINITION

CHAPTER II

DESIGN DEFINITION

Resultant Approach - Of the approaches discussed in Chapter I, the stroke generator provides the best system for the cost. In order to improve the long term stroke generation accuracy, and to eliminate scaling problems, the following design was developed. The overall operation is defined in Figs. 6 and 7. The basic idea is that a digital counter is programmed UP and DOWN in both X and Y after the X_c and Y_c position commands have been direct-set into the counter. The digital value is converted to an analog voltage by the D/A Converter. In this way, any symbol that is composed of a series of straight line segments can be generated. D/A ladders have excellent long term stability; therefore, change of voltage scaling with time will not present any significant problem. Also, since the X_c and Y_c position definitions and the symbology generation are both performed in the same ladder, no mis-registration between the symbol and offset can occur.

The required display shown in Fig. 2 can be visualized as a combination of simultaneous X and Y deflections of the CRT electron beam (Fig. 7). The vertical sweep is scaled so that 0 is the bottom of the CRT and 1000 is the top of the CRT. The horizontal sweep is scaled so that 0 is the left edge of the CRT and 1000 is the right edge. Since the screen is 3 inches in diameter, the scale factor is 3 inch/1000 bits = 0.003 in/bit. As shown in Fig. 2, the total vertical symbol size is 2.888 inches. This was purposely made undersize to prevent running of the

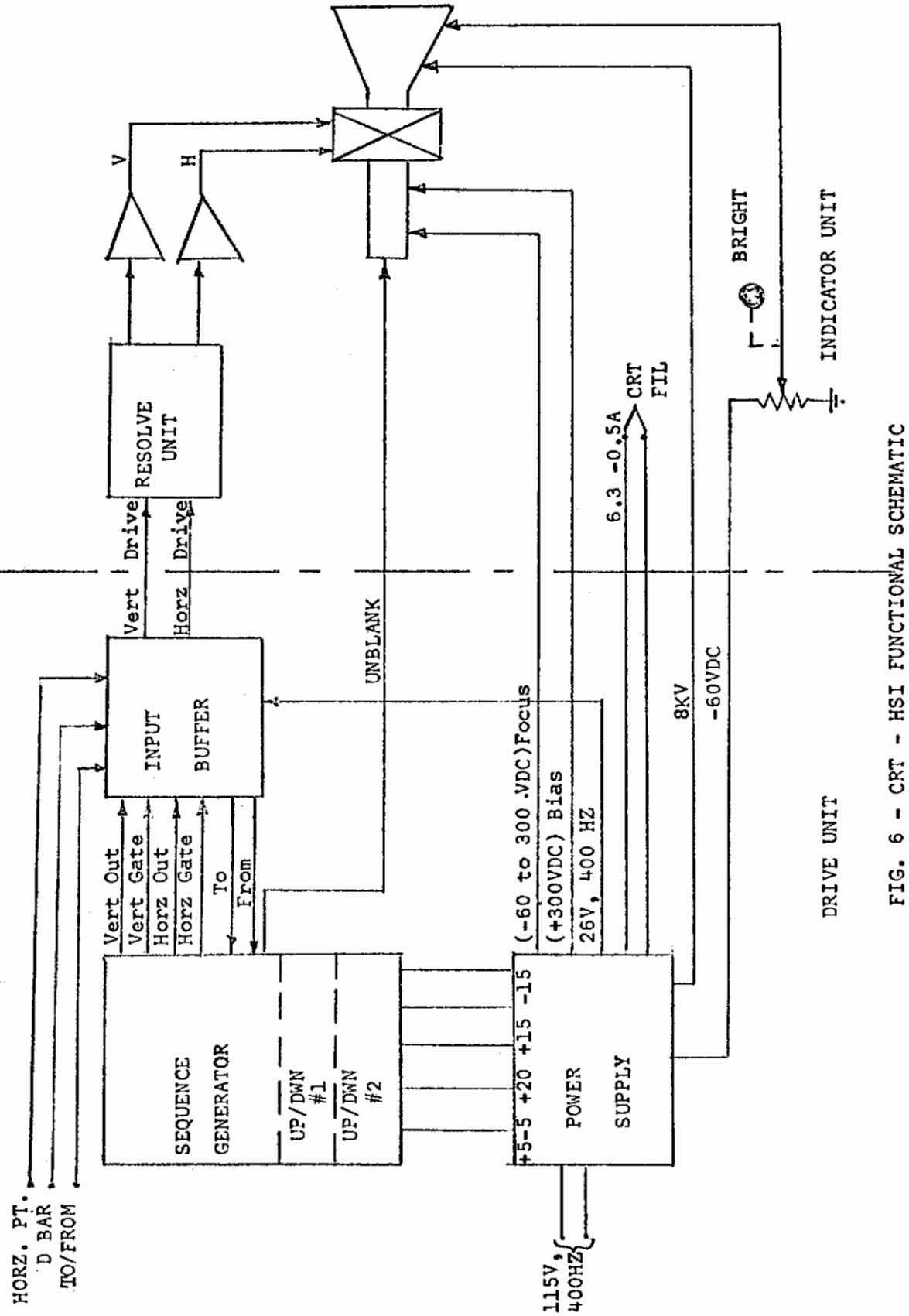


FIG. 6 - CRT - HSI FUNCTIONAL SCHEMATIC

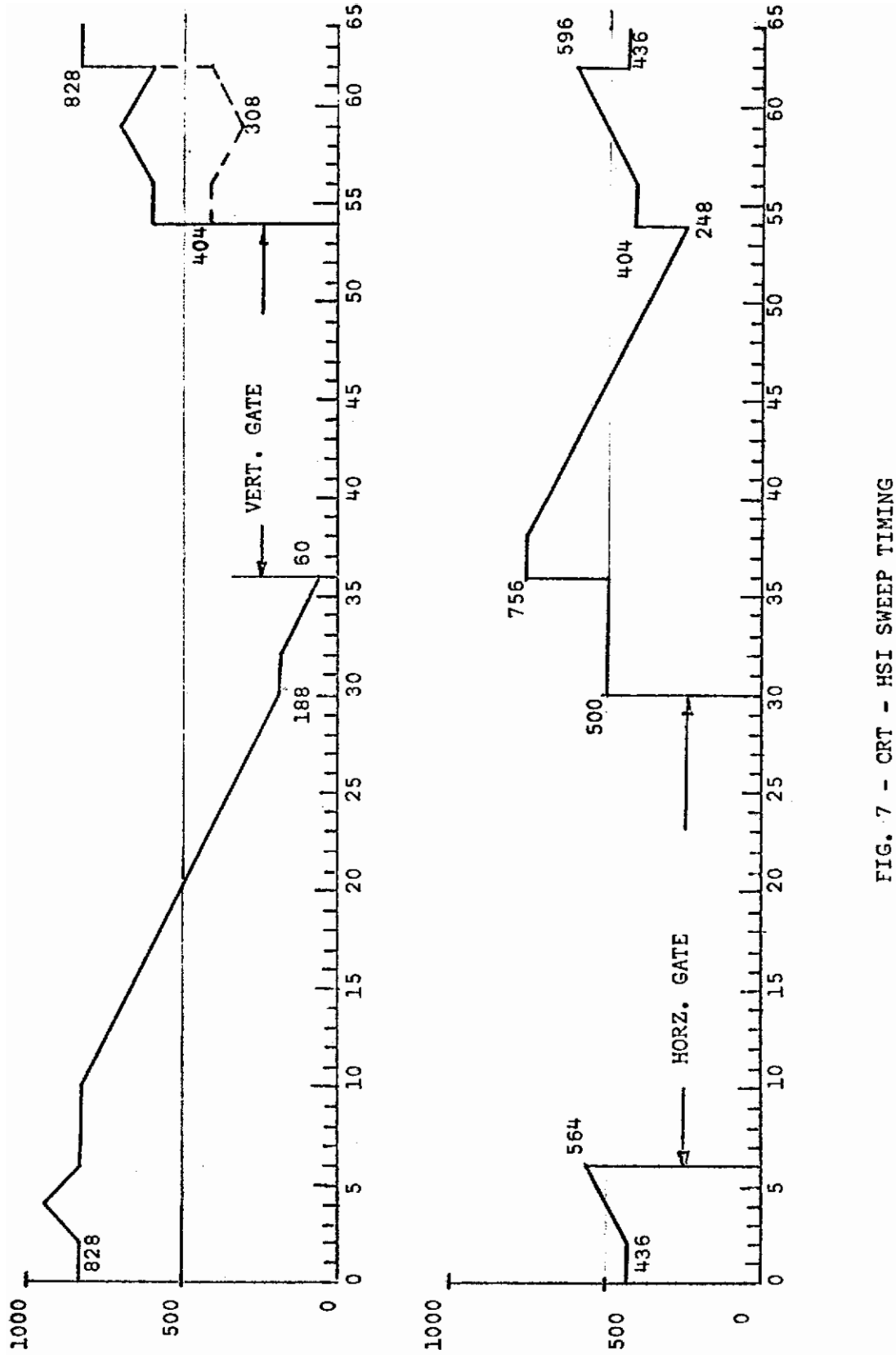


FIG. 7 - CRT - HSI SWEEP TIMING

pointer off-scale with slight changes in system scaling due to time and temperature.

The symbol generation cycle is broken into 64 segments in Fig. 7. 0 to 2 is a blanked segment that allows the D/A converter to transition to it's commanded value. During 2 to 6, the heading pointer is generated by commanding the vertical counter UP from 2 to 4 and DOWN from 4 to 6, at twice the horizontal clock rate; the horizontal is commanded UP for the entire 2 to 6 interval. From 6 to 10, the vertical counter is stopped. The horizontal counter is a "don't care" item during 6 to 30, as the horizontal deviation signal from the radio is selected by the Horizontal Gate. This provides left/right deviation of the displayed vertical line that is generated by having the vertical counter count down from 10 to 30. During time 10 to 30, the Blank signal is interrupted four times to provide two deviation markers on each side of the center. From time 30 to 32, the vertical counter is stopped and the horizontal counter is direct set to 500 (0 volts). The tail of the heading pointer is generated from 32 to 26, by allowing the vertical counter to count down while the horizontal counter remains stopped at 500. From 36 to 38, the horizontal counter is direct-set t 756 and the vertical deviation gate is initiated for an interval of 36 to 54. While the radio deviation signal is controlling the vertical, the horizontal counter counts down from 38 to 54. During this time the Blank signal is

interrupted four times to provide two deviation markers on each side of the center. Symbol generation time 54 to 62 has three possible states: TO, FROM, or $\overline{TO} \cdot \overline{FROM}$. These correspond to radio detected signals of flying toward the station, away from the station, and within the radio cone of silence, respectively. In any case, the horizontal counter is direct-set to 404 during 54 to 56, and commanded UP from 56 to 62. If the input is TO, the vertical counter is direct-set to 596, commanded UP from 56 to 59, and DOWN from 59 to 62. If the input is FROM, the vertical counter is direct-set to 404, commanded DOWN from 56 to 59, and UP from 59 to 62. If the input is $\overline{TO} \cdot \overline{FROM}$, the counters are "don't care" values, as the display will be unblanked during the interval. From 62 to 64, the vertical counter is direct-set to 828, and the horizontal to 436, to set up the system for a repeat of the cycle.

The resulting control signals required are shown in Fig. 8. The signals are:

BLANK - "0" cuts off CRT, "1" displays symbol

H GATE - "0" selects horz. D/A Output, "1" selects horz. radio deviation input.

V DWN - "0" is no command, "1" commands vertical counter in the decreasing direction.

V UP - "0" is no command, "1" commands vertical counter in the increasing direction.

H UP - "0" is no command, "1" commands horizontal counter in the increasing direction.

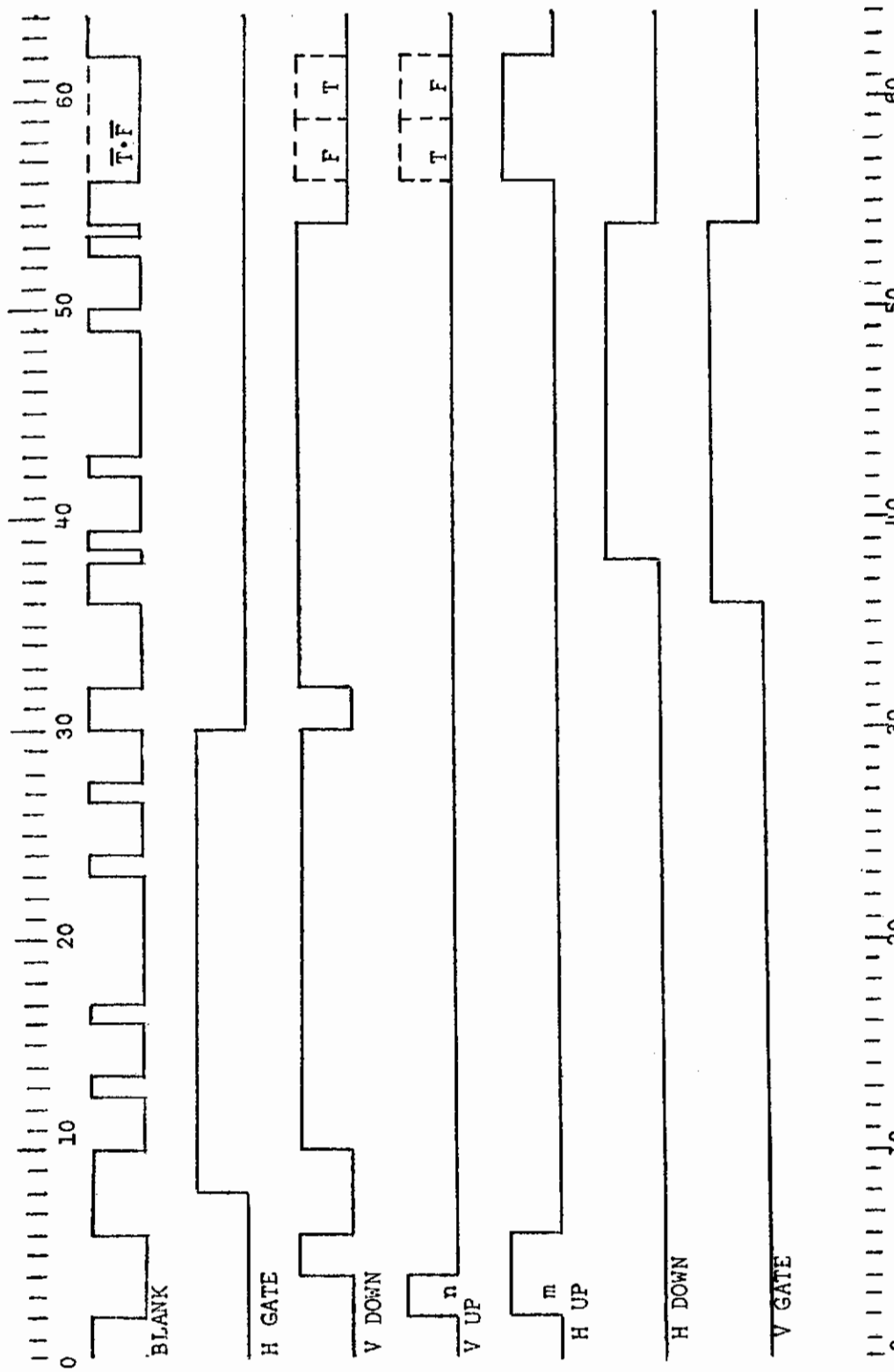


FIG. 8 - DISPLAY CONTROL TIMING DIAGRAM

H DWN - "0" is no command, "1" commands horizontal counter in the decreasing direction.

V GATE - "0" selects vertical D/A output, "1" selects vertical radio deviation input.

Times from 0 to 2, 6 to 10, 30 to 32, 36 to 38, 54 to 54, and 62 to 64, are blanked due to the fact that the vertical and/or the horizontal counters are direct-set at these times. Since the CRT is cut-off, no retrace lines will be seen, as the beam transitions from one position to the next direct-set value.

The timing chain is defined by noting that the normal vertical counting rate has a ratio of 32 bits/count. Thus, for 64 counts, the step-down from the clock must be:

(64 counts/frame) (32 bits/count) = 2048 bits frame = 2^{11} bits/frame

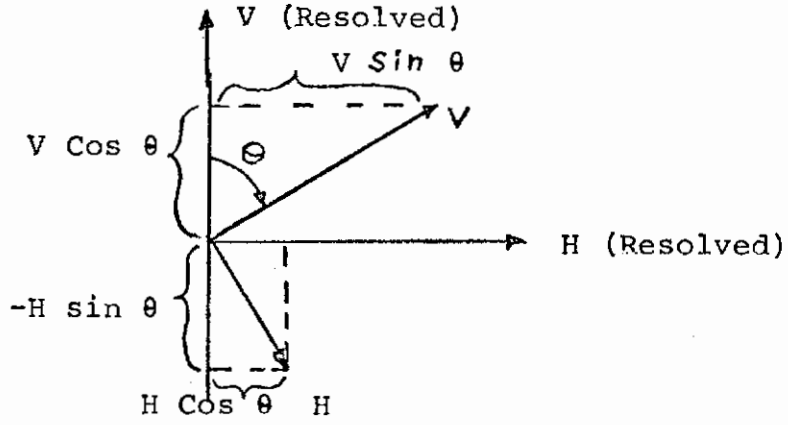
thus, an eleven stage JK flip flop set is required. Also, the vertical counter must travel twice the rate of the horizontal during time 2 to 6, in order to produce the 60 degree triangle. Thus, a 12th stage must be added to produce the double rate clock at this time.

The basic clock frequency is obtained from use of the constraint that it is desired to have approximately 60 frames/sec. to prevent the eye from detecting any flicker. The frequency of the clock at the end of the 12 bit chain is:

(60 frames/sec.) (2^{12}) = 245,760 K Hz.

Thus, the nominal clock frequency chosen was 240 K Hz. It should be noted that the clock frequency is not critical, due to the fact that a frame rate of 30 cps or lower is required before objectionable flicker is noticed by the human eye. This means that the clock could decrease all the way down to 120 K Hz.

The output of the Input Buffer Unit (Fig. 6), is that defined in Fig. 2, with vertical and horizontal deviations as commanded by the Horizontal Pointer and D Bar radio inputs. However, it is required that the system provide 360 degree rotation. This is accomplished by means of the sine/cosine potentiometer scheme shown in Fig. 9. This is derived from the coordinate rotation diagram shown below:



Thus, the resolved signals are:

$$V\ (\text{Resolved}) = V \cos\theta - H \sin\theta$$

$$H\ (\text{Resolved}) = V \sin\theta + H \cos\theta$$

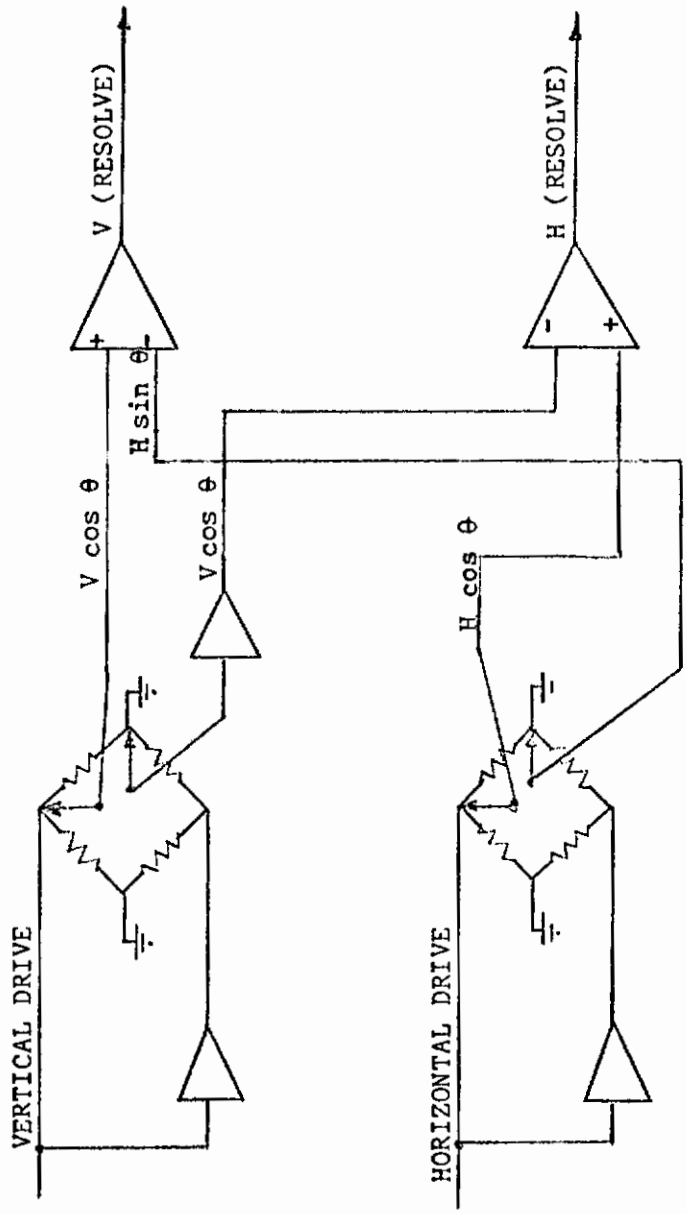


FIG. 9 - COORDINATE ROTATION MECHANIZATION

CHAPTER III

LOGIC DESIGN

Basic Timing - As defined in Chapter II, the system requires that the 240 KC clock be counted down by 2^{12}. This is mechananized as shown in Fig. 10. The schematic uses nomenclature as defined in Appendix A.

The clock is composed of one microcircuit chip, which contains two - 4 input nands. The capacitors are fed back into the extender inputs, which are connected directly into the input of the inverting amplifier of each microcircuit. The operation proceeds as follows:

If the output of (1) is 5 volts, this is applied to the base of (2) which causes it to turn on, which forces the output of (2) to a zero; thus maintaining a 5 volt output of (1). As C_2 charges at $T_2 = R_{B2}\ C_2$ through the input impedance of the base, the base current will no longer maintain the "ON" condition. When (2) turns off, this forces (1) to 0 and the delay cycle repeats for (1) with $T_1 = R_{B_1}\ C_1$. Assuming the base impedances and capacitors are equal, the operating time constant is:

$T_1 = 0.5\ C_X \times 10^{-9}$ sec.

The positive going rise time for the positive going output is approximately 20% of the positive duration, and the fall time is approximately 50 nanoseconds.

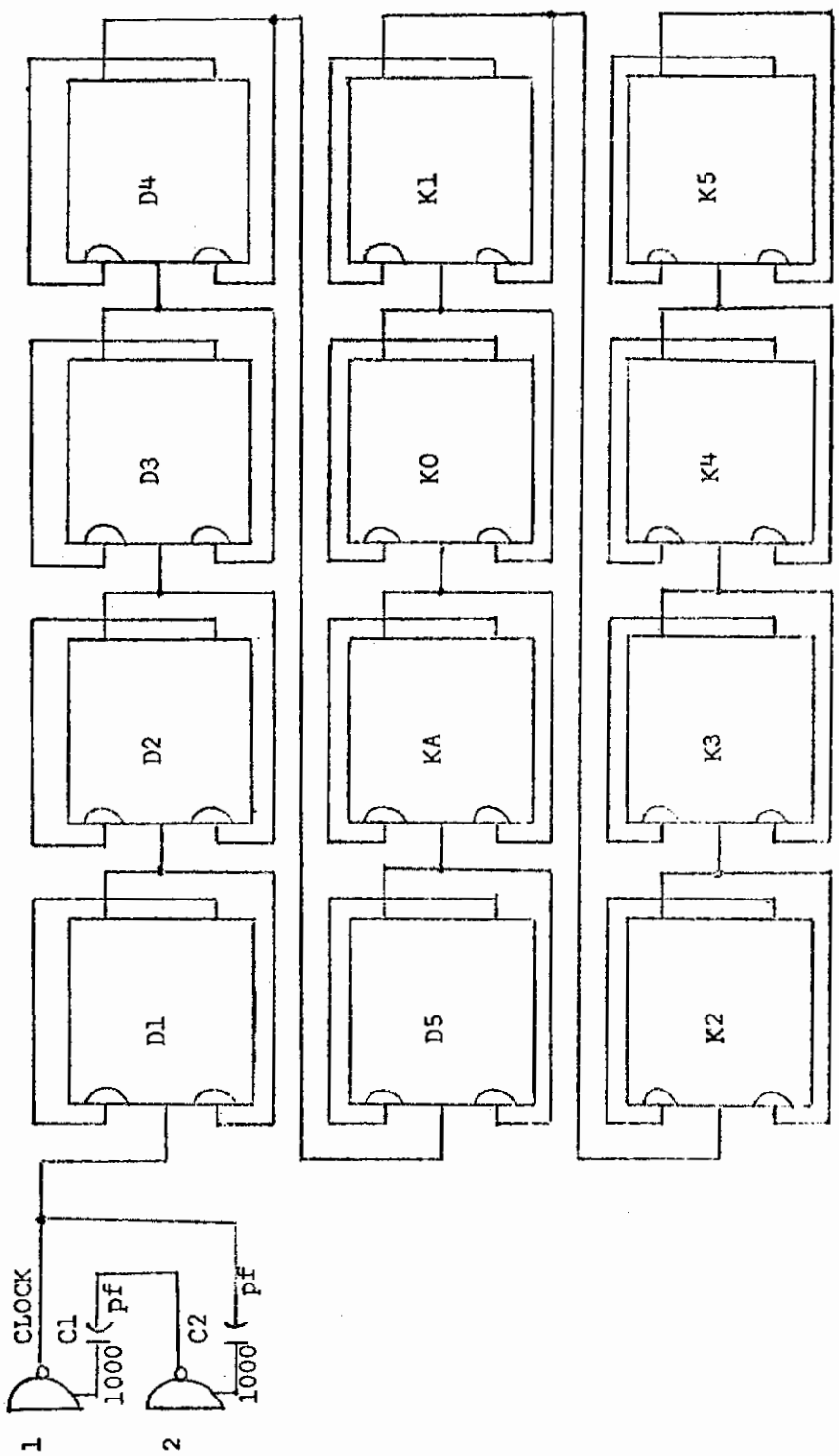


FIG. 10 - TIMING CHAIN

The frequency can be determined by the equation - $f = \frac{200}{C}$ M Hz , were C is in pico farads.

The closest standard capacitor is 1000 pf ; thus the output frequency is 200 KC. Because of capacitor variation with temperature, the output frequency will vary ± 10% over the normal operating environment. This translates into an output frame rate variation from 40 to 48 Hz. This is well above the lower frame rate of 30 Hz, that would be noticeable to the human eye. Therefore, no temperature compensation is provided. The clock waveform is shown in Fig. 11.

The division of the clock output by 2^{12} is obtained by using the flip flops D1 to K5. Each of the flip flops has the $\overline{Q}$ output connected to the S1 input and the Q input connected to the C1 input. If the Q = low and $\overline{Q}$ = high, the fall of the clock will set Q = high and $\overline{Q}$ = low. Every fall of the clock will then reverse the output of the flip flop to produce a divide by two function. The Q output of each flip flop is used as the clock for the next, thus frequency of the K5 output = clock frequency/2^{12} . The limiting timing resolution in the system is the generation of the blanking of the deviation bars into four dots. This requires the KA output; thus the Q and $\overline{Q}$ outputs

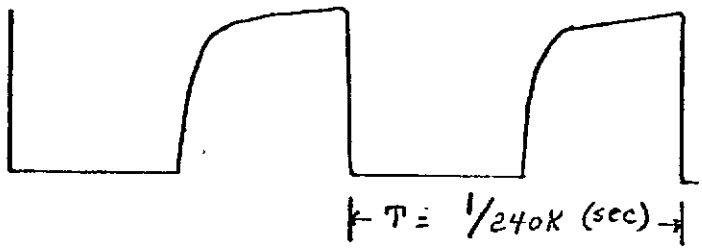


Figure 11

Clock Waveform

from KA through K5 are brought out.

Up/Down Counter - The UP/DOWN Counter design requires three - 4 bit binary coded decimal (BCD) registers to control three - 4 bit D/A converters in the range of counts from 0 to 1000. If the outputs of each 4 bit counter are defined as F1 to F4 which are the least significant bit (LSB) to the most significant bit (MSB), the required counting set is:

F4	F3	F2	F1	Ouput
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

The system to be mechanized uses the clocked Set (S) and Clear (C) inputs of the master-slave flip flop defined in Appendix A. S and a clock transitions Q to a "1". C and a clock transitions Q to a "0". These transitions for F1 through F4 are shown as follows:

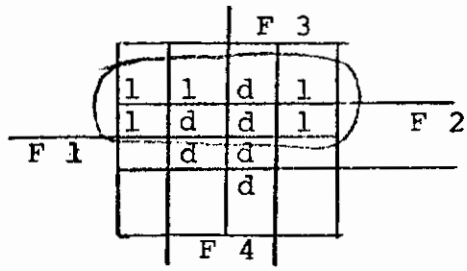
	F4	F3	F2	F1	U	D
Set 1	0	0	0	0	1	d
	0	0	1	0	1	d
	0	1	0	0	1	d
	0	1	1	0	1	d
	1	0	0	0	1	d
	0	0	0	0	d	1
	1	0	0	0	d	1
	0	1	1	0	d	1
	0	1	0	0	d	1
	0	0	1	0	d	1
Reset 1	0	0	0	1	1	d
	0	0	1	1	1	d
	0	1	0	1	1	d
	0	1	1	1	1	d
	1	0	0	1	1	d
	1	0	0	1	d	1
	0	1	1	1	d	1
	0	1	0	1	d	1
	0	0	1	1	d	1
	0	0	0	1	d	1

	F4	F3	F2	F1	U	D
Set 2	0	0	0	1	1	d
	0	1	0	1	1	d
	1	0	0	0	d	1
	0	1	0	0	d	1
Reset 2	0	0	1	1	1	d
	0	1	1	1	1	d
	0	1	1	0	d	1
	0	0	1	0	d	1
Set 3	0	0	1	1	1	d
	1	0	0	0	d	1
Reset 3	0	1	1	1	1	d
	0	1	0	0	d	1
Set 4	0	1	1	1	1	d
	0	0	0	0	d	1
Reset 4	1	0	0	0	d	1
	1	0	0	1	1	d
Carry	0	0	0	0	d	1
	1	0	0	1	1	d

It should be noted that UP and DOWN commands cannot occur simultaneously. Therefore, when one is "1", the other is "don't care" (d).

FF1 Logic - A look at the Set 1 logic shows that there are really only 5 transition points, and that the U and D inputs subsume into don't cares. The four flip flop output states can then be drawn on a Veitch diagram (5).

Set 1

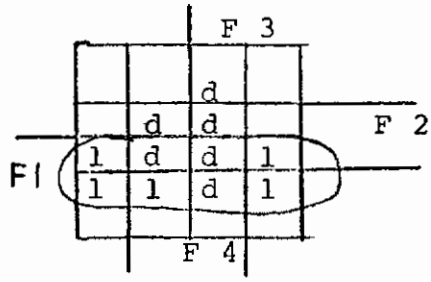


The minimum cover is found to be:

$$\text{Set 1} = \overline{F\ 1}$$

A look at the Reset 1 logic shows that the outputs again subsume to only 5 transitions with U and D inputs being don't cares. These are plotted as:

Reset 1

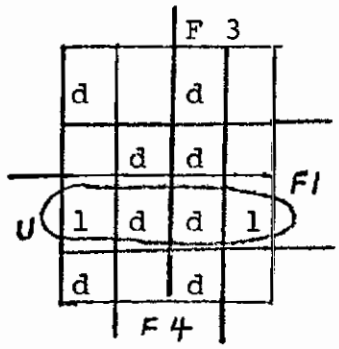


The minimum cover is found to be:

$$\text{Reset 1} = F\ 1$$

FF2 Logic - A look at Set 2 logic shows that $\overline{F2}$ is a common factor and can be broken into three sub-arrays:

	F4	F3	F2	F1	U	D
7	0	0	d'	1	1	d
	0	1	d'	1	1	d



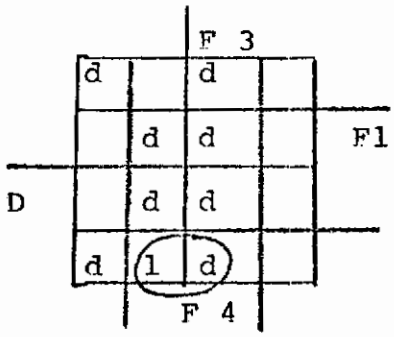
By inspection, F3 subsumes; therefore -

$$7' = U \cdot F1$$

However, a later use in the reset requires a smaller cube; thus the value is defined as:

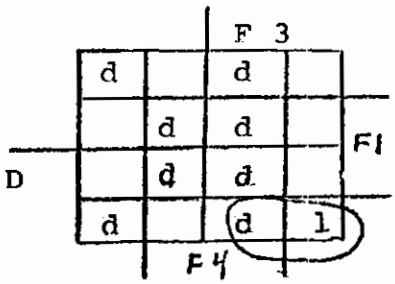
$$7 = U \cdot F1 \cdot \overline{F4}$$

	F4	F3	F2	F1	U	D
6	1	0	d'	0	d	1



$$6 = D \cdot \overline{F1} \cdot F4$$

	F4	F3	F2	F1	U	D
9	0	1	2	0	d	1



$$9 = D \cdot \overline{F1} \cdot F3$$

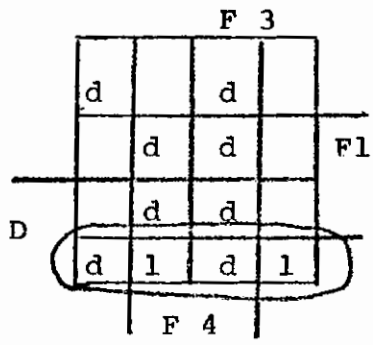
Thus, Set 2 = 7v 6v 9

The Reset 2 logic shows that F2 is a common factor and can be broken into the following sub-arrays:

	F4	F3	F2	F1	U	D
7	0	9	d'	1	1	d
	0	1	d'	1	1	d

This is the same as 7 for the Set 2 logic.

	F4	F3	F2	F1	U	D
19	0	1	d'	0	d	1
	0	0	d'	0	d	1



$19 = D \cdot \overline{F1}$

Thus, Reset 2 = 7 v 19

FF 3 Logic - The Set 3 logic can be recognized to contain a common factor $\overline{F3}$, and the two remaining cubes subsume into the following array:

F4	F3	F2	F1	U	D
d'	d'	d'	d'	1	d
d'	d'	d'	d'	d	1

This could be mechanized with only UvD, but due to use of a common cube with Reset 3, the first cube can be covered by -

5 {d' d' 1 1 1 d}

The second cube can be covered by using 6 from the FF2 Set logic:

6 {1 d' d' 0 d' 1}

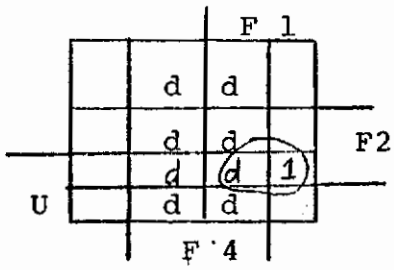
$6 = F4 \cdot \overline{F1} \cdot U$

Thus, Set 3 = 5v6

The Reset 3 logic has a common factor F3, and the remaining cubes subsume into the form -

F4	F3	F2	F1	U	D
0	d'	d'	d'	1	d
0	d'	d'	d'	d	1

The first cube can be plotted as:

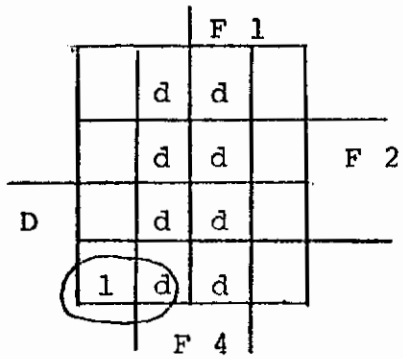


It can be seen that 5 from Set 3 logic can be used as a cover if F2 and F1 don't cares are assigned a value of 2.

	F4	F3	F2	F1	U	D
5	d'	d'	1	1	1	d

5 = F2 · F1 · U

The second cube can be constructed by assigning F2 and F1 don't cares as "0".



The cube can be mechanized as:

	F4	F3	F2	F1	U	D
4	d'	d'	0	0	d	1

4 = $\overline{F2}$ · $\overline{F1}$ · D

Thus, Reset 3 = 4v5

FF4 Logic - The Set 4 logic subsumes into the following array:

F4	F3	F2	F1	U	D
0	d'	d'	d'	1	d
0	d'	d'	d'	d	1

By assigning F1 and F2 the value of "1", it can be seen that the first cube can be realized as:

3 { 0 d' 1 1 1 d }

3= $\overline{F4}$ • 5

By assigning F1, F2, and F3 the value "0", the second cube can be realized as:

2 { 0 0 0 0 d 1 }

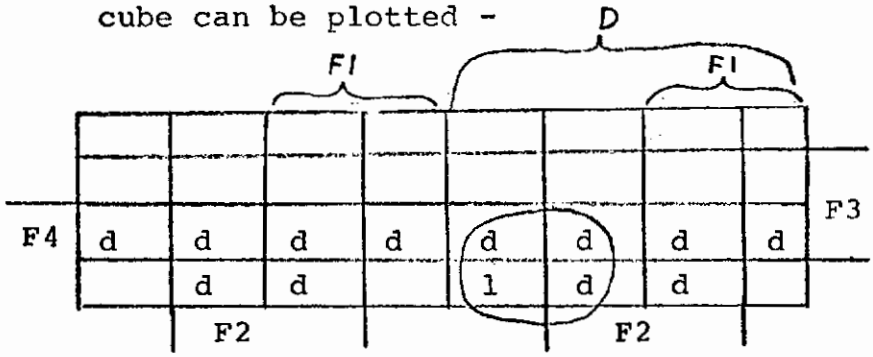
2 = $\overline{F4}$ • $\overline{F3}$ • 4

Thus, Set 4 = 2v3

The Reset 4 logic subsumes into the following array:

F4	F3	F2	F1	U	D
1	0	0	d'	d	1
1	0	0	d'	1	d

By assigning F1 to a value of "0", the first cube can be plotted -

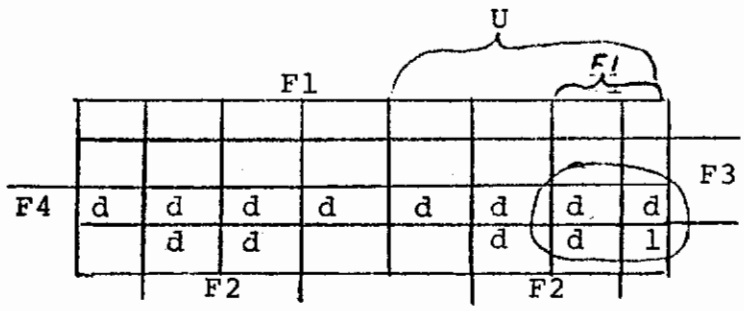


The first cube can then be realized by recognizing form 6 of the Set 2 logic:

6 { 1 d' d' 0 d 1 }

6 = F4 • $\overline{F1}$ • D

By assigning F1 to the value of "1", the second cube can be plotted -



The second cube can be realized as:

$1\{1\ d\ d\ 1\ 1\ d\}$

$1 = F4 \cdot F1 \cdot U$

Thus, Reset 4 = 1v6

By inspection, it is easily seen that the carry is made up of the "OR" of 2 of Set 4 and 1 of Reset 4.

Thus, C2 = 1v2

The resulting decade counter is shown schematically in Fig. 12. A total count from 0 to 999 is obtained by connecting three counters in series. The first counter (1's) uses the system clock as the CL input. The second counter (10's) uses the carry (C2) of the 1's counter as it's CL input. Finally, the third counter (100's) uses the carry (C2) of the 10's counter as it's CL input.

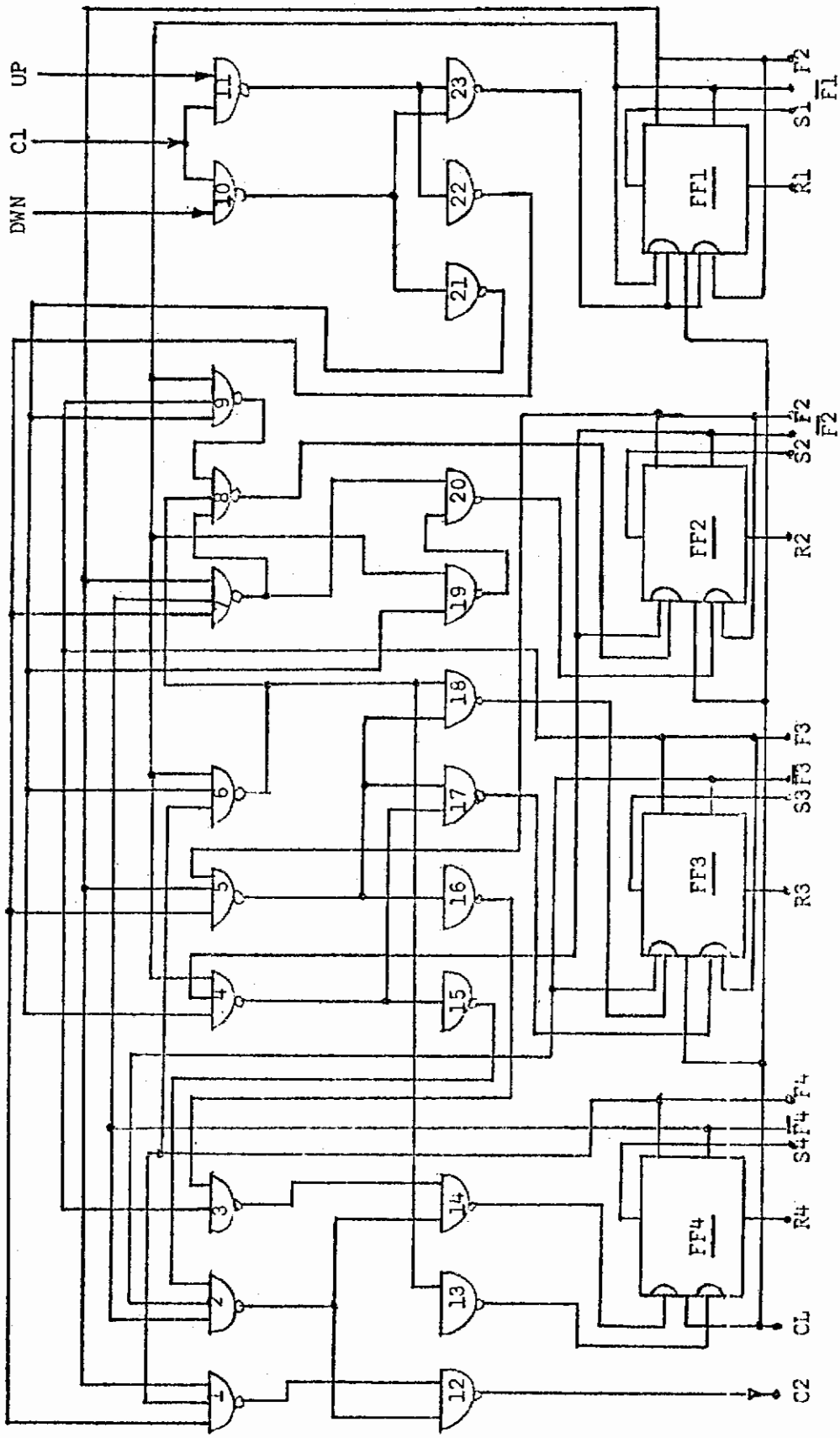


FIG. 12 - 4 BIT UP/DOWN DECADE COUNTER

Counter Control - As shown in Fig. 7, the Vertical Up/Down Counter must be direct-set to values of 828, 404, or 596. The horizontal must be direct-set to 436, 500, 756, and 404. This is accomplished by placing a "0" pulse into S1 to S4 (Fig. 12) to direct-set Q=1 in the JK flip flop or a "0" pulse into R1 to R4 to direct-set Q=). The basic change intervals can be defined aa t30 to 32 ($t\overline{31}$). t36 to 38 ($t\overline{36}$), t54 to 56 ($t\overline{54}$), and t62 to 64 ($t\overline{63}$).

The following listing defines the relationship between the set value, the reset/set JK flip flop state, and the timing:

Vertical Counter

		100 Counter				10 Counter				1 Counter			
Time	Value	4	3	2	1	4	3	2	1	4	3	2	1
T 63	828	1	0	0	0	0	0	1	0	1	0	0	0
T54(T)	596	0	1	0	1	1	0	0	1	0	1	1	0
T54(F)	404	0	1	0	0	0	0	0	0	0	1	0	0
Reset Waveform		T54	T63	S1	S2	S2	S1	T54	S2	T54	T63	S2	S1
Set Waveform		T63	T54	-	S12	S12	-	T63	S12	T63	T54	S12	-

Horizontal Counter

		100 Counter				10 Counter				1 Counter			
Time	Value	4	3	2	1	4	3	2	1	4	3	2	1
T63	436	0	1	0	0	0	0	1	1	0	1	1	0
T31	500	0	1	0	1	0	0	0	0	0	0	0	0
T36	758	0	1	1	1	0	1	0	1	1	0	0	0
T54	404	0	1	0	0	0	0	0	0	0	1	0	0
Reset Waveform		S13	-	S7	S1	S13	S7	S16	S15	S7	S17	S16	S13
Set Waveform		-	S13	T36	S17	-	$T\overline{36}$	$T\overline{36}$	S14	$T\overline{36}$	S1	$T_{\overline{63}}$	-

The S waveforms consist of the required combinations of $t\overline{31}$, $t\overline{36}$, $t\overline{54}$, and $t\overline{63}$, which are defined in Fig. 13. The basic logic timing waveforms required to generate the S terms are shown in Fig. 14. From the timing chart, it can be seen that:

$t31 = \overline{K5}\ K4\ K3\ K2\ K1$, $t36 = K5\ \overline{K4}\ \overline{K3}\ K2\ \overline{K1}$

$t54 = K5\ K4\ \overline{K3}\ K2\ K1$, $t63 = K5\ K4\ K3\ K2\ K1$

From Fig. 13 it can be seen that:

S1 = t54vt63

S7 = S1vt31

S10= S1vt36

S8 = t31vt36vt63

S14= t36vt63

S15= t31vt54

S13= S14vS15

S16= S15vt36

S3 = t54·Tvt63

S12= t54·T

S2 = t54·Fvt63

S11= t54·F

S17= t31vt36

This is realized as shown in Fig. 15.

The final set of control waveforms that must be realized are shown in Fig. 8.

The H GATE is "1" from time 8 to 30. This is most economically realized by setting a RS flip flop (Appendix A)

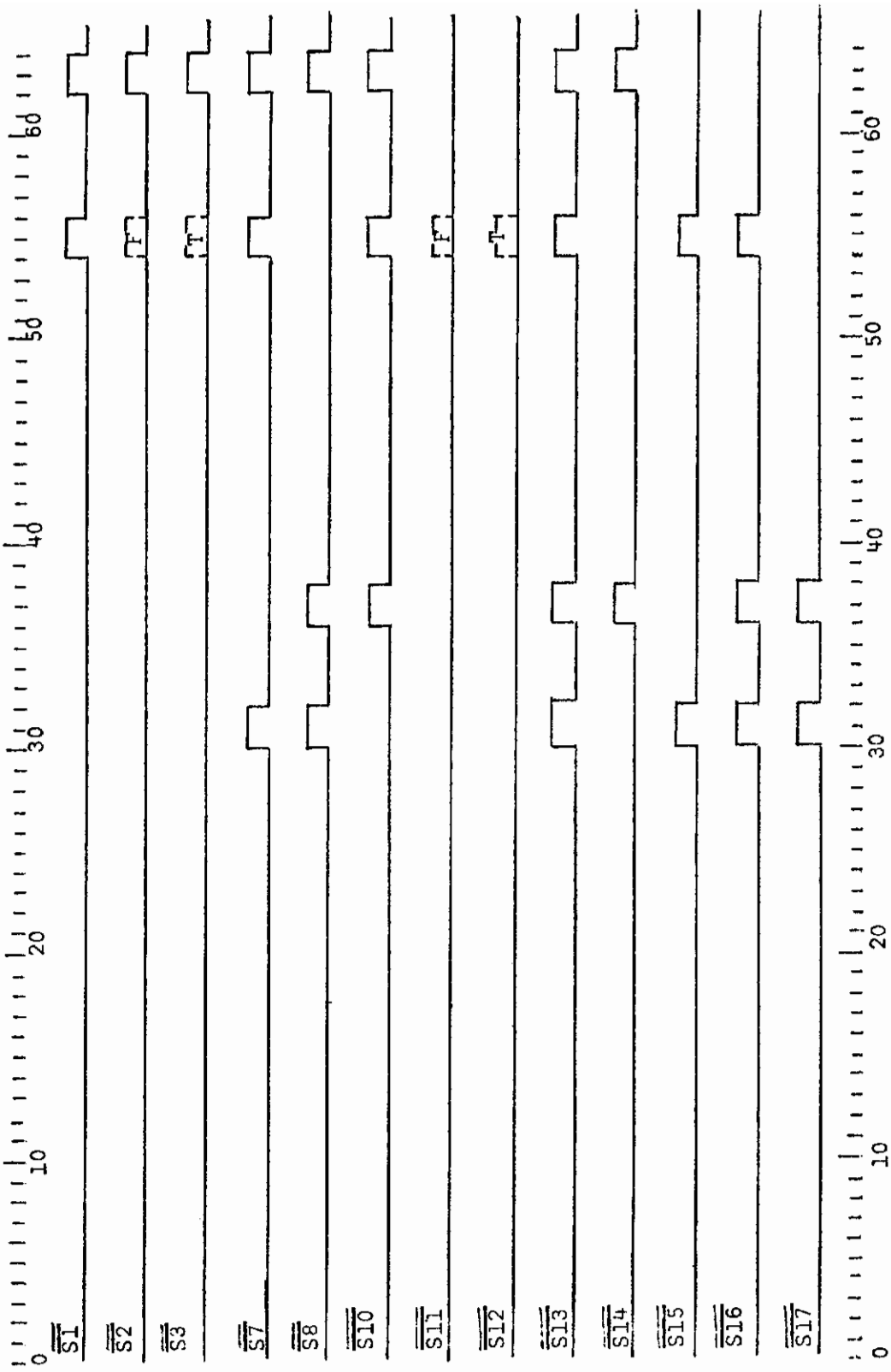


FIG. 13 - DIRECT SET TIMING WAVEFORMS

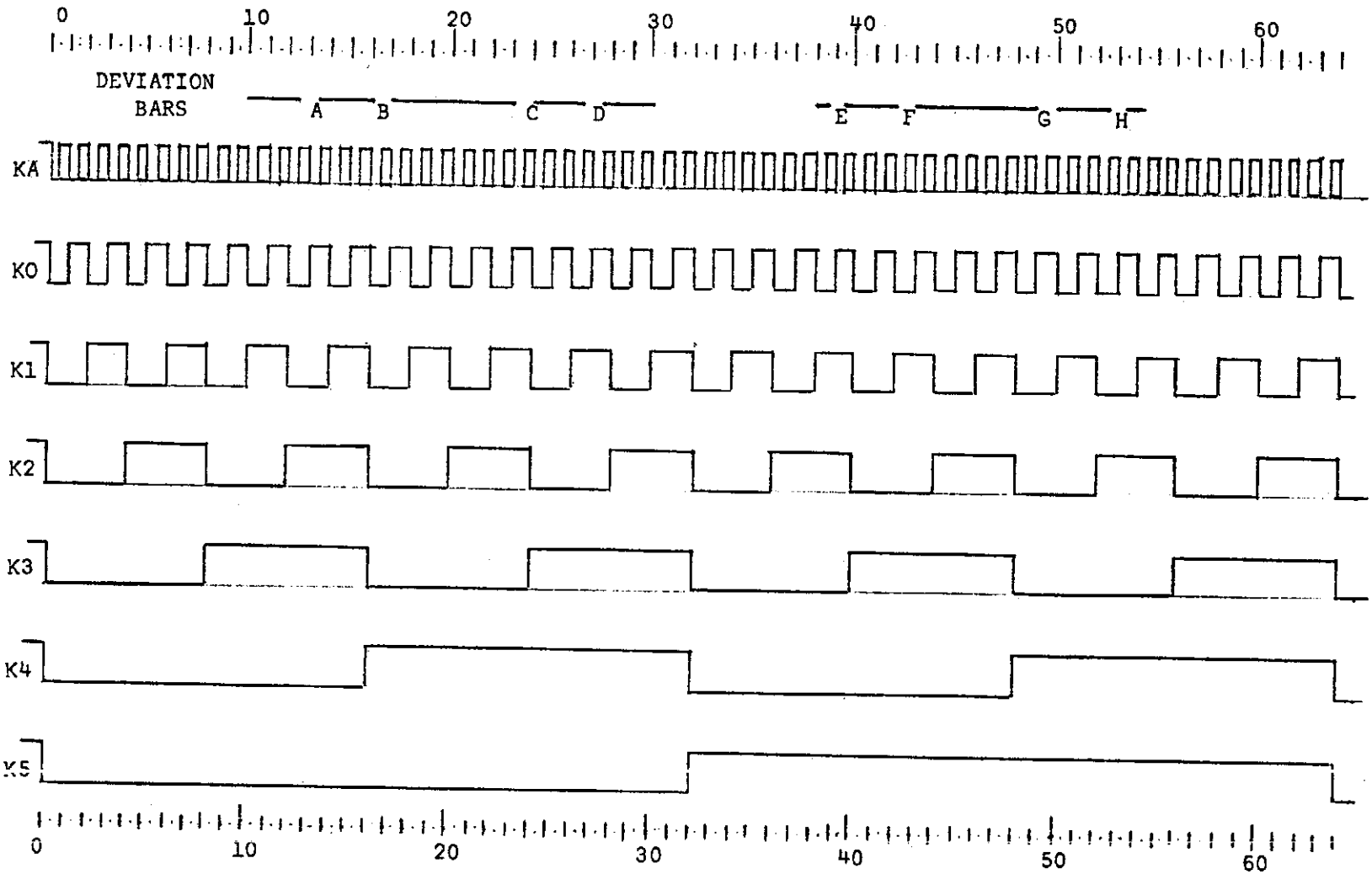


FIG. 14 - BASIC LOGIC TIMING

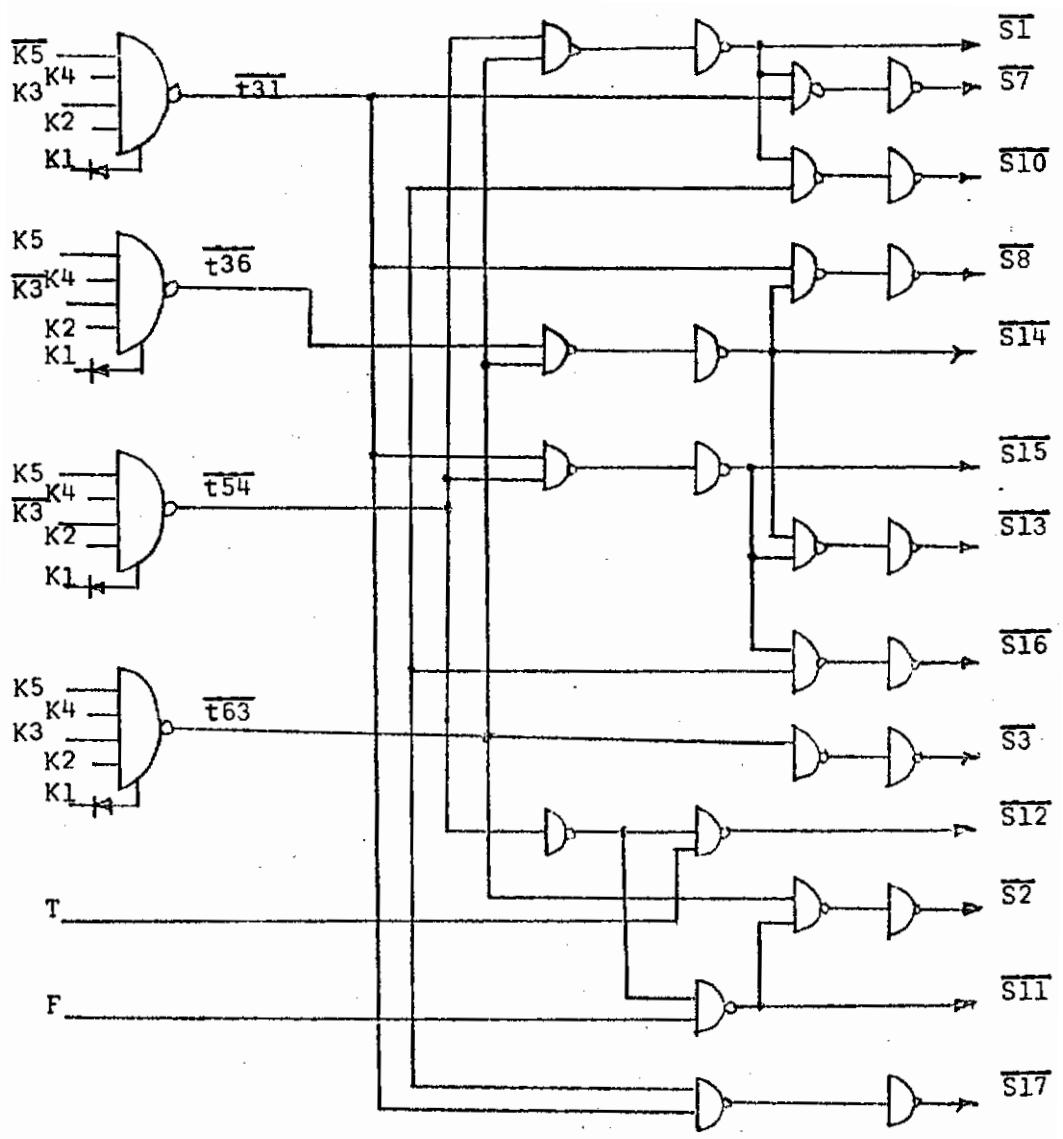


FIG. 15 - DIRECT SET GENERATION MECHANIZATION

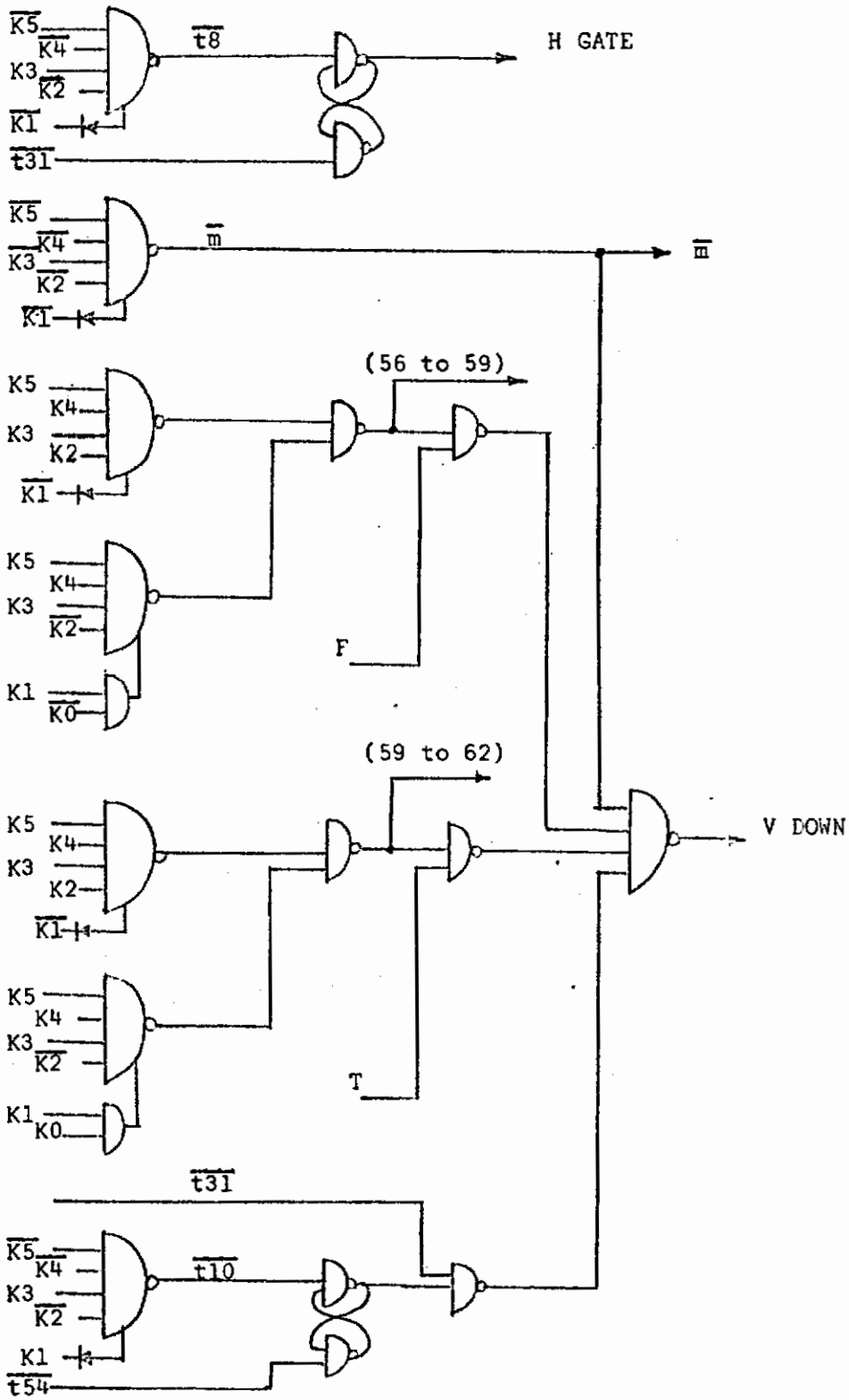


FIG. 16 - CONTROL WAVEFORM MECHANIZATION
(H GATE AND V DOWN)

using t8 = $\overline{K5}\ \overline{K4}\ \overline{K3}\ \overline{K2}$ K1 and resetting it with t31. The mechanization is shown in Fig. 16.

The V DOWN waveform can be generated by"ORing"pulse m, (interval 4 to 6), the interval 56 to 59 and F, the interval 59 to 62 and T, and the interval 10 to 54 gated by t31. It should be noted that the interval 36 to 54 is a"don't care" area; however, if V DOWN were stopped at 36, all the D/A transistors would be turned on simultaneously-which loads down the regulators to such an extent that the system does not recover during the 56 to 62 interval - with resulting objectionable distortion of the waveform. The pulse m can be expressed as: $\overline{K5}\ \overline{K4}\ \overline{K3}$ K2 $\overline{K1}$. The interval 56 to 59 and F can be expressed as F (K5 K4 K3 $\overline{K2}$ K1 v K5 K4 K3 $\overline{K2}$ K1 $\overline{K0}$). The interval 59 to 62 and T can be expressed as: T(K5 K4 K3 K2 $\overline{K1}$ v K5 K4 K3 $\overline{K2}$ K1 K0). The interval 10 to 54 can be obtained by setting a RS flip flop with $t\overline{10}$ = $\overline{K5}\ \overline{K4}$ K3 $\overline{K2}$ K1 and resetting with t54. The Q output of the RS is gated by $t\overline{31}$ to complete the generation. These four inputs are "OR" ed to form the V DOWN mechanization shown in Fig. 16.

The VUP waveform can be generated by "ORing" n = $\overline{K5}\ \overline{K4}\ \overline{K3}\ \overline{K2}$ K1, the interval 56 to 59 from the V DOWN mechanization and T, and the interval 59 to 62 from the V DOWN mechanization. The VUP mechanization is shown in Fig. 17.

The HUP waveform can be generated by "ORing" n from VUP,with n,56 to 59, and 59 to 62 from V DOWN. This is shown in Fig. 17.

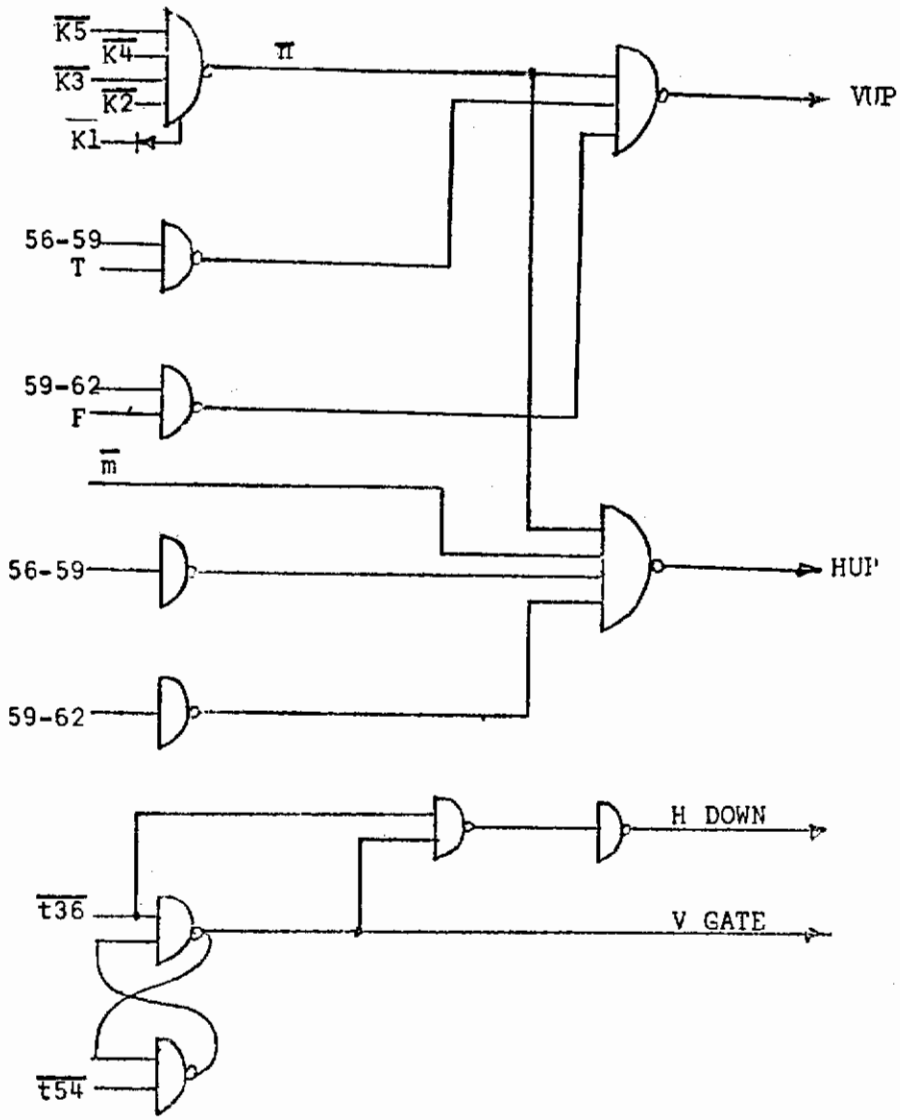


FIG. 17 - CONTROL WAVEFORM MECHANIZATION
(VUP, HUP, H DOWN AND V GATE)

The V Gate waveform can be easily realized by setting a RS flip flop with $t\overline{36}$ and resetting with $t\overline{54}$. This is shown in Fig. 17.

The H DOWN waveform can be realized by simply inhibiting the V GATE waveform with t36. This is shown in Fig. 17.

Display Blanking - The blanking of the display is composed of two parts. The first is to blank the display during the direct-set intervals, so that the transients between the two set positions will not be displayed. The second portion is to blank both the horizontal and vertical deviation bars to provide two dot deviation markers on either side of the center.

The direct-set interval blanking is accomplished as follows - the blanking from 62 to 2, and from 2 to 10, is mechanized (Fig. 18) by setting a RS flip flop with $t\overline{63}$ and resetting it with $t\overline{10}$. The output of the RS is inhibited by $\overline{m}$ and $\overline{n}$ to realize the desired function. The intervals t31, t36, t54, and t63 are realized using $s\overline{13}$. When the radio input is neither TO nor FROM, the (56 to 59) and (59 to 62) inputs from V DOWN are "anded" with $\overline{T}$ and $\overline{F}$ to provide the final input to the BLANK 1 output. At this point it can be noticed in Fig. 7 that the horizontal clock (HCL) is always 120 K Hz, and must be stopped only during the direct-set intervals; thus, HCL can be realized by

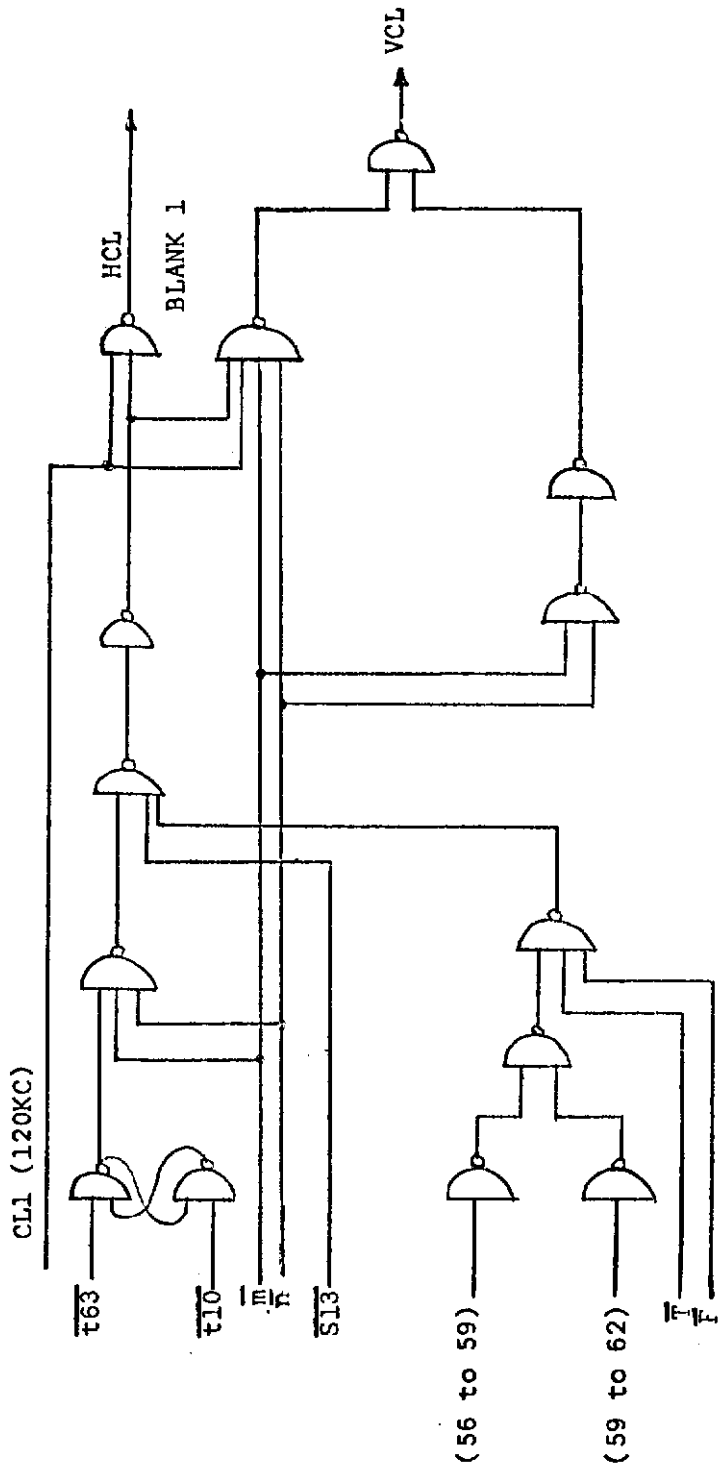


FIG. 18 - CONTROL WAVEFORM MECHANIZATION
(HCL, BLANK 1 and VCL)

gating CL1 with BLANK 1 (Fig. 18).

Also from Fig. 7, it is noted that the vertical clock (VCL) must provide 240 K Hz during time 2 to 6 and normal 120 K Hz at all other times. This accomplished (Fig. 18) by applying $\overline{m}$ and $\overline{n}$ to a nand whose output will go to "1" only during m and n times. This allows CL2 (240 K Hz) to produce a VCL output through the "OR" only during m and n times. The other part of the VCL output is produced by applying CL1 (120 K Hz) to a nand whose other three inputs inhibit the clock during intervals m, n, and S13.

The second portion of the blanking for the deviation dots can be realized from the following set of equations:

Vertical Bar Blanking

Top 2 $\left\{\begin{matrix}\overline{K5}\ \overline{K4}\ K3\ K2\ \overline{K1}\ \overline{K0}\ KA \\ \overline{K5}\ \overline{K4}\ K3\ K2\ \overline{K1}\ K0\ \overline{KA}\end{matrix}\right\}$

Top 1 $\left\{\begin{matrix}\overline{K5}\ K4\ \overline{K3}\ \overline{K2}\ \overline{K1}\ \overline{K0}\ \overline{KA} \\ \overline{K5}\ K4\ \overline{K3}\ \overline{K2}\ K1\ \overline{K0}\ KA\end{matrix}\right\}$

Bot 1 $\left\{\begin{matrix}\overline{K5}\ K4\ \overline{K3}\ K2\ K1\ K0\ \overline{KA} \\ \overline{K5}\ K4\ \overline{K3}\ K2\ K1\ K0\ KA\end{matrix}\right\}$

Bot 2 $\left\{\begin{matrix}\overline{K5}\ K4\ K3\ \overline{K2}\ K1\ \overline{K0}\ KA \\ \overline{K5}\ K4\ K3\ \overline{K2}\ K1\ K0\ \overline{KA}\end{matrix}\right\}$

Horizontal Bar Blanking

Left 2 $\left\{\begin{matrix}K5\ \overline{K4}\ \overline{K3}\ K2\ K1\ \overline{K0}\ KA \\ K5\ \overline{K4}\ \overline{K3}\ K2\ K1\ K0\ \overline{KA}\end{matrix}\right\}$

Left 1 $\left\{\begin{matrix}K5\ \overline{K4}\ K3\ \overline{K2}\ K1\ \overline{K0}\ \overline{KA} \\ K5\ \overline{K4}\ K3\ \overline{K2}\ K1\ \overline{K0}\ KA\end{matrix}\right\}$

Rt 1 $\left\{\begin{matrix}K5\ K4\ \overline{K3}\ \overline{K2}\ \overline{K1}\ K0\ \overline{KA} \\ K5\ K4\ \overline{K3}\ \overline{K2}\ \overline{K1}\ KO\ KA\end{matrix}\right\}$

Rt 2 $\left\{\begin{matrix}K5\ K4\ \overline{K3}\ K2\ \overline{K1}\ \overline{K0}\ KA \\ K5\ K4\ \overline{K3}\ K2\ \overline{K1}\ K0\ \overline{KA}\end{matrix}\right\}$

This cubical complex can be factored as defined in Miller (6). The purpose of factoring is the resulting reduction in circuitry required to realize the logical circuit and the reduction of inputs into the fan-in limited nand elements. It should be noted that we have no assurance of obtaining a minimum factored form for the complex. Some other factor set may indeed result in a simpler logic circuit. If the complex as written were realized directly using 2-4 input nands and extenders, the resulting circuit w would require 19 microcirciuts.

The factoring algorithm using masking cubes starts by defining the coordinate masking product M as:

M	0	1	x	u
0	0	u	u	u
1	u	1	u	u
x	u	u	u	u
u	u	u	u	u

We define the masking product between a pair of cubes $c^r = (c_1, c_2 \ldots cn)$ and $c^s = (d_1, d_2, \ldots dn)$ is denoted c^r Mc^s and dquals C^r $Mc^s = (C_1, Md_1; C_2\ Md_2, \ldots c_n\ MD_n)$. We call the coordinates which are u's the u part of C_M and the other coordinates the n part, calling this C_M1.

First, the equations are formed into a cubical complex in which the KA portions of Top 1, Bot. 1, Left 1, and Rt. 1 have been realized to be"don't care"cubes; therefore,have been subsumed:

	K5	K4	K3	K2	K1	K0	KA
a)	0	0	1	1	0	0	1
b)	0	0	1	1	0	1	0
c)	0	1	0	0	0	0	x
d)	0	1	0	1	1	1	x
e)	0	1	1	0	1	0	1
f)	0	1	1	0	1	1	0
g)	1	0	0	1	1	0	1
h)	1	0	0	1	1	1	0
i)	1	0	1	0	1	0	x
j)	1	1	0	0	0	1	x
k)	1	1	0	1	0	0	1
l)	1	1	0	1	0	1	0

To find the best factor (greatest column height times column width) c^r M c^s must be formed for all pairs of the cover a through l. The resulting best masking cube is picked which has the maximum number of coordinates in its x part, calling this C_{Ml}. Typical pairs are -

aMb = 0 0 1 1 0 u u
aMc = 0 u u u 0 0 u
aMd = 0 u u 1 u u u
⋮
aMl = u u u 1 0 u u
bMc = 0 u u u 0 u u

(etc.)

It can be rapidly be seen from this process that $\overline{K5}$ is the best common factor for cubes a through f. The complex is then written with the non-factored cubes on the top, then the common factor, then the factored cubes with the cubes deleted.

g)	1	0	0	1	1	0	1
h)	1	0	0	1	1	1	0
i)	1	0	1	0	1	0	x
j)	1	1	0	0	0	1	x
k)	1	1	0	1	0	0	1
l)	1	1	0	1	0	1	0
CM1	0	u	u	u	u	u	u
a)		0	1	1	0	0	1
b)		0	1	1	0	1	0
c)		1	0	0	0	0	x
d)		1	0	1	1	1	x
e)		1	1	0	1	0	1
f)		1	1	0	1	1	0

The process is repeated for the cubes under CM1 until no new factor can be found, then the process is repeated for the cubes g through l until all possible factors are found. This process resulted in the factored set as follows:

K5	K4	K3	K2	K1	K0	KA
1	u	u	u	u	u	u
	0	u	u	u	u	u
		0	1	1	u	u
					0	1
					1	0
		1	0	1	0	x
	1	0	u	u	u	u
			0	0	1	x
			1	0	u	u
					0	1
					1	0
0	u	u	u	u	u	u
	0	1	1	0	u	u
					0	1
					1	0
	1	u	u	u	u	u
		0	u	u	u	u
			0	0	0	x
			1	1	1	x
		1	0	1	u	u
					0	1
					1	0

$$\text{Blank 2} = \overline{K5}(\overline{K4}K3K2\overline{K1}(\overline{K0}KAvK0\overline{KA})vK4(\overline{K3}(\overline{K2K1K0}vK2K1K0)v$$
$$(K3\overline{K2}K1(\overline{K0}KAvK0\overline{KA}))v$$
$$K5(\overline{K4}(\overline{K3}K2K1\overline{K0}KAvK0\overline{KA})v(K3\overline{K2}K1\overline{K0})v$$
$$K4\overline{K3}(\overline{K2K1}K0vK2\overline{K1}(\overline{K0}KAvK0\overline{KA}))$$

This is mechanized as shown in Fig. 19. using 4 quad two input, 2 triple three input, and 4 dual four input microcircuits for a total of 8 microcircuits and a diode for an extender. This is a considerable improvement over the 19 microcircuits that would be required if no factoring had been attempted.

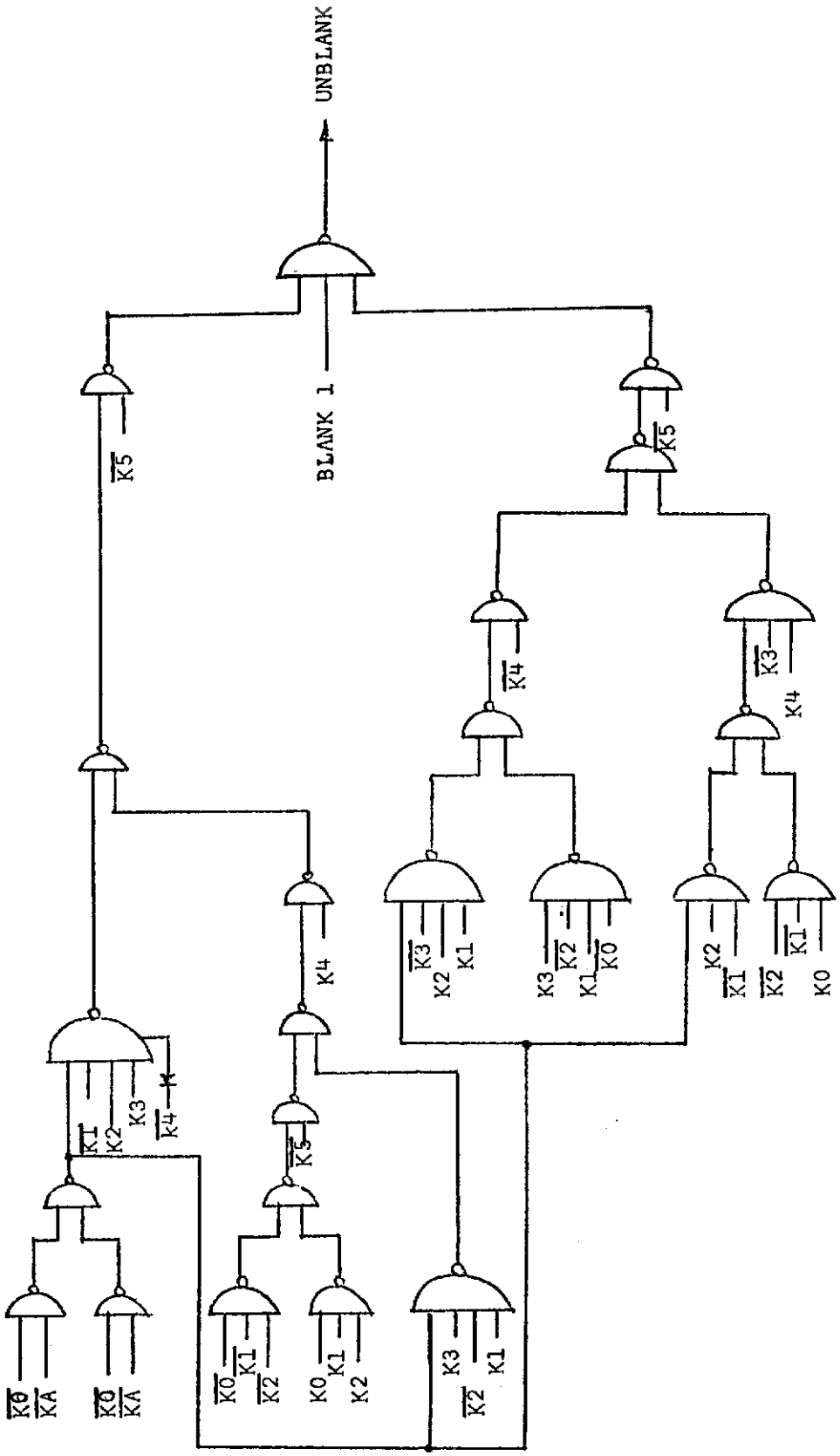


FIG. 19 - UNBLANK WAVEFORM MECHANIZATION

CHAPTER IV

DIGITAL/ANALOG CONVERTER ANALYSIS

General Requirements - The BCD D/A converter must process the three Up/Down decade counter values into a DC voltage that has 1,000 equal steps. Each of the counters has outputs F1 through F4 as shown in fig 12. Since the count is BCD, only 10 out of the 16 possible combinations are used; therefore, the + and - reference voltages of the ladder must be weighted to provide an output voltage equal to zero when the count equals 5 (0101). The 100's D/A ladder is connected directly to the D/A output to produce the most significant voltages. The 10's ladder is applied to the 100's ladder through a weighting resistor to provide 1/10 the output voltage control. The 1's ladder is applied to the 10's ladder weighting resistor through another weighting resistor to produce an additional 1/10 reduction in output control.

Weighted R Ladder - The most straightforward ladder that can be constructed is the weighted resistance ladder (fig 20) (7,8,9,10). The basic operation of the ladder can be defined by looking at the operation of Q1. If CRS is cut off, point A will be set to +5.2 volts. Thus, when the input is "0", point A will be clamped to approximately the +0.5 drop through the forward biased diode for the "0" state voltage. When the input (F4) rises to 5V, the diode will be cut off to produce the desired 5.2 volt bias in the 1 state. When the input is "0", the base voltage is -1.3. Thus, the base/emitter junction of Q1 is back biased,

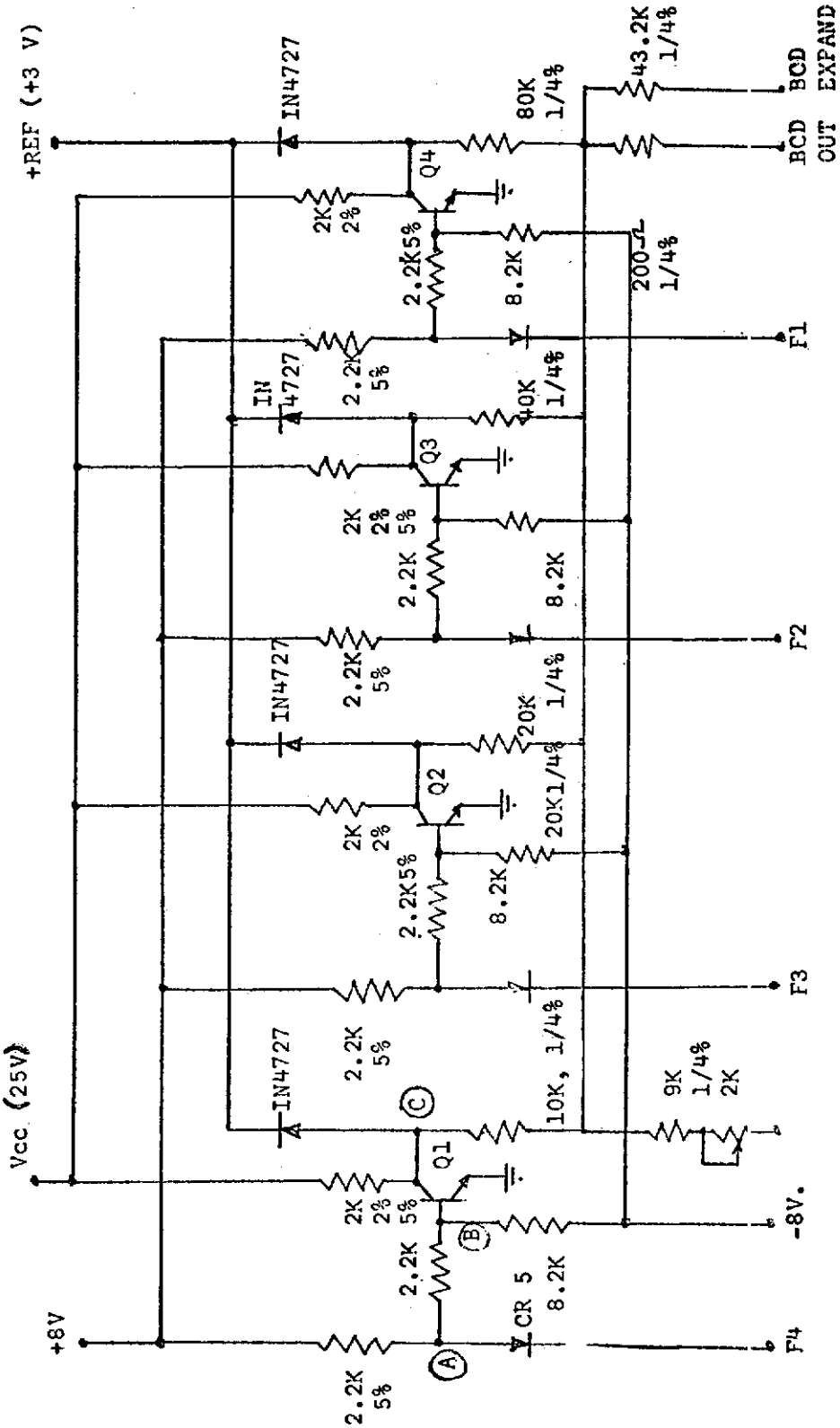
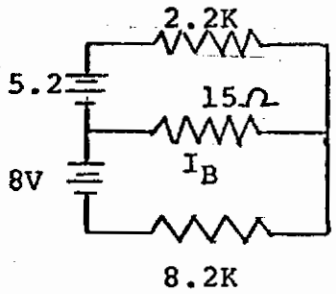


FIG. 20 - WEIGHTED RESISTOR LADDER

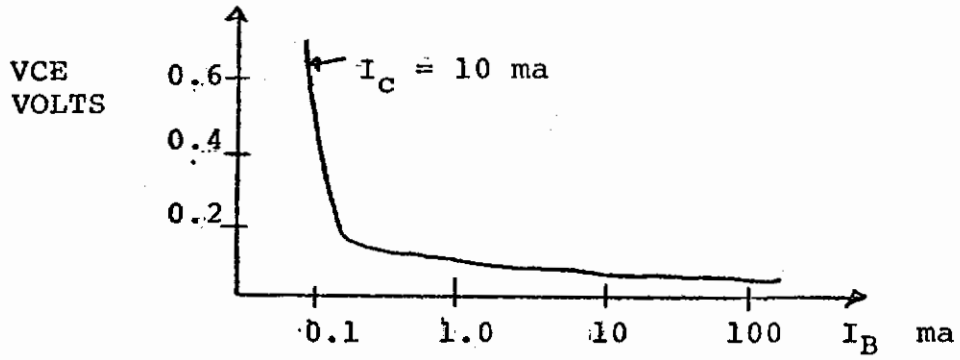
so that the collector/emitter junction is cut off. This causes point C to try to rise to +25V; however, it is clamped to approximately 3.5V by the 3V positive reference and the drop through the forward biased diode. To maintain the desired over-all ladder accuracy of 0.5%, diodes CR1 to CR4 must have matched forward voltage drops within $\pm$ 50 mv . When the input is "1", point B becomes positive such that the base/emitter junction of Q1 becomes forward biased and causes the collector/emitter junction to be clamped to nearly ground potential. The base/emitter has a nominal impedance of 15 ohms. Thus, the base current is:



$$I_B = \frac{5.2}{2.2K} - \frac{8}{8.2K} = 1.38 \text{ ma}.$$

I_C SAT = 28/R1 = 28/2K = 14 ma.

Since the 2N2219 has a B variation from 35 to 73, I_B SAT = I_C/B; 0.14 ma $< I_B$ SAT < 0.40 ma. Thus, it can be seen that the transistor is driven well into saturation by the 1.38 ma base current. The 2N2219 has a collector saturation voltage characteristic.



The saturation offset voltage contributed by V_{CE} not clamping to zero will be approximately 50 mv.

The undesirable side affect of choosing a transistor with a low V_{CE} offset voltage is that this is achieved at the expense of increased storage time. The normal turn off delay (ts) for this configuration is approximately 50 to 80 nano sec. The result of this condition in the D/A converter is an "on" overlap time due to a second transistor being turned on with a typical turn on rise time of 20 to 40 nano sec, while the previous transistor has a "0" base voltage level, but is still clamped due to storage delay. The overlap when both are "on" is approximately 40 nano sec. This causes a spike in the D/A output. A typical spike experienced in this system is shown in fig 21 for a change in the hundreds digit. Both transistors are turned on, which causes storage spike 200 mv in amplitudes. The stored charge decays to I_B SAT within 0.2 usec. At this time the transistor turns off and the voltage decays to the final value at the time constant of the external circuit within 2 usec. This characteristic limits the counter operation to f = 1/2 usec = 500 KHz. In this system the first stage counter toggles at half the clock or 120 KC; therefore, the operation of the ladder is well within the frequency limits. A Fourier analysis of the waveforms generated in the X and Y D/A ladders (fig 7) shows that very little distortion will occur when using a video bandwidth of 50KHz. Therefore, the 500KHz

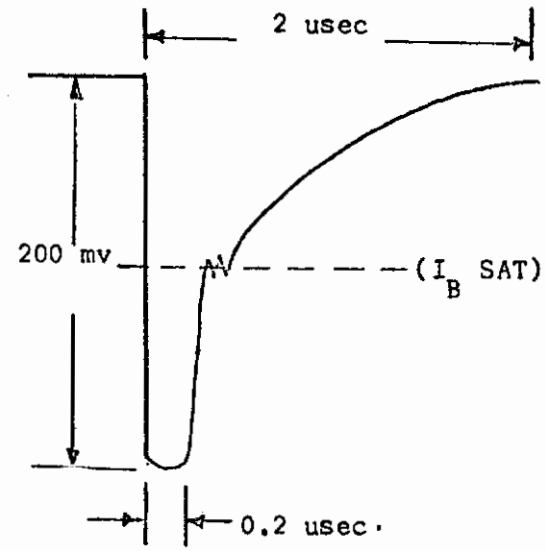


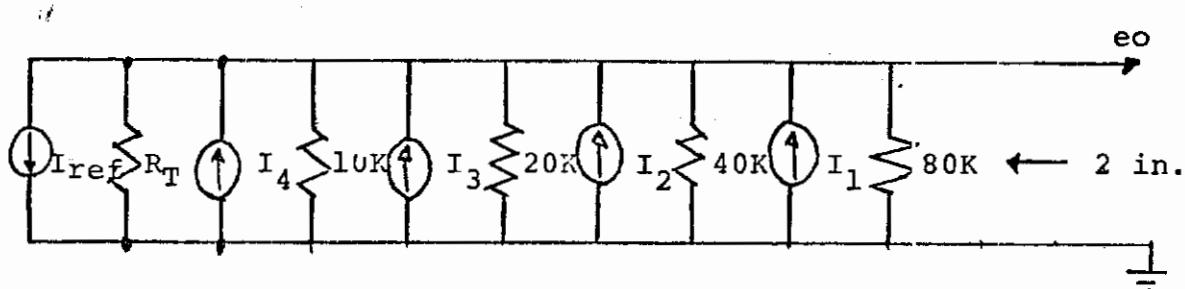
FIG. 21 - STORAGE TIME SPIKE

spikes are easily eliminated by means of a low pass filter. In this system, this is automatically produced by the inductive filtering of the Horizontal and Vertical deflection coils on the cathode ray tube.

The circuit in fig 20 can be reduced to the following equivalent circuit by constructing the Norton equivalent of each of the voltage sources and where:

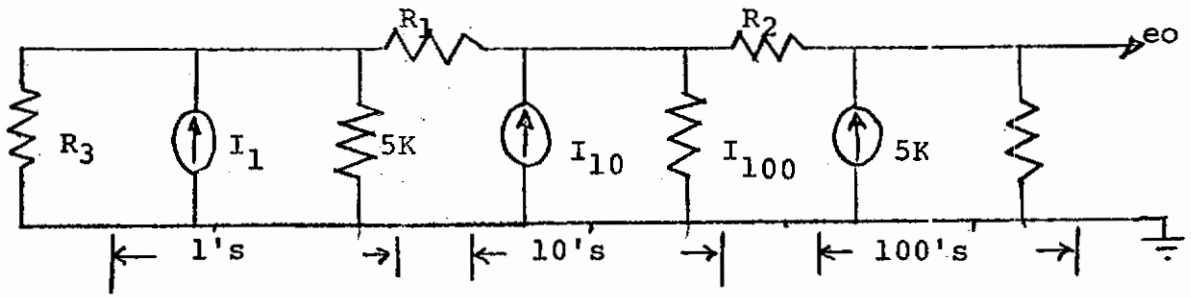
$I_{ref} = -3.5/R_1$, $I_4 = +3.5/10K$ or 0, $I_2 = +3.5/20K$ or 0,

$I_2 = +3.5/40K$ or 0, $I_2 = +3.5/20K$ or 0.

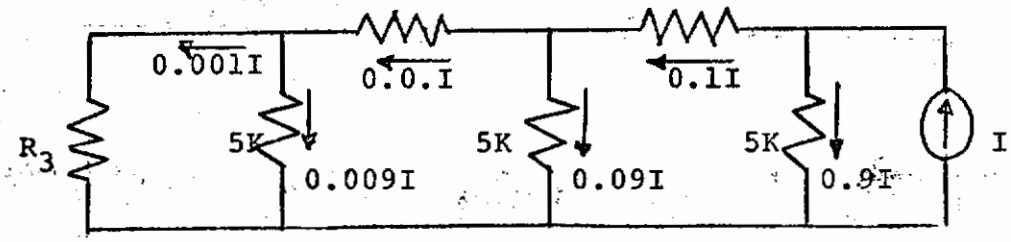


The output voltage (e_o) can be calculated by use of the superposition theorem to determine the contribution of each current generator individually. It can be seen by inspection, that the binary weighted resistors will give ten equal voltage steps for an output in response to a BCD input set. The I_{ref} adjustment will determine the bias of the output voltage.

Since R_T is nominally adjusted to 10K, the input impedance of the ladder will be 5K ohms. The expansion of the three decade ladders is accomplished as shown below:



The output current of the 100's ladder-I_{100}- is developed directly as the e_o voltage. The output current of the 10's ladder (I_{10}) is divided by 10 through R_2. The output current of the 1's ladder (I_1) is divided by 10 through the R_3R_1 network, then divided again by 10 through R_2. The values of R_1, R2, and R_3 can be determined by defining the currents through the 5K resistors to 1/10 of each other as shown below:



This yields the set of equations.

$$0.009\ I(5K) + 0.001\ I(R_3) = 0$$
$$0.001\ I(R_3) + 0.01\ I(R_1) + 0.1\ I(R_2) = 0.9\ I(5K)$$
$$0.09\ I(5K) + 0.1\ I(R_2) = 0.9\ I(5K)$$

These equations yield:

R_1 = 40.5K ohms R_2 = 40.5K ohms, R_3 = 45K ohms.

R/2R Ladder - This type of ladder (fig 22) has the advantage of only having two values of resistance; therefore, it lends itself to thin film depositing techniques. A hybrid microcircuit 4-bit ladder UT-1000 built by Sprague, is used in this system (11,12). It offers small size, low power consumption, high reliability, and ease of manufacture. The ladder consists of five 50K ohm and four 25K ohm tantalum resistors, deposited on a silicon substrate and mounted in a 0.160 X 0.265 in flat pack. Each resistor is adjusted to a tolerance of $\pm$ 0.5% and can be matched to a 0.5% spread. As a

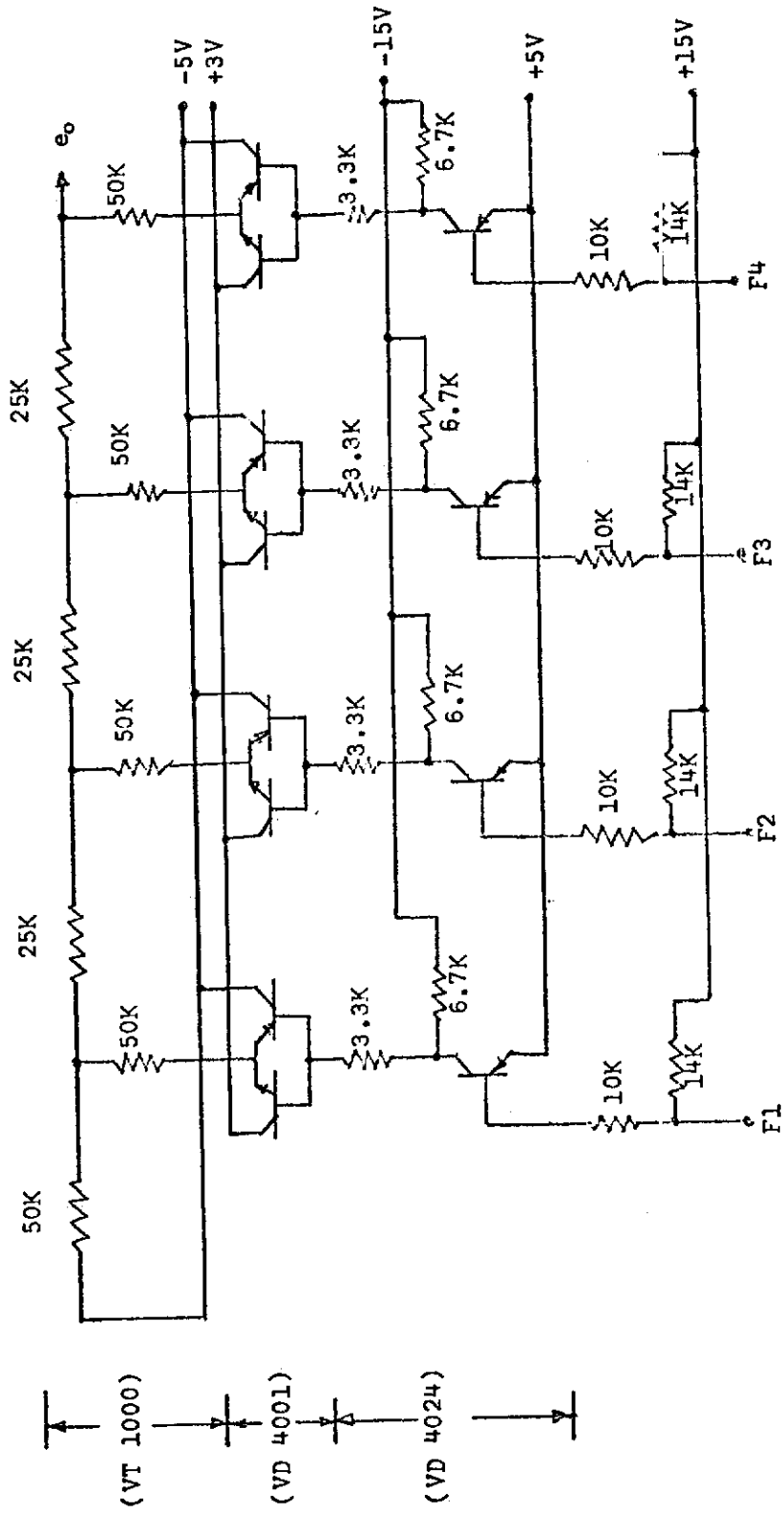


FIG. 22 - R/2R LADDER

result, the maximum analog error, due to the resistors, is ± 0.25%. This maximum error, however, occurs only when the MSB is energized and all others are off or vice versa. In actual operation, the resistors are randomly off; tolerance and bit accuracy is then much better than this worst case situation. Bit accuracy is typically 10 to 11 and results in approximately 0.05% to 0.1% error in the analog output signal.

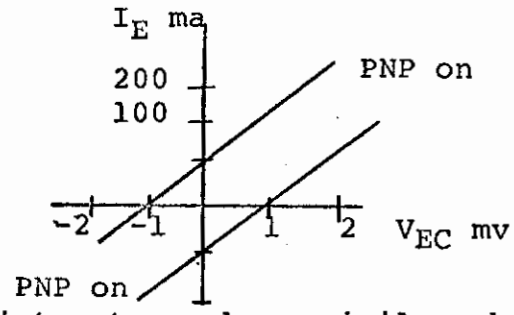
The resistances have a typical temperature coefficent of -150 ppm/°C. In actuality, the effective match of the temperature coefficients for the entire circuit is much better, as in the case of resistance value matching, often reaching a few ppm/°C. Typical output voltage variation for a 10V reference over -55°C to +125°C is 1 mv.

The settling time of the D/A converter is approximately 2 to 4 usec. Unfortunately, since the storage time of good chopper transistors, such as used in the ladder switch, is relatively long, it is difficult to produce a fast converter with low switching errors.

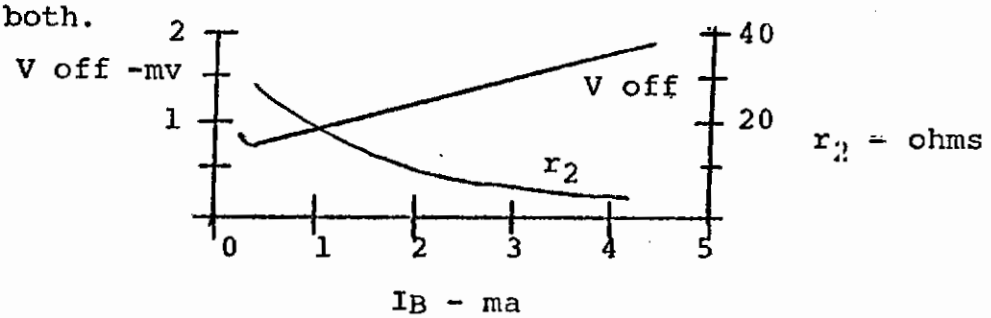
The operation of the ladder can be defined by looking at one stage of the ladder (fig 22). The buffer amplifier UD4024 is used to convert the digital input signal into positive and negative drive signals to the ladder switch (UD4001). The buffer transistor accepts "0" in the range of 0.25 ± 0.25 volts. The "1" level can vary from 1.5 to

5 volts. The positive (1) input signal from the 945 flip flop of 5V through 6K ohms causes the transistor to be cut off due to +8V developed at the base through the 14K ohm divider. When cut off, the -15 voltage supply causes base current to flow in the PNP switch base-collector to -5V. The low (0) input signal the buffer stage is turned on and provides approximately 1 ma of base current to the NPN switch to select the +3V reference voltage.

The complementary circuit was chosen for the VD4001 switch to provide the lowest possible offset voltage and to provide the ability to drive from a single line. In this configuration, the transistors are operated in the inverse direction (collector and emitter reversed) to obtain the lowest possible offset voltage. As shown in the curve below, the offset voltage is even lower because the V off and I_E (rs) components of the offset voltage are of opposite polarity.

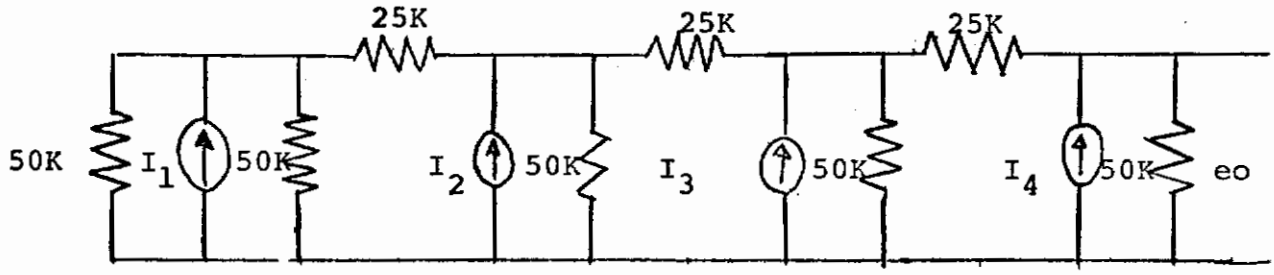


Since both transistor types have similar characteristics, the V off and I_E (rs) curves shown below are characteristic of both.



These curves show that I_P can be adjusted to yield nearly zero offset.

The circuit in fig 22 can be reduced to the following equivalent circuit by constructing the Norton equivalent of each of the voltage sources and where $I_1 = I_2 = I_3 = I_4 = +3/50K$ or $-5/50K$.



Since the ladder is symmetrical, (1/2) I_4 is provided to e_o, (1/4) I_3, (1/8) I_2, and (1/16) I_1. As with the weighted resistance ladder, it can be seen by inspection that with the F1 to F4 inputs controlled by a BCD counter, the analog output will generate 10 equal voltage steps.

Since the ladder is symmetrical, the impedance of the ladder looking in from the output terminals is found by inspection to be 25K ohms. Thus, the three decade counters will be connected identically to that of the weighted resistance ladder, except that the resistances are five times greater. Thus, the resistances are:

$R_1 = 202.5K$ ohms, $R_2 = 202.5K$ ohms, $R_3 = 225K$ ohms.

V. POWER SUPPLY DESIGN

In the CRT HSI, there are seven voltage regulators with the following output capabilities.

+3.1v @2a., +5v @2a., -5v @2a., +15v @.6a.,
-15v @.6a, +330v @1 ma., and -68v @1 ma.

There also is a 7v @.5a A.C. coil used for the CRT filament supply.

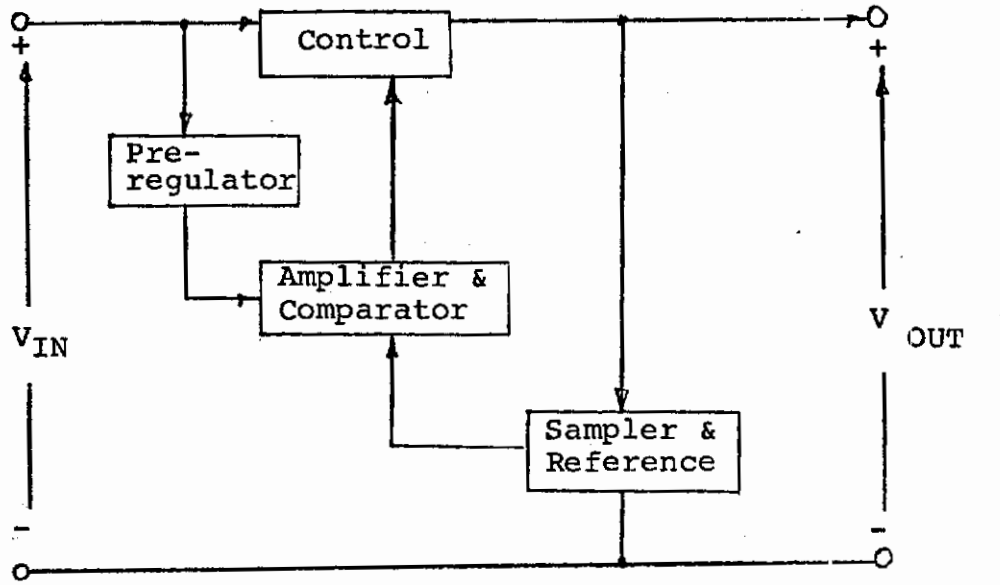
A. Low Level Regulators (ACA Drawing 108891)

+3.1 v and ± 5 v., were designed with the National Semiconductor LM 100, which is an integrated circuit voltage regulator in a T05 package, for the following reasons:

1. The +3.1 v and -5 v supplies are the reference voltages for the D/A converter which needs a maximum of .5% regulation and the LM100 has a typical line regulation of .05%/V, a load regulation of .1%, and a temperature stability of .4% from -55°C to 125°C.
2. Space and cost are saved because the same characteristics could only be met with precision discrete parts that are bulky and costly. Furthermore, the parts would have to be matches, by hand selection.
3. Reliability is greatly increased since the LM100 is an integrated circuit.
4. Current capabilities are easily increased by cascading power transistors.

B. ±15 V. Regulators (ACA Drawing 108877)

The +15v. and -15v. regulators were designed with discrete components because the regulation requirements were less stringent. The design followed the conventional regulator design as shown in block diagram form below.



Referring to the +15v. regulator schematic, the following circuit elements can be associated with the above blocks.

Pre regulator: CR10 - Motorola constant current diode.

Control: Transistors Q1 & Q3

Amplifier & Comparator: Q4, C7 & R5

Sampler and Reference: CR4, 5 & 6 and R3

The function of each component is as follows.

C3 and C9 provide input and output filtering, respectively. CR10 provides a constant base bias current to the control transistors Q1 & Q3. It is superior to a resistor in reducing output ripple.

C7 bypasses input ripple and noise to R3 to further suppress output voltage variations. Q4 bypasses the bias current to Q1 to ground to provide negative feedback. Its degree of turn-on depends upon the output voltage. R5 limits the base drive current transients passing thru the reference diodes. CR4, 5 & 6 are the reference diodes. CR 5 & 6 along with VBE of Q4 provide negative temperature coefficients to cancel the positive coefficient of CR4.

R3 provides a bias path for the diodes.

C. +330v and -60v. Regulators (ACA Drawing 108877)

The +330v and -60v regulators were designed simply, because they provide low bias currents at non-critical regulation.

C1 & C5 provide filtering.

Two zeners, a 150v and 180v, are used in series instead of a 330v zener to provide a smaller positive temperature coefficient.

R1 must be a carbon resistor because it has a positive temperature coefficient to counteract the zeners' coefficients. That is, as the temperature increases, R1 increases so that the bias current to CR1 & CR2 decreases. This decreases the reference voltage because the voltage drop across zener impedance decreases.

The same design philosophy holds for the -60v regulator.

HIGH VOLTAGE POWER SUPPLY

The cathode ray tube requires a second acceleration potential of about 9,000 volts d.c. at 25 microamps, for a total of .225 watts. Because of this small power requirement, the HV supply was designed as a d.c. to d.c. converter, which would be input regulated when operating off the regulated +15v. supply.

To obtain 9kv d.c. from 15v d.c., it is necessary to first chop the d.c. voltage so that a transformer can be efficiently used to boost the voltage up to 1,200 volts. The voltage is not transformed directly to 9,000v. because the breakdown voltage of Formvar covered wire in the transformer. Breakdown occurs at approximately 2,500v. In order to achieve a breakdown voltage in excess of 9kv directly in a transformer with wire closely wound on a core, wire with very thick insulation would be needed - plus a much larger core. In fact, the size of such a transformer is at least 100 times larger than the one used in the CRT-HSI.

The 1,200v. peak-to-peak square wave is rectified and multiplied x 8 by a standard 8 stage diode--capacitor multiplier. This arrangement is effectively used because of the low load current.

This form of design has enabled the entire converter to be housed in a 1.4 cu. in. package and to be mounted in the indicator near the cathode ray tube. Thus, the requirement for high voltage connectors and leads from the driver to the indicator is obviated; thereby, increasing the reliability and safety of the system. Also, this allows the driver to be remotely located at distances up to 40 feet.

CIRCUIT DESCRIPTION (FIGURE 23)

The +15v.d.c. appears across the collectors of Q1 and Q2 which form a push-pull pair. As C2 builds up charge, voltage is induced in the base drive windings. One of the transistors will turn on before the other due to the material unbalance in gains between them. Assume Q1 saturates first, then the collector current increases linearly with time due to the constant voltage across the primary winding. At the same time, a voltage is induced in the base drive winding of Q1 which supplies the necessary drive. As the primary current increases, a value is reached with is greater than $\beta_1 I_{B1}$ (the value of I_{B1} is limited by R_1.) Q1 then comes out of saturation, the primary voltage begins to decrease, the base drive voltage follows suit. This is a regenerative action so the transistors change state extremely fast. Q2 then turns on, the cycle is repeated. Thus, the voltage induced in the secondary winding is a square wave.

The action of the multiplier proceeds as follows. On the -V half of the square wave C4 is charged up to V (v is 625v.) through diode D2 (as shown in Figure 23). On the +V half, C5 is charged up to the voltage equal to the sum of V_{C4} +V = 2V through diode 3. Similarly after 8 cycles all the capacitors will be charged and the total voltage across the lower string of capacitors will be 8 times the peak-to-peak input voltage minus the forward drop of 8 diodes. Note that maximum voltage across each capacitor and each diode is only the peak-to-peak input value. Thus, there is no need for a bulky high voltage filtering capacitor.

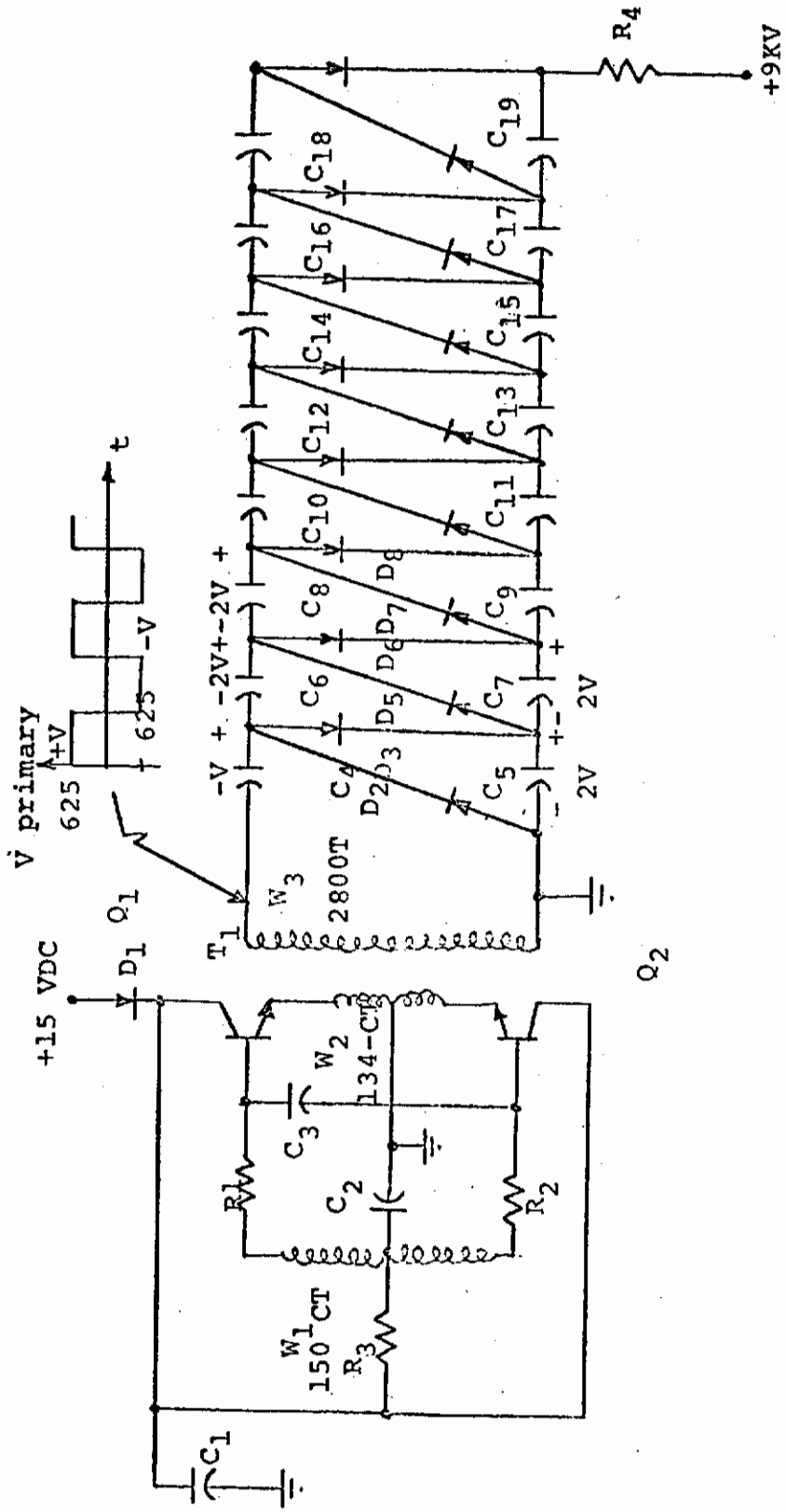


Figure 23

High Voltage Power Supply

LOAD REGULATION

In order to keep the design simple and the package small, no provision was made for regulation with respect to load variations in the high voltage supply. The acceleration current changes as a function of the brightness. Consequently as the brightness is increased from black to maximum whiteness the high voltage decreases about 15%. Additionally, as the acceleration potential falls, the size of the CRT display increases as the inverse of the square root of the acceleration voltage. Thus, a circuit was designed to increase the d.c. input voltage to the high voltage supply, whose output is a function of the brightness pot setting. The input to the correction circuit is obtained from the wiper of the brightness potentiometer. The output goes to the high voltage supply input.

An emprical relationship between the voltage from wiper to ground of the brightness pot to the input voltage of the high voltage supply which maintains the 9kv output constant was derived. This is the transfer function of the correction circuit and is shown in Figure 24.

The circuit that generates this transfer characteristic is shown in Figure 25.

CIRCUIT OPERATION

The input to the circuit is the 50k brightness pot which is connected across R5, between terminals 5 and 3. The output of the circuit drives the high voltage correction circuit and comes from terminals 4 and 2. The operation of the circuit is as follows.

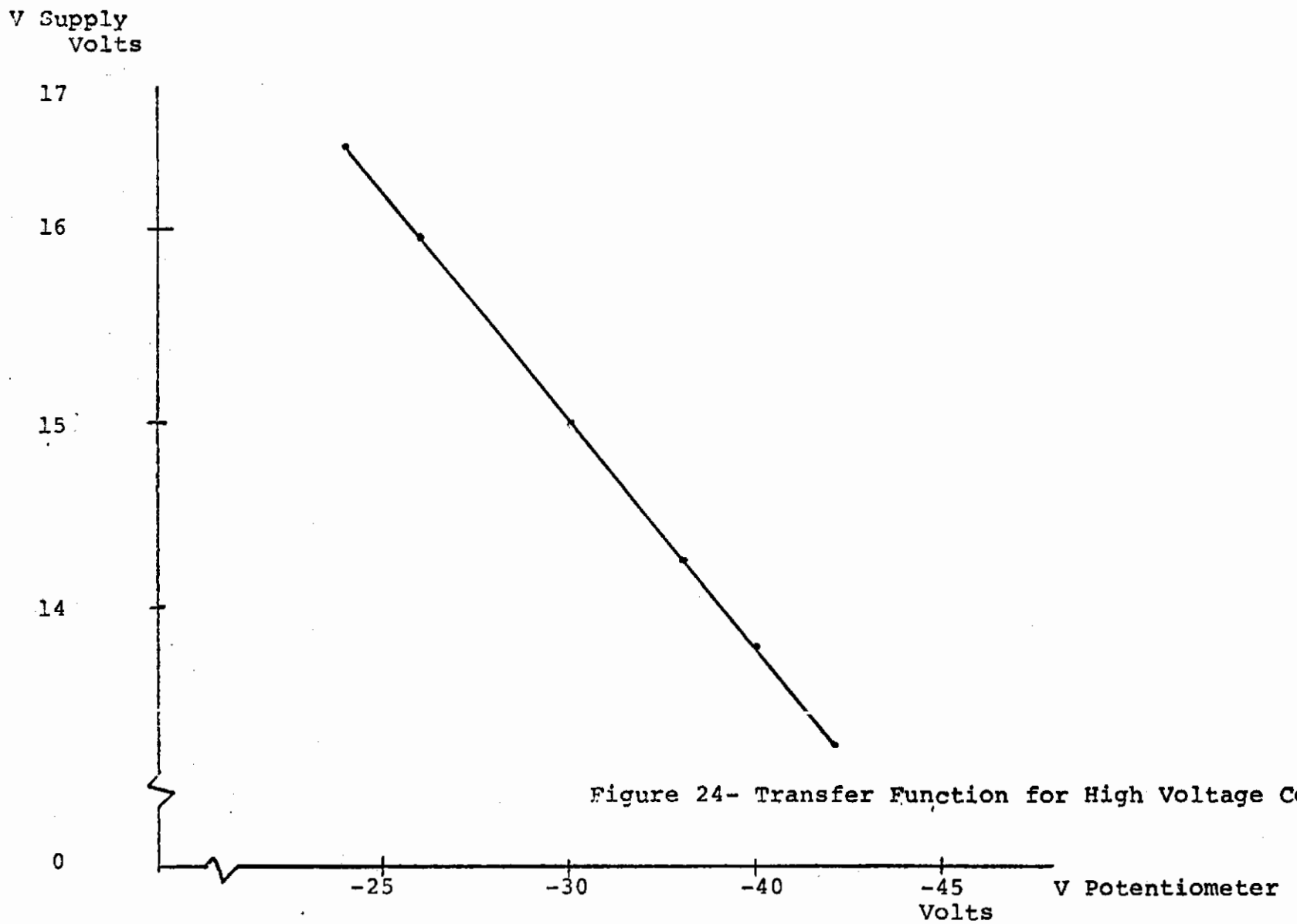


Figure 24- Transfer Function for High Voltage Correction

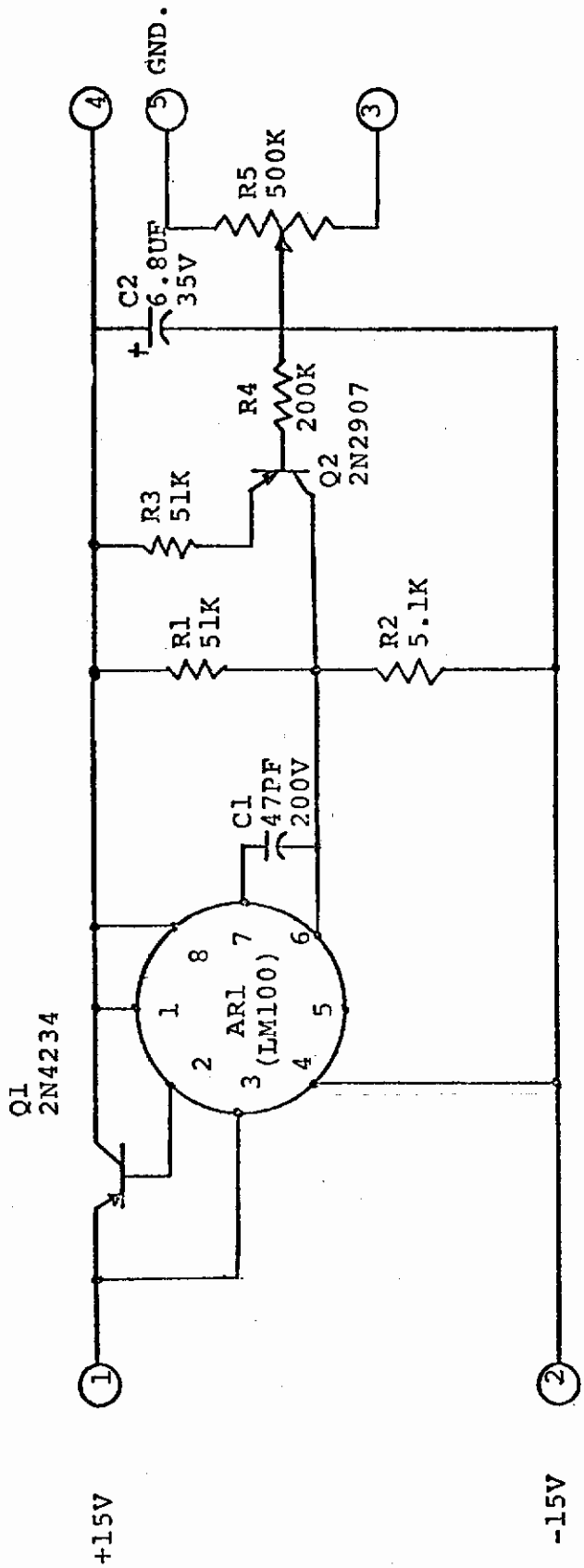
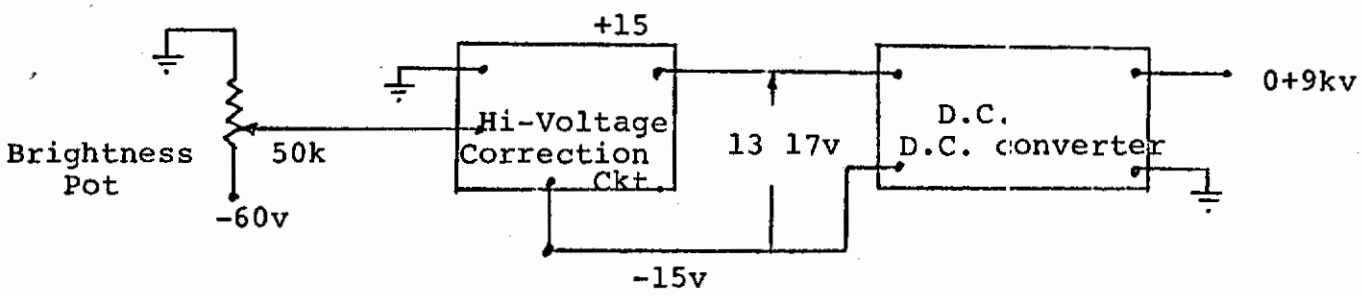


Figure 25

High Voltage Correction Circuit

AR1 is an integrated circuit voltage regulator. Q1 is attached to increase its current capability. The purpose of the circuit is to maintain a constant voltage to the high-voltage supply regardless of the load current drawn. This voltage, however, must adjust. Thus, the need for Q2 is the voltage divider feedback to the regulator; it acts as a variable resistor which determines the level which the regulator will maintain. As point 3 goes more negative, Q3 turns on harder and passes more current. Thus, the resistance is decreased and the output voltage decreases. Capacitor C2 helps stabilize the output voltage under load transients.

In block diagram form the whole high voltage systems is shown below.



VI. INPUT BUFFER DESIGN (ACA Drawing 108733)

Horizontal Pointer and D Bar - The Horizontal Pointer and D Bar inputs are DC signals (0 to ± 150 mv) from the radio set which produce an amplitude modulated signal which is a function of the deviation from the desired flight path. Since the signals are essentially the same, only the Horizontal Pointer input will be described. The Horizontal Pointer input is applied to pins 29 and 17. The D Bar input is applied to pins 57 and 73.

The input 29-17 has a selected R1 one thousand ohm ± 3% resistor to provide the required load impedance back to the radio. The input circuit is ungrounded; therefore only the R1 impedance is seen. The chopper transistors Q1 and Q2 are gated by the secondaries of T1 which represent the 0 and π phases of the 400 Hz reference voltage. The resulting output of T5 is a bipolar chopped square wave of 0 or π phase whose amplitude is proportional to the input voltage and whose phase is determined by the sign of the input voltage. This signal is amplified by AR2. The amplified signal is full-wave demodulated in the bridge (Z2), with the resulting DC value developed across C15 and C15. This voltage is limited at approximately +3 volts by CR3/CR4 and -3 volts by CR7/CR8.

Hand V Out Switching - As in the case of the input units, the Hand V Out switching are identical; therefore, only the Vertical will be discussed. The output switching is controlled by the 0 or 5v input of V GATE on pin 9. When the input is 5v, Q10 is turned on. The voltage division of R49 and R50 from +15v reduces the base voltage at Q12 to 7.5 volts. This forward biases Q12 such that +15 volts is applied to Q14, which is thus back biased off. The 15 volts from the collector of Q12 forward biases Q8 such that the Vert. Out from the D/A ladder at R41 is clamped to ground for positive pulses. The Q12 collector voltage also is applied to Q16 through the CR11 zener which drops 6.2 volts to limit the transistor turn-on drive. With Q15 turned on, Q19 is forward biased, which clamps any negative voltage out of R14 to ground. The collector voltage of -15V at Q15 back biases Q18. Thus, Q14 and Q18 are back biased such that their open impedance allows the deviation signal to be applied to pin 21 through R75 and R10. Q8 and Q19 are forward biased so that the D/A ladder output at R41 is clamped to ground and is not presented to the summing junction 21.

When the vertical gate goes to 0 volts, the situation is reversed; where Q14 and Q18 are clamped to ground with Q8 and Q19 back biased. In this condition, the D/A ladder voltage is applied to the summing junction at pin 21 and the deviation signal is inhibited.

TO/FROM - The TO/FROM input from the radio set is a (0 to ± 50mv) DC signal applied across pins 85 and 89. This voltage is chopped by the CR1, CR2, and T3 circuit which pulses the B+ on AR1. The

output of T4 is positive or negative half-wave pulses depending whether the input is positive or negative. This is phases detected by Z1 which develops a DC voltage across C5. When the output at C5 is positive, Q5 is turned on. Thus, the output at 77 goes from approximately 5v to 0v. This represents a logical output of not TO ($\overline{T}$). When the output at C5 is negative, Q6 is turned on which clamps the collector to ground. This opens Q7, such that a positive voltage on the base of Q7 turns it on. Thus, the output at 81 goes from approximately 5V to 0V. This represents a logical output of not FROM ($\overline{F}$). The turn on of Q5 or Q6 is adjusted to occur for an input of ±12.5 mv. Between these two voltages neither is on to provide a dead zone.

VII. RESULTS AND CONCLUSIONS

A flyable prototype was constructed and is shown in Figure 26. The concept produced a stable, easily integrated display. The operation of the unit and its interface is identical to that of the Dual Cross-Pointer HSI (F33615-67-C-0250) that the CRT-HSI will replace.

It is concluded that the Cathode Ray Tube Horizontal Situation Indicator can be successfully used to replace the present electromechanical HSI units. Also, since mechanical, moving part segments are replaced by micro-circuit and silicon transistor construction, much increased reliability will result.

It is recommended that this concept be extended to generate more complex waveforms on displays such as the aircraft attitude indicator by simply increasing the digital clock rate and adding increased programming control of the X and Y up/down counters.

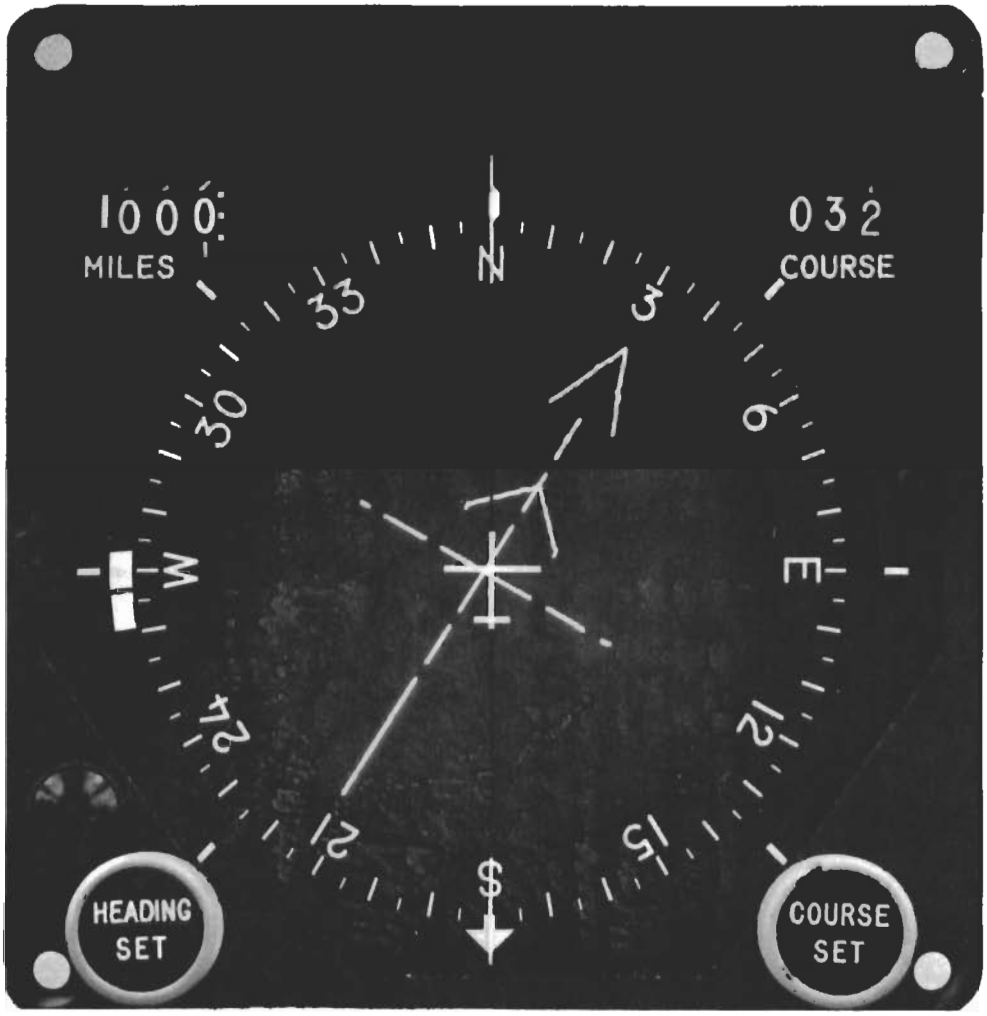


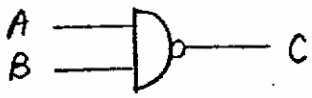
Figure 26 - Prototype CRT-HSI Display

APPENDIX A

LOGIC DIAGRAM DEFINITION

2 Input Nand

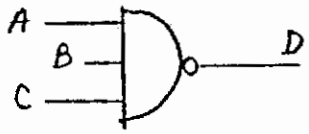
The circuit is shown schematically as:



$C = \overline{A \cdot B}$

The fan-out limit for this gate is 8.

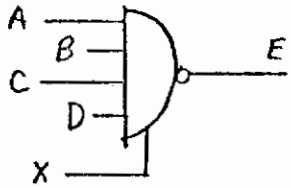
3 Input Nand - The circuit is shown schematically as:



$D = \overline{A \cdot B \cdot C}$

The fan-out limit of this gate is 8.

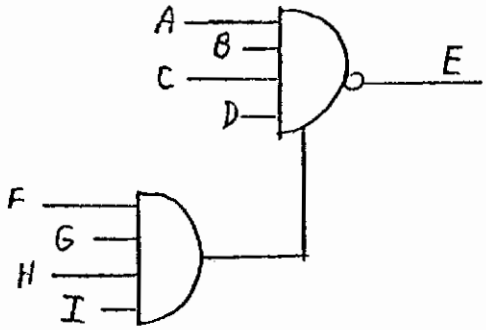
4 Input Nand - The circuit is shown schematically as:



$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

The fan-out limit of this gate is 25. By using 4 input extenders connected to X, the fan-in to the nand can be extended to 20.

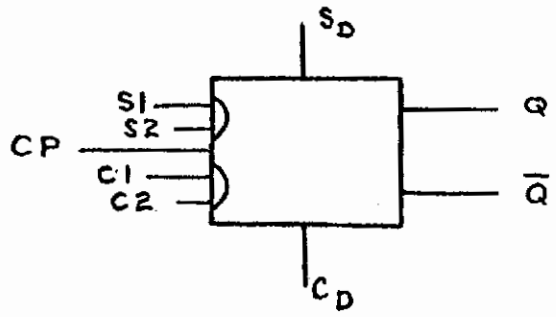
4 Input Extender -The extender is shown schematically in conjunction with the 4 input nand as:



$E = \overline{A \cdot B \cdot C \cdot D \cdot F \cdot G \cdot H \cdot I}$

The typical output capacitance of each extender is 5 pf; thus, a limit of 5 - 4 input extenders is used to prevent severely limiting the operation of the 4 input nand. The extenders must be located as close as possible to the nand to minimize lead capacitance.

Clocked, Master Slave, Flip Flop - The circuit is shown schematically as:



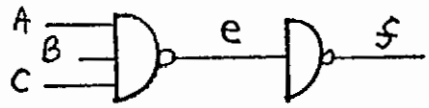
The flip flop can operate as a master-slave clocked unit or as a direct-set unit.

In the direct-set mode a low voltage at C_D will cause the slave to toggle to $\overline{Q}$ = high and Q = low, no matter what the configuration of the clocked input. S_D low reverses the Q states from that of C_D.

In the clocked mode, when S1 and S2 are high along with CP, this information sets the state of the master flip flop. As soon as the CP voltage falls toward low, the set information is copied into the slave flip flop to set Q = high and $\overline{Q}$ = low. C1 and C2 inputs being high reverse the process. It should be noted that since the operation depends only on voltage levels, this circuit

will operate on any waveform that meets the voltage requirements. The fan out of the circuit is 10.

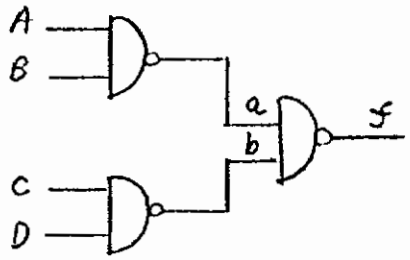
AND Mechanization - The function, f = A·B·C can be mechanized:



$$e = \overline{A \cdot B \cdot C}$$

$$f = \overline{e} = \overline{\overline{A \cdot B \cdot C}} = A \cdot B \cdot C$$

OR Mechanization - the function, f = A·BvC·D can be mechanized:

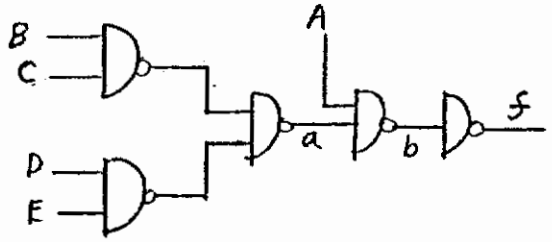


$$a = \overline{A \cdot B}, \quad b = \overline{C \cdot D}$$

$$f = \overline{a \cdot b} = \overline{\overline{A \cdot B} \cdot \overline{C \cdot D}}$$

$$f = A \cdot B \vee C \cdot D$$

FACTOR Mechanization - The function, f = A(B·CvD·E) can be mechanized:

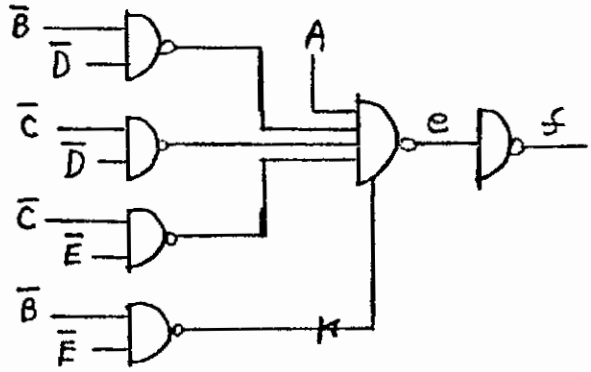


a = B·CvD·E, from the OR mechanization

$b = \overline{A \cdot a}$

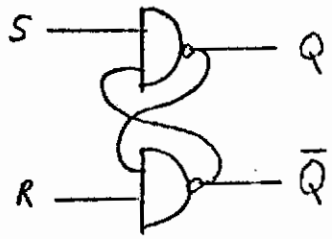
$f = \overline{\overline{A \cdot a}} = A \cdot a = A(B \cdot C \vee D \cdot E)$

An alternate mechanization can be provided by:



$f = \overline{\overline{e}} = \overline{A} \vee (\overline{B} \cdot \overline{D} \vee \overline{C} \cdot \overline{D} \vee \overline{C}\ \overline{E} \vee \overline{B}\ \overline{E}) = \overline{A} \vee (\overline{\overline{B \cdot C} \vee \overline{D \cdot F}}) = A\ (B \cdot C \vee D \cdot E)$

RS Flip Flop Mechanization - This function can be mechanized by use of two nands connected as shown below:



Assuming an initial condition of $\overline{Q} = 1$ and $Q = 0$, and both S and R = 1, the $\overline{Q} = 1$ coupled with S = 1 force Q = 0. The Q = 0 forces $\overline{Q} = 1$ no matter what the state of R.

When S is set to 0, Q is forced to 1. The condition R = Q = 1 sets $\overline{Q} = 0$. $\overline{Q} = 0$ latches Q = 1 regardless of the following state of S.

With Q = 1, and R set to 0, the $\overline{Q}$ output is forced to 1 with Q forced to 0.

APPENDIX B

ALIGNMENT PROCEDURE CRT - HSI

NOTE: 1. Connect test connector to Processor Unit.

2. Start with +D/A Reference and -D/A Reference at approximately +3V and -8V respectively.

3. Rotate heading pointer to north up.

1. (+) 5VDC Alignment - - Connect voltmeter between GRD and +5V test points. Adjust +5V potentiometer for a reading of +5 ±0.5V.

2. +D/A Reference Alignment - - Connect voltmeter between GRD and +Reference test points. Adjust +D/A REF potentiometer for a reading of +3.1 ±0.03V.

3. Coarse (-) D/A Reference Alignment - - While observing Vertical Output, times 54 to 62 is made approximately zero volts by adjusting -D/A REF potentiometer.

4. Ladder Balance

a. Vertical

1. Adjust 10's BAL potentiometer while observing the vertical output with a Z pre-amp until best line linearity is obtained.

2. Adjust 1's BAL potentiometer for best linearity.

b. Horizontal

Perform the same steps as vertical by using the horizontal 10's and 1's BAL potentiometers.

5. Connect Indicator to Processor

6. Focus - - Adjust FOCUS potentiometer for sharp displayed lines on the Indicator cathode ray tube (CRT).

7. -D/A Reference - - While observing CRT display, adjust -D/A REF potentiometer until the tail at the bottom of the screen is in alignment with the rest of the vertical pointer.

8. Size

a. Vertical

Adjust VERT SIZE potentiometer to place vertical pointer at the top edge of the CRT.

b. Horizontal

Adjust HORZ SIZE until the length of both vertical and horizontal deviation bars between the 1st dots are equal.

9. Centering

Adjust VERT and HORZ CENTERING potentiometers to place deviation bar center crossing underneath the aircraft symbol.

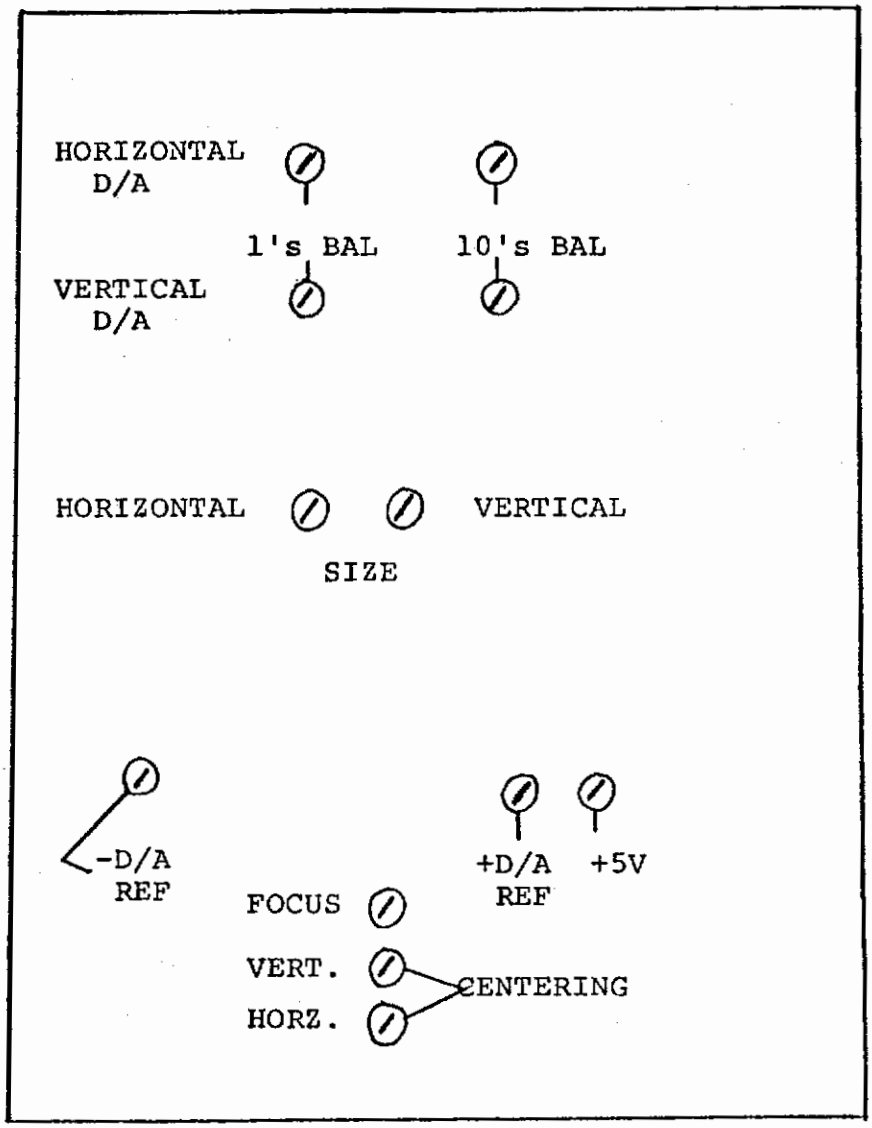


Figure 27 - CRT-HSI ALIGNMENT POTENTIOMETERS

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13. ABSTRACT

The contract study demonstrated that the electro-mechanical elements in the center section of a Horizontal Situation Indicator (HSI) could be successfully replaced by electronically generated symbols on a cathode ray tube, thus allowing the HSI to be used as a multi-mode display for future requirements of the Air Force.

The course pointer, vertical deviation bar, horizontal deviation bar, ant the TO/FROM indications were generated by digitally programming an Up/Down counter for both the X and Y axis. The outputs were converted to CRT sweep voltages by a digital to analog converter. The generated symbol set was rotated with respect to aircraft heading by resolving the X,Y sweep voltages.

A flyable prototype was successfully contructed and delivered to the Air Force Flight Dynamics Laboratory.

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Horizontal Situation Indicator						
Cathode Ray Tube Display						
Stroke Generator Symbol Generation						
Display Control						

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