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FOREWORD

The research was conducted in support of Project 8119, "Checkout and Hazard Control Techniques," (Robt. D. Sherrill, Project Engineer) which is directed by the Support Techniques Branch (R. J. Gavfert, Chief) of the Air Force Aero Propulsion Laboratory.

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An additional task performed under this contract was the design and construction of an error detection device which implemented a specified error detection code. The results of that task are reported in "Error Detection Code and Device," by Theodore S. Lewis and Walter J. Huebner.

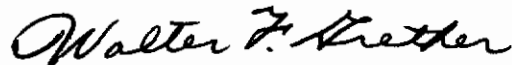
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ABSTRACT

One of the two objectives of this project was the development of error control techniques for the man-computer interface of an automatic checkout system. To minimize human error in man-computer communication in the automatic checkout complex, precedence and connection matrix techniques for use with total and partial simulation methods were developed to detect errors in operational automatic checkout computer programs. Precedence and connection matrix techniques for use with total simulation methods were incorporated into a simulation computer program which comprised a total simulation of the computer which controls an operational automatic checkout system. The modified simulation was then used to process several computer runs of an operational automatic checkout computer program. The basic conclusions drawn from the results of the study of error control methods were that precedence and connection matrix techniques used with total and partial simulation methods can be useful in detecting errors in operational computer-controlled automatic checkout systems, and that further study and development should be made to allow incorporation of the techniques in present and future computer-controlled automatic checkout systems with minimum modification.

PUBLICATION REVIEW

This technical documentary report is approved.



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SECTION I

INTRODUCTION

The first objective of this project was to develop error control methods to minimize human error in man-computer communication in the automatic checkout complex.

An automatic checkout complex is a man-machine system in which the status of a hardware system is determined by the use of automatic test equipment and the system is then brought into conformance with pre-determined standards by a human operator. The automatic test equipment is controlled by a digital computer, and it is necessary for a man to communicate with this control computer through the use of computer programs. This communication creates a man-computer interface, and it is in relation to this interface that error prevention, detection, and correction techniques were studied. The error control methods which ultimately were developed were the use of precedence and connection matrix techniques with total and partial simulation methods to detect errors in operational automatic checkout programs.

Precedence matrix techniques make use of constraints on the order in which steps may be performed. Connection matrix techniques make use of the connections that exist between automatic checkout equipment and equipment under test. Precedence and connection matrix techniques, implemented as part of total simulation methods, may be used to test the order in which a checkout program is executed and the validity of connections that are requested between equipments. Precedence matrix techniques may be used with partial simulation methods to trace through all paths of an operational automatic checkout program, and to test the order of execution of instructions for conformance with precedence constraints. Partial simulation methods are restricted to programs in which instructions are not modified.

Precedence and connection matrix techniques used with total simulation methods were implemented in a total computer simulation program for an operational automatic checkout system to evaluate the practicability of incorporating the techniques in present and future computer-controlled automatic checkout systems. A number of computer runs were made by processing an operational automatic checkout program through the computer simulation program which had been modified to incorporate precedence and connection matrix techniques. The results were then evaluated, and conclusions and recommendations were made.

SECTION II

AUTOMATIC CHECKOUT SYSTEMS

A. INTRODUCTION

Checkout is a two stage process in which the status of a system is determined, and the status information is then used to bring the system into conformance with predetermined standards. The classical method for determining the status of a system was to manually measure the response of the total system to all valid ranges of appropriate stimuli and to interpret the measurements. The difficulties inherent in this method, such as the problem of sampling from systems produced in large quantities, testing all options and combinations of options, or determining status on a statistical basis, were, in general, solved satisfactorily.

However, for the increasingly complex space and weapon systems, classical checkout methods were no longer adequate. The principal reasons for this were the following:

1. Manual testing involved excessive wear on the equipment under test -- the prime equipment (Ref. 1).
2. Real-time operation required greatly reduced action and reaction times.
3. An entire system could not usually be activated to reproduce operational conditions exactly.
4. System checkout was a single factor in the complex of informational needs of the prime equipment and the total system of which the prime equipment was a part (Ref. 2). Examples of the informational needs were data for failure prediction, reliability estimation, command decisions, supply, logistics, etc.

Thus, some or all of the checkout system must be automated, and the automatic checkout system must be integrated into the total system of which the automatic checkout system and prime equipment are a part. A discussion of the extent to which a system should be automated is contained in other sources (Refs. 3, 4, 5) and will not be considered here. It was assumed in this study, for the reasons discussed above, that the checkout system contains a stored-program digital computer, and that the automatic checkout system and prime equipment are integrated into the total system.

B. MAN-COMPUTER COMMUNICATION IN THE AUTOMATIC CHECKOUT SYSTEM

The existence of a computer in a system creates the need for communication with the computer. There are, in general, two levels of man-computer communication, the compiler level and the assembly or machine language level. Without engaging in a detailed discussion of the precise meaning of the two levels, the assembly language is oriented toward the computer and the compiler language is oriented toward the problem; assembly languages require an intimate knowledge of the computer on which the problem is to be run, while compiler languages require little or no knowledge of the computer; assembly languages describe a problem solution in terms of machine-oriented instructions, compiler languages describe the solution in a language approximating the actual language of the problem.

The principal virtues of a compiler language as compared to an assembly language are that it requires less effort to learn, programs are more easily written and modified, errors are more easily corrected, programs are more easily understood by persons other than the author, and programs may be compiled on a number of different computers. The disadvantages of a compiler are that the efficiency of the compiled program (object program) is generally less than that of an assembled program, the time to compile is greater than the time to assemble, the compiler language program may have to be compiled on a larger computer than the assembly language program, that is, larger than the computer on which it is to be run, (although this can be true of assembly language programs), and finally, it may not be possible to implement certain program modules in compiler language that can be implemented in assembly language.

The advantages and disadvantages of compilers vs. assemblers is a subject which has been exhaustively treated over a number of years. Because a compiler language for automatic checkout equipment (ACE) seems to hold the most promise for future development of not only automatic checkout systems, but the total system (Ref. 6), the existence of a compiler for automatic checkout equipment was assumed for this study. The compiler was assumed to operate on a general purpose digital computer which may or may not be linked directly to the ACE computer (in general, it will not be linked).

C. MAN-MACHINE STRUCTURE IN THE AUTOMATIC CHECKOUT SYSTEM

Figure 1 illustrates the structure of a generalized automatic checkout system which contains a digital computer (ACE computer) which is linked to the automatic checkout equipment. A compiler language exists for the ACE computer and the compiler operates on a general purpose digital computer which is not linked to the ACE computer. The automatic checkout equipment programmer is the human originator of operational checkout programs which are run on the ACE computer and which operate the automatic checkout equipment. The programs are written in the compiler language (source programs) and are compiled on the general purpose digital computer

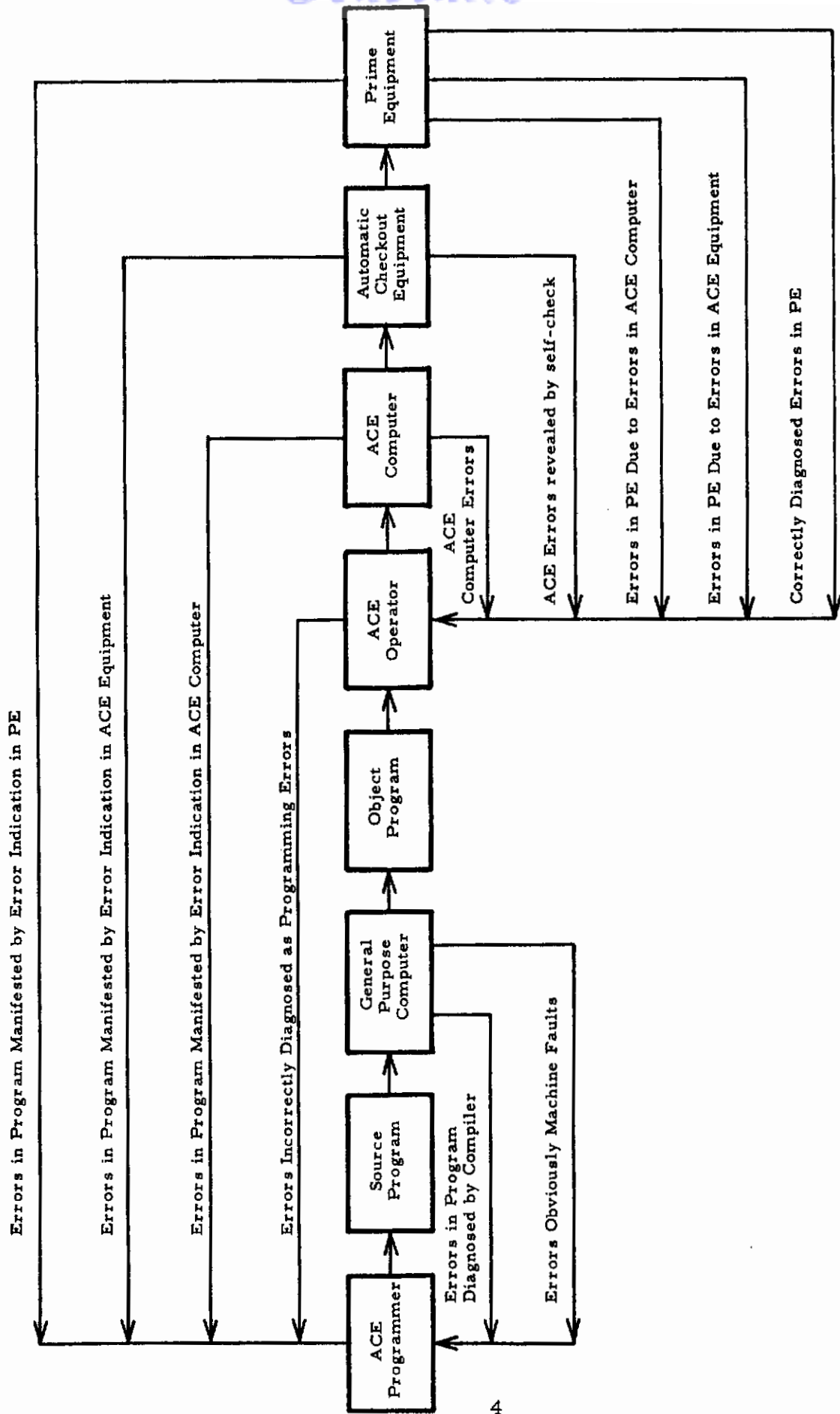


Figure 1 - Automatic Checkout System

to produce the machine language programs (object programs) which operate the ACE computer.

The human operator of the automatic checkout equipment runs the object program on the ACE computer to check out the prime equipment (PE). If the checkout of the prime equipment or the self-checking features of the automatic checkout equipment are not completely under object program control, the feedback from the automatic checkout and prime equipment through the object program allows the operator to perform those functions which are not performed by the object program.

The automatic checkout system has been described as it would perform if no unanticipated errors occurred at any point in the system. However, unanticipated errors do occur and cause degradation of the prime equipment, time delays, increased costs, and loss of confidence in the automatic checkout equipment. Some of the errors which can occur are shown in Figure 1. In general, the errors can be categorized as hardware errors and human errors. The nature of these errors and their impact on the automatic checkout system will now be discussed in detail.

D. ERRORS IN THE AUTOMATIC CHECKOUT SYSTEM-HARDWARE ERRORS

1. Errors in the General Purpose and ACE Computers

Failures can occur in any of the internal components of the computers, in any of the peripheral equipment, and in any of the communication links. Errors can also occur in the input-output media such as magnetic and paper tape and punched cards.

2. Errors in the Automatic Checkout Equipment

Failures can occur in any of the components of the automatic checkout equipment and in any of its communication links.

3. Errors in the Prime Equipment

Failures can occur in any component of the prime equipment and in its communication links with the automatic checkout equipment.

E. ERRORS IN THE AUTOMATIC CHECKOUT SYSTEM-HUMAN ERRORS

1. System Design Errors

Errors can occur in the design of any module of the system or in the configuration of the modules. An error is considered to be any deficiency which does not allow a module or configuration of modules to accomplish its objectives.

2. Computer Programming Errors

Errors can occur in the writing of checkout programs and in the writing of software programs (compilers, assemblers, translators, etc.). The errors can occur in the logic of the programs or in the mechanics of transferring the programs from thought to hard copy.

3. Human Operator Errors

Errors can occur in the human operation of any of the hardware including the general purpose computer, the ACE computer, the automatic checkout equipment, and the prime equipment. However, any errors which are directly or indirectly due to computer programming errors are not to be considered operator errors.

F. IMPACT OF HARDWARE ERRORS ON THE AUTOMATIC CHECKOUT SYSTEM

1. Impact of Errors in the General Purpose Computer, ACE Computer, and Automatic Checkout Equipment

The impact of failures in any of the components, communication links, input-output media of the computers, or the automatic checkout equipment, is a function of the point in the system at which it is possible to detect the errors. For instance, the loss of a bit on a magnetic tape which contains input to the general purpose computer will usually be diagnosed as the tape is being read, and an isolating error indication will be given.

Consider, on the other hand, the alteration of a pair of bits on the tape in such a way that a parity error does not occur, and the alteration manifests itself only as an erroneous failure indication in the prime equipment when a checkout program is run. Considerable effort may be expended in diagnosing the error as an error in the computer program, and considerably more effort in tracing it to a hardware error. The point at which errors can be detected is a function of the design of the system for error detection and correction.

The distance in terms of stages of equipment between the point at which an error occurs and the point at which it is detected is defined to be the error propagation distance. The propagation distance is of great significance because certain types of errors require a measure of time and effort to detect and correct which increases more than linearly with the propagation distance.

Errors in the automatic checkout equipment have a potential propagation distance which is less than that for programming errors, but the difficulty in isolating the errors as not due to the prime equipment is as great.

2. Impact of Errors in the Prime Equipment

One major objective of the automatic checkout system is the detection, isolation, and correction of faults in the prime equipment. The efficiency with which this is accomplished is dependent upon the design of the system, the efficiency of the computer programs written for this purpose, and the skill of the automatic checkout equipment operator. It is also dependent upon the design of the system for the elimination of spurious prime equipment fault indications.

G. IMPACT OF HUMAN ERRORS ON THE AUTOMATIC CHECKOUT SYSTEM

1. Impact of System Design Errors

Manifest errors in system design are serious but will generally become apparent before the system is operational. Errors of omission are even more serious if that which is omitted is the incorporation into the system of error detection and correction features. Because the effect of errors may increase exponentially with their propagation distance, the effect of the omission of error detection and correction and self-checking features may be correspondingly great.

2. Impact of Computer Programming Errors

The effect of computer programming errors both in the operational programs and the compiler is similar to that of hardware errors. The effect is a function of the point at which it is possible to detect the errors. The farther the errors are propagated, the greater the effort required to isolate them from other possible causes of failure. Of even greater concern is the possibility that they may go undetected for long periods or may never be detected. Such a case can occur if errors are in program modules which are exercised infrequently, if they result in a faulty hardware component being diagnosed as faultless, or if the checkout program does not check all possible sources of error. The undetected error is of great concern because it can and has caused the loss of a system or can lead to an erroneous assessment of total system strength.

Correction of programming errors after their detection is generally much easier than the detection. However, the correction can cause considerable delay if the general purpose computer is remote from the automatic checkout equipment. In real time operations, errors may not be tolerable.

3. Impact of Human Operator Errors

The effect of operator errors is, of course, dependent upon the degree to which the operator has control of operation. The greater the degree of sophistication and self-checking of the hardware and programs, the less the opportunity for operator errors.

SECTION III

ERROR PREVENTION, DETECTION, AND CORRECTION (ERROR CONTROL) IN THE AUTOMATIC CHECKOUT SYSTEM

A. INTRODUCTION

The sources of error in the automatic checkout system have been categorized as hardware and human. While the effect of hardware errors is quite significant, the concern of this study is with the human error in the automatic checkout system. Hardware errors will therefore be discussed further only as they relate to human errors.

As has been discussed, human error in the automatic checkout system may occur at three points in the system: the design stage, the computer programming area, and the equipment operation area. Methods for error prevention, detection (including isolation), and correction at each of these three points in the system will now be discussed. For the remainder of this report, error prevention, detection, and correction will be referred to as error control.

B. ERROR CONTROL IN DESIGN STAGE

Error control in the design stage refers to both the error control of design errors and the incorporation of error control techniques into the automatic checkout system. Error control of design errors is the classical systems design, analysis, and engineering problem that has been and is being studied by many groups. It will not be considered further. The incorporation of error control techniques in the automatic checkout system as they relate to human error can be dichotomized into error control for computer programming errors and error control for equipment operation errors. These are included in the following two sections.

C. ERROR CONTROL FOR COMPUTER PROGRAMMING

It has been pointed out that computer programming errors can be propagated through the entire automatic checkout system and can result not only in large expenditures of time and effort for diagnosis and correction, but also in the degradation or loss of the physical system or its capability. The propagation distance must therefore be reduced as far as possible.

There are two categories of computer programming errors: errors in the logic of a program and clerical errors in the mechanics of transferring the program from the mental concept to the hard copy. An example of a logical error is a set of instructions which causes a test sequence to be performed out of order. An example of a clerical error is the writing of an I for a l. Logical errors are much more significant than clerical errors, but each requires error control. Significant general methods of error control which are presently used or which might be developed for each category are outlined below.

1. Logical Errors in Computer Programming

a. Error Prevention

1) Flow diagrams of the general flow of operations are constructed from the model of the problem to be programmed.

2) Detailed coding flow diagrams are developed from the general flow diagrams.

3) At least one test case is manually traced through the flow diagrams described above using representative data with a small number of significant figures.

4) At least one test case is manually traced through the program instructions of the completed program.

5) Persons other than the author of the program also perform 3) and 4).

b. Error Detection

1) Methods are developed which relate the logical structure of the compiler language program (source program) with the constraints of the hardware which the program tests.

2) The prime equipment, automatic checkout equipment, and ACE computer are simulated on the general purpose digital computer. The machine language program (object program) is then entered into this simulation, and the accuracy of the program is tested by the use of precedence and connection matrix techniques (7, 8).

3) Simulation methods are developed which do not require full-scale simulation of the prime equipment, automatic checkout equipment, and ACE computer. The partial simulation method (9) is used to trace all paths of a program and to test the conformity of every path to precedence constraints.

4) General techniques are developed to indicate to the automatic checkout equipment operator, or to a diagnostic program, those fault indications in the hardware which are due to programming errors.

c. Error Correction

1) Errors are corrected by reprogramming in source language, and the program is recompiled.

2) Errors are corrected by reprogramming in machine language.

3) Techniques are developed to automatically correct certain classes of errors in source language.

4) Techniques are developed to automatically correct certain classes of errors in machine language.

2. Clerical Errors in Computer Programming

a. Error Prevention

1) Pre-printed forms are used which prevent as many syntactical errors as possible.

2) Hard copy at each stage of programming is carefully checked manually for clerical errors.

3) 1. a. 3), 4), and 5) apply equally well to the prevention of clerical errors.

b. Error Detection

1) The compiler will contain diagnostic procedures to detect many of the classes of clerical errors which occur.

2) 1. b. 2), 3), and 4) apply equally well to the detection of clerical errors.

c. Error Correction

1) Techniques for correction of logical errors apply equally well to the correction of clerical errors.

D. ERROR CONTROL FOR EQUIPMENT OPERATION

There are two major equipment types that are operated by humans in the automatic checkout system: the general purpose computer, and the prime equipment - automatic checkout equipment - ACE computer complex. The operation of the general purpose computer is a classical problem in computer systems operation and will not be considered further. The operation of the automatic checkout complex is a function of the division of operations between the automatic checkout equipment and the human operator. The general categories of human error are set-up errors such as erroneous set-up of hardware, wrongly connected lines, incorrectly mounted tapes, etc. and feedback errors such as erroneous interpretation of output, not correctly following displayed instructions, interpreting prime equipment faults as non-prime equipment faults, etc. Methods of error control that are presently being used or which might be developed for each of these categories are outlined below.

1. Set-up Errors in Equipment Operation

a. Error Prevention

1) The set-up of all hardwares is detailed in clearly-written, unambiguous reference material.

2) Communication points between hardwares are carefully labeled.

3) Dials, knobs, tape mountings, indicators, etc., are designed to prevent erroneous inputs or readings.

4) All anticipated operator errors are detailed in reference material as to nature, symptom, probability of occurrence, method of avoidance.

b. Error Detection

1) The hardware is designed to indicate certain classes of erroneous set-ups or inputs.

2) The computer programs are designed to diagnose and indicate certain classes of erroneous set-up or inputs.

3) 1. a. 4) applies equally well to error detection.

c. Error Correction

1) The error is corrected manually by the operator.

2) The error is corrected automatically by the computer programs.

2. Feedback Errors in Equipment Operation

a. Error Prevention

1) Feedback information is displayed in the manner most conducive to optimal use of the information.

2) Manuals are prepared to aid in the interpretation of feedback information.

b. Error Detection

1) Procedures for reaction to feedback are designed to enhance the probability that incorrect operator reaction produces an error indication.

c. Error Correction

1) The error is corrected manually by the operator.

2) The error is corrected automatically by the computer programs.

E. SELECTION OF ERROR CONTROL METHODS TO BE STUDIED

Of the error control methods that could be developed for use in the automatic checkout system, the use of precedence and connection matrix techniques with total and partial simulation methods to detect errors in

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operational automatic checkout programs yielded the best compromise between ultimate pay-off of the techniques and the probability that such techniques could be developed within the scope of the project. We decided that it was not sufficient merely to develop precedence and connection matrix techniques, but that an attempt should be made to evaluate their usefulness in an operational automatic checkout system.

Consequently, precedence and connection matrix techniques used with total and partial simulation methods were developed for use in the automatic checkout system, and implementation of the techniques used with total simulation methods was effected in the computer simulation of a computer-controlled automatic checkout system. The scope of this study did not permit implementation of the techniques used with partial simulation.

The automatic checkout system which was selected for implementation was the VATE (Versatile Automatic Testing Equipment) System constructed by Hughes Aircraft Company. An explanation of precedence and connection matrix techniques, the reasons for selecting the VATE System, the implementation of the techniques in the VATE System, and the evaluation of results are described in detail in subsequent sections.

SECTION IV

PRECEDENCE MATRIX AND CONNECTION MATRIX TECHNIQUES

A. INTRODUCTION

The principal error control methods on which this study focused were the use of precedence and connection matrix techniques with total and partial simulation methods to detect errors in operational automatic checkout computer programs. Precedence matrices are graphical representations of the order in which steps must be performed or in which it is desired to perform them. Thus, it can be said, "Step A precedes Step B," or "Step D follows Step C," or "Step E and Step F can be performed in either order."

Connection matrices are graphical representations of the connections that exist between points in automatic checkout equipment and points in prime equipment. The connecting links may be cables or telemetry communication. The cable or telemetry communication may originate and terminate at either the automatic checkout equipment or the prime equipment.

Total simulation methods are methods that require the total simulation of a system. For the use of precedence and connection matrix techniques, the simulation required is of the digital computer which controls the checkout process. The simulation is constructed so as to process, in a manner as similar to that of the digital computer as possible, programs which have been written for the digital computer. Additional simulations of the automatic checkout and prime equipment are desirable but not essential.

Partial simulation methods are methods that require the simulation of part of a system. For the use of precedence and connection matrix techniques, the required partial simulation is essentially a translation process capable of identifying branching type instructions in the instruction repertoire of the digital computer which controls the checkout process. Every path through a program can be traced using the branching type instructions.

Precedence and connection matrix techniques are used with total simulation methods in the following way. As the simulation processes the instructions of an automatic checkout program, the order of execution of the instructions and the requested connections can be checked against the precedence and connection matrices. Diagnostics can then be written for violations of precedences or invalid connections, or comments written for the ordering of steps or the requesting of connections that are consistent with the precedence and connection matrices.

Precedence and connection matrix techniques are used with partial simulation methods as follows. The partial simulation traces through every path of the automatic checkout program by executing only branching type instructions. As each path is traced, the sequencing of the instructions is checked against the precedence matrix. Diagnostics are written for illegal

sequences, and comments are written for sequences consistent with the precedence matrix.

The remainder of this section contains a more detailed explanation of the use of precedence and connection matrix techniques with total and partial simulation methods. To facilitate understanding of the methods, an artificial, but realistic, example is taken from a subsequence of tests on a missile.

B. EXAMPLE OF SUBSEQUENCE OF TESTS IN AUTOMATIC CHECKOUT PROGRAM

To illustrate precedence and connection matrix techniques, a subsequence of tests on a missile X is presented in Table 1. The first four tests in the Table measure the accuracy, with respect to predetermined limits, of one a. c. and two d. c. voltages which are used as stimuli. The pitch loop is shorted while the yaw loop is tested. A 3 volt d. c. stimulus is applied to the yaw loop, the flippers of the missile are given .8 seconds to stabilize, and the differential voltage across the actuator potentiometer of one of the flippers, which is linearly related to the angular movement of the flipper, is measured.

The voltage is converted to degrees per volt of stimulus and tested against specified limits. If outside of the limits, hydraulic power is removed, a diagnostic is printed, and a branch is made to an adjustment routine. If the degrees per volt is within limits, the second flipper is tested in the same way. When both flippers pass the test, the short is removed from the pitch loop, the yaw loop is shorted, and the pitch loop is tested in the same way. If a branch is made to an adjustment routine, return is then made to step 1. When both the yaw and pitch loops are checked out, the delta max parameter is tested.

Figure 2 shows an approximate testing circuit for the subsystem of missile X. The 15 volt d. c. and 107.5 volt a. c. stimuli are not shown. The numbered points are stimulus, stimulus acceptance, response, and response acceptance points. A stimulus point is a point in the automatic testing equipment at which a stimulus is initiated. A stimulus acceptance point is a point in the equipment under test at which the stimulus induces a physical change - for example, the opening or closing of a switch. A response point is a point in the equipment under test at which a measurement is made, for example, a voltmeter. A response acceptance point is a point in the automatic testing equipment at which a measurement is recorded, usually for transformation to a digital form. Points 1, 5, 7, 9, 13, 17, 19, 21, 25 are stimulus points, points 2, 6, 8, 10, 14, 18, 20, 22, 26 are stimulus acceptance points, points 3, 11, 15, 23, 27 are response points, points 4, 12, 16, 24, 28 are response acceptance points.

The following section describes the use of precedence matrices to detect errors in a computer program embodying the tests described in Table 1 for the hardware diagrammed in Figure 2.

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TABLE 1

SUB-SEQUENCE OF TESTS ON MISSILE X

1. Measure $+ 3 \pm .15$ volts d. c. stimuli voltage.
2. Measure $+ 15 \pm 1.0$ volts d. c. stimuli voltage.
3. Measure 107.5 ± 7.5 volts a. c. (pp) 4 CPS stimuli voltage.
4. Measure $4.0 \pm .2$ CPS frequency a. c. stimuli voltage.
5. Apply short to pitch loop.
6. Apply 3 volt d. c. stimulus to yaw loop.
7. Wait .8 seconds for flippers to stabilize at final position.
8. Measure differential voltage across actuator pot of flipper no. 1.
9. Convert differential voltage of flipper no. 1 to degrees.
Divide by voltage to obtain degrees/volt.
10. Test $3.16 \leq \text{degrees/volt} \leq 3.50$.
11. If no, remove hydraulic power, print diagnostic, go to control system adjustment, routine 2 (Step 26).
12. Convert differential voltage of flipper no. 3 to degrees and divide by 3 to obtain degrees/volt.
13. Test $3.16 \leq \text{degrees/volt} \leq 3.50$.
14. If no, remove hydraulic power, print diagnostic, go to control system adjustment, routine 2 (Step 26).
15. Remove short from pitch loop and apply short to yaw loop.
16. Apply 3 volt d. c. stimulus to pitch loop.
17. Wait .8 seconds for flippers to stabilize at final position.
18. Measure differential voltage across flipper no. 2.
19. Convert differential voltage of flipper no. 2 to degrees and divide by 3 to obtain degrees/volt.
20. Test $3.16 \leq \text{degrees/volt} \leq 3.50$.
21. If no, remove hydraulic power, print diagnostic, go to control system adjustment, routine 2 (Step 26).
22. Convert differential voltage of flipper no. 4 to degrees and divide by 3.
23. Test $3.16 \leq \text{degrees/volt} \leq 3.50$.
24. If no, remove hydraulic power, print diagnostic, go to control system adjustment, routine 2 (Step 26).
25. Test Delta Max. Parameter. Go to exit.
26. Make adjustments (Routine 2) and return to Step 1.

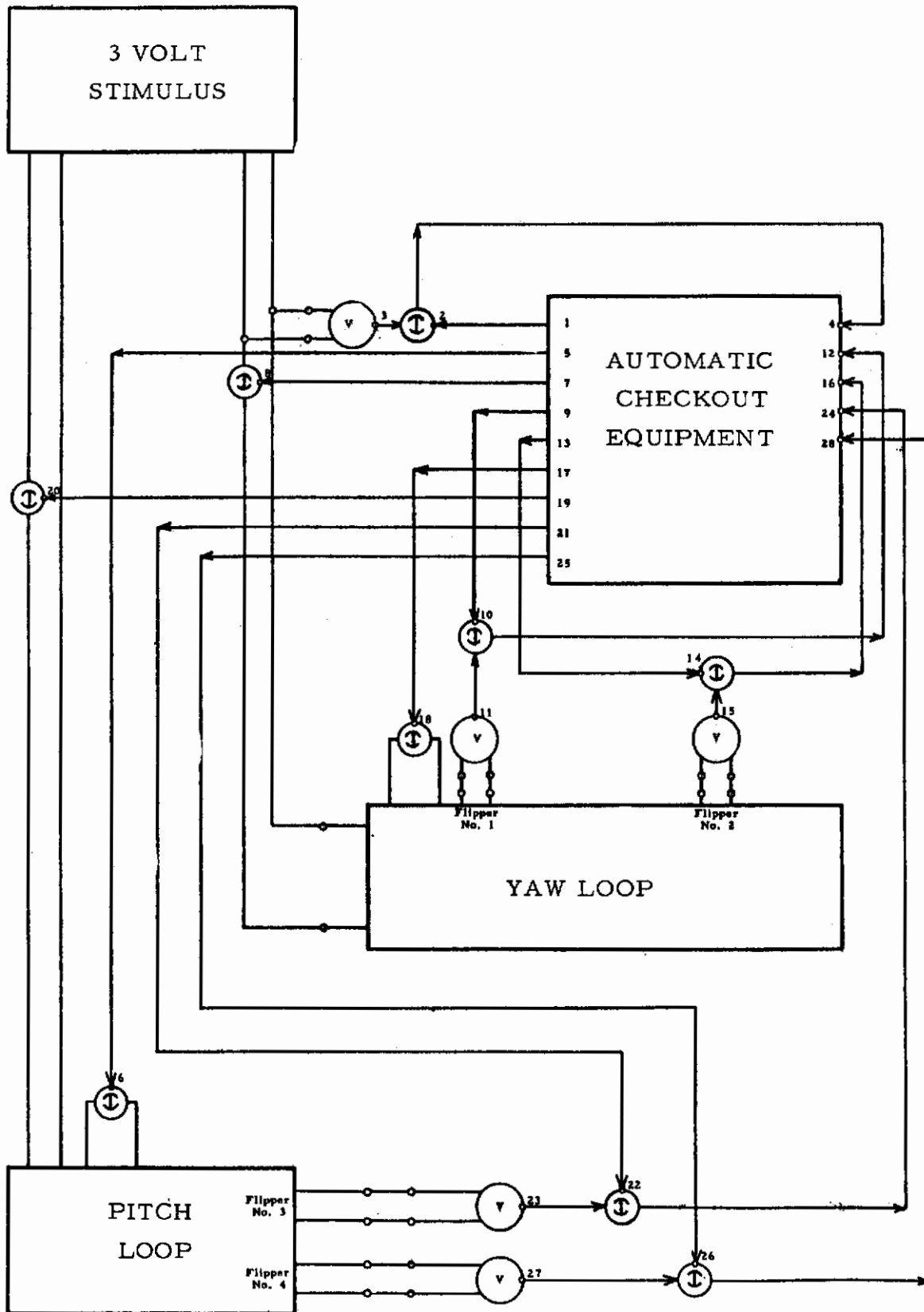


Figure 2 - Diagram of Test Circuit for Subsystem of Missile X

C. PRECEDENCE MATRICES USED FOR ERROR DETECTION

A precedence matrix is a graphical representation of the ordering that exists among a set of elements. Ordering means simply that for each pair of elements A and B in a set of elements, it can be said that A must precede B, B must precede A, or that neither must precede the other. It is not necessary to state explicitly the ordering among all pairs of elements. From the following rules, the ordering relations among certain pairs of elements can be used to find the ordering relation between each pair of elements:

1. If A precedes B and B precedes C, then A precedes C (transitivity).
2. A cannot precede A (non-reflexivity).
3. If A precedes B, B cannot precede A (anti-symmetry).

We refer to Table 1 for examples of these rules. The pitch loop is shorted before a stimulus is applied to the yaw loop to prevent interaction of the two loops. Therefore, step 5 must precede step 6. From rule 2, step 5 cannot precede itself, that is, the pitch loop cannot be shorted before it is shorted. From rule 3, step 6 cannot precede step 5; that is, a stimulus cannot be applied to the yaw loop before the pitch loop is shorted.

Now, step 7 - stabilization of the flippers - cannot take place until the yaw loop is stimulated. Therefore step 6 must precede step 7. From rule 1, step 5 must therefore precede step 7; that is, the pitch loop must be shorted before the flippers are stabilized.

An aid to the visualization of precedences between elements is the use, as illustrated in Figure 3, of a precedence chart, sometimes called a balloon chart. The circles represent steps, and the arrows connect pairs of steps. The tail of the arrow is joined to the step which directly precedes the step to which the head of the arrow is joined. Thus, step 7 directly precedes step 8. A step can be executed only if the steps at the tail of all solid arrows leading into the element have been executed. Thus, step 6 can be executed only after both steps 1 and 5 have been executed.

However, a decision step in the sequence of steps will cause one of two branches to be taken. Whichever branch is taken, some steps will be bypassed. Therefore, it will no longer necessarily be true that all steps with arrows leading into a single step must be executed before that step. An example of this is step 26. It may be executed after any of the steps with arrows leading into it have been executed. To provide for this case, dashed arrows are used to denote this "or" case; that is, if any step whose dashed arrow leads into a step is executed, it satisfies the requirements of all steps having dashed arrows leading into the step.

We are now in a position to construct the precedence matrix illustrated in Figure 4 for the 26 steps of Table 1. It can be constructed

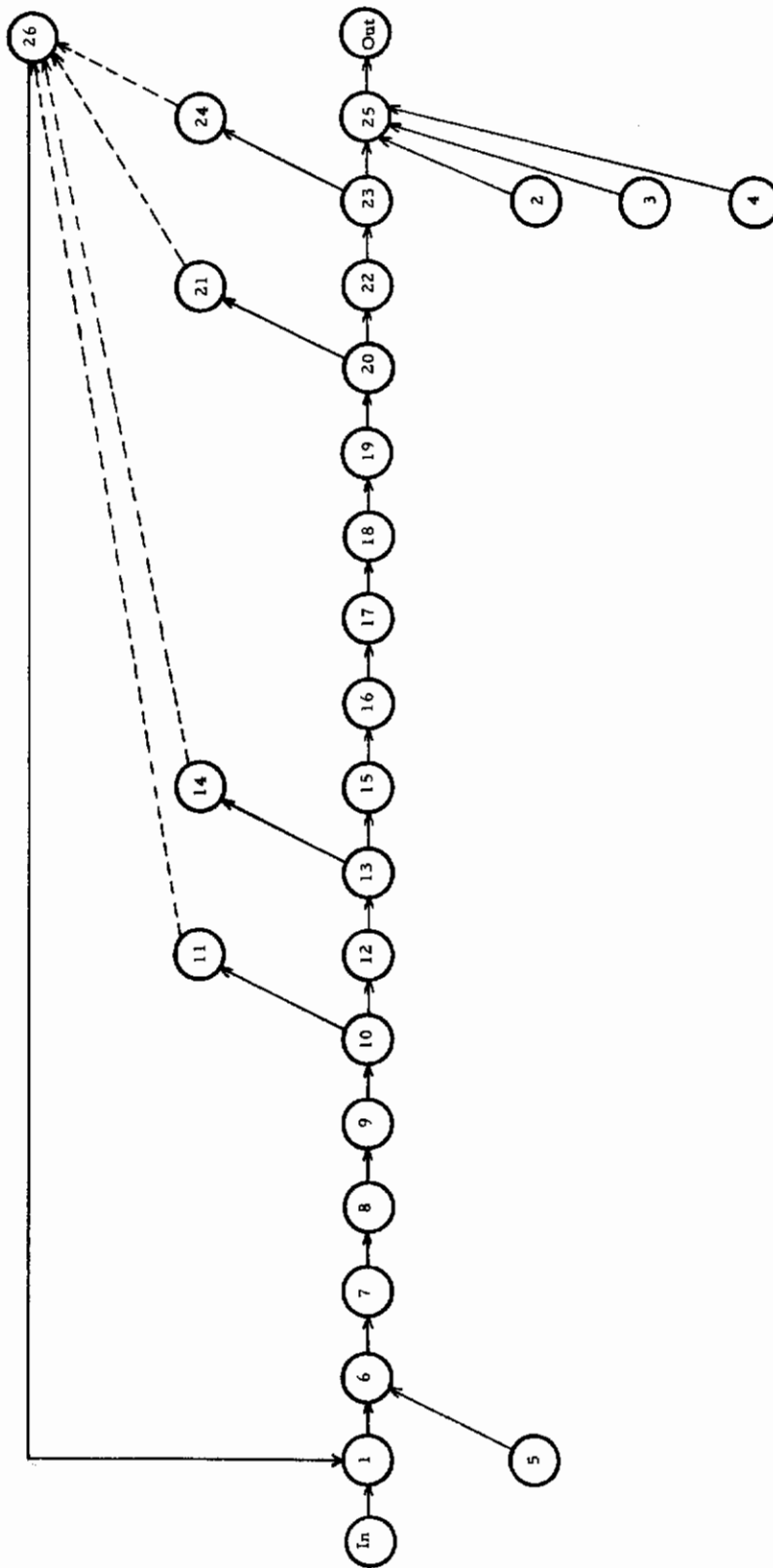


FIGURE 3. PRECEDENCE CHART OF SUB-SEQUENCE OF TESTS ON MISSILE X.

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
1					1																				
2																									1
3																									1
4																									1
5					1																				
6						1																			
7							1																		
8								1																	
9									1																
10										1	1														
11																									+2
12												1													
13													1	1											
14																									+2
15															1										
16																1									
17																	1								
18																		1							
19																			1						
20																				1	1				
21																									+2
22																							1		
23																								1	1
24																									+2
25																									
26	-1																								

FIGURE 4. PRECEDENCE MATRIX OF SUB-SEQUENCE
OF TESTS ON MISSILE X

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directly from Table 1 or from the precedence chart of Figure 3. First, the numbers 1 through 26 are listed across the top and down the left-hand side of the matrix. Next, each pair of elements having a direct precedence is entered into the matrix as follows:

The step at the tail of the arrow is found on the left-hand side of the matrix. This is its row. The step at the head of the arrow is found along the top. This is its column. If the arrow is solid, a 1 is placed at the intersection of the row and column. This indicates that the step in the row must precede the step in the column. If the arrow is dashed, a 2 is placed at the intersection to indicate that the step in the row is part of a group of steps, one of which must precede the step in the column.

All pairs of steps joined by a single arrow are entered into the precedence matrix. These are all of the first-order relationships; that is, all of the relationships in which step A directly precedes step B. The balloon chart is especially useful for constructing the precedence matrix as each single arrow indicates a first-order relationship.

Now, the matrix needs one further modification. One of the objectives of constructing the precedence matrix is to test for inconsistencies. Inconsistencies are steps which violate any of the three rules described above which govern precedence; that is, transitivity, antireflexivity, and antisymmetry. However, loops will cause violation of all three rules, and loops exist in practically all computer programs.

A loop is a sequence of steps in which one of the steps returns to a step which has already been executed. For example, in Table 1, step 26 returns to step 1 which has already been executed. This is legitimate because the testing cycle should be repeated after an adjustment has been made to an out-of-tolerance component. However, in testing for illegal loops and other inconsistencies, the legitimate loops will manifest themselves. It is desired then to mark legitimate loops so that they can be identified when testing for inconsistencies.

Legitimate loops are marked by identifying the link which returns to an instruction which has already been executed. The 1 in the precedence matrix for that link is then changed to a -1. For example, step 26 returns to step 1, therefore there is a -1 in the precedence matrix in row 26 and column 1. In all consistency tests performed on the precedence matrix, -1's will be treated as zeros or blanks, thereby eliminating the links completing a loop, and consequently "cutting" the loop.

The precedence matrix has been constructed. It is now necessary to answer two questions. First, does the matrix truly represent the precedences inherent in the hardware or sequence of tests? Secondly, are there any inconsistencies in the matrix?

The answer to the first question is that there is no way to test the matrix itself to appraise its representativeness. However, it is possible to use alternate methods to produce the precedence matrix to obtain a check on

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the input matrix. For example, the precedence chart could be input in some form and used to produce automatically the precedence matrix. The two matrices should then be identical; comparison will show whether they are or not.

The answer to the second question can be derived by use of two methods, principal submatrices and matrix multiplication. The principal submatrices method checks the consistency of a precedence matrix by deleting zero rows and columns. In effect, it eliminates entrances and exits until there are no more entrances and exits. If there are rows and columns which have not been eliminated, then there are inconsistencies in the matrix. The method in detail is as follows.

The precedence matrix is scanned for a row or column which contains all zeros (-1's are treated as zeros). If there are none, the process is terminated. If there is a zero row or column, it is deleted along with its corresponding column or row. If all rows and columns have been eliminated when the process is terminated, the matrix is consistent. If not, there are inconsistencies in the matrix.

In Figure 4, row 26 contains all zeros (-1 is treated as zero) and is therefore eliminated. Column 26 is also eliminated. Row and column 25 are eliminated, then row and column 24, etc., until all rows and columns are eliminated indicating that the precedence matrix was consistent. Had there been a 1 at the intersection of row 7 and column 5, for example, row 7 and column 7 could not be eliminated, nor could rows and columns 6, 5, and 1. The matrix would have been shown to be inconsistent which is correct if we require that step 7 precede step 5 when we have required that 5 precede 6 and 6 precede 7.

The matrix multiplication method checks the consistency of a precedence matrix by establishing successively higher-order precedence relationships until no more can be established, or until an inconsistency has been revealed. A higher-order relationship is one in which A precedes B, but A and B are separated by several steps. For example, in Figure 3, step 15 precedes step 20, but four other steps intervene.

An inconsistency is revealed when an element is shown to precede itself. For example, if the loop from step 26 to step 1 had not been cut, higher order relationships would cause element 1 eventually to precede itself because 1 precedes 6 which precedes 7 . . . which precedes 26 which precedes 1. Redundancies are also revealed by this method. A redundancy is a precedence relation, explicitly stated in the precedence matrix, which is implied by other precedence relations. For example, if a 1 had been placed in row 5 and column 7, it would be shown to be redundant because it is implied by the 1's in row 5 and column 6 and row 6 and column 7. Redundancies are not inconsistencies, but they may indicate that an indirect relation was not recognized or that a mistaken entry was made.

The details of the matrix multiplication method are as follows. The precedence matrix is multiplied by itself by normal matrix multiplication, except that each entry is treated as a 1 except -1's which are treated as

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zeros. A product of 1 will result in those cases where a 1 occurs in the same numbered rows and columns. For example, in Figure 3, a 1 occurs when row 5 is multiplied by column 7, implying that step 5 precedes step 7. This is a second-order relation and is the implication of row 5 preceding row 6 and row 6 preceding row 7. If the product of a row and a column is greater than one, then there is an error in one of the matrices, and a diagnostic is printed.

The resulting 1's are stored along with the original matrix. If a 1 is generated for which an entry already exists, this redundancy is noted and the process is continued. If a 1 is generated on a diagonal, this implies that a step precedes itself, and constitutes an inconsistency. This is noted and the process is terminated. The matrix which results from multiplying the original precedence matrix by itself is again multiplied by the original precedence matrix, the 1's are stored, and the process continues until either an inconsistency is noted or a matrix of all zeros is produced. The final matrix, which is the collection of the original precedence matrix and all of the 1's generated, will contain all of the explicit and implicit precedence relations which exist among the steps.

We have shown how to construct a precedence matrix, how to appraise its conformity to reality, and how to check its consistency. It remains to describe the use of the precedence matrix in detecting errors in checkout programs.

First, a distinction must be made between the two types of precedences, hardware and flow diagram. Hardware precedences are constraints on the order in which it is physically possible to activate the elements of a hardware system. A power tool, for example, must be plugged in and switched on before it can be operated. The plugging in and switching on must both therefore precede the operating, even though the first two steps can be done in either order.

Flow diagram precedences are constraints on the order in which it is desired to execute steps. They derive their name from the flow diagram, which is a graphical representation of the sequencing of steps. The steps of a flow diagram may represent any process, physical or mental, hardware or software, and their desired order may have any motivation.

For example, flow diagram precedences may constrain a power tool, in the interests of safety, to be plugged in before it is switched on, even though it is physically possible to commute these steps. Or they may constrain the instructions of a computer program, for computational accuracy, to be executed in a given order even though there is a wide latitude on the possible order of execution.

A gray area in the definition of precedences is in the realm of destructive hardware activations. It may physically be possible to activate hardware in a given order, and yet the hardware may be degraded by the process. Precedences which prevent degradation of hardware are flow diagram precedences by the definition given. But they must reasonably be regarded as hardware precedences since it can be assumed that degradation of hardware is always to be avoided.

1. Precedence Matrices Used with Total Simulation

For the total simulation method, it is assumed that a simulation program exists which operates on each instruction of an object (machine language) program. The simulation examines each instruction, checks it for correct format, checks each field of the instruction for validity, then executes the instruction and examines the states of all registers for possible violation of computer hardware restrictions (numeric overflows, underflows, tape redundancies, etc.).

As the object program instructions are executed by the simulator, the precedence matrix is used to check that the sets of instructions which correspond to the steps of the precedence matrix are executed in accordance with the precedence relations expressed in the precedence matrix. The steps in the precedence matrix can refer either to computer program steps or to activations of hardware.

In order to perform the precedence checks, it is necessary that the simulation program have available not only the precedence matrix, but also the link between the matrix and the computer instructions; that is, the simulation program must be able to identify the computer instruction which corresponds to the beginning of each step and the computer instruction which corresponds to the end of the step.

The information which links the precedence matrix to the computer instructions can be expressed in two forms. In the first form, it is assumed that some computer register has unique states for each point of reference to a step in the precedence matrix. For example, arithmetic register A may contain a binary configuration that is unique for each reference to a step in the precedence matrix. A table is then constructed in which one column contains the precedence matrix steps, and the other two columns contain the binary configurations of register A which correspond to the initiation and termination of that step.

In the second form of link, it is assumed that the locations in computer memory are known where starting and ending instructions which correspond to each precedence matrix step are executed. A table is then constructed in which the first column contains the number of the precedence matrix step, the second column contains the location of the instruction which represents the beginning of that step, and the third column contains the location of the instruction which represents the end of that step.

The latter table above can be generated and input by the programmer, or it can be generated by an assembler or compiler if the symbolic name of each assembler or compiler instruction that corresponds to a precedence matrix step is marked in a special way. For example, names starting with ST could be reserved for instructions which correspond to the initiation of a matrix step, and names starting with EN could be reserved for instructions which terminate a matrix step. Numbers appended to letters could give the number of the step. For example, ST13 and EN13 would be the starting and ending instruction of the group of instructions which correspond to step 13 in the precedence matrix.

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Whichever form the link between the computer program and the precedence matrix takes, a table is constructed which informs the simulation when it is at the beginning and at the end of a precedence matrix step. Thus, as the simulation processes an instruction, it queries the table to determine if the instruction is the start or end of a precedence matrix step.

If an instruction is the start of a precedence matrix step - call it step Y - then a temporary storage location is tested to determine if the last precedence matrix step initiated has been terminated. If not, a diagnostic is printed. If it was terminated, then the precedence matrix is queried in the following way. Column Y is scanned for entries. If there are no entries, then there are no precedence restrictions on when it can be executed, and execution is performed.

If there are 1's or -1's, then the steps for the rows corresponding to any of the 1's or -1's must be executed before Y can be executed. If there are 2's then the step for one of the rows corresponding to the 2's must be executed before Y is executed. If we assume, however, that a process is used whereby all entries in a column are replaced by zero when the indicated precedences are satisfied, then if the column contains all zeros, execution is performed, and if it contains any non-zero entries, a diagnostic is printed.

The process for reducing a column to zero when all precedences are satisfied is as follows. First, a matrix - call it matrix M - identical to the initial precedence matrix, is constructed. Then, as each step is executed, that is, when both the starting and ending instructions corresponding to the step are executed, all of the entries in the row in matrix M for that step are replaced by zero. For each 2 that is set to zero, all of the other 2's in the same column are also set to zero. This is to satisfy the "or" condition mentioned previously.

One condition must still be satisfied: that of the -1's, the condition of looping. It is handled as follows. When a -1 is replaced by zero, the number of the column in which the -1 appeared is recorded. The next time the step corresponding to that column is executed, the entire matrix M is restored from the original precedence matrix. Thus, when the program loops back, the precedence relations must be satisfied anew.

2. Precedence Matrices Used with Partial Simulation

A partial simulation method may be used to trace through all paths of a program. Precedence matrix techniques may then be used to check that each path is in conformance with the precedence constraints. The method can be used only with programs in which instructions are not altered during execution of the program. The details of this method are as follows.

It is assumed that a simulation program exists which checks the operation code of each instruction of an object program to determine if it is a branching type instruction; that is, to determine if the choice of the next instruction to be executed is limited to one instruction or more than one. If it is not a branching type instruction, the next instruction is processed.

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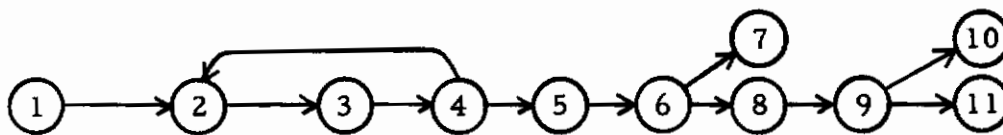
If the instruction is a branching type, then each branch is stored in a table. One of the branches is then chosen, and the program processes that instruction next. The process continues until a termination instruction, stored in a table of termination instructions, is encountered. The simulation program then returns to the last branching instruction, chooses another branch, and continues processing from that instruction. When all the branches of the last branching instruction have been processed, the program returns to the next-to-the-last branching instruction, etc., until all paths of the program have been traced.

Each path, as it is traced, is checked against the precedence matrix. If violations occur, diagnostics are written, the path is terminated, and the next path is taken. Each path is also written out as it is traced. The path may then be used to generate test cases of input data or to manually trace through the program for debugging purposes.

One difficulty in the method is that computer programs contain many legitimate loops. If the loops are not provided for, the simulation program will process the first such loop indefinitely. This can be avoided by storing the location of each instruction executed. If a branch is made to a previously executed instruction, then a comment is written on the trace of that path that a loop back to an instruction is made, and the next branch is processed.

It is not necessary to store in a separate computer word, the location of each step executed. A single bit within a computer word can be set to 1 to indicate that the step corresponding to that bit has been processed. For example, 900 36-bit words could be used to store the execution of 32,400 instructions.

A simple example will illustrate the use of precedence matrices with partial simulation methods. Suppose a program proceeds from location 1 to 2 to 3 to 4 then branches to 5 or back to 2. From 5 it proceeds to 6 then branches to 7 or 8. From 8 it proceeds to 9 then branches to 10 or 11. 7, 10, and 11 are terminating instructions. The balloon diagram for this program is the following:



The partial simulation processes instructions 1, 2, 3, and 4 and stores each number in the table of instructions processed. It notes that instruction 4 is a branching instruction and stores 2 and 5 in the table of branches. It chooses 2 and begins to process it. It then notes that 2 has already been processed and writes out the path of the program as "1, 2, 3, 4, loop back to 2." It then goes to the last branch, which is 5, processes 5 and 6, stores them in the table of instructions processed, and notes that 6 is a branching instruction.

Locations 7 and 8 are stored in the branch table, and 7 is chosen for processing. 7 is a terminating instruction and the path, "1, 2, 3, 4, 5, 6, 7,"

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is written out. The program returns to the last branching instruction 6, and now chooses 8 to be processed. 9 is then processed, 10 and 11 are stored in the branch table, and 10 is processed. The path, "1, 2, 3, 4, 5, 6, 8, 9, 10," is written out, 11 is processed, and the path, "1, 2, 3, 4, 5, 6, 8, 9, 11," is written out. All paths have now been traced.

The precedence matrix for this program is the following:

	COLUMN										
	1	2	3	4	5	6	7	8	9	10	11
1		1									
2			1								
3				1							
4		-1			1						
5						1					
ROW 6							1	1			
7											
8									1		
9										1	1
10											
11											

As each of the four paths is traced, the precedence matrix is checked for violation of precedences. In this example, each of the four paths is in conformance with the precedences, and all 11 program steps are represented in the precedence matrix. In a normal program, the steps in the precedence matrix would probably be limited to branching steps and entry points into loops.

This completes the description of the use of precedence matrices to detect errors in object programs. The following section describes the use of connection matrices to detect errors in object programs.

D. CONNECTION MATRICES USED FOR ERROR DETECTION

A connection matrix is a graphical representation of the connecting links between the automatic checkout equipment and the equipment-under-test, in this case Missile X. The connecting links may be hard-line, that is, cables, or they may be RF links. The significant factor is that points exist in the automatic checkout equipment which generate stimuli or read responses, points exist in the equipment-under-test which accept stimuli or create responses, and a link may or may not exist between any pair of these points.

In Figure 5, the connections between stimulus, stimulus acceptance, response, and response acceptance points are illustrated. The stimulus and response points are entered across the left-hand side and the stimulus

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STIMULUS ACCEPTANCE AND RESPONSE ACCEPTANCE POINTS

	2	4	6	8	10	12	14	16	18	20	22	24	26	28
1	1													
3		-1												
5			1											
7				1										
9					1									
11						-1								
13							1							
15								-1						
17									1					
19										1				
21											1			
23												-1		
25													1	
27														-1

FIGURE 5. CONNECTION MATRIX OF SUB-SEQUENCE OF TESTS ON MISSILE X.

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acceptance and response acceptance points are entered across the top. For each stimulus point which is linked to a stimulus acceptance point, a 1 is entered at the intersection of the stimulus point row and stimulus acceptance point column. For each response point that is linked to a response acceptance point, a -1 is entered at the intersection of the response point row and response acceptance point column.

In Figure 5, stimulus point 5 is linked to stimulus acceptance point 6, and a 1 is entered in the row marked 5 and the column marked 6. Response point 3 is linked to response acceptance point 4, and a -1 is entered in the row marked 3 and the column marked 4. As in the case of the precedence matrix, the conformity of the connection matrix to the reality of the hardware must be tested either by carefully checking circuit diagrams of the hardware, or by using an alternate method for producing a connection matrix and comparing the two.

It will be assumed for connection matrices, as for precedence matrices, that a table can be constructed with which the simulation can determine that a row or column entry in the connection matrix has been referenced. The table would consist of one column listing the row entries followed by the column entries and a second column listing either the state of some register when the column or row heading is referenced or the instruction location of the reference.

The connection matrix would then be used as follows. For each instruction, the simulation would scan the table to determine if the connection matrix had been referenced. If so, the number of the reference would be recorded. If a previous reference had been recorded, then the two references would be tested to see if they were both row or column entries. If so, a diagnostic would be printed.

If the two references were not both row or column entries, the intersection of the row corresponding to one and the column corresponding to the other would be tested for a non-zero entry. If the entry is zero, no link exists, the references are not valid, and a diagnostic is printed. If the entry is non-zero, the sign of the entry must be tested. If the first reference was a row reference, then the sign of the entry should be positive. If the first reference was a column reference, then the sign of the entry should be negative. If the test reveals that the sign is incorrect, a diagnostic is printed. If the entry is correct, a flag is set to indicate that a link was completed and that the next reference will be the start of a new link.

The following section describes, in detail, the implementation in the VATE System of precedence and connection matrix techniques used with total simulation methods. The scope of the project did not allow implementation in the VATE System of precedence matrix techniques used with partial simulation methods.

SECTION V

IMPLEMENTATION IN THE VATE SYSTEM OF PRECEDENCE AND CONNECTION MATRIX TECHNIQUES USED WITH TOTAL SIMULATION METHODS

A. INTRODUCTION

To evaluate the practicability of using precedence and connection matrix techniques with total simulation methods to detect errors in checkout programs, it was desired to implement the techniques in an operational computer-controlled automatic checkout system. The automatic checkout system must have a total simulation computer program. As far as could be determined, the VATE (Versatile Automatic Test Equipment) System was the only automatic checkout system which was computer-controlled and had a total simulation computer program.

In the VATE System, Hughes Aircraft Company HCM-111 computers are used to control the checkout process. The HCM-111 is a drum-storage stored program computer with approximately 40,000, 22-bit words of storage. A simulation program was written by Hughes for the IBM 7090 to simulate the operation of the HCM-111. This simulation program, and the other materials and staff consultation time required to incorporate precedence and connection matrix techniques in the VATE System, were made available by Hughes Aircraft Company.

Flow diagram and hardware precedence matrix and connection matrix techniques were successfully implemented in the VATE simulator, and a number of test runs were made with an operational automatic checkout program. This section contains a detailed description of the implementation; the following section contains an evaluation of the results of the implementation.

B. METHOD OF IMPLEMENTATION

In order to implement precedence and connection matrix techniques in the VATE System, the following elements were required to produce a simulation system modified by the techniques:

- Specifications for the HCM-111 and its programming system.
- A link between the precedence and connection matrices and the execution of computer program instructions.
- A precedence matrix for the hardware precedences.
- A precedence matrix for the flow diagram precedences.
- A connection matrix for the connections between the automatic checkout equipment and the prime equipment.

- Continued*
- The simulation computer program.
 - A set of computer program modules incorporated in the simulator to test the consistency of the precedence matrices, to read and write data, to test conformance of the order of execution of instructions with the precedences as manifested by the precedence matrices, and to test the validity of requested connections between the automatic checkout and prime equipment.
 - An operational automatic checkout computer program with which to validate the techniques.

Given all of these elements, the modified simulation system operates as follows. The precedence and connection matrices, and the data required to relate these to the execution of the object program, are read. The precedence matrix is checked for consistency, and diagnostics are written if inconsistencies are found. The operational automatic checkout program (system program) is then read.

As each instruction of the system program is executed, the data relating instructions to the precedence matrix is used to determine if the precedence matrix has been referenced. If not, execution proceeds. If the matrix has been referenced, the precedences are checked to determine if any have been violated. The connection matrix is then checked to determine if the proper connections have been made.

If violation of precedences or connections occur, diagnostics are written, and the program is terminated. If violations do not occur, comments to that effect are written, and execution of the system program proceeds. Each element of the modified simulation system will now be described in detail.

1. Specifications of the HCM-111 and Its Programming System

The Hughes Aircraft Company HCM-111 is a drum-storage stored program computer with approximately 40,000, 22-bit words of storage. The rotating drum has 128 channels or tracks, most of which contain 320 words or sectors. The instruction repertoire of twenty-three orders varies in format, but basically, each order specifies the channel from which the next order is to be read, the function to be performed by the present order, and the number of sectors to wait (words-to-wait) before reading the order from the next channel.

Thus, if we are presently executing a transfer order from channel 160, sector 100, the next channel to be read is 165, and the words-to-wait are 150; then the next order will be executed from channel 165, sector 251. Channels, sectors, and words-to-wait are expressed in the octal number system, that is, to the base 8, rather than in the decimal system.

A detailed description of the instruction repertoire of the HCM-111 and, in fact, of the entire VATE System, is contained in a five volume set of manuals prepared by Hughes Aircraft Company - VATE Project - Technical

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Training Section - and will not be presented here. However, the specific order used to relate hardware activation to the precedence matrix will be discussed.

Digital and analog outputs from the HCM-111 to the automatic checkout equipment and prime equipment, and inputs from these equipments to the HCM-111 are effected by reference to "P," which is the designation of the computer logic and registers which process digital and analog inputs and outputs. Basically, when an order causes information to be sent to P (P as a destination), digital or analog outputs are sent to the automatic checkout equipment and prime equipment. When information is required from P (P as a source), digital or analog inputs from the equipments are derived.

A number of orders can have P as a source and can consequently derive analog or digital inputs. However, the TPK order is the only order in which P is a destination and is consequently the only order which creates digital or analog outputs. Therefore, to simplify modification of the HCM-111 simulator, the TPK order was chosen as the link between the hardware activation precedence matrix and the execution of the operational automatic checkout program.

It is necessary to understand the TPK order in order to understand its use in the implementation of precedence and connection matrix techniques. Suppose the instruction 165TPK001 is stored in channel 165, sector 100 (165.100) and the constant 13770131 is stored in channel 165, sector 101 (165.101). The interpretation of the instruction 165TPK001 is the following: "use the constant stored in 165.101 to create an output to the equipments."

The last three octal digits, 131, of the constant in 165.101 determine whether the output will be digital or analog. They also determine, for analog outputs, which of 64 DC analog memory devices will be selected and, for digital outputs, which of 65 groups of 10 digital outputs (toggle circuits) will be selected.

If a digital output has been referenced, the first ten binary digits (1377=1101111111) of the constant in 165.101 determine the setting (open or ground) of each of ten toggle circuits. If an analog output has been referenced, the first nine bits of the constant are the magnitude (with sign) of the adjustment factor to be applied to the selected analog device.

2. Link Between the Precedence and Connection Matrices and the Execution of Computer Program Instructions

From the above discussion of the TPK instruction, a method of linking hardware precedence and connection matrices to the execution of the checkout program becomes apparent. Digital and analog outputs can be sent to the equipments only by use of a TPK order. Therefore, when the simulator processes a TPK order, a check is made to determine if the precedence matrix has been referenced.

For hardware precedences, the links between the precedence matrix and the checkout program are lists (link lists) of the values that the

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constants following the TPK orders will have for the TPK orders that correspond to the initiation and termination of each step in the precedence matrix. For example, if the first step in the precedence matrix is initiated by a TPK order stored in 167.100 and is terminated by a TPK in 162.253, then the first entry in the starting link list will be the value of the constant in 167.101 and in the ending list will be the value of the constant in 162.254.

Flow diagram precedences can be independent of hardware since they can express the flow of computation rather than of hardware activations. To encompass both cases, flow diagram precedences are linked to the checkout program by the HCM-111 locations at which the steps of the flow diagram are initiated and terminated.

For example, if the instruction which initiates the third step in the precedence matrix is executed in 155.320, and that which terminates the third step is executed in 157.113, then the third entry in the flow diagram starting link list will be 157.113 and in the flow diagram ending link test will be 155.320.

Connections between the automatic checkout equipment and the prime equipment occur with digital output hardware activations, with a TPK order creating the digital output. The high order ten binary digits of the constant following the TPK order contain the settings of toggle switches which ultimately create a link between the equipments.

The links between the connection matrix and the checkout program are 1) a list of all permissible combinations of ten bits, 2) for each permissible combination of ten bits, the column in the connection matrix which corresponds to the component in the automatic checkout system at one end of the connection, and 3) the column which corresponds to the component in the automatic checkout equipment at the other end of the connection.

3. Construction of Precedence, Connection, and Link Matrices

The hardware precedence matrix represents the constraints on the order in which elements of the hardware can be activated. The flow diagram precedence matrix represents the constraints on the order in which program steps may be executed. The connection matrix represents the connections which exist between the automatic checkout equipment and the prime equipment. The link matrices link the precedence and connection matrices to the execution of the automatic checkout program.

The hardware precedence and connection matrices are constructed from a knowledge of the flow of computation of the automatic checkout program and of the HCM-111 locations in which selected orders are executed. The construction of each type of matrix will be treated in detail in a later section in which the use of these matrices with a selected automatic checkout program is described.

4. The HCM-111 Simulation Program

The HCM-111 simulator is a several thousand instruction simulation computer program written for the IBM 7090 in assembly language (FAP). The simulator executes HCM-111 orders in a manner not identical, but very similar, to their execution in the HCM-111 itself. The simulator reads an HCM-111 program and additional data which tell the simulator, among other things, where to start and stop execution, which HCM-111 channels can be used for storing orders, and the sequence of values which should be input from the hardware if it is desired that the values be non-zero.

The simulator performs many tests on an order before it is executed. For example, it tests that the order is indeed an order and not a constant. It tests the operation code of the order for validity, and it tests that the value of words-to-wait is within allowable limits. The simulator does not test the order of execution against the hardware precedences or flow diagram precedences, or the validity of connections, although it does produce a listing which could be used to make these tests by hand.

There is a unique set of instructions in the simulator which process the TPK order. A transfer was inserted among these instructions to the computer program modules which process hardware precedence and connection matrices. There is a location in the simulator that is executed for all instructions. A transfer to the computer program module which processes flow diagram precedence matrices was inserted at that location.

5. Computer Program Modules for Precedence and Connection Matrices

Appendix I contains a prose description, flow charts, and a computer program listing of the program modules which were written to implement the use of precedence and connection matrices in the VATE System. The following description of the modules is qualitative and brief and is included here to facilitate the understanding of subsequent material.

Six computer program modules were written for use with the simulator. The six modules are named as follows:

- MAIN PROGRAM
- READ
- WRITE
- START
- CHEKIN
- PREC

MAIN PROGRAM is a small FORTRAN routine which controls the order of execution of the five other subroutines and the simulator.

READ is a FORTRAN subroutine which reads all of the required information, including matrices.

WRITE is a FORTRAN subroutine which writes all of the diagnostics and comments which result from testing for precedences and connections.

START is a FAP subroutine which tests the precedence matrices for consistency.

CHEKIN is a FAP subroutine that tests the flow diagram precedence matrix for violations of precedences when the precedence matrix has been referenced during the execution by the simulator of a checkout program order.

PREC is a FAP subroutine that tests the hardware precedence matrix for violations of precedences, and the connection matrix for illegal connections, when these matrices have been referenced during execution of the simulator.

The Main Program calls READ which reads the dimension of the matrices, the matrices themselves, and a constant which indicates the type of precedence matrix that was read - flow diagram or hardware. START is then called to test the precedence matrix for consistency using the row and column deletion method. If the matrix is not consistent, diagnostic information is written, and the program is terminated.

If the precedence matrix is consistent, a comment to that effect is written, and the HCM-111 simulator is called. The simulator reads the automatic checkout program to be executed and proceeds to process the program. If the precedence matrix is a hardware type, each TPK instruction causes PREC to be called, which tests the constant in K to see if the precedence matrix is referenced. If not, return is made to the simulator and processing continues.

If the TPK instruction references the precedence matrix, the precedences and connections are tested for violations. If violations occur, diagnostics are written and the program is terminated. If they do not occur, a comment to that effect is written and return is made to the simulator.

If the precedence matrix is a flow diagram type, CHEKIN is called as each new order of the checkout program is processed. If the location of that order references the precedence matrix, the precedences are tested, and the program is terminated if violations exist or return is made to the simulator if violations do not exist.

6. Operational Automatic Checkout Programs

The D17 Computer Voltage Output Diagnosis automatic checkout program was used to validate the precedence and connection matrix.

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techniques. The D17 program is designed to load and execute instructions in the D17 computer which force the voltage output logic and registers to assume predetermined logic states. If the voltage output logic is faulty, the voltage output registers will assume other than the predetermined logic states.

The program operates in eight sequential segments; the D17 must sequentially pass all eight segments before the voltage output logic may be considered to be functioning correctly. The functions of the eight segments are the following:

- Segments 1 and 2 determine if it is possible to reset all the voltage output flip-flops to their false and true states, respectively.
- Segment 3 determines if any of the set-reset gates for specified flip-flops are faulty.
- Segment 4 determines if the logic driver can be set false.
- Segment 5 determines if specified logic drivers and the corresponding AND-diodes on two primary-AND gates are functioning properly.
- Segment 6 checks specified timing terms and a diode on a specified primary AND gate.
- Segments 7 and 8 check specified diodes on two primary AND gates.

C. DETAILS OF IMPLEMENTATION WITH OPERATIONAL AUTOMATIC CHECKOUT PROGRAM

The modified simulation system was used to process the D17 Computer Voltage Output Diagnosis automatic checkout program (D17 Program). The following six steps in the D17 Program were used to construct a hardware precedence matrix, a connection matrix, and link matrices:

1. Set loading digital outputs.
2. Reset digital outputs CIT and ECI.
3. Set digital output DFF.
4. Set digital output HLT off, digital outputs RUN and SCY on.
5. Set master reset.
6. D17 synchronized, reset master reset.

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Each of the six steps correspond to a single TPK order, so that the initiating and terminating order for each step are identical. The channel and sector of execution, and the value of K for each of the steps are the following:

	<u>Channel and Sector</u>	<u>Order</u>	<u>K</u>	<u>Step</u>
1.	160.154	160TPK001	0.1610124	Set Loading DOS
2.	160.374	160TPK001	0.7550135	Reset DOCIT, DOECI
3.	160.376	160TPK001	1.3770131	Set DODFF
4.	160.402	160TPK004	0.2600132	Set DOHLT OFF, DORUN, DOSCY ON
5.	160.407	160TPK001	0.0000136	Set MASTER RESET
6.	160.131	160TPK001	1.0000136	SYNCHED, RESET MASTER RESET

The hardware precedences constrain the six steps to be performed in the order given. Thus, step 1 must precede step 2, step 2 must precede step 3, step 3 must precede step 4, step 4 must precede step 5, and step 5 must precede step 6. The precedence matrix is the following, where an entry of 1 indicates that the step for the row containing the 1 precedes the step for the column containing the same 1:

		COLUMN					
		1	2	3	4	5	6
ROW	1		1				
	2			1			
	3				1		
	4					1	
	5						1
	6						

The KFIRST and KSEC link lists, which contain the value of K for each reference to the start and end of a precedence matrix step, are the following:

	<u>KFIRST</u>	<u>KSEC</u>
1.	000001610124	000001610124
2.	000007550135	000007550135
3.	000013770131	000013770131
4.	000002600132	000002600132
5.	000000000136	000000000136
6.	000010000136	000010000136

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The connection matrix is the following, where a 1 represents a link between the row entry device and the column entry device for the row and column in which the 1 appears:

		PRIME EQUIPMENT					
		1	2	3	4	5	6
AUTOMATIC CHECKOUT EQUIPMENT	1	0	1	0	0	0	0
	2	1	0	0	0	0	0
	3	1	0	0	0	0	0
	4	0	0	1	1	0	0
	5	0	1	0	0	0	0
	6	0	0	0	0	0	0

The connection link list contains a list of all permissible bit configurations and the row and column of the connection matrix referenced by each bit configuration. The bit configuration appears in the middle four octal digits, the column referenced appears in the next to the last octal digit, and the row in the low order octal digit. The connection link list is the following:

1. 000001610102
2. 000007550103
3. 000013770201
4. 000002600205
5. 000000000304
6. 000010000404

For the flow diagram precedence matrix, seven program steps were chosen. The steps are executed in the following channels and sectors:

<u>STEP</u>	<u>CHANNEL AND SECTOR</u>
1	166. 111
2	014. 420
3	174. 100
4	160. 154
5	160. 120
6	161. 101
7	176. 157

The program flow is from step 1 to step 2 to step 3 to step 4, loop back to step 2, then to step 3, to step 5, loop back to step 2, then to step 3, to step 6, to step 7, and out. The precedence matrix is the following, where 1 is as described above, and a -1 represents a loop back to a previously executed step:

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		COLUMN						
		1	2	3	4	5	6	7
ROW	1	0	1	0	0	0	0	0
	2	0	0	1	0	0	0	0
	3	0	0	0	1	1	1	0
	4	0	-1	0	0	0	0	0
	5	0	-1	0	0	0	0	0
	6	0	0	0	0	0	0	1
	7	0	0	0	0	0	0	0

The KFIRST and KSEC link lists are the following:

	<u>KFIRST</u>	<u>KSEC</u>
1.	000000166111	000000166111
2.	000000014420	000000014420
3.	000000174100	000000174100
4.	000000160154	000000160154
5.	000000160120	000000160120
6.	000000161101	000000161101
7.	000000176157	000000176157

Appendix II contains listings of the execution of the D17 Program with the modified simulation system for each of the following conditions:

1. No precedences or connections specified.
2. The hardware precedence matrix, connection matrix, and KFIRST and KSEC lists given above.
3. A modified hardware precedence matrix for which the D17 Program will violate precedences.
4. A modified connection matrix for which the D17 Program will call for invalid connections.
5. The flow diagram precedence matrix and KFIRST and KSEC lists given above.
6. A modified flow diagram precedence matrix for which the D17 Program will violate precedences.
7. An inconsistent flow diagram precedence matrix.

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It is seen from Appendix II that comments that the precedence and connections were valid were written when no violation occurred and that diagnostics were written when precedences were violated or connections were not valid. In addition, a comment was written when the precedence matrix was consistent, and diagnostics were written when the precedence matrix was inconsistent.

SECTION VI

EVALUATION OF IMPLEMENTATION IN VATE SYSTEM OF PRECEDENCE AND CONNECTION MATRIX TECHNIQUES USED WITH TOTAL SIMULATION METHODS

A. INTRODUCTION

Precedence and connection matrix techniques developed in this study are general techniques and are intended to be applicable to any computer-controlled automatic checkout system. The techniques were implemented in the VATE System to assess their practicability and to gain a clearer insight into the general problems that are encountered in implementing these techniques in operational systems. One implementation does not establish a general case, but the following evaluations are felt to be reasonable ones.

B. EVALUATION OF HARDWARE PRECEDENCE MATRIX TECHNIQUES

Although hardware precedences can be used to detect errors in operational automatic checkout programs, they are usually not very restrictive. That is, there are normally not very many physical constraints on the sequencing of hardware activation. However, hardware precedences have the advantage of being independent of the computer programs used to test the hardware and of being invariant for as long as the hardware remains unchanged. The hardware precedence and link matrices can be constructed and used unchanged for relatively long periods.

C. EVALUATION OF FLOW DIAGRAM PRECEDENCE MATRIX TECHNIQUES

Flow diagram precedences can be useful in detecting errors in any type of computer program and, specifically, in operational automatic checkout programs. The two difficulties in using them are: 1) they are a function of the desired order of execution of program steps and are subject to frequent change and to greater error in constructing the precedence matrix, and 2) the link matrix may have to contain the location in computer storage in which the steps are executed, in which case it, too, is subject to frequent change because of changes in the coding or in the program steps.

The second difficulty can be minimized if, for each program step, there exists a unique state of some computer register which is not a function of the location of execution of program steps. In the VATE System, the "P" register satisfied this condition for all steps which created analog or digital outputs. The unique states of the register will be invariant, and the link matrix need be changed only when new steps are added to the precedence matrix rather than each time the coding of the program is changed manually or the program is recompiled.

If a compiler language exists for writing automatic checkout programs, then the link matrix can be generated automatically by marking

the start and end of steps, perhaps with special tags, and including computer program modules in the compiler which will generate and write out either the location of execution of the steps or the unique states of some register. This process would minimize the effort and the errors attendant on the construction of the link matrix.

Difficulties in constructing precedence matrices for flow diagram precedences may be minimized by careful construction of the balloon chart illustrated in Figure 3 and careful translation of the balloon chart into the precedence matrix. Alternatively, the precedence matrix could be constructed with and without the use of the balloon chart and the two matrices checked for identity.

D. EVALUATION OF CONNECTION MATRIX TECHNIQUES

Connection matrix techniques are useful in detecting errors in operational automatic checkout programs. The greater the number of possible connections, the more useful are the techniques. In the VATE System, the link matrix could have sufficed to determine legitimate connections without the connection matrix because the link matrix listed all of the bit configurations which represented legitimate connections. However, if the link matrix was constructed as the ultimate list of legitimate connections, but all connections may not yet have been effected, than a connection matrix would be required and could be updated as connecting lines were installed in the operational system.

E. EVALUATION OF PROGRAMMING AND SPACE REQUIREMENTS

The effort required to incorporate precedence and connection matrix techniques in a simulation system is relatively small compared to the effort required to write the total simulation system. However, the space required may be not inconsiderable. If there are N rows in both the precedence and connection matrices, then approximately $3N^2 + 9N$ locations are required for storage of matrices and about 1,000 locations for storage of other data. If there are 30 rows in both the precedence and connection matrices, then roughly 4,000 locations would be required. Sophisticated programming techniques could reduce this requirement. The fact that a simulation is usually written for a larger computer also reduces the severity of this condition.

F. EVALUATION OF SIDE-BENEFIT OF CONSTRUCTION OF MATRICES

The necessity for constructing precedence, connection, and link matrices has a side-benefit in that it requires the person, probably a test engineer, who is forming the precedence and connection matrices to study the precedences and connections in detail and to verify their accuracy and representativeness by various methods. It requires the person, probably an engineer-programmer, who is constructing the link matrices, to study the relation between the program and the hardware in detail. The procedures are desirable even if the matrices are not subjected to machine processing.

CONCLUSIONS AND RECOMMENDATIONS

The practicability of using precedence and connection matrix techniques with total simulation methods to detect errors in operational automatic checkout computer programs has been demonstrated by implementing the techniques in the VATE System. The techniques should be practicable for any computer-controlled automatic checkout system for which a simulation computer program exists for a large scale computer. If the simulation is written for a smaller computer, storage problems must be analyzed carefully.

The practicability of using precedence and connection matrix techniques with partial simulation methods was not demonstrated with an implementation, but appears to be reasonable. The method has the advantage of requiring only a partial simulation, which entails considerably less effort and storage than a total simulation. It might be possible to implement this method on a medium or small-scale computer.

On the basis of this study, the following recommendations are made:

1. Development of precedence and connection matrix techniques used with total and partial simulation methods should be continued to the point that implementation in any computer-controlled automatic checkout system can be made with minimum effort.
2. Modification of the methods to include automatic error correction, as well as detection, should be investigated.
3. Compiler languages and systems developed for processing automatic checkout computer programs should have provision for the inclusion of modules to process precedence and connection matrix related statements.

Continents
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APPENDIX I

COMPUTER PROGRAM MODULES FOR IMPLEMENTATION OF PRECEDENCE AND CONNECTION MATRIX TECHNIQUES

A. INTRODUCTION

Six computer programs were written to implement precedence and connection matrix techniques. They were: MAIN PROGRAM, READ, WRITE, START, CHEKIN, and PREC. MAIN PROGRAM controls the flow of the other five programs. The READ program reads the input data. The WRITE program writes diagnostics and comments. START checks the consistency of the precedence matrix. CHEKIN checks flow diagram precedences. PREC has, as entry points, PINMAT and POUTMT which check hardware precedences. CHEKIN is actually a third entry point of PREC.

Communication between programs is accomplished by use of the FORTRAN COMMON feature. By means of a COMMON statement, variables are placed in a given order at the high order locations in core storage. If all programs have the same COMMON statements, then variables placed in COMMON will have the same location for all programs and can be passed on from one program to the next. The COMMON variables, their meanings, and the present size of variable arrays are the following:

ACON is a 75 x 1 array which contains all of the valid bit configurations for connections from the prime equipment to the automatic checkout equipment.

BCNT is the number of lines of output which have been stored in the write buffer of the VATE simulator.

BCON is a 75 x 1 array which contains all of the valid bit configurations for connections from the automatic checkout equipment to the prime equipment.

COLUMN is temporary storage used in START and PREC.

CONMAT is the 25 x 25 connection matrix.

DATAD is the value in the VATE simulator of the constant following a TP instruction.

ENDYET is a flag to signal that a precedence matrix step has started (1) or ended (0).

FDORTP is an input value which signals that flow diagram precedences (1) or hardware precedences (2) are being processed.

KFIRST is a 25 x 1 array which contains the links between the start of precedence matrix steps and the execution of automatic checkout program instructions.

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KSEC is a 25 x 1 array which contains the links between the end of precedence matrix steps and the execution of automatic checkout program instructions.

KTEMER is a variable whose value signals the diagnostic or comment to be written by WRITE.

KWUNS is a 25 x 1 array whose values indicate that a row in the precedence matrix and its corresponding column do (0) or do not (1) contain all zeros.

KXNUM is an input value which is the number of rows in the precedence matrix. It is synonymous with NN.

KXNUMA = KXNUM + 1.

KXSQ = (KXNUM) x (KXNUM).

LUPZER is a variable which contains the number of the column in the precedence matrix in which a -1 was zeroed out. If the row corresponding to that column is executed, then a legitimate loop has been entered.

MATRIX is the 25 x 25 precedence matrix.

NEWMAT is the 25 x 25 precedence matrix whose elements are never altered. It is used to restore MATRIX.

NN is an input value which is the number of rows in the precedence matrix. It is synonymous with KXNUMA.

NPLUS1 = NN + 1.

NSQ = (NN) x (NN).

N2MINN = NSQ - NN.

N2MIN1 = NSQ - 1.

N2MNP1 = NSQ - NN + 1.

SECEX is the sector referenced by the instruction being executed by the VATE simulator.

SGNC is the channel of the instruction being executed by the VATE simulator.

SGNL is the sector of the instruction being executed by the VATE simulator.

SGXC is the channel referenced by the instruction being executed by the VATE simulator.

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The computer programs MAIN PROGRAM, READ, WRITE, START, CHEKIN, and PREC are documented in detail on the following pages.

B. MAIN PROGRAM

1. Purpose

MAIN PROGRAM provides executive control over the flow of information through subroutines READ, WRITE, VATE, START, CHEKIN, and PREC.

2. Input Formats

No input data is required for MAIN PROGRAM.

3. Output Formats

There is no output data from MAIN PROGRAM.

4. Method

MAIN PROGRAM calls START, VATE, and then calls EXIT to terminate the run.

5. Error Checks and Diagnostic Printouts

MAIN PROGRAM contains no error checks or diagnostic printouts. They are part of subroutines READ, WRITE, VATE, START, CHEKIN, and PREC.

6. Listings

The following is a listing of MAIN PROGRAM:

```
*      LIST8
*      LABEL
*      FORTRAN
CMAIN PROGRAM
      CALL START
      CALL VATE
      CALL EXIT
      END
```

C. SUBROUTINE READ

1. Purpose

Subroutine READ reads all of the input data, except for the operational automatic checkout program, and writes out the input data.

2. Input Formats

A sample listing of input data is given on the following page. The precise format of the input data, which is on punched cards, is the following:

a. The first input card contains, in columns 1-5, the dimension of the precedence matrix, that is, the number of rows in the precedence matrix. The number must end in column 5.

b. The next set of input cards contains the KFIRST link matrix which is the link between the start of each precedence matrix step and the execution of the object program. There are as many entries as steps in the precedence matrix. Each entry is twelve octal digits and ends in a column which is a multiple of 20. Thus, the four entries on a card would be punched in columns 9-20, 29-40, 49-60, and 69-80. If there were 10 KFIRST entries, 3 cards would be required. For hardware precedences, each entry would have four leading zeros followed by the eight octal digits of the constant following the TPK instruction. For flow diagram precedences, each entry would have 6 leading zeros followed by the six octal digits which are the channel and sector in which the instruction which begins a precedence matrix step is executed.

c. The next set of input cards contains the KSEC matrix which is the link between the end of each precedence matrix step and the execution of the object program. The format is exactly the same as for the KFIRST matrix.

d. The next set of input cards contains MATRIX which is the precedence matrix. The matrix is entered by columns from left to right, and each entry occupies two columns, one for sign, and the other for magnitude. For positive numbers, the sign column may be left blank. All 80 columns are used unless there are less than 80 entries. For example, a 6 x 6 matrix would use only 72 columns; a 7 x 7 matrix would use all 80 columns of the first card and 18 columns of the second card.

e. The next set of input cards contains CONMAT, the connection matrix. The format is exactly the same as for the precedence matrix. The dimension of CONMAT is taken to be the same as for MATRIX. This will not always hold true. The program should probably be modified to allow entry of the dimension of CONMAT separately.

f. The next set of input cards contains the ACON matrix, which is the listing of all bit configurations which represent legitimate connections which would carry inputs from the hardware. The format and dimension is

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exactly the same as for the KFIRST matrix, except that the leading eight octal digits represent the connection bit configuration, the ninth and tenth digits are the column referenced in the connection matrix, and the eleventh and twelfth are the row.

g. The next set of input cards contains the BCON matrix, which is the listing of all bit configurations which represent legitimate connections which would carry outputs to the hardware. The format is exactly the same as for the ACON matrix. CONMAT, ACON, and BCON must be included even for flow diagram precedences, in which case the appropriate number of blank cards may be used.

h. The last input card contains a 1 or a 2 in column 5 and is the value of FDORTP. A 1 means that the input is for flow diagram precedences; a 2 is for hardware precedences.

3. Output Formats

Each input card is reproduced in the output exactly as it is read, except that FDORTP is written out in column 3.

4. Method

READ is called by, and returns to, subroutine START. The detailed program steps are the following:

1. The first input card is read, stored in KXNUM, and written out.
2. KXSQ is set equal to $(KXNUM) \times (KXNUM)$.
3. KFIRST, KSEC, MATRIX, CONMAT, ACON, BCON, and FDORTP are each read, stored, and then written.
4. NN is set equal to KXNUM.
5. NSQ is set equal to KXSQ.
6. Return is made to the calling routine.

5. Error Checks and Diagnostic Printouts

READ contains no error checks or diagnostic printouts.

6. Limitations and Restrictions

CONMAT, ACON, and BCON must be entered even for flow diagram precedences, in which case the appropriate number of blank cards will be used. For $KXNUM = 7$, for example, 6 blank cards would be used.

7. Listings

A listing of READ is given on the following page.

LISTING OF SUBROUTINE READ

```
* LIST8
* LABEL
* FCRTAN
CREAD
SUBROUTINE READ
DIMENSION MATRIX(625),KFIRST(25),KSEC(25),KWUNS(25),
1 NEWMAT(625),ACCN(75),BCON(75),CONMAT(625)
COMMON DATA,MATRIX,NEWMAT,KFIRST,KSEC,KWUNS,KTEMR,KXNUM,KXNUMA,
1 NN,LUPZER,COLUMN,ENDYET,NSQ,N2MINN,N2MNP1,NPLUS1,N2MIN1,
2 CCNMAT,ACCN,BCCN,KXSQ,SGNC,SGNL,SGXC,SECEX,BCNT,FDORTP
READ INPUT TAPE 5,10,KXNUM
WRITE OUTPUT TAPE 6,10,KXNUM
KXSC=KXNUM*KXNUM
READ INPUT TAPE 5,20,(KFIRST(J+1),J=1,KXNUM)
WRITE OUTPUT TAPE 6,20,(KFIRST(J+1),J=1,KXNUM)
READ INPUT TAPE 5,20,(KSEC(J+1),J=1,KXNUM)
WRITE OUTPUT TAPE 6,20,(KSEC(J+1),J=1,KXNUM)
READ INPUT TAPE 5,30,(MATRIX(J+1),J=1,KXSQ)
WRITE OUTPUT TAPE 6,30,(MATRIX(J+1),J=1,KXSQ)
READ INPUT TAPE 5,30,(CCNMAT(J+1),J=1,KXSQ)
WRITE OUTPUT TAPE 6,30,(CONMAT(J+1),J=1,KXSQ)
READ INPUT TAPE 5,20,(ACCN(J+1),J=1,KXNUM)
WRITE OUTPUT TAPE 6,20,(ACCN(J+1),J=1,KXNUM)
READ INPUT TAPE 5,20,(BCON(J+1),J=1,KXNUM)
WRITE OUTPUT TAPE 6,20,(BCON(J+1),J=1,KXNUM)
READ INPUT TAPE 5,40,FCORTP
WRITE OUTPUT TAPE 6,50,FDORTP
40 FCRMAT(15)
50 FCRMAT(1X12)
10 FCRMAT(15)
20 FCRMAT(4(8XC12))
30 FCRMAT(4012)
NN=KXNUM
NSC=KXSC
RETURN
END
```

D. SUBROUTINE WRITE

1. Purpose

Subroutine WRITE writes out the comments and diagnostics which are generated by subroutines START, CHEKIN, and PREC.

2. Input Formats

Input to WRITE is through locations in COMMON. The locations required are KTEMER, MATRIX, KXSQ, KWUNS, NN, SGNC, SGNL, SGXC, SECEX.

3. Output Formats

The following outputs may be written by WRITE:

- a. "CONSISTENT MATRIX," if START has verified the consistency of a precedence matrix.
- b. "INCONSISTENT MATRIX," if START has discovered an inconsistency in a precedence matrix. The matrices MATRIX and KWUNS will also be written.
- c. "ERROR NUMBER ," if an error has occurred in CHEKIN or PREC. The error numbers indicate the following types of errors:
ERROR NUMBER 2 - Present step started before previous step ended (CHEKIN or PREC).
ERROR NUMBER 3 - Number other than -1, 0, 1, or 2 in precedence matrix (CHEKIN or PREC).
ERROR NUMBER 4 - Precedences not satisfied (CHEKIN or PREC).
ERROR NUMBER 5 - Connection not in ACON matrix (PREC).
ERROR NUMBER 6 - Connection not in BCON (PREC).
ERROR NUMBER 11 - Connection not valid (PREC).
- d. "PRECEDENCE OK FOR START OF STEP," if CHEKIN or PREC has verified that the start of a precedence matrix step satisfies precedences.
- e. "PRECEDENCE OK FOR END OF STEP," if CHEKIN or PREC has verified that the end of a step satisfies precedences.
- f. "SGNC.SGNL, SGXC.SECEX," each time CHEKIN or PREC is entered.

g. "CONNECTIONS OK," if PREC has verified that a requested connection is valid.

h. "PRECEDENCE OK FOR ENTRY INTO LEGITIMATE LOOP," if CHEKIN or PREC processes an instruction which is an entry point into a legitimate loop.

4. Method

Write is called by subroutines START, CHEKIN, AND PREC. The details of the method are the following:

a. KTEMER has values from zero to twelve. For use as an index, KTEMER is incremented by 1, and KTEM is set equal to this value. A "GO TO" statement is now executed with KTEM as the index.

b. For KTEMER=0 (KTEM=1), the comment "CONSISTENT MATRIX" is written and return is made to the calling routine.

c. For KTEMER=1 (KTEM=2), the comment "INCONSISTENT MATRIX" is written, and the matrices MATRIX and KWUNS are written. MATRIX contains the values of the precedence matrix at the time that the inconsistency in the matrix is diagnosed. The non-zero, non-negative elements are an aid to diagnosing the inconsistency. An additional diagnostic aid is the KWUNS matrix which contains 1's for rows or columns not zeroed out and zeros otherwise. Return is then made to the calling routine.

d. For KTEMER=2, 3, 4, 5, and 6 (KTEM=3, 4, 5, 6 and 7), a set of instructions in the VATE simulator whose entry point is OUTPDM is called. This causes the VATE output storage region to be written out and to be reinitialized. This is necessary because VATE stores 5 lines (110 words) of data and then writes out the 5 lines in blocked output. If this information is not written out before DUMP is called, it will be lost. The diagnostic "ERROR NUMBER" is then written with the value of KTEMER, and exit is made to the FORTRAN DUMP routine.

e. For KTEMER=7 (KTEM=8), OUTPDM is called to empty the VATE buffer. This is done so that the comment which is about to be written will immediately precede the line of data to which it refers. The comment "PRECEDENCE OK FOR START OF STEP" is then written and return is made to the calling routine.

f. For KTEMER=8 (KTEM=9), the same sequence as in step e is performed, except that the comment "PRECEDENCE OK FOR END OF STEP," is written.

g. For KTEMER=9 (KTEM=10), OUTPDM is called, the values of SGNC, SGNL, SGXC, and SECEX are written, and return is made to the calling routine.

h. For KTEMER=10 (KTEM=11), the comment "CONNECTIONS OK" is written and return is made to the calling routine.

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i. For KTEMER=11 (KTEM=12), the same sequence as in step d is performed.

j. For KTEMER=12 (KTEM=13), the comment "PRECEDENCE OK FOR ENTRY INTO LEGITIMATE LOOP" is written and return is made to the calling routine.

5. Error Checks and Diagnostic Printouts

There are no error checks. The diagnostic printouts are listed in "Output Formats."

6. Limitations and Restrictions

There are presently thirteen diagnostics. To add a diagnostic for new values of KTEMER, it is necessary only to add statement numbers to the "GO TO" statement and coding at those statement numbers which print comments or diagnostics.

7. Listings

A listing of WRITE is given on the following page.

LISTING OF SUBROUTINE WRITE

```
* LISTB
* LABEL
* FCRTAN
SUBROUTINE WRITE
DIMENSION MATRIX(625),KFIRST(25),KSEC(25),KWLNS(25),
1 NEWMAT(625),ACCN(75),BCON(75),CONMAT(625)
COMMON DATA,MATRIX,NEWMAT,KFIRST,KSEC,KWLNS,KTEMER,KXNUM,KXNUMA,
1 NN,LUPZER,COLUMN,ENDYET,NSQ,N2MINN,N2MNP1,NPLUS1,N2MIN1,
2 CONMAT,ACCN,HCCN,KXSQ,SGNC,SGNL,SGXC,SECEX,BCNT,FDORTP
KTEM=KTEMER+1
GC TC (100,200,300,300,300,300,300,400,500,600,700,300,750),KTEM
100 WRITE OUTPUT TAPE 6,110
110 FCRMAT(19F CONSISTENT MATRIX )
GC TC 900
200 WRITE OUTPUT TAPE 6,210
210 FCRMAT(21F INCONSISTENT MATRIX )
WRITE OUTPUT TAPE 6,220,(MATRIX(J+1),J=1,KXSQ)
220 FCRMAT(40I2)
WRITE OUTPUT TAPE 6,230,(KWLNS(J+1),J=1,NN)
230 FCRMAT(20(2X,I2))
GC TC 900
300 CALL CUTPCM
WRITE OUTPUT TAPE 6,310,KTEMER
310 FCRMAT(14F ERROR NUMBER I3)
GC TC 800
400 CALL CUTPCM
WRITE OUTPUT TAPE 6,410
410 FCRMAT(33F PRECEDENCE OK FOR START OF STEP )
GC TC 900
500 CALL CUTPCM
WRITE OUTPUT TAPE 6,510
510 FCRMAT(31F PRECEDENCE OK FOR END OF STEP )
GC TC 900
600 CALL CUTPCM
WRITE OUTPUT TAPE 6,610,SGNC,SGNL,SGXC,SECEX
610 FCRMAT(1X,C3,1F.,C3,10X,03,1H.,03)
GC TC 900
700 WRITE OUTPUT TAPE 6,710
710 FCRMAT(16F CONNECTIONS OK )
GC TC 900
750 WRITE OUTPUT TAPE 6,760
760 FCRMAT(46F PRECEDENCE CK FOR ENTRY INTO LEGITIMATE LOOP )
GC TC 900
800 CALL CLMP
900 CONTINUE
RETURN
END
```

E. SUBROUTINE START

1. Purpose

Subroutine START performs the following functions:

- a. START calls READ to read all of the input data except the operational automatic checkout program.
- b. START computes a number of values required for subsequent subroutines.
- c. START determines whether connections called for in the BCON matrix are valid and marks the entries which are not.
- d. START tests the consistency of the precedence matrix and writes a comment if it is consistent or a diagnostic if it is not.

2. Input Formats

Input to START is through locations in COMMON. The locations in COMMON required are MATRIX, KFIRST, KSEC, KXNUM, NN, NSQ, CONMAT, ACON, BCON, KXSQ.

3. Output Formats

Outputs from START are the following:

- a. Calls to subroutine WRITE to write "CONSISTENT MATRIX" and return, or "INCONSISTENT MATRIX" and exit.
- b. The computation of the values of various COMMON variables required for subroutines CHEKIN and PREC. The COMMON variables which are computed are NEWMAT, KXNUMA, N2MINN, N2MNP1, NPLUS1, N2MIN1.

4. Method

The precedence matrix is tested for consistency by eliminating from the precedence matrix all zero rows and their corresponding columns, and all zero columns and their corresponding rows. If all rows are eliminated, the matrix is consistent. If all rows cannot be eliminated, then the matrix is inconsistent. The details of the program are as follows:

- a. The index registers are stored and READ is called to read the input data. KXNUMA, NSQ, N2MINN, N2MNP1, NPLUS1, and N2MIN1 are computed, and NN is placed in the decrement of instructions W3D, W13D, W15D, and W4D. REPEAT, LUPZER, ZERCOL, COLUMN, and ENDYET are initialized to zero.
- b. The BCON array contains the bit configurations that represent connections between the automatic checkout equipment and the prime

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equipment. Each entry in BCON has the bit configurations in octal digits 1-8, the column in the connection matrix referenced by that configuration in digits 9-10, and the row in digits 11-12. An entry of BCON is picked up, digits 9-10 are stored in COLTEM, and digits 11-12 are stored in ROWTEM.

c. The index of the location in the connection matrix = $(\text{COLTEM} - 1) \times (\text{NN}) + \text{ROWTEM}$. Thus, if COLTEM=4, ROWTEM=3, and NN=5, then index = $3(5) + 3 = 18$; the location would be the 18th entry in CONMAT. For the BCON entry, the entry in CONMAT is picked up.

d. If the CONMAT entry is zero, there is no connection. The sign of the BCON entry is set negative and stored back into BCON. If the CONMAT entry is non-zero, the sign is not changed.

e. If all BCON entries have not been processed, return is made to step b.

f. If all entries have been processed, the entries in MATRIX are stored permanently in NEWMAT, and all of the entries in KWUN are set to 1. There is an entry for each row of the precedence matrix. When that entry is zero, then the row and its corresponding column contain no positive entries. When the KWUNS entry is a 1, then the row and column each contain at least one positive entry.

g. NN is stored in index registers 4 and 2, and 1 in index register 1.

h. A KWUNS entry is picked up.

i. If the KWUNS entry is a zero, transfer is made to step n. If it is non-zero, a MATRIX column entry is picked up.

j. If the MATRIX column entry is positive, transfer is made to step n. If it is zero or negative, index register 4 is decremented by 1.

k. If not all of the entries in the column have been tested, another column entry is picked up and transfer is made to step j.

l. If all column entries have been tested, a zero is stored in REPEAT to signal that at least one zero column has been found, and a zero is stored in the KWUNS entry for this column. ZERCOL, which contains the number of zero columns, is incremented by 1 and tested to determine if it equals NN.

m. If ZERCOL=NN, then all of the rows and columns of the matrix have been eliminated, and the matrix is consistent. Transfer is made to step x. If ZERCOL \neq NN, then the row that corresponds to the present zero column is zeroed out.

n. Index register 1 is incremented by 1 to pick up the next column. The value in index register 1 is multiplied by NN and placed in index register 2 to pick up the last entry in the column. The entries are picked up in reverse order.

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o. If index register 1 is not greater than NN, then all the columns have not been processed, and transfer is made to step h. If all the columns have been processed, REPEAT is incremented by 1 and tested for the value 3.

p. If REPEAT=3, then there are no more zero rows or columns and the matrix is inconsistent. Transfer is made to step w. If REPEAT is less than 3, then the rows are to be tested for zero rows.

q. NSQ-NN+1 is placed in XR4 to pick up the last row of the precedence matrix. The rows are picked up in reverse order. NN is placed in index register 2, and 1 is placed in index register 1.

r. A KWUNS entry is picked up. If it is zero, transfer is made to step v. If it is not zero, transfer is made to step s.

s. A MATRIX entry is picked up. If it is non-zero, a transfer is made to step v. If it is zero, NN is subtracted from index register 4 to pick up the next row entry.

t. If all the entries in a row have not been processed, transfer is made to step s. If all have been processed, REPEAT and the KWUNS entry for this row are set to zero, and ZERCOL is incremented by 1.

u. If ZERCOL=NN, the matrix is consistent, and transfer is made to step x. If not, the column that corresponds to the zero row is zeroed out.

v. Index register 1 is incremented by 1 to pick up the next row. The value of (index register 1)+NSQ-NN is placed in index register 4 to pick up the last entry of the next row, and index register 2 is set to NN. If all rows have not been tested, transfer is made to step r. If all rows have been tested, REPEAT is incremented by 1 and tested for the value 3. If REPEAT=3, the matrix is inconsistent, and transfer is made to step w. If REPEAT \neq 3, transfer is made to step g.

w. KTEMER is set to 1, and WRITE is called to write a diagnostic (INCONSISTENT MATRIX). Transfer is made to step y.

x. KTEMER is set to zero, and WRITE is called to write a comment (CONSISTENT MATRIX).

y. MATRIX is restored from NEWMAT, the index registers are restored, and return is made to the calling routine.

5. Error Checks and Diagnostic Printouts

Two basic error checks are made. First, the BCON entries are checked for invalid connections. If any are found, the BCON entry is made negative. Second, the consistency of the precedence matrix is tested. If it is consistent, a comment to that effect is written by setting KTEMER=0 and calling WRITE. If it is inconsistent, a diagnostic is written by setting KTEMER=1 and calling WRITE.

6. Limitations and Restrictions

All of the matrices must have their elements stored backwards and starting at a location one less than the matrix name. This is the way that READ now stores the matrices. This simplifies the indexing of all of the instructions that process the matrices.

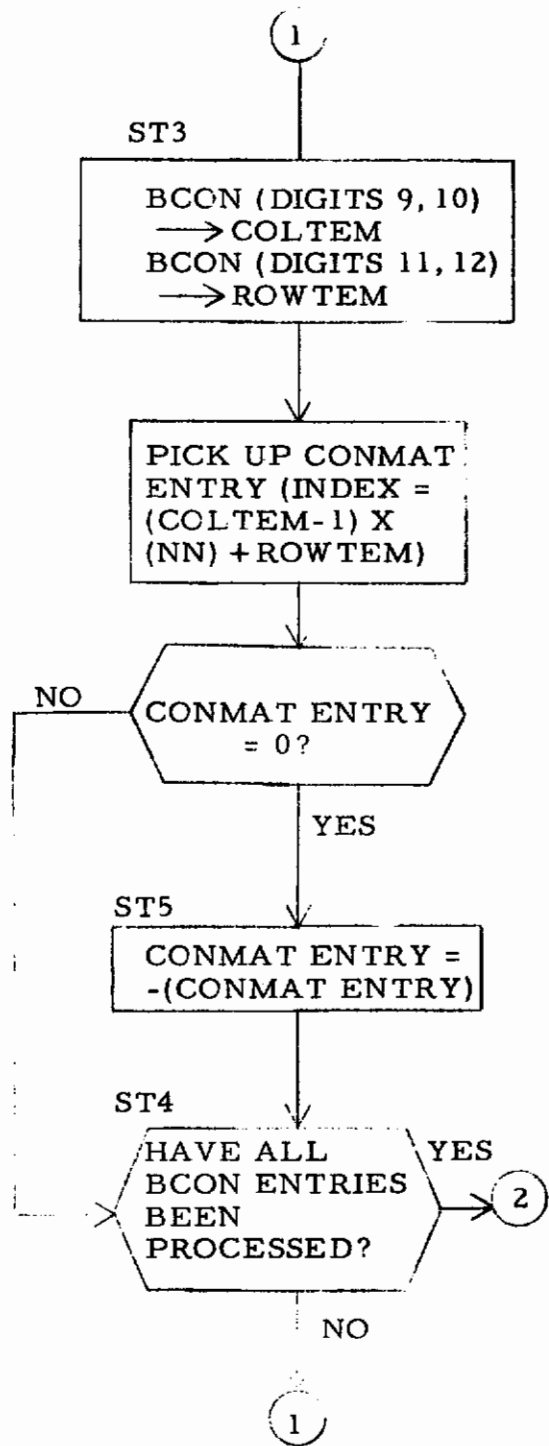
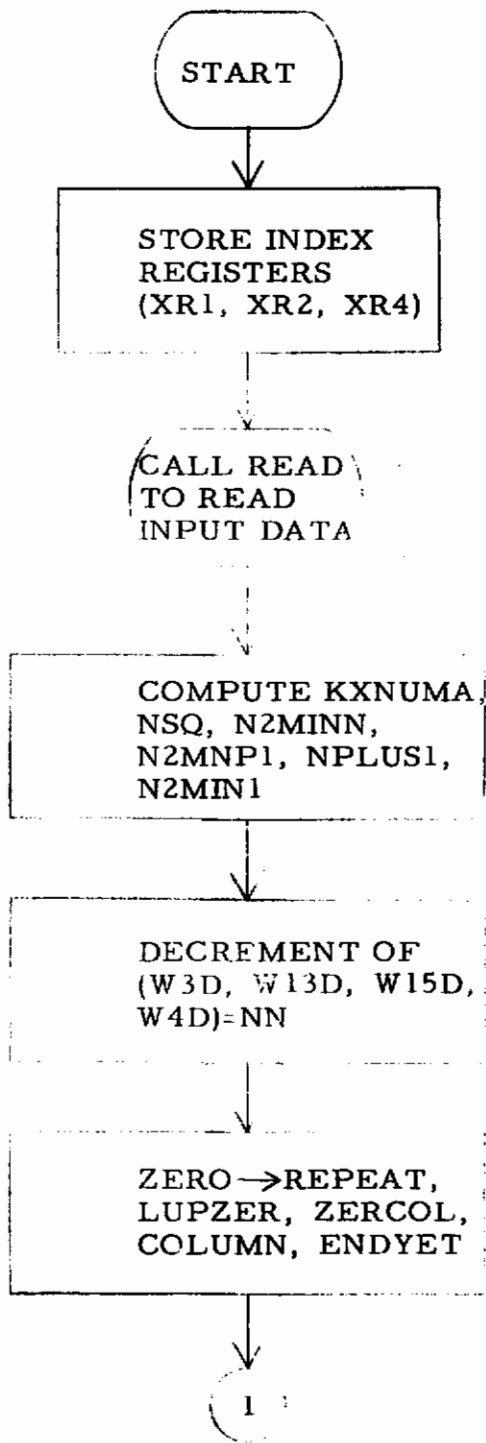
7. Flow Charts

Detailed flow charts are given on the following pages.

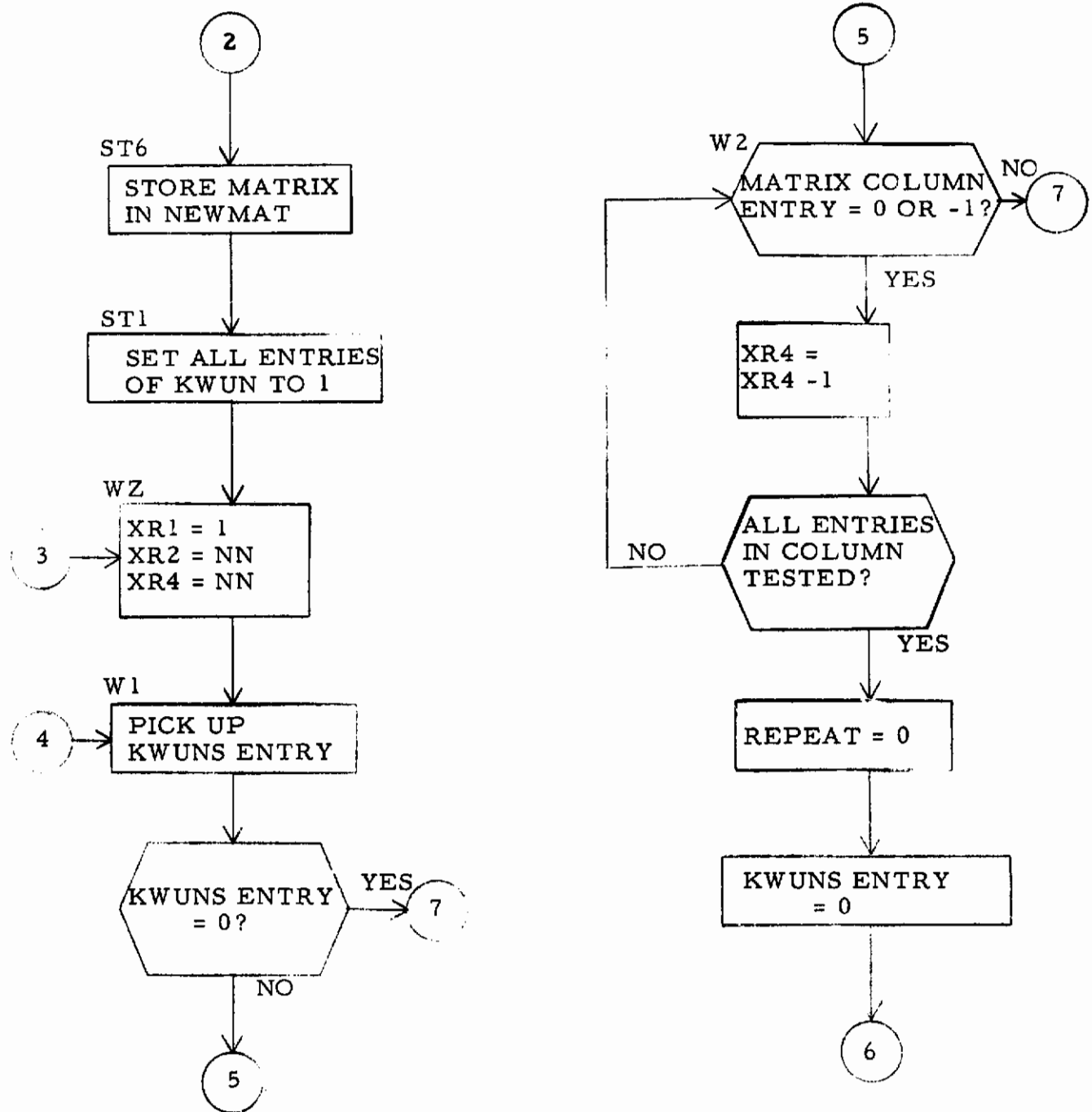
8. Listings

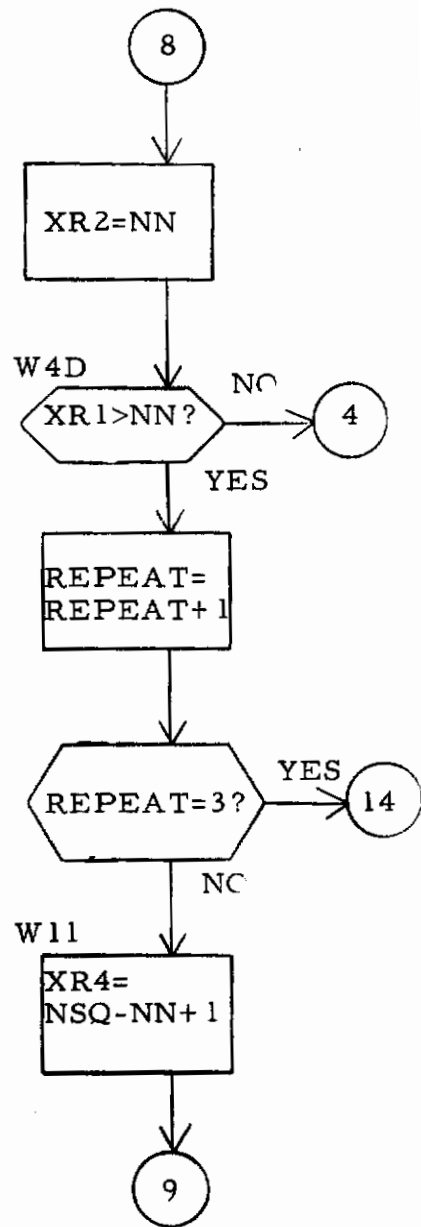
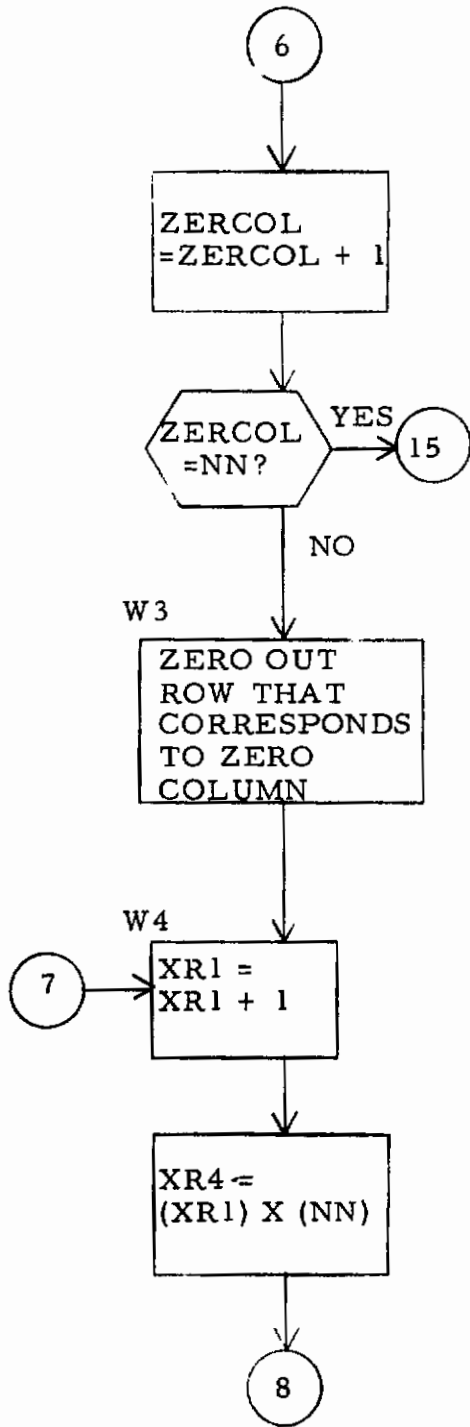
Listings of START are on the four pages following the flow charts.

FLOW CHARTS OF SUBROUTINE START

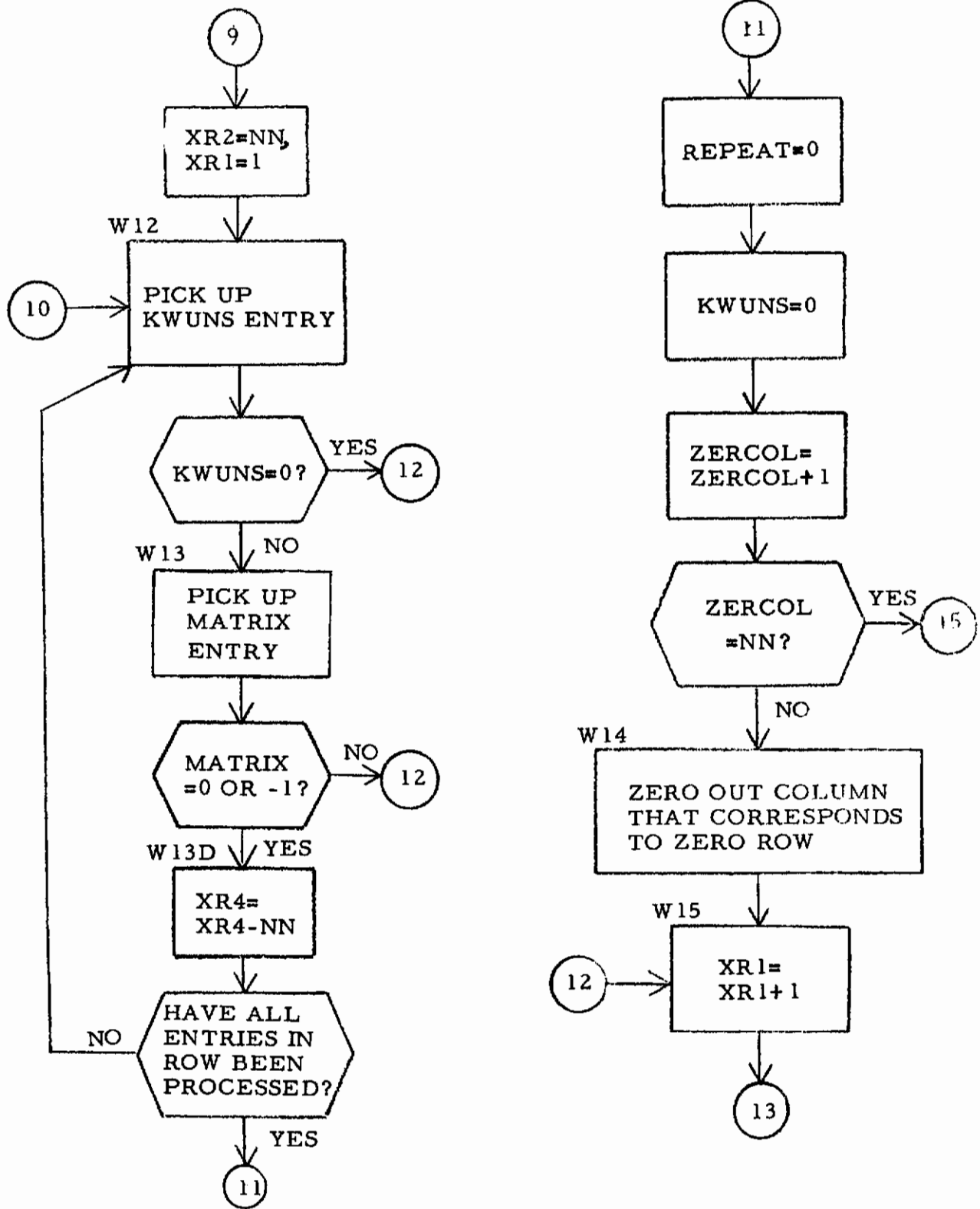


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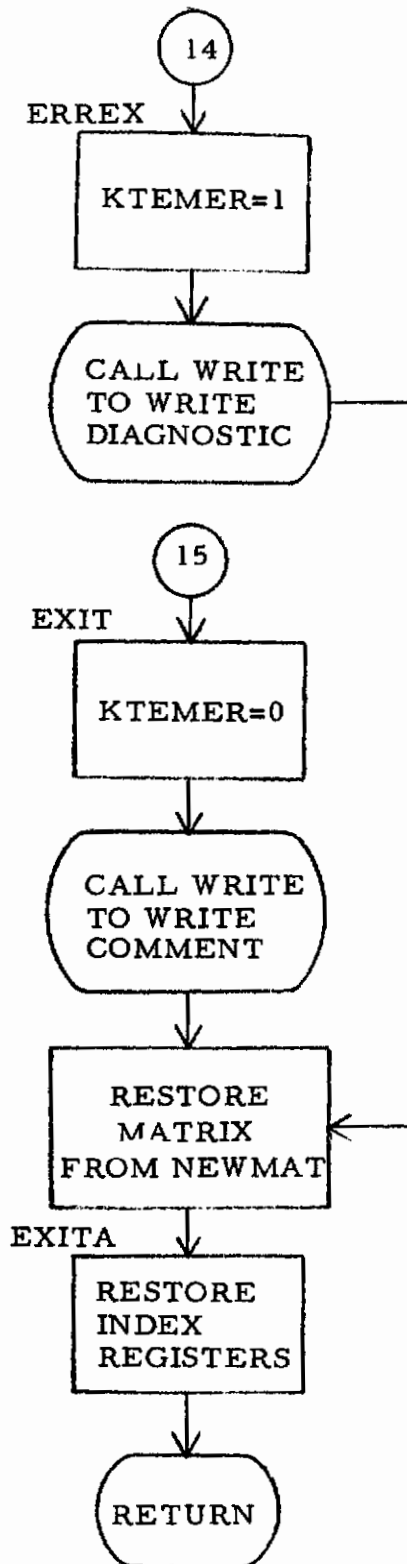
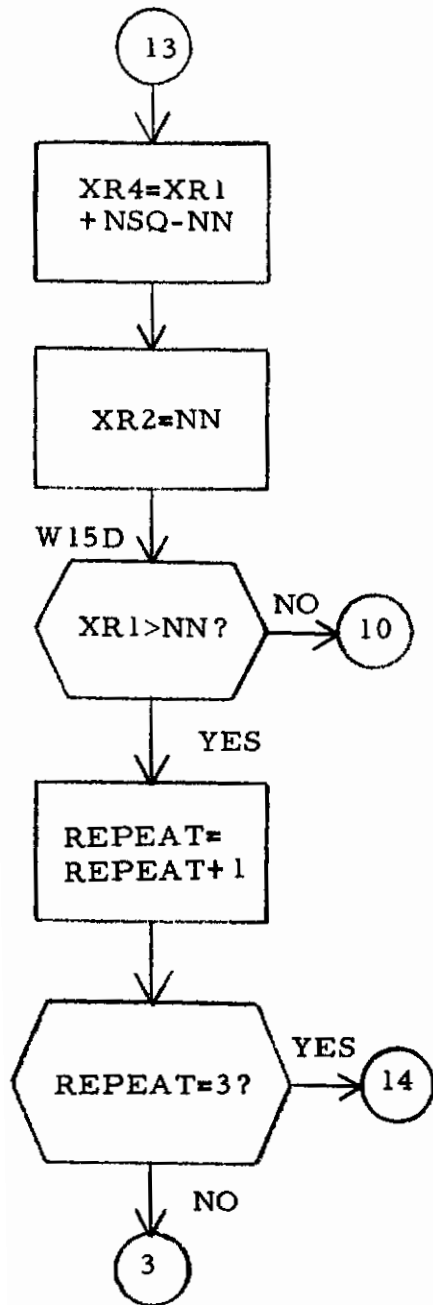




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LISTING OF SUBROUTINE START

```

* LABEL
* PACK
* FAP
COUNT 1000
*START READS PRECEDENCE MATRIX AND TESTS CONSISTENCY
ENTRY START READS PRECEDENCE MATRIX AND TESTS CONSISTENCY
DATAD COMMON 1
MATRIX COMMON 625
NEWMAT COMMON 625
KFIRST COMMON 25
KSEC COMMON 25
KWUNS COMMON 25
KTEMER COMMON 1
KXNUM COMMON 1
KXNUMA COMMON 1
NN COMMON 1
LUPZER COMMON 1
COLUMN COMMON 1
ENDYET COMMON 1
NSQ COMMON 1
N2MINN COMMON 1
N2MNP1 COMMON 1
NPLUS1 COMMON 1
N2MINI COMMON 1
CONMAT COMMON 625
ACON COMMON 75
BCON COMMON 75
KXSQ COMMON 1
SGNC COMMON 1
SGNL COMMON 1
SGXC COMMON 1
SECEX COMMON 1
BCNT COMMON 1
FDORTP COMMON 1
START SXD XR1+1 STORE INDEX REGISTERS
      SXD XR2+2
      SXD XR4+4
      CALL READ READ PRECEDENCE MATRIX AND START AND
*      END OF STEP ARRAYS
      CLA KXNUM FORM KXNUM+1
      ADD ONED STORE IN KXNUMA
      STO KXNUMA CLEAR ACCUMULATOR AND MQ REGISTERS
      MPY ZERO MAKE SURE SIGN OF ACCUMULATOR IS POSITIVE
      SSP NN FORM NN SQUARED
      LDQ NN
      MPY NN
      ALS 17 COMPENSATES FOR BOTH IN DECREMENT
      STO NSQ STORE IN NSQ
      SUB NN FORM NSQ-N
      STO N2MINN STORE IN N2MINN
      ADD ONED FORM NSQ-N+1
      STO N2MNP1 STORE IN N2MNP1
      CLA NN FORM NN+1
      ADD ONED
      STO NPLUS1 STORE IN NPLUS1
      ADD NN FORM 2NN-1
      SUB TWOD
      STO N2MINI STORE IN N2MINI
      CLA NN

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```

STD      W13D
STD      W15D
CLA      NN
STD      W4D
CLA      N2MNP1
STD      W15
STZ      REPEAT          INITIALIZE LOCATIONS
STZ      LUPZER
STZ      ZERCOL
STZ      COLUMN
STZ      ENDYET
LXD      NN,4            PUT NN INTO XR4
ST3      CLA      BCON,4    PICK UP ENTRY IN BCON
LDQ      MASK77         PUT 77 IN ROWTEM AND COLTEM
STQ      ROWTEM         TO PICK UP LOW ORDER 2 CHARACTERS
STQ      COLTEM         STORE LOW ORDER 2 DIGITS * COLUMN
ANS      ROWTEM         PICK UP LOW ORDER 2 CHARACTERS=ROW
ARS      6              IN CONNECTION MATRIX. SHIFT RIGHT 6
SUB      =1             PICK UP COLUMN -1 TO COMPUTE CONNECTION
ANS      COLTEM         MATRIX ENTRY. STORE IN COLTEM.
ARS      6              DROP COLUMN NUMBER FROM BCON ENTRY
ALS      12            RESTORE REST OF ENTRY
STO      BCON,4         STORE 23 BITS BACK INTO BCON
PXD      0,0           ZERO OUT ACCUMULATOR
LDQ      NN            PUT NN INTO Q
LRS      18            SHIFT DECREMENT INTO ADDRESS IN Q
MPY      COLTEM        FORM (COLUMN-1) NN
XCA      XCA           PUT Q INTO ACCUM.
ADD      ROWTEM        FORM NN (COLUMN-1) +ROW
PAX      ,2            PUT INDEX OF CONMAT INTO XR2
CLA      CONMAT,2      PICK UP CONNECTION MATRIX ENTRY
TZE      ST5           IF ZERO, NO CONNECTION=GO TO ST5
ST4      TIX      ST3,4,1 IF NOT ALL BCON PROCESSED, GO TO ST3
TRA      ST6           IF ALL BCON PROCESSED, GO TO ST6
ST5      CLA      BCON,4 SET BCON ENTRY TO MINUS FOR NO CONNECTION
SSM
STO      BCON,4         STORE BACK INTO BCON
TRA      ST4
ST6      LXD      NSQ,4
ST2      CLA      MATRIX,4 STORE MATRIX PERMANENTLY IN MEWMAT
STO      NEWMAT,4
TIX      ST2,4,1
LXD      NN,1          PUT NN IN IXR1
ST1      CLA      ONED   PUT 100000 IN ARRAY KWUNS(1=ROW NOT ALL ZEROS)
STO      KWUNS,1
TIX      ST1,1,1
WZ      LXD      NN,4            IXR4 CONTAINS ELEMENT NUMBER
LXD      NN,2 IXR2 CONTAINS NUMBER OF ELEMENTS(=NUMBER OF ROWS)
AXT      1,1           XR1=COLUMN NUMBER
W1      CLA      KWUNS,1    TEST IF COLUMN ALREADY ZEROED OUT
TZE      W4            IF SO, GO TO W4
W2      CLA      MATRIX,4   IF NOT, PICK UP COLUMN ENTRY
TZE      *+2           IF ZERO OR MINUS, CONTINUE TESTING
TPL      W4            IF PLUS, GO TO W4
TIX      *+1,4,1       SUBTRACT 1 FROM IXR4
TIX      W2,2,1 TEST ALL ENTRIES IN COLUMN TESTED IF NOT, GO TO W2
STZ      REPEAT        IF COLUMN ALL ZEROS, STORE ZERO IN REPEAT
STZ      KWUNS,1 ZERO OUT ENTRY IN KWUNS TO SHOW COLUMN ALL ZEROS
CLA      ZERCOL        ZERCOL IS COUNT OF NUMBER ZERO COLUMNS
ADD      ONED
STO      ZERCOL

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```

SUB      NN      TEST ALL COLUMNS ZERO
TZE     EXIT     IF 50, GO TO EXIT
SXD     XRTEM.1  IF NOT, STORE XR1 SO ROW CAN BE ZEROED OUT
PXD     .1       PUT XR1 IN ACCUM.
LXD     NN.1     PUT NN IN XR1
ADD     N2MINN   FORM COLUMN NUMBER+NSQ-N
PDX     .2       PLACE IN XR2
W3      STZ     MATRIX.2  ZERO OUT ROW
W3D     TIX     **1.2.**  DECREMENT XR2 BY NN
TIX     W3.1.1  TEST ENTIRE ROW ZEROED OUT IF NOT, GO TO W3
LXD     XRTEM.1  RELOAD XR1
W4      TXI     **1.1.1  INCREMENT COLUMN NUMBER BY 1
MPY     ZERO     CLEAR ACCUMULATOR AND MQ REGISTERS
SSP     .1       MAKE SURE SIGN OF ACCUMULATOR IS POSITIVE
PXD     .1       FORM (COLUMN NUMBER) X (NN)
XCA
MPY     NN
ALS     17      COMPENSATES FOR BOTH IN DECREMENT
PDX     .4      PLACE IN XR4
LXD     NN.2
W4D     TXL     W1.1.**  IF ALL COLUMNS NOT PROCESSED, GO TO W1
CLA     REPEAT  ALL COLUMNS PROCESSED, ADD 1 TO REPEAT
ADD     ONED
STO     REPEAT
SUB     THREE   IF REPEAT IS THREE, NO ROW AND NO COLUMN IS ALL ZEROES
TZE     ERREX   GO TO ERROR EXIT
TRA     W11     IF REPEAT IS NOT THREE, GO TO W11
W11     LXD     N2MNP1.4 W11 TESTS ROWS FOR ZEROES PUT NSQ-N+1 IN XR4 FOR ROW1
LXD     NN.2    PUT NN IN XR2
AXT     1.1     PUT 1 IN XR1
W12     CLA     KWUNS.1  IF ROW ALREADY ZERO, GO TO W15
TZE     W15
W13     CLA     MATRIX.4  IF NOT, TEST FOR ALL ZEROES
TZE     **2     IF ZERO OR MINUS, CONTINUE TESTING
TPL     W15     IF PLUS, GO TO W15
W13D    TIX     **1.4.**  SUBTRACT NN FROM XR4
TIX     W13.2.1  TEST WHOLE ROW PROCESSED, IF NOT, GO TO W13
STZ     REPEAT  IF ROW ALL ZEROES, ZERO OUT REPEAT TO CONTINUE TESTING
STZ     KWUNS.1  ZERO OUT ENTRY IN KWUNS
CLA     ZERCOL  INCREASE COUNT OF ZERO COLUMNS
ADD     ONED
STO     ZERCOL
SUB     NN      TEST ALL COLUMNS ZEROED OUT
TZE     EXIT     IF 50, GO TO EXIT
SXD     XRTEM.1  IF NOT, ZERO OUT COLUMN, STORE XR1
MPY     ZERO     CLEAR ACCUMULATOR AND MQ REGISTERS
SSP     .1       MAKE SURE SIGN OF ACCUMULATOR IS POSITIVE
PXD     .1       FORM (COLUMN NUMBER) X (NN)
XCA
MPY     NN
ALS     17      COMPENSATES FOR BOTH IN DECREMENT
PDX     .2      PUT IN XR2
LXD     NN.1    PUT NN IN XR1
W14     STZ     MATRIX.2  ZERO OUT ENTRY IN MATRIX
TIX     **1.2.1  SUBTRACT 1 FROM XR2
TIX     W14.1.1  TEST WHOLE COLUMN ZEROED OUT, IF NOT, GO TO W14
LXD     XRTEM.1  RELOAD XR1
W15     TXI     **1.1.1
PXD     .1
ADD     N2MINN   COMPUTE XR4 TO PICK UP NEXT ROW
PDX     .4

```

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```

LXD      NN:2
W1SD TXL  W12:1,**      IF ALL ROWS NOT TESTED, GO TO W12
CLA      REPEAT        ALL ROWS TESTED, ADD ONE TO REPEAT
ADD      ONED
STO      REPEAT
SUB      THREE IF REPEAT IS THREE, NO ROWS OR COLUMNS ARE ALL ZEROES
TZE      ERREX        GO TO ERROR EXIT
TRA      WZ           OTHERWISE, GO TO WZ
ERREX   CLA  ONED      ERROR EXIT
STO      KTEMER      STORE ONE IN KTEMER FOR INCONSISTENT MATRIX
CALL     WRITE      WRITE ERROR MESSAGE
TRA      EXITA
EXIT    STZ  KTEMER    STORE ZERO IN KTEMER FOR CONSISTENT MATRIX
CALL     WRITE      WRITE MESSAGE (CONSISTENT MATRIX)
EXITA   LXD  NSQ:4     RESTORE MATRIX
EX1     CLA  NEWMAT:4
STO      MATRIX:4
TIX      EX1:4:1
LXD      XR1:1       RESTORE INDEX REGISTERS
LXD      XR2:2
LXD      XR4:4
TRA      1,4        RETURN TO CALLING ROUTINE
ZERO    OCT  0
ONED    OCT  1000000
TWOD    OCT  2000000
THREED  OCT  3000000
XR1     PZE
XR2     PZE
XR4     PZE
ZERCOL  PZE
REPEAT  PZE
XRTEM   PZE
MASK77  OCT  000000000077
ROWTEM  PZE
COLTEM  PZE
END
```

F. SUBROUTINES CHEKIN AND PREC

1. Purpose

Subroutine CHEKIN checks the order of execution of steps in the automatic checkout program for conformance with flow diagram precedences. Subroutine PREC checks the order of execution for conformance with hardware precedences and the requested connections for validity.

2. Input Formats

a. CHEKIN is actually one of three entry points to PREC. The other two are PINMAT and POUTMT. A CALL CHEKIN statement is used for entry to CHEKIN to check flow diagram precedences. A CALL PINMAT is used for entry to PINMAT to check hardware precedences and connections for digital and analog inputs from the automatic checkout and prime equipment. A CALL POUTMT statement is used for entry to POUTMT to check hardware precedences and connections for digital and analog outputs to the automatic checkout and prime equipment.

b. Inputs to CHEKIN and PREC are through the values of locations in COMMON. The locations required are DATAD, MATRIX, NEWMAT, KXNUM, NN, LUPZER, ENDYET, NSQ, N2MINN, N2MNP1, NPLUS1, N2MIN1, CONMAT, ACON, BCON, KXSQ, SGNC, SGNL, SGXC, SECEX, and FDORTP.

3. Output Formats

There are two basic outputs from PREC, printed diagnostics or comments, and an updated precedence matrix. The diagnostics and comments are detailed in "Error Checks and Diagnostic Printouts." The precedence matrix is updated as follows. If a precedence matrix step is being initiated, ENDYET will be set to 1. If this step is an entry point to a legitimate loop, MATRIX is restored from NEWMAT, and LUPZER is set to zero. If a precedence matrix step is being terminated, ENDYET is set to zero, and the row corresponding to the step is zeroed out. If there is a -1 in the row, it is stored in LUPZER before it is zeroed out. If there are 2's in the row, then all of the 2's in the columns in which the 2's in the row appear are also zeroed out.

4. Method

a. For entry point CHEKIN, KPTEM is set to 3, and FDORTP is tested for the value 1. If $FDORTP \neq 1$, then the precedence matrix represents hardware precedences; transfer is made to the calling routine. If $FDORTP = 1$, SGNL is stored in the lower order 9 bits of the accumulator, SGNC is stored in the next 9 bits, and DATEM is set equal to this value. DATEM now contains the channel and sector of execution of the present instruction. This value will be used to determine if a precedence matrix step has been referenced. Transfer is made to step d.

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b. For entry point PINMAT, KPTEM is set to 1, and transfer is made to step c. For entry point POUTMT, KPTEM is set to 2, and transfer is made to step c.

c. FDORTP is tested for the value 2. If $FDORTP \neq 2$, only flow diagram precedences are being processed; transfer is made to the calling routine. If $FDORTP = 2$, DATEM is set equal to DATAD, and transfer is made to step d.

d. The index registers are stored, NN is stored in the decrement of C4, and KXNUM is stored in index register 4.

e. DATEM is matched against all the KFIRST entries. If there is a match, this instruction is the start of a precedence matrix step; transfer is made to step h. If there is no match, transfer is made to step f.

f. KXNUM is stored in index register 4, and DATEM is matched against the KSEC entries. If there is a match, this instruction is the end of a precedence matrix step. Transfer is made to step i. If there is no match, transfer is made to step g.

g. The index registers are restored, and return is made to the calling routine.

h. COLUMN is set equal to index register 4. This is the precedence matrix step being started. KTEMER=9 and WRITE is called to write "SGNC, SGNL, SGXC, SECEX." ENDYET is tested for zero. If $ENDYET \neq 0$, the last precedence matrix step has not been completed. KTEMER=2, and WRITE is called to write "ERROR NUMBER 2." If $ENDYET = 0$, transfer is made to step p.

i. COLUMN=index register 4. This is the precedence matrix step being ended. KTEMER=9, and WRITE is called to write "SGNC, SGNL, SGXC, SECEX." NN is stored in index register 4, and $COLUMN + NSQ - NN$ is stored in index register 2.

j. A row entry is picked up. If it is negative, transfer is made to step l; if it is zero, transfer is made to step k; if 1, transfer to step m; if 2, transfer to step n; if none of these values, KTEMER=3, and WRITE is called to write "ERROR NUMBER 3."

k. Index register 2 is decremented by NN. If all entries in the row have not been processed, transfer is made to step j. If all have been processed, KTEMER=8, and WRITE is called to write the comment, "CONSISTENT MATRIX." Transfer is then made to step t by means of a TSX statement. At the termination of the steps beginning at step t, transfer is made back, at which time transfer is made to step g.

l. LUPZER is set equal to column.

m. The matrix entry is zeroed out, and transfer is made to step k.

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n. Index register 1 is set equal to (index register 4) x (NN). Index register 4 is stored, and index register 4 is then set equal to NN.

o. The entries in the column in which a 2 was zeroed out in the precedence matrix row being processed are scanned for 2's. If 2's are found, they are set to zero. Index register 4 is then restored, and transfer is made to step n.

p. ENDYET is set to 1 to signal that a precedence matrix step has been started but not ended. LUPZER is then tested against COLUMN. If they are not equal, transfer is made to step q. If they are equal, entry is being made into a legitimate loop. MATRIX is restored from NEWMAT, LUPZER=0, KTEMER=12, and WRITE is called to write "PRECEDENCE OK FOR ENTRY INTO LEGITIMATE LOOP." Transfer is made to step q.

q. NN is stored in index register 4, and index register 4 is set to (COLUMN) x (NN). Each entry in the column corresponding to the precedence matrix step being started is tested. If any entry is positive, the precedences are being violated; transfer is made to step s. If all of the entries are non-positive, then the precedences are satisfied; KTEMER=7, and WRITE is called to write "PRECEDENCE OK FOR START OF STEP." Transfer is made to step t.

r. KXNUM is stored in index register 4, DATEM is placed in the accumulator, and transfer is made to step f.

s. KTEMER=4, and WRITE is called to write "ERROR NUMBER 4."

t. NN is stored in index register 1; index register 4 is stored. If KPTEM=2, transfer is made to step u. If KPTEM=3, transfer is made to step v. Otherwise, the ten connection bits of DATEM are tested against the ACON entries. If a match is found, TEMPB=index register 4, and transfer is made to step v. If no match is found, KTEMER=5, and WRITE is called to write "ERROR NUMBER 5."

u. TEMPB is set equal to the ten connection bits of DATEM. The magnitude of each BCON entry is matched against TEMPB. If no match is found with any BCON entry, KTEMER=6, and WRITE is called to write "ERROR NUMBER 6." If a match is found, the BCON entry is tested. If negative, KTEMER=11, and WRITE is called to write "ERROR NUMBER 11." If the BCON entry is positive, KTEMER=10, and WRITE is called to write "CONNECTION OK." Index register 4 is restored, and transfer is made to step v.

v. Return is made to the calling routine.

5. Error Checks and Diagnostic Printouts

Diagnostics or comments are written by setting KTEMER equal to the appropriate value and calling subroutine WRITE. The following are the values of KTEMER, the error checks which produced them, the diagnostics

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or comments written, and the action taken after the diagnostic or comment is written:

KTEMER=2. The present step was started before the previous step ended. "ERROR NUMBER 2" is written, and the program is terminated.

KTEMER=3. There was an entry other than -1, 0, 1, 2 in the precedence matrix. "ERROR NUMBER 3" is written, and the program is terminated.

KTEMER=4. The precedences are violated. "ERROR NUMBER 4" is written, and the program is terminated.

KTEMER=5. The connection called for is not in the ACON matrix. "ERROR NUMBER 5" is written, and the program is terminated.

KTEMER=6. The connection called for is not in the BCON matrix. "ERROR NUMBER 6" is written, and the program is terminated.

KTEMER=7. The precedences are satisfied for the start of a step. "PRECEDENCE OK FOR START OF STEP" is written and processing continues.

KTEMER=8. The precedences are satisfied for the end of a step. "PRECEDENCE OK FOR END OF STEP" is written and processing continues.

KTEMER=9. The start or end of a step is being processed. "SGNC. SGNL, SGXC. SECEX" is written and processing continues.

KTEMER=10. A requested connection is valid. "CONNECTIONS OK" is written and processing continues.

KTEMER=11. A requested connection is invalid. "ERROR NUMBER 11" is written, and the program is terminated.

KTEMER=12. Entry has been made into a legitimate loop. "PRECEDENCE OK FOR ENTRY INTO A LEGITIMATE LOOP" is written and processing continues.

6. Limitations and Restrictions

a. Only the last -1 found in a row being zeroed out is stored. This should be changed to allow storage of several -1's.

b. PINMAT was not used in this application. Later changes (most of which are in the processing of the connection matrix) were not included in PINMAT processing.

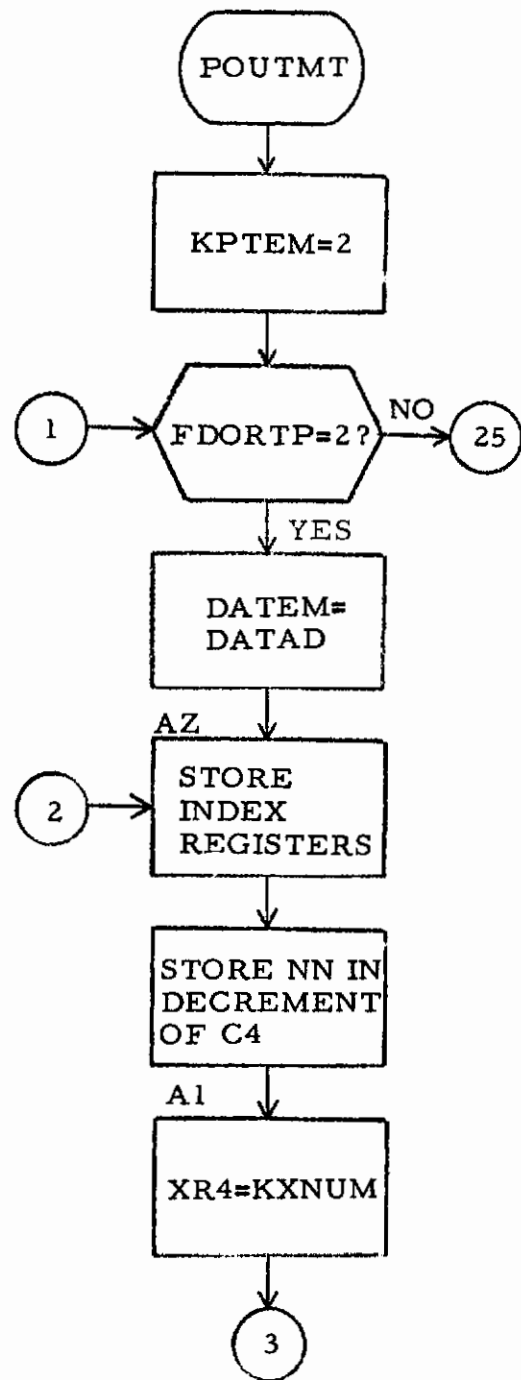
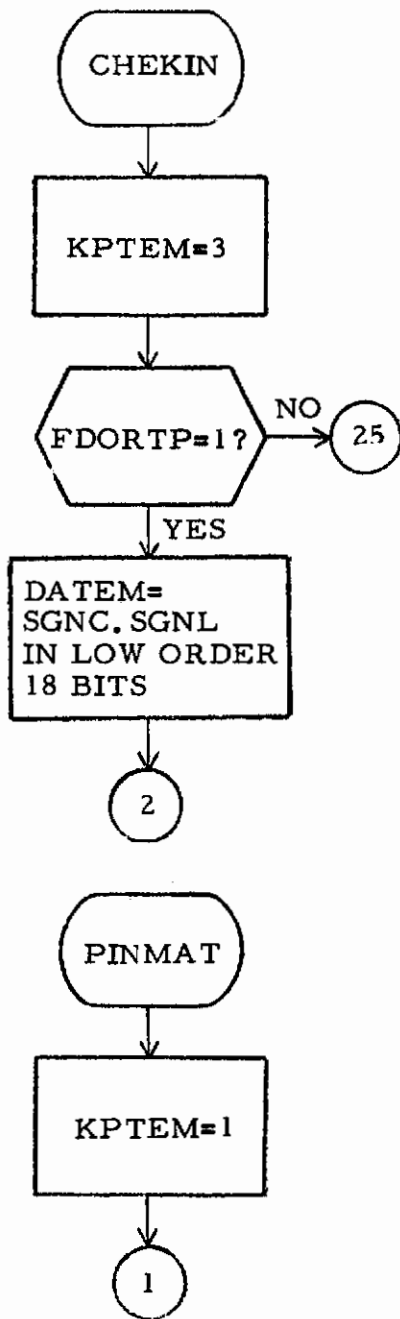
7. Flow Charts

The detailed flow charts of PREC are given on the following eight pages.

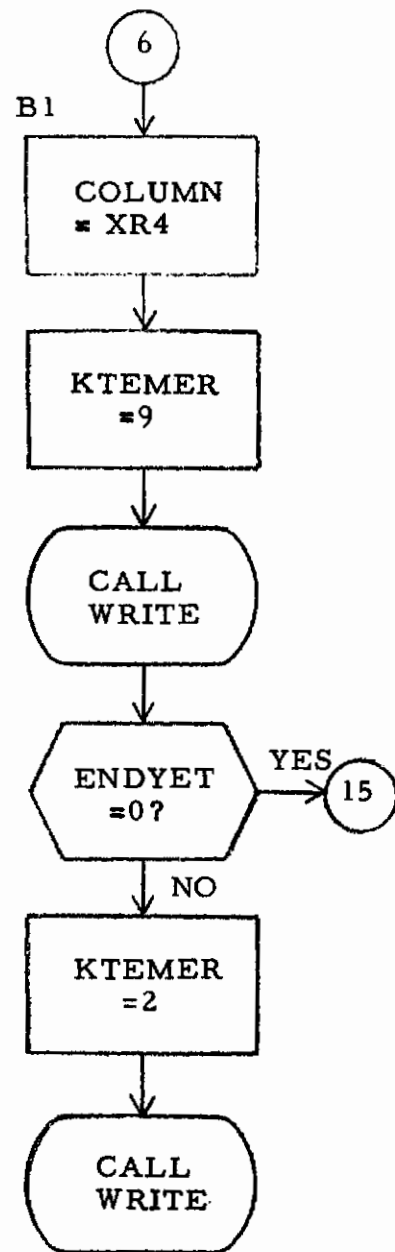
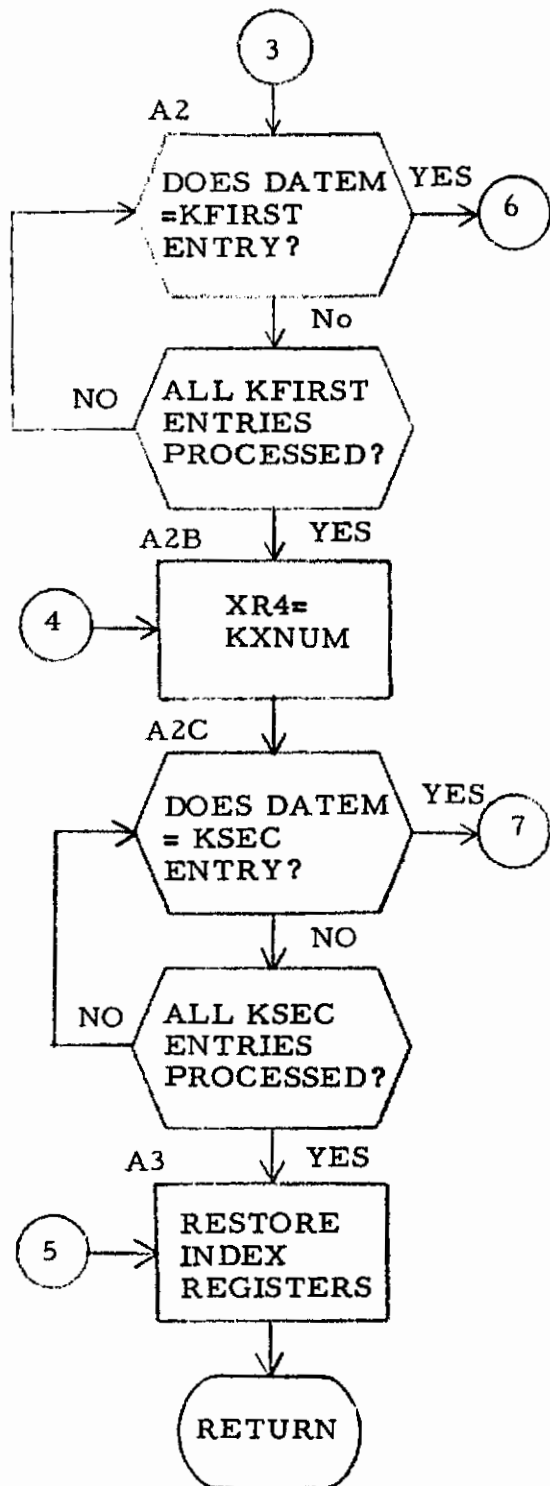
8. Listings

Listings of PREC are given on the pages following the flow charts.

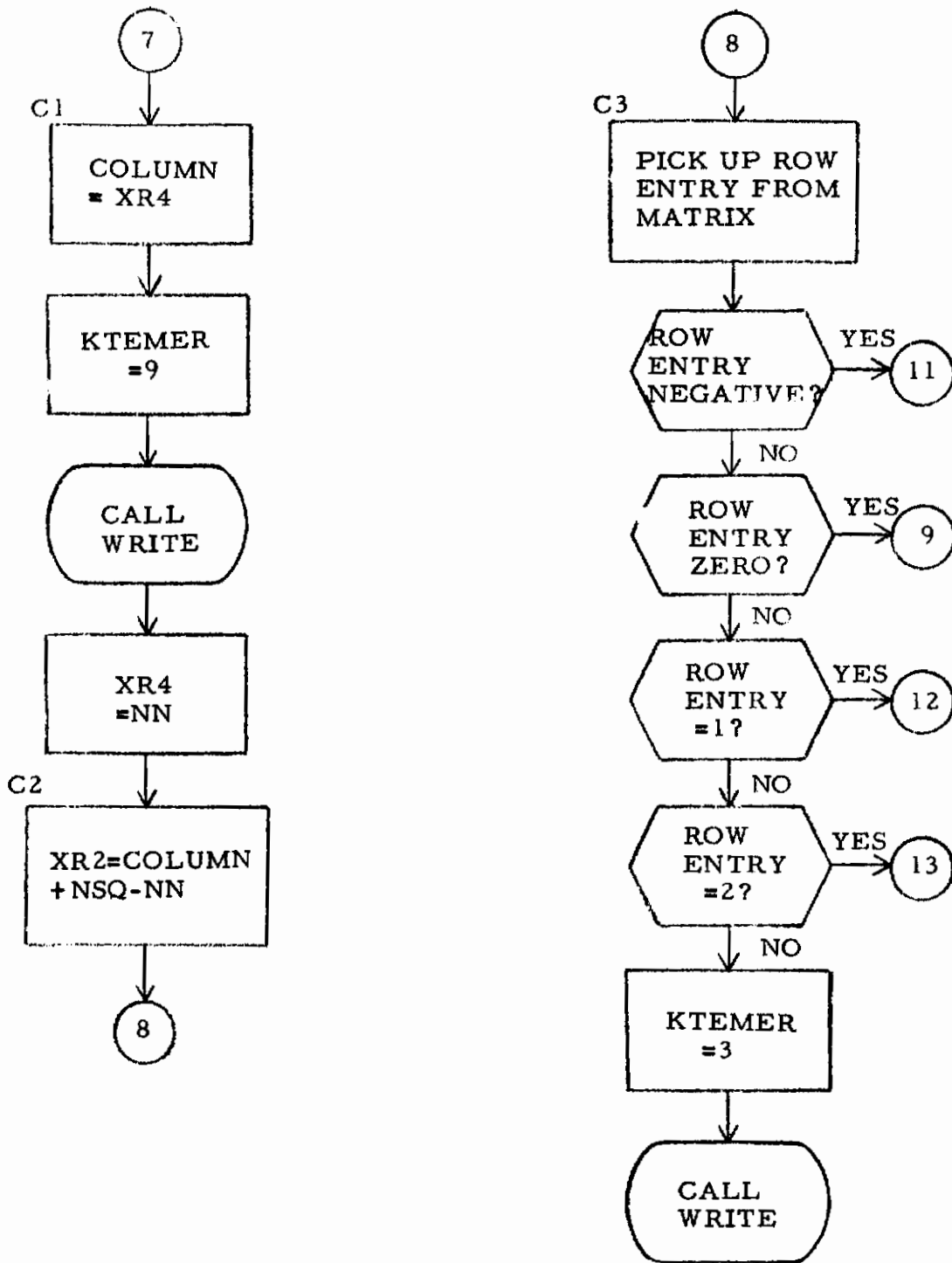
FLOW CHARTS OF SUBROUTINES CHEKIN AND PREC



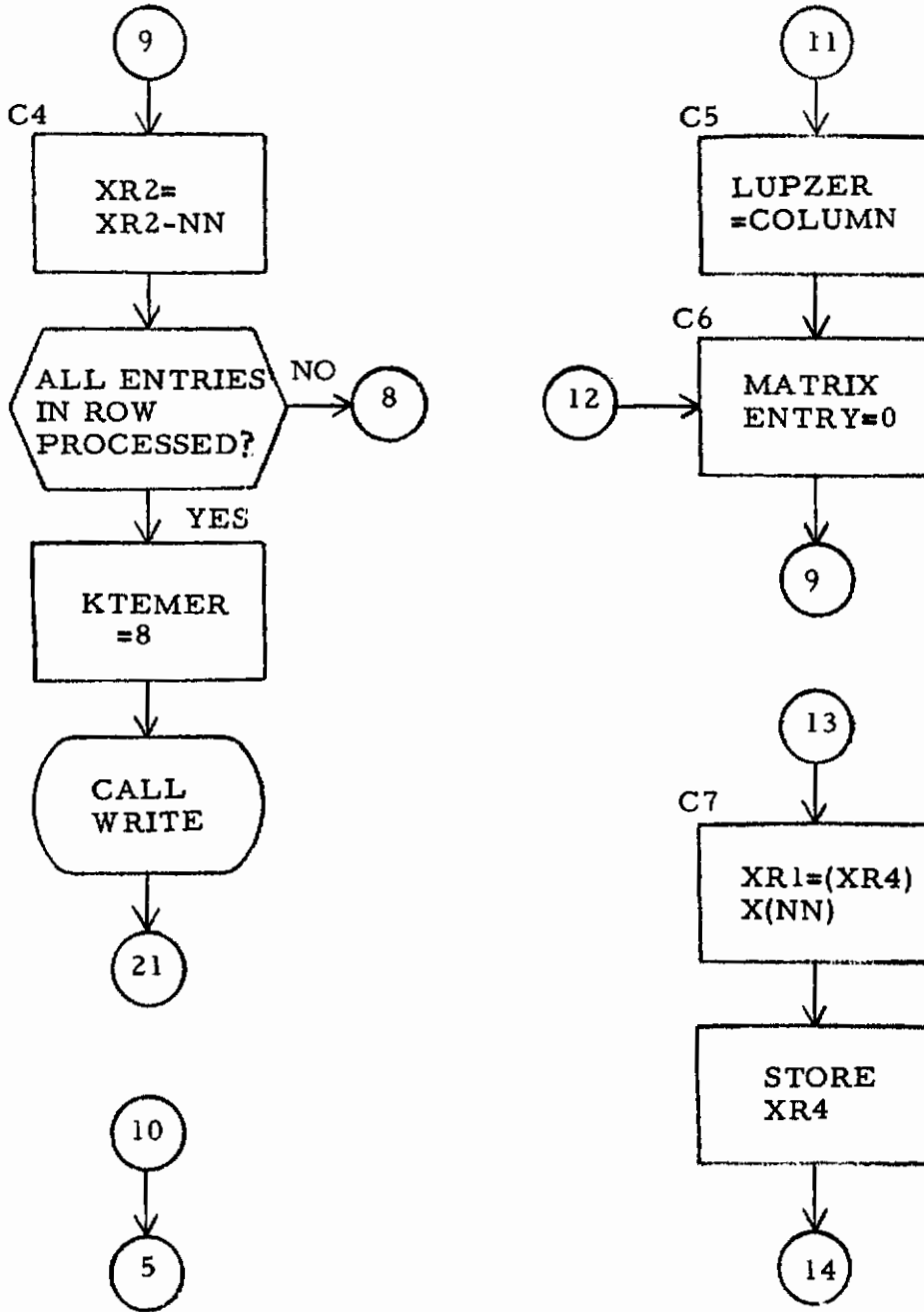
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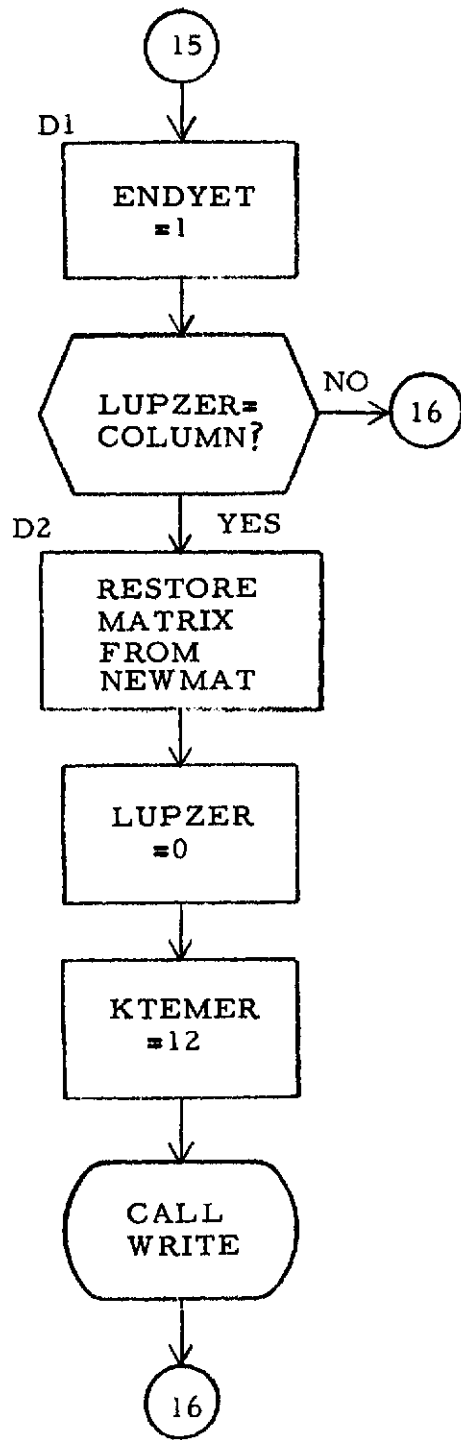
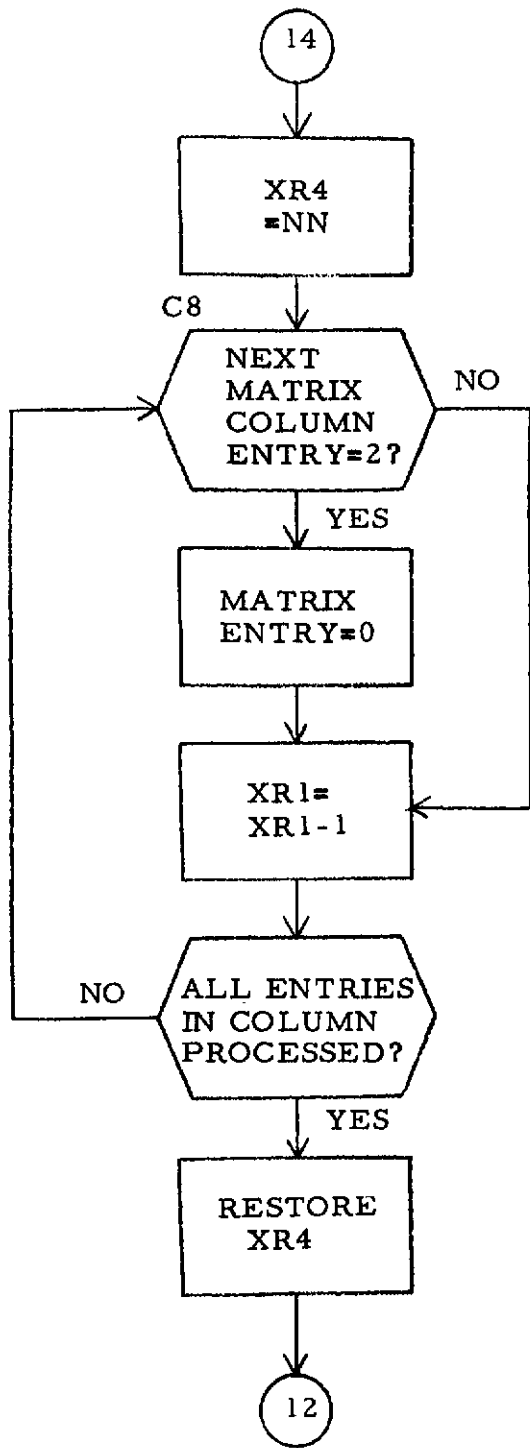


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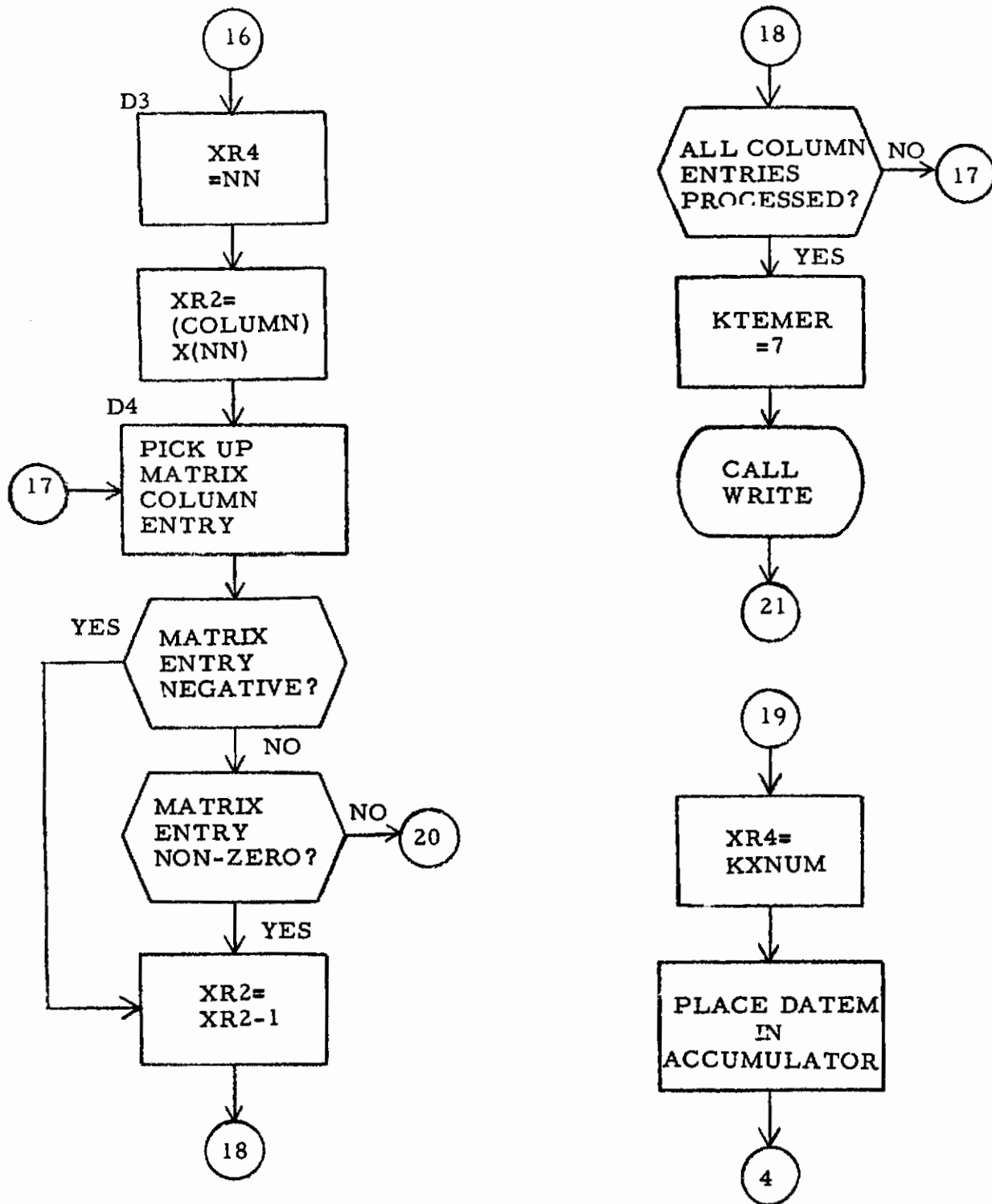


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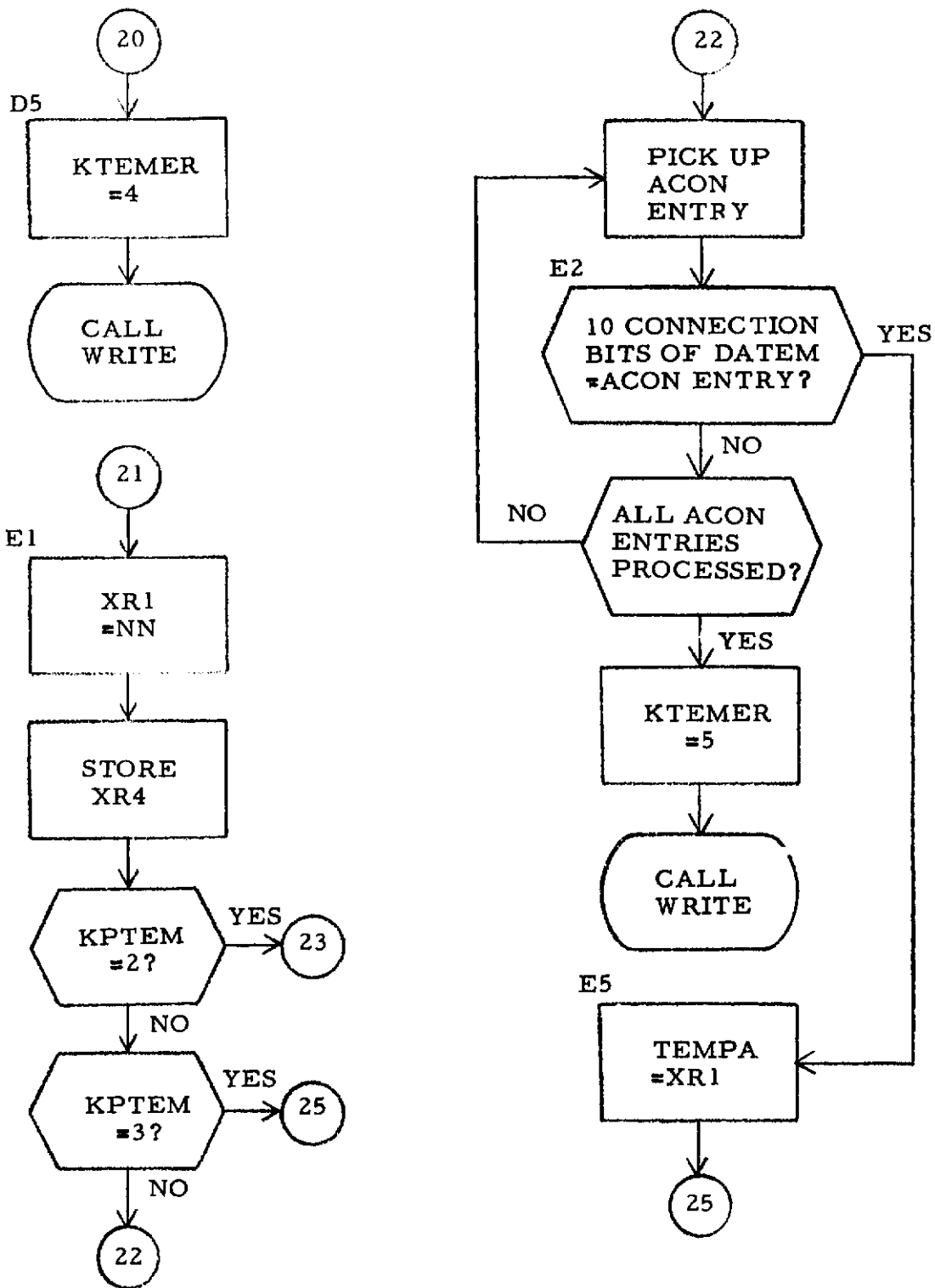


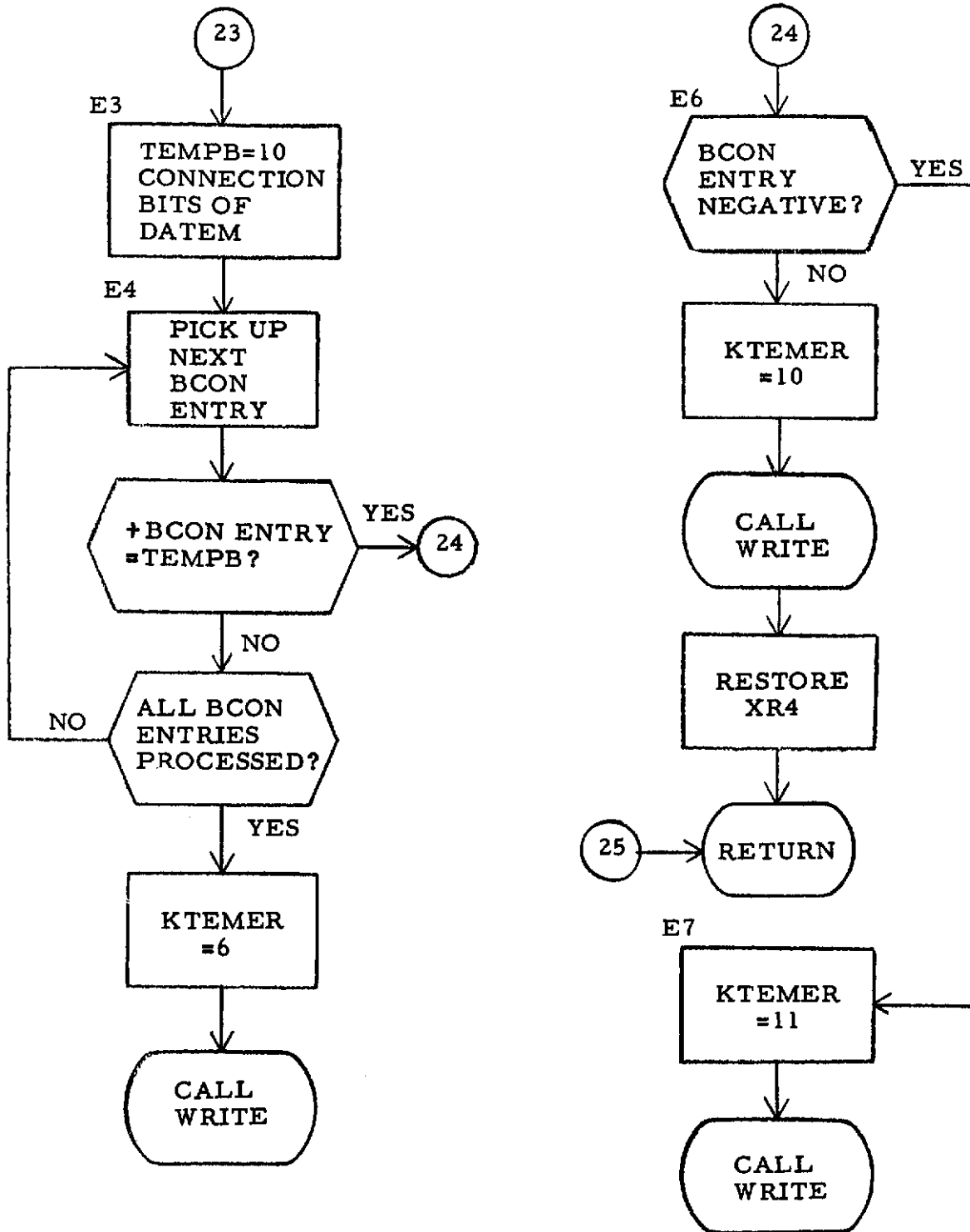


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Control
LISTING OF SUBROUTINES CHEKIN AND PREC

```

* LABEL
* PACK
* FAP
      CCUNT      1000
*PREC          TESTS PRECEDENCES AND CONNECTIONS
      ENTRY     CHEKIN
      ENTRY     PINMAT
      ENTRY     PCUTMT
DATAC  CCMPCN  1
MATRIX CCMPCN 625
NEWMAT CCMPCN 625
KFIRST CCMPCN 25
KSEC   CCMPCN 25
KWUS   CCMPCN 25
KTEPER CCMPCN 1
KXNUM  CCMPCN 1
KXNUMA CCMPCN 1
NN     CCMPCN 1
LUPZER CCMPCN 1
CCLUPA CCMPCN 1
ENDYET CCMPCN 1
NSQ    CCMPCN 1
N2MINA CCMPCN 1
N2MNP1 CCMPCN 1
NPLUS1 CCMPCN 1
N2MIA1 CCMPCN 1
CONMAT CCMPCN 625
ACCA   CCMPCN 75
BCCA   CCMPCN 75
KXSC   CCMPCN 1
      SGNC   CCMPCN 1
      SGAL   CCMPCN 1
      SGXC   CCMPCN 1
      SECEX  CCMPCN 1
BCNT   CCMPCN 1
FCRTP  CCMPCN 1
CHEKIN CLA     TP=HEED      STORE THREE TO SIGNAL FLOW CHART TYPE
      STC     KPTEM
      CLA     FCCRTP       TEST FOR FLOW DIAGRAM TYPE (1)
      SUB     CNED        IF ONE, THEN THIS IS FLOW DIAGRAM TYPE
      TNZ     1,4        IF NOT =1, RETURN
      CLA     SGNC        SET UP DATEM FOR P.C. COMPARISON
      ALS     9
      ACC     SGAL
      STC     DATEM
      TRA     AZ
PINMAT CLA     CNED       PTEM=1 FOR P INPUT
      STC     KPTEM
      TRA     ++3
PCUTMT CLA     TWCC       PTEM=2 FOR P OUTPUT
      STC     KPTEM
      CLA     FCCRTP       TEST FOR TP TYPE OF BRANCH
      SUB     TWCC       TP TYPE OF BRANCH =2
      TNZ     1,4        IF NOT =2, RETURN
      CLA*   DATAC       PICK UP WORD AFTER TP
      STC     DATEM      PLACE IN TEMPORARY STORAGE
AZ     SXC     XR1,1
      SXC     XR2,2
      SXC     XR4,4
      CLA     NN

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A1	STC	C4	STORE NN IN DECREMENT OF TIX INSTRUCTION
	LXC	KXNUM,4	KXNUM=NUMBER OF ROWS IN MATRIX
	CLA	CATEM	PICK UP WORD FOLLOWING TPX OR TXP
A2	CAS	KFIRST,4	COMPARE TO TABLE OF BEGINNINGS OF STEPS
	TRA	**2	
	TRA	B1	IF EQUAL, GO TO B1
	TIX	A2,4,1	
A2B	LXD	KXNUM,4	IF NOT, COMPARE TO TABLE OF ENDS OF STEP
	CLA	CATEM	
A2C	CAS	KSEC,4	
	TRA	**2	
	TRA	C1	IF EQUAL, GO TO C1
	TIX	A2C,4,1	IF NOT, TRY NEXT ENTRY IN KSEC TABLE
A3	LXC	XR1,1	RELOAD INDEX REGISTERS
	LXD	XR2,2	
	LXD	XR4,4	
	TRA	1,4	RETURN TO CALLING ROUTINE
B1	SXC	COLUMN,4	PROCESSES START OF PRECEDENCE MATRIX STEP
	CLA	NINED	
	STC	KTEMER	
	CALL	WRITE	
	CLA	ENCYET	DETERMINE IF LAST COLUMN COMPLETELY PROCESSED
	TZE	C1	IF NOT, D1 NOT ZERO AND ERROR OCCURRED
	CLA	TWCC	PUT 2 IN KTEMER TO INDICATE THAT
	STC	KTEMER	STEP STARTED BEFORE PREVIOUS STEP ENDED
	CALL	WRITE	CALL WRITE SUBROUTINE
C1	SXC	COLUMN,4	C1 PROCESSES END OF PRECEDENCE MATRIX STEP
	CLA	NINED	WRITE OUT SGNC, SGNL, SGXC, SECEX
	STC	KTEMER	
	CALL	WRITE	
	STZ	ENCYET	
	LXD	NN,4	PUT NUMBER OF ROWS IN XR4
C2	CLA	N2MINN	ADD COLUMN NUMBER TO (UNSQURED-N) AND PUT INTO
	ADD	COLUMN IXR2, WANT	TO ZERO OUT ROW BECAUSE STEP COMPLETED
	PDX	,2	BUT MUST ALSO ZERO OUT COLUMNS CONTAINING
			Z'S ZEROED OUT
C3	CLA	MATRIX,2	PICK UP LAST ENTRY IN ROW
	FMI	C5	IF MINUS(ENTRY POINT TO LOOP) GO TO C5
	TZE	C4	IF ZERO, GO TO PICK UP NEXT ENTRY
	SUB	CNED	
	TZE	C6	IF ONE, GO TO C6 TO ZERO OUT
	SUB	CNED	
	TZE	C7	IF 2, GO TO C7 TO ZERO OUT COLUMN
	CLA	THREED	NUMBER OTHER THAN -1,0,1,2
	STC	KTEMER	STORE 3 IN KTEMER TO INDICATE ERROR
	CALL	WRITE	WRITE ERROR MESSAGE
C4	TIX	**1,2,**	SUBTRACT NN FROM IR2 TO PICK UP NEXT ENTRY IN ROW
	TIX	C3,4,1	TEST ALL ENTRIES IN ROW PROCESSED. IF NOT, GO TO C3
	CLA	EIGHTD	
	STC	KTEMER	
	CALL	WRITE	
	TSX	E1,4	TEST CONNECTIONS
	TRA	A3	IF ROW PROCESSED, GO TO A3 TO EXIT
C5	CLA	COLUMN	THIS IS ENTRY POINT TO BEGINNING OF LOOP. STORE
	STC	LUPZER	THIS COLUMN NUMBER IN LUPZER SO MATRIX CAN BE RENEWED
	TRA	C6	GO TO C6
C6	STZ	MATRIX,2	ZERO OUT THIS ROW ENTRY
	TRA	C4	GO TO C4
C7	MPY	ZERC	CLEAR ACCUMULATOR AND MQ REGISTERS
	SSP		MAKE SURE SIGN OF ACCUMULATOR IS POSITIVE

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PXC      ,4          ZERO OUT TWOS IN PRESENT COLUMN
XCA
MPY      NN
ALS      17         COMPENSATES FOR BOTH IN DECREMENT
PDX      ,1
SXD      XRTEM,4    STORE IXR4 IN XRTEM
LXD      NN,4       PUT NN IN IXR4
C8 CLA      MATRIX,1  PICK UP LAST ENTRY IN COLUMN
SUB      TWCD       TEST IF 2
TNZ      ++2        IF NOT, DO NOT ZERO OUT
STZ      MATRIX,1   IF 2, ZERO OUT
TXI      ++1,1,-1  SUBTRACT 1 FROM IXR1 TO PICK UP NEXT ENTRY IN COLUMN
TIX      C8,4,1    TEST ALL ENTRIES IN COLUMN PROCESSED. IF NOT, GO TO C8
LXD      XRTEM,4    RELOAD IXR4
TRA      C6         GO TO C6
D1 CLA      CNED     C1 PROCESSES BEGINNING OF STEP
STO      ENCYET     STORE 1 IN ENCYET TO SIGNAL STEP BEGUN
CLA      LUPZER     TEST IF THIS STEP IS ENTRY INTO START OF LOOP
SUB      CCOLUMN
TNZ      C3         IF NO, GO TO D3.
LXD      NSC,4     IF YES, MATRIX MUST BE REFRESHED. PUT NN SQUARED IN IXR4
D2 CLA      NEWMAT,4  PICK UP ENTRY IN PERMANENT MATRIX
STC      MATRIX,4   STORE IN TEMPORARY MATRIX
TIX      C2,4,1    TEST ALL ENTRIES RESTORED. IF NOT, GO TO D2
STZ      LUPZER     ZERO OUT LUPZER
CLA      TWELVD     WRITE COMMENT FOR ENTERING LEGITIMATE LOOP
STC      KTEMER
CALL     WRITE
TRA      A2B
D3 LXD      NN,4     GO TO TEST FOR END OF STEP
PUT NN IN IXR4 TO TEST COLUMN ALL ZERGES
(PRECEDENCES SATISFIED)
MPY      ZERG       CLEAR ACCUMULATOR AND MQ REGISTERS
SSP
LDC      CCOLUMN    MAKE SURE SIGN OF ACCUMULATOR IS POSITIVE
MPY      NN         FORM (COLUMN NUMBER) X (NN)
ALS      17         COMPENSATES FOR BOTH IN DECREMENT
PDX      ,2         PLACE IN XR2
D4 CLA      MATRIX,2  PICK UP LAST ENTRY IN COLUMN
TMI      ++2        IF MINUS, TREAT AS ZERO
TNZ      C5         IF NONZERO, GO TO D5 FOR ERROR MESSAGE
TXI      ++1,2,-1  SUBTRACT 1 FROM IXR2
TIX      D4,4,1    TEST ALL COLUMN ENTRIES PROCESSED. IF NOT,
GO TO D4
CLA      SEVEND
STC      KTEMER
CALL     WRITE
TSX      E1,4       TEST CONNECTIONS
LXD      KXNUM,4    PUT KXNUM IN IXR4
CLA      DATM
TRA      A2B
D5 CLA      FCURD     GO TO A2B TO TEST FOR END OF STEP
STORE 4 IN KTEMER TO SIGNAL THAT
STC      KTEMER     PRECEDENCES NOT SATISFIED
CALL     WRITE      WRITE ERROR MESSAGE
E1 LXD      NN,1     PUT NN INTO XR1
SXD      XRTEM4,4   STORE INDEX REGISTER 4 IN TEMP STORAGE
CLA      KPTM
SUB      TWCC
TZE      E3
SUB      CNED
TZE      1,4

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	CLA	DATEM	
	ANA	MASKA	
E2	CAS	ACCN,1	
	TRA	**2	
	TRA	E5	
	TIX	E2,1,1	
	CLA	FIVED	
	STC	KTEPER	
	CALL	WRITE	
E3	CLA	DATEM	PICK UP TEN BITS THAT ARE DIGITAL OUTPUTS
	ANA	MASKA	STORE IN TEMPB
	STC	TEMPB	PICK UP BCON ENTRY
E4	CLA	BCCN,1	MAKE POSITIVE
	SSP		IF EQUAL TO TEMPB, GO TO E6
	CAS	TEMPB	IF NOT EQUAL, GO TO **2
	TRA	**2	IF EQUAL, GO TO E6
	TRA	E6	IF NOT ALL BCON PROCESSED, GO TO E4
	TIX	E4,1,1	
	CLA	SIXC	
	STC	KTEPER	
	CALL	WRITE	
E5	SXD	TEMPA,1	
	TRA	1,4	
E6	CLA	BCCN,1	PICK UP BCON ENTRY WITH SIGN
	TMI	E7	IF MINUS, THERE IS NO CONNECTION-GO TO E7
	CLA	TEND	IF PLUS, O.K.-WRITE CONNECTION OK.
	STC	KTEPER	
	CALL	WRITE	GO TO WRITE:
	LXD	XRTEM4,4	RESTORE INDEX REGISTER 4
	TRA	1,4	RETURN
E7	CLA	ELEVDC	WRITE NO CONNECTION
	STC	KTEPER	
	CALL	WRITE	GO TO WRITE
ZERC	CCT	0	
CNED	CCT	1000000	
TWOC	CCT	2000000	
THKEED	CCT	3000000	
FCURC	CCT	4000000	
FIVED	CCT	5000000	
SIXC	CCT	6000000	
SEVEND	CCT	7000000	
EIGHTD	CCT	10000000	
NINED	CCT	11000000	
TENC	CCT	12000000	11 IN DECREMENT
ELEVDC	CCT	13000000	12 IN DECREMENT
TWELVD	CCT	14000000	
KPEM	PZE		
XR1	PZE		
XR2	PZE		
XR4	PZE		
XRTEM	PZE		
XRTEM4	PZE		
MASKA	OCT	000017770000	
TEMPA	PZE		
TEMPB	PZE		
DATEM	PZE		
	END		

APPENDIX II

LISTINGS OF COMPUTER RUNS OF OPERATIONAL AUTOMATIC CHECKOUT PROGRAM WITH SIMULATOR MODIFIED TO INCLUDE PRECEDENCE AND CONNECTION MATRIX TECHNIQUES

A. INTRODUCTION

The VATE simulator was modified to include flow diagram and hardware precedence matrix techniques and connection matrix techniques. An operational automatic checkout program was then used with the modified simulator to validate the techniques.

The following seven computer runs were made:

1. A run with no precedence constraints.
2. A run in which hardware precedences and connections were satisfied.
3. A run in which hardware precedences were violated.
4. A run in which invalid connections were requested.
5. A run in which flow diagram precedences were satisfied.
6. A run in which flow diagram precedences were violated.
7. A run in which an inconsistent precedence matrix was specified in the input data.

At the time at which the operational automatic checkout program was used for validation, it contained an error which caused termination before completion of execution of the program. However, a sufficient portion of the program was processed to enable validation of the precedence and connection matrix techniques.

On the listings of the runs, after the echo print of the input data, the first column, LABEL, is an identification number taken from the input card of the checkout program instruction being executed. The second column, REV, is the drum revolution during which the instruction is executed. The third and fourth columns, CHN and SEC, are the channel and sector in which the automatic checkout instruction is being executed. The next three columns, NC, OP, and W/W constitute the instruction being executed. The next two columns, DEST and SRC, are the destination and source for this instruction. The next three columns, OLD DEST, SOURCE, and NEW DEST, are the octal contents of the old destination, the source, and the new destination. The next column, TN, contains an 02 for instructions in permanent memory and a 77 for instructions executed in the variable registers. The last column, ERRORS, contains code numbers for the errors that are detected by the simulator during execution of the program. These errors are not necessarily

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related to the errors detected by the computer programs which implement precedence and connection matrix techniques.

The validation runs are discussed in detail in the following sections.

B. COMPUTER RUN WITH NO PRECEDENCES

A run was made using no precedence constraints in order to show a listing of the output that would result from a run with the simulator unmodified by precedence and connection matrix techniques. The run is listed on the following pages.

LABEL	REV	CFN	SEC	NC	OP	A/W	DEST	SRC	CLD	DEST	SOURCE	NEW	DEST	TH	ERRORS
08700	001	166.111		166	BLFK	CC5	F.2	K.112	C.0000000		G.0000200	0.0000200		02	
08700	001	166.111		166	BLFK	CC5	F.3	K.113	C.0000000		0.0000004	0.0000004		02	
08700	001	166.111		166	BLFK	CC5	F.4	K.114	C.0000000		1.6700037	1.6700037		02	
08700	001	166.111		166	BLFK	CC5	F.5	K.115	C.0000000		0.0200000	0.0200000		02	
08700	001	166.111		166	BLFK	CC5	F.6	K.116	C.0000000		0.0000000	0.0000000		02	
08706	001	166.117		166	BLJK	C10	J.CC	K.120	C.0000000		0.2610477	0.2610477		02	
08706	001	166.117		166	BLJK	C10	J.C1	K.121	C.0000000		0.2004500	0.2004500		02	
08706	001	166.117		166	BLJK	C10	J.C2	K.122	C.0000000		0.0451033	0.0451033		02	
08706	001	166.117		166	BLJK	C10	J.C3	K.123	C.0000000		0.5012330	0.5012330		02	
08706	001	166.117		166	BLJK	C10	J.C4	K.124	C.0000000		0.1437714	0.1437714		02	
08706	001	166.117		166	BLJK	C10	J.C5	K.125	C.0000000		0.0000000	0.0000000		02	
08706	001	166.117		166	BLJK	C10	J.C6	K.126	C.0000000		0.0000000	0.0000000		02	
08706	001	166.117		166	BLJK	C10	J.C7	K.127	C.0000000		0.0000000	0.0000000		02	
08715	001	166.130		160	JUMP	072			C.0000000		0.0000000	0.0000000		02	
50000	001	160.222		160	TFZ	C14	C.324*F.4		C.0000000		1.6700037	1.6700037		02	
50200	001	160.240		160	TFZ	CC2	F.1	Z.	C.0000000		0.0000000	0.0000000		02	
50300	001	160.242		160	TFK	C10	F.4	K.244	1.6700037		1.6100456	1.6100456		02	
09800	001	160.254		160	TEK	CC1	E.	K.255	0.0000000		1.6000053	1.6000053		02	
10000	001	160.256		C14	JUMP	141			0.0000000		0.0000000	0.0000000		02	
51700	001	014.420		C14	JUMP	000			0.0000000		0.0000000	0.0000000		02	
51800	001	014.421		C14	TCE	CC1	C.22*E.		C.0000000		1.6000053	1.6000053		02	
52000	001	014.423		C14	REPT	017	C2C		C.0000000		0.0000000	0.0000000		02	
52100	001	014.424		C14	TCJ	000	C.025*J.C5		C.0000000		0.0000050	0.0000050		02	
52100	001	014.425		C14	TCJ	000	C.026*J.C6		C.0000000		0.0000000	0.0000000		02	
52100	001	014.426		C14	TCJ	000	C.027*J.C7		C.0000000		0.0000000	0.0000000		02	
52100	001	014.427		C14	TCJ	000	C.030*J.C0		C.0000000		0.0000000	0.0000000		02	
52100	001	014.430		C14	TCJ	000	C.031*J.11		C.0000000		0.0000000	0.0000000		02	
52100	001	014.431		C14	TCJ	000	C.032*J.12		C.0000000		0.0000000	0.0000000		02	
52100	001	014.432		C14	TCJ	000	C.033*J.13		C.0000000		0.0000000	0.0000000		02	
52100	001	014.433		C14	TCJ	000	C.034*J.14		C.0000000		0.0000000	0.0000000		02	
52100	001	014.434		C14	TCJ	000	C.035*J.15		C.0000000		0.0000000	0.0000000		02	
52100	001	014.435		C14	TCJ	000	C.036*J.16		C.0000000		0.0000000	0.0000000		02	
52100	001	014.436		C14	TCJ	000	C.037*J.17		C.0000000		0.0000000	0.0000000		02	
52100	001	014.437		C14	TCJ	000	C.040*J.C0		C.0000000		0.2610477	0.2610477		02	
52100	001	014.440		C14	TCJ	000	C.041*J.C1		C.0000000		0.2004500	0.2004500		02	
52100	001	014.441		C14	TCJ	000	C.042*J.02		C.0000000		0.0450103	0.0450103		02	
52100	001	014.442		C14	TCJ	000	C.043*J.03		C.0000000		0.5012330	0.5012330		02	
52100	001	014.443		C14	TCJ	000	C.044*J.04		C.0000000		0.1437714	0.1437714		02	
52100	001	014.445		C14	REPT	CC7	C1C		C.0000000		0.0000000	0.0000000		02	
52100	001	014.446		C14	TFZ	000	C.047*F.7		C.0000000		0.0000000	0.0000000		02	
52100	001	014.447		C14	TFZ	000	C.050*F.C		C.0000000		0.0000000	0.0000000		02	
52100	001	014.450		C14	TFZ	000	C.051*F.1		C.0000000		0.0000000	0.0000000		02	
52100	001	014.451		C14	TFZ	000	C.052*F.2		C.0000000		0.0000000	0.0000000		02	
52100	001	014.452		C14	TFZ	000	C.053*F.3		C.0000000		0.0000000	0.0000000		02	
52100	001	014.453		C14	TFZ	000	C.054*F.4		C.0000000		1.6100456	1.6100456		02	
52100	001	014.454		C14	TFZ	000	C.055*F.5		C.0000000		0.0200000	0.0200000		02	
52100	001	014.455		C14	TFZ	000	C.056*F.6		C.0000000		0.0000000	0.0000000		02	
52100	001	014.457		C14	REPT	CC6	CC7		C.0000000		0.0000000	0.0000000		02	
52100	001	014.460		C14	TCH	000	C.061*H.01		C.0000000		0.0000000	0.0000000		02	
52100	001	014.461		C14	TCH	000	C.062*H.02		C.0000000		0.0000000	0.0000000		02	
52100	001	014.462		C14	TCH	000	C.063*H.03		C.0000000		0.0000000	0.0000000		02	
52100	001	014.463		C14	TCH	000	C.064*H.04		C.0000000		0.0000000	0.0000000		02	
52100	001	014.464		C14	TCF	000	C.065*H.05		C.0000000		0.0000000	0.0000000		02	

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54300	002	014.C66	C14	THC	CCC	H-C7	C.067*	0.000000	0.000000	0.000000	0.000000	02
54400	002	014.067	C14	JUMP	000			0.000000	0.000000	0.000000	0.000000	02
54500	002	014.070	C14	THX	CCC	H.11	X.	0.000000	0.000000	0.000000	0.000000	02
54600	002	014.071	C14	THX	CCC	H.12	X.	0.000000	0.000000	0.000000	0.000000	02
54700	002	014.072	C14	THX	CCC	H.13	X.	0.000000	0.000000	0.000000	0.000000	02
54800	002	014.073	C14	THX	CCC	H.14	X.	0.000000	0.000000	0.000000	0.000000	02
54900	002	014.074	C14	THX	CCC	H.15	X.	0.000000	0.000000	0.000000	0.000000	02
55000	002	014.075	C14	THC	CCC	R.		3.777777	1.600053	1.600053	1.600053	02
55100	002	014.076	C14	TDC	000	D.	C.	0.000000	0.000000	0.000000	0.000000	02
55200	002	014.077	174	TEX	CCC	E.	X.	1.500053	0.000000	0.000000	0.000000	02
00000	002	174.100	160	JUMP	C53			0.000000	0.000000	0.000000	0.000000	77
10300	002	160.154	160	TPK	CC1	P.124	K.155	0.000000	0.000000	0.000000	0.000000	02
10500	002	160.156	160	REPT	CC7	C1C		0.000000	0.000000	0.000000	0.000000	02
10600	002	160.157	160	TCF	CC0	C.260	*F.C	0.000000	0.000000	0.000000	0.000000	02
10660	002	160.160	160	TOF	CC0	O.261	*F.1	0.000000	0.000000	0.000000	0.000000	02
10600	002	160.161	160	TOF	CC0	C.262	*F.2	0.000000	0.000000	0.000000	0.000000	02
10600	002	160.162	160	TOF	CC0	O.263	*F.3	0.000000	0.000000	0.000000	0.000000	02
10600	002	160.163	160	TOF	CC0	O.264	*F.4	0.000000	1.610456	1.610456	1.610456	02
10600	002	160.164	160	TOF	CC0	O.265	*F.5	0.000000	0.000000	0.000000	0.000000	02
10600	002	160.165	160	TOF	CC0	O.266	*F.6	0.000000	0.000000	0.000000	0.000000	02
10600	002	160.166	160	TOF	CC0	O.267	*F.7	0.000000	0.000000	0.000000	0.000000	02
10700	002	160.170	160	JUMP	045	G2C		0.000000	0.000000	0.000000	0.000000	02
10800	002	160.236	160	REPT	C17			0.000000	0.000000	0.000000	0.000000	02
10900	002	160.237	160	TCJ	000	O.340	*J.C0	0.000000	0.2610477	0.2610477	0.2610477	02
10900	002	160.240	160	TCJ	000	C.341	*J.01	0.000000	0.2094500	0.2094500	0.2094500	02
10900	002	160.241	160	TCJ	000	C.342	*J.02	0.000000	0.0450103	0.0450103	0.0450103	02
10900	002	160.242	160	TCJ	000	O.343	*J.03	0.000000	0.5012330	0.5012330	0.5012330	02
10900	002	160.243	160	TCJ	000	C.344	*J.04	0.000000	0.1437714	0.1437714	0.1437714	02
10900	002	160.244	160	TOJ	000	C.345	*J.C5	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.245	160	TOJ	000	O.346	*J.C6	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.246	160	TOJ	000	C.347	*J.C7	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.247	160	TOJ	000	C.350	*J.10	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.250	160	TOJ	000	O.351	*J.11	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.251	160	TOJ	000	C.352	*J.12	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.252	160	TOJ	000	O.353	*J.13	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.253	160	TOJ	000	C.354	*J.14	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.254	160	TOJ	000	O.355	*J.15	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.255	160	TOJ	000	C.356	*J.16	0.000000	0.000000	0.000000	0.000000	02
10900	002	160.256	160	TOJ	000	O.357	*J.17	0.000000	0.000000	0.000000	0.000000	02
11000	002	160.260	160	JUMP	113			0.000000	0.000000	0.000000	0.000000	02
11300	002	160.374	160	TPK	CC1	P.135	K.375	0.000000	0.7550135	0.7550135	0.7550135	02
11500	002	160.376	160	TPK	CC1	P.131	K.377	0.000000	1.3770131	1.3770131	1.3770131	02
11700	002	160.400	160	TEK	CC1	E.	K.401	0.000000	1.6000017	1.6000017	1.6000017	02
11900	002	160.402	160	TPK	004	P.132	K.403	0.000000	0.2600132	0.2600132	0.2600132	02
12100	002	160.407	160	TPK	CC1	P.136	K.410	0.000000	0.000000	0.000000	0.000000	02
12300	002	160.411	160	JUMP	006			0.000000	0.000000	0.000000	0.000000	02
51700	002	014.420	G14	JUMP	CC0			0.000000	0.000000	0.000000	0.000000	02
51800	002	014.421	014	TOE	CC1	C.C22	*E.	0.000000	1.6000017	1.6000017	1.6000017	02
52000	002	014.423	C14	REPT	C17	G2C		0.000000	0.000000	0.000000	0.000000	02
52100	002	014.424	C14	TOJ	000	C.C25	*J.C5	0.000000	0.000000	0.000000	0.000000	02
52100	002	014.425	C14	TOJ	000	C.C26	*J.C6	0.000000	0.000000	0.000000	0.000000	02
52100	002	014.426	C14	TOJ	000	O.C27	*J.C7	0.000000	0.000000	0.000000	0.000000	02
52100	002	014.427	C14	TCJ	000	C.C30	*J.C10	0.000000	0.000000	0.000000	0.000000	02
52100	002	014.430	014	TOJ	000	C.C31	*J.C11	0.000000	0.000000	0.000000	0.000000	02
52100	002	014.431	014	TOJ	000	O.C32	*J.C12	0.000000	0.000000	0.000000	0.000000	02
52100	002	014.432	014	TCJ	000	C.C33	*J.C13	0.000000	0.000000	0.000000	0.000000	02
52100	002	014.433	014	TOJ	000	C.C34	*J.C14	0.000000	0.000000	0.000000	0.000000	02

52100	002	014.434	014	TGJ	000	C.C35*J.15	0.0000000	0.0000000	0.0000000	02
52100	002	014.435	014	TGJ	000	C.C36*J.16	0.0000000	0.0000000	0.0000000	02
52100	002	014.436	014	TGJ	000	C.C37*J.17	0.0000000	0.0000000	0.0000000	02
52100	002	014.437	014	TGJ	000	C.C40*J.00	0.0000000	0.0000000	0.0000000	02
52100	002	014.440	014	TGJ	000	C.C41*J.C1	0.0000000	0.0000000	0.0000000	02
52100	002	014.441	014	TGJ	000	C.C42*J.C2	0.0000000	0.0000000	0.0000000	02
52100	002	014.442	014	TGJ	000	C.C43*J.C3	0.0000000	0.0000000	0.0000000	02
52100	002	014.443	014	TGJ	000	C.C44*J.04	0.0000000	0.0000000	0.0000000	02
52200	002	014.445	014	REPT	007	01C	0.0000000	0.0000000	0.0000000	02
52300	002	014.446	014	TGF	000	C.C47*F.7	0.0000000	0.0000000	0.0000000	02
52300	002	014.447	014	TGF	000	C.C50*F.0	0.0000000	0.0000000	0.0000000	02
52300	002	014.450	014	TGF	000	C.C51*F.1	0.0000000	0.0000000	0.0000000	02
52300	002	014.451	014	TGF	000	C.C52*F.2	0.0000000	0.0000000	0.0000000	02
52300	002	014.452	014	TGF	000	C.C53*F.3	0.0000000	0.0000000	0.0000000	02
52300	002	014.453	014	TGF	000	C.C54*F.4	0.0000000	0.0000000	0.0000000	02
52300	002	014.454	014	TGF	000	C.C55*F.5	0.0000000	0.0000000	0.0000000	02
52300	002	014.455	014	TGF	000	C.C56*F.6	0.0000000	0.0000000	0.0000000	02
52400	002	014.457	014	REPT	006	007	0.0000000	0.0000000	0.0000000	02
52500	002	014.460	014	TGH	000	C.C61*H.01	0.0000000	0.0000000	0.0000000	02
52500	002	014.461	014	TGH	000	C.C62*H.02	0.0000000	0.0000000	0.0000000	02
52500	002	014.462	014	TGH	000	C.C63*H.03	0.0000000	0.0000000	0.0000000	02
52500	002	014.463	014	TGH	000	C.C64*H.04	0.0000000	0.0000000	0.0000000	02
52500	002	014.464	014	TGH	000	C.C65*H.05	0.0000000	0.0000000	0.0000000	02
52500	002	014.465	014	TGH	000	C.C66*H.06	0.0000000	0.0000000	0.0000000	02
52500	002	014.466	014	TGH	000	C.C67*H.07	0.0000000	0.0000000	0.0000000	02
52600	002	014.470	014	JUMP	001		0.0000000	0.0000000	0.0000000	02
52700	002	014.472	014	REPT	020	021	0.0000000	0.0000000	0.0000000	02
52800	002	014.473	014	TGX	000	G.14 X.	0.0000001	0.0000001	0.0000001	02
52800	002	014.474	014	TGX	000	G.15 X.	0.0000001	0.0000001	0.0000001	02
52800	002	014.475	014	TGX	000	G.16 X.	0.0000001	0.0000001	0.0000001	02
52800	002	014.476	014	TGX	000	G.17 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.477	014	TGX	000	G.00 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.000	014	TGX	000	G.01 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.001	014	TGX	000	G.02 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.002	014	TGX	000	G.03 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.003	014	TGX	000	G.04 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.004	014	TGX	000	G.05 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.005	014	TGX	000	G.06 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.006	014	TGX	000	G.07 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.007	014	TGX	000	G.10 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.010	014	TGX	000	G.11 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.011	014	TGX	000	G.12 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.012	014	TGX	000	G.13 X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.013	014	TGX	000	G.14 X.	0.0000001	0.0000001	0.0000001	02
52900	003	014.015	014	THX	000	H.16 X.	0.0000001	0.0000001	0.0000001	02
53000	003	014.016	015	THX	002	H.17 X.	0.0000001	0.0000001	0.0000001	02
53100	003	015.021	014	TCC	001	C. 022*	1.6000053	1.6000017	1.6000017	02
53200	003	014.023	014	REPT	017	020	0.0000000	0.0000000	0.0000000	02
53300	003	014.024	014	TJC	000	J.C5	0.0000000	0.0000000	0.0000000	02
53300	003	014.025	014	TJC	000	J.C6	0.0000000	0.0000000	0.0000000	02
53300	003	014.026	014	TJC	000	J.C7	0.0000000	0.0000000	0.0000000	02
53300	003	014.027	014	TJC	000	J.C8	0.0000000	0.0000000	0.0000000	02
53300	003	014.030	014	TJC	000	J.11	0.0000000	0.0000000	0.0000000	02
53300	003	014.031	014	TJC	000	J.12	0.0000000	0.0000000	0.0000000	02
53300	003	014.032	014	TJC	000	J.13	0.0000000	0.0000000	0.0000000	02
53300	003	014.033	014	TJC	000	J.14	0.0000000	0.0000000	0.0000000	02
53300	003	014.034	014	TJC	000	J.15	0.0000000	0.0000000	0.0000000	02

53300	003	014.C35	014	TJC	CCC	J.16	C.C36*	0.000000	0.000000	0.000000	0.000000	02	
53300	003	014.C36	014	TJC	000	J.17	C.C37*	0.000000	0.000000	0.000000	0.000000	02	
53300	003	014.C37	014	TJC	000	J.C0	C.C40*	0.2610477	0.2610477	0.2610477	0.2610477	02	
53300	003	014.C40	014	TJC	CCC	J.C1	C.C41*	0.2004500	0.2004500	0.2004500	0.2004500	02	
53300	003	014.C41	014	TJC	CCC	J.C2	C.C42*	0.0450103	0.0450103	0.0450103	0.0450103	02	
53300	003	014.C42	014	TJC	000	J.C3	C.C43*	0.5012330	0.5012330	0.5012330	0.5012330	02	
53300	003	014.C43	014	TJC	CCC	J.C4	C.C44*	0.1437714	0.1437714	0.1437714	0.1437714	02	
53300	003	014.C45	014	JUMP	000	F.7	C.C47*	0.000000	0.000000	0.000000	0.000000	02	
53500	003	014.C46	014	BLFC	010	F.C	C.C50*	0.000000	0.000000	0.000000	0.000000	02	
53500	003	014.C46	014	BLFC	010	F.1	C.C51*	0.000000	0.000000	0.000000	0.000000	02	
53500	003	014.C46	014	BLFC	010	F.2	C.C52*	0.000000	0.000000	0.000000	0.000000	02	
53500	003	014.C46	014	BLFC	010	F.3	C.C53*	0.000000	0.000000	0.000000	0.000000	02	
53500	003	014.C46	014	BLFC	010	F.4	C.C54*	1.6100456	1.6100456	1.6100456	1.6100456	02	
53500	003	014.C46	014	BLFC	010	F.5	C.C55*	0.000000	0.000000	0.000000	0.000000	02	
53500	003	014.C46	014	BLFC	010	F.6	C.C56*	0.000000	0.000000	0.000000	0.000000	02	
53600	003	014.C57	014	JUMP	000			0.000000	0.000000	0.000000	0.000000	02	
53700	003	014.C60	014	THC	000	H.C1	C.C61*	0.000000	0.000000	0.000000	0.000000	02	
53800	003	014.C61	014	THC	000	H.C2	C.	1.6000017	1.6000017	1.6000017	1.6000017	02	
53900	003	014.C62	014	THC	000	H.C3	C.C63*	0.000000	0.000000	0.000000	0.000000	02	
54000	003	014.C63	014	THC	000	H.C4	C.C64*	0.000000	0.000000	0.000000	0.000000	02	
54100	003	014.C64	014	THO	000	H.C5	C.C65*	0.000000	0.000000	0.000000	0.000000	02	
54200	003	014.C65	014	THC	000	H.C6	C.C66*	0.000000	0.000000	0.000000	0.000000	02	
54300	003	014.C66	014	THC	000	H.C7	C.C67*	0.000000	0.000000	0.000000	0.000000	02	
54400	003	014.C67	014	JUMP	000			0.000000	0.000000	0.000000	0.000000	02	
54500	003	014.C70	014	THX	000	H.11	X.	0.000000	0.000000	0.000000	0.000000	02	
54600	003	014.C71	014	THX	000	H.12	X.	0.000000	0.000000	0.000000	0.000000	02	
54700	003	014.C72	014	THX	000	H.13	X.	0.000000	0.000000	0.000000	0.000000	02	
54800	003	014.C73	014	THX	000	H.14	X.	0.000000	0.000000	0.000000	0.000000	02	
54900	003	014.C74	014	THX	000	H.15	X.	0.000000	0.000000	0.000000	0.000000	02	
55000	003	014.C75	014	TBC	000	B.	C.	3.7777777	1.6000017	1.6000017	1.6000017	02	
55100	003	014.C76	014	TDC	000	D.	C.	1.6000053	1.6000017	1.6000017	1.6000017	02	
55200	003	014.C77	174	TEX	000	E.	X.	1.6000017	0.000000	0.000000	0.000000	02	
00000	003	174.100	160	JUMP	017			0.000000	0.000000	0.000000	0.000000	77	
12500	003	16C.120	160	XTRP	010	K.123	P.012	0.000000	0.000000	0.000000	0.000000	02	
13100	003	16C.131	160	TPK	001	P.136	K.132	1.6000136	1.6000136	1.6000136	1.6000136	02	
13300	004	16C.132	160	JUMP	434			0.000000	0.000000	0.000000	0.000000	02	
13400	004	16C.070	160	XTRP	004	K.073	P.010	0.000000	0.000000	0.000000	0.000000	02	
13800	004	16C.075	160	TSK	003	S.	K.076	1.7400000	1.7400000	1.7400000	1.7400000	02	
14200	004	16C.101	160	JUMP	077			0.000000	0.000000	0.000000	0.000000	02	
14300	004	16C.201	160	TDK	005	D.	K.202	1.6000017	1.6000017	1.6000017	1.6000017	02	
14700	004	16C.207	160	BLJK	017	J.10	K.210	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.11	K.211	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.12	K.212	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.13	K.213	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.14	K.214	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.15	K.215	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.16	K.216	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.17	K.217	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.C0	K.220	0.2610477	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.C1	K.221	0.2004500	1.4000000	1.4000000	1.4000000	02	
14700	004	16C.207	160	BLJK	017	J.C2	K.222	0.0450103	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.C3	K.223	0.5012330	1.6030114	1.6030114	1.6030114	02	
14700	004	16C.207	160	BLJK	017	J.C4	K.224	0.1437714	1.6273000	1.6273000	1.6273000	02	
14700	004	16C.207	160	BLJK	017	J.C5	K.225	0.000000	0.000000	0.000000	0.000000	02	
14700	004	16C.207	160	BLJK	017	J.C6	K.226	0.000000	0.000000	0.000000	0.000000	02	
15400	004	16C.227	161	BLFK	010	F.C	K.230	0.000000	1.7573161	1.7573161	1.7573161	02	

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Contracts

53800	005 014.061	C14 THC	C00	H.C2	C.	1.6000017	1.6100000	02	
53900	005 014.062	C14 THC	CCC	H.C3	C.C63*	0.0000000	0.0000000	02	
54000	005 014.063	C14 THC	CCO	H.C4	C.C64*	0.0000000	0.0000000	02	
54100	005 014.064	C14 THC	CCO	H.C5	C.C65*	0.0000000	0.0000000	02	
54200	005 014.065	C14 THC	CCC	H.C6	C.C66*	0.0000000	0.0000000	02	
54300	005 014.066	C14 THC	CCO	H.C7	C.C67*	0.0000000	0.0000000	02	
54400	005 014.067	C14 JUMP	CCO			0.0000000	0.0000000	02	
54500	005 014.070	C14 THX	CCO	H.11	X.	0.0000001	0.0000001	02	
54600	005 014.071	C14 THX	CCC	H.12	X.	0.0000001	0.0000001	02	
54700	005 014.072	C14 THX	CCO	H.13	X.	0.0000001	0.0000001	02	
54800	005 014.073	C14 THX	CCO	H.14	X.	0.0000001	0.0000001	02	
54900	005 014.074	C14 THX	CCC	H.15	X.	0.0000001	0.0000001	02	
55000	005 014.075	C14 TBC	CCO	B.	C.	3.7777777	1.6100000	02	
55100	005 014.076	C14 TDC	CCO	D.	C.	0.0000000	1.6100000	02	
55200	005 014.077	174 TEX	CCO	E.	C.	1.6100000	0.0000001	02	
00000	005 174.100	161 JUMP	CCO		X.	0.0000000	0.0000000	77	
19700	005 161.101	161 REPT	017	C2C		0.0000000	0.0000000	02	ERR
19800	005 161.102	161 TKG	CCO	G.C3	K.103	0.0000001	0.0000000	02	ERR
19800	005 161.103	161 TKG	CCO	G.C4	K.104	0.0000001	0.0000000	02	ERR
19800	005 161.104	161 TKG	CCO	G.C5	K.105	0.0000001	0.3400000	02	ERR
19800	005 161.105	161 TKG	CCO	G.C6	K.106	0.0000001	1.3000000	02	ERR
19800	005 161.106	161 TKG	CCO	G.C7	K.107	0.0000001	1.2400000	02	ERR
19800	005 161.107	161 TKG	CCO	G.10	K.110	0.0000001	0.2000000	02	ERR
19800	005 161.110	161 TKG	CCC	G.11	K.111	0.0000001	1.1400000	02	ERR
19800	005 161.111	161 TKG	CCO	G.12	K.112	0.0000001	0.1000000	02	ERR
19800	005 161.112	161 TKG	CCO	G.13	K.113	0.0000001	0.0400000	02	ERR
19800	005 161.113	161 TKG	CCO	G.14	K.114	0.0000001	1.0000000	02	ERR
19800	005 161.114	161 TKG	CCO	G.15	K.115	0.0000001	1.7562625	02	ERR
19800	005 161.115	161 TKG	CCO	G.16	K.116	0.0000001	0.0000000	02	ERR
19800	005 161.116	161 TKG	CCO	G.17	K.117	0.0000001	0.0000000	02	ERR
19800	005 161.117	161 TKG	CCO	G.CC	K.120	0.0000001	1.7642021	02	ERR
19800	005 161.120	161 TKG	CCO	G.C1	K.121	0.0000001	1.7670160	02	ERR
19800	005 161.121	161 TKG	CCO	S.C2	K.122	0.0000000	0.0000000	02	ERR
21200	005 161.122	161 REPT	C11	C12		0.0000000	0.0000000	02	ERR
21300	005 161.124	161 THK	CCO	H.C5	K.125	0.0000000	0.0000000	02	ERR
21300	005 161.125	161 THK	CCO	H.C6	K.126	0.0000000	1.7451161	02	ERR
21300	005 161.126	161 THK	CCO	H.C7	K.127	0.0000000	1.7767622	02	ERR
21300	005 161.127	161 THK	CCO	H.10	K.130	0.0000000	0.0000000	02	ERR
21300	005 161.130	161 THK	CCO	H.11	K.131	0.0000001	0.0000000	02	ERR
21300	005 161.131	161 THK	CCO	H.12	K.132	0.0000001	1.7451161	02	ERR
21300	005 161.132	161 THK	CCO	H.13	K.133	0.0000001	1.7750020	02	ERR
21300	005 161.133	161 THK	CCO	H.14	K.134	0.0000001	1.7702242	02	ERR
21300	005 161.134	161 THK	CCO	H.15	K.135	0.0000001	0.0000000	02	ERR
21300	005 161.135	161 THK	CCO	H.16	K.136	0.0000001	1.6102353	02	ERR
22000	005 161.137	161 TDJ	CC2	D.	J.00	1.6100000	1.7651000	02	ERR
22100	005 161.142	161 TCF	CCO	C.	F.3	1.6100000	0.0000000	02	ERR
22200	005 161.143	161 THK	CC1	H.C4	K.144	0.0000000	0.2610477	02	ERR
22300	005 161.145	176 JUMP	011			0.0000000	1.7767622	02	ERR
00000	005 176.157	176 XTRC	CC1	K.16C	C.	0.0000000	0.0000000	02	ERR
00000	005 176.161	176 ABJ	CCO	B.	J.02	0.0000007	0.0000007	77	ERR
00000	005 176.162	176 READ	011	E.	K.164	0.0000011	0.0000011	77	ERR
00000	005 176.174	175 SDX	CC5	D.	X.	0.0000000	0.3400000	77	ERR
00000	005 175.176	175 TDJ	CC1	D.	J.17	1.7777777	1.7777777	77	ERR
00000	005 175.200	175 AEJ	CC1	E.	J.01	0.0000000	0.0000010	77	ERR
00000	005 175.202	177 TSE	001	S.	E.	0.0000000	1.7400000	77	ERR
00000	005 177.204	177 SJX	002	J.C5	X.	0.0000044	1.7400000	77	ERR
00000	005 177.207	177 SJX	002	J.10	X.	0.0000000	0.0000001	77	ERR

00000	005	177.212	177 TBC	CC0	B.	C.	0.000011	0.2610477	5.2610477	77
00000	005	177.213	177 RIGHT	CC2	B.		0.2610477	0.0000003	0.0261047	77
00000	005	177.216	176 TCB	CC0	B.		0.2610477	0.0261047	0.0261047	77
00000	005	176.217	176 XTRC	CC1	K.220	B.	0.0000007	0.0261047	0.0000007	77
00000	005	176.221	176 A-J	-CC0	B.	J.02	0.0000007	0.0000002	0.0000011	77
00000	005	176.222	176 READ	CC1	E.	K.224	0.0000011	0.0000000	0.0000000	77
00000	005	176.234	175 SDX	CC5	D.	X.	0.0000010	0.0000001	0.0000007	77
00000	005	175.242	177 TSE	CC1	S.	E.	0.0000006	0.0000000	0.0000000	77
00000	005	177.244	177 SJX	CC2	J.C5	X.	0.0000043	0.0000001	0.0000042	77
00000	005	177.247	177 SJX	CC2	J.10	X.	0.0000005	0.0000001	0.0000004	77
00000	005	177.252	177 RGT	CC0	B.	C.	0.0000011	0.0261047	0.0261047	77
00000	005	177.253	177 RGT	CC2	B.		0.0261047	0.0000003	0.0261047	77
00000	005	177.256	176 TCB	CC0	C.		0.0261047	0.0000004	0.0000004	77
00000	005	176.257	176 XTRC	CC1	K.260	C.	0.0000007	0.0000000	0.0000004	77
00000	005	176.261	176 ABJ	CC0	H.	J.02	0.0000004	0.0000002	0.0000006	77
00000	005	176.262	176 READ	CC1	E.	K.267	0.0000006	0.0000000	0.0000000	77
00000	005	176.274	175 SDX	CC5	D.	X.	0.0000007	0.0000001	0.0000006	77
00000	005	175.302	177 TSE	CC1	S.	E.	0.0000000	0.0000000	0.0000000	77
00000	005	177.304	177 SJX	CC2	J.C5	X.	0.0000042	0.0000001	0.0000000	77
00000	005	177.307	177 SJX	CC2	J.10	X.	0.0000004	0.0000001	0.0000003	77
00000	005	177.312	177 TBC	CC0	B.	C.	0.0000006	0.0000000	0.0000000	77
00000	005	177.313	177 RGT	CC2	B.		0.0000004	0.0000003	0.0000004	77
00000	005	177.316	176 TCB	CC0	C.	B.	0.0000004	0.0000003	0.0000000	77
00000	005	176.317	176 XTRC	CC1	K.320	C.	0.0000007	0.0000000	0.0000000	77
00000	005	176.321	176 ABJ	CC0	B.	J.02	0.0000000	0.0000002	0.0000000	77
00000	005	176.322	176 READ	CC1	E.	K.333	0.0000002	0.0000000	0.0000000	77
00000	005	176.334	175 SDX	CC5	D.	X.	0.0000002	0.0000000	0.0000000	77
00000	005	175.342	177 TSE	CC1	S.	E.	0.0000006	0.0000001	0.0000005	77
00000	005	177.344	177 SJX	CC2	J.C5	X.	0.0000041	0.0000000	0.0000000	77
00000	005	177.347	177 SJX	CC2	J.10	X.	0.0000003	0.0000001	0.0000002	77
00000	005	177.352	177 TBC	CC0	B.	C.	0.0000002	0.0000000	0.0000000	77
00000	005	177.352	177 RGT	CC2	B.		0.0000002	0.0000000	0.0000000	77
00000	005	177.356	176 TCB	CC0	C.	B.	0.0000000	0.0000000	0.0000000	77
00000	005	176.357	176 XTRC	CC1	K.360	C.	0.0000007	0.0000000	0.0000000	77
00000	005	176.361	176 ABJ	CC0	B.	J.02	0.0000001	0.0000002	0.0000000	77
00000	005	176.362	176 READ	CC1	E.	K.372	0.0000003	0.0000000	0.0000000	77
00000	005	176.374	175 SDX	CC5	D.	X.	0.0000005	0.0000001	0.0000000	77
00000	005	175.402	177 TSE	CC1	S.	E.	0.0000000	0.0000000	0.0000000	77
00000	005	177.404	177 SJX	CC2	J.C5	X.	0.0000040	0.0000001	0.0000000	77
00000	005	177.407	177 SJX	CC2	J.10	X.	0.0000002	0.0000001	0.0000001	77
00000	005	177.412	177 TBC	CC0	B.	C.	0.0000003	0.0000000	0.0000000	77
00000	005	177.413	177 RGT	CC2	B.		0.0000001	0.0000000	0.0000000	77
00000	005	177.416	176 TCB	CC0	C.	B.	0.0000000	0.0000000	0.0000000	77
00000	005	176.417	176 XTRC	CC1	K.420	C.	0.0000007	0.0000000	0.0000000	77
00000	005	176.421	176 ABJ	CC0	H.	J.02	0.0000006	0.0000002	0.0000000	77
00000	005	176.422	176 READ	CC1	E.	K.425	0.0000010	0.0000000	0.0000000	77
00000	005	176.434	175 SDX	CC5	D.	X.	0.0000004	0.0000000	0.0000000	77
00000	005	175.442	177 TSE	CC1	S.	E.	0.0000000	0.0000000	0.0000000	77
00000	005	177.444	177 SJX	CC2	J.C5	X.	0.0000037	0.0000001	0.0000000	77
00000	005	177.447	177 SJX	CC2	J.10	X.	0.0000001	0.0000000	0.0000000	77
00000	005	177.452	177 TBC	CC0	B.	C.	0.0000010	0.0000000	0.0000000	77
00000	005	177.453	177 RGT	CC2	B.		0.0000000	0.0000000	0.0000000	77
00000	005	177.456	176 TCB	CC0	C.	B.	0.0000026	0.0000002	0.0000002	77
00000	005	176.457	176 XTRC	CC1	K.460	C.	0.0000007	0.0000000	0.0000000	77
00000	005	176.461	176 ABJ	CC0	B.	J.02	0.0000002	0.0000000	0.0000000	77
00000	005	176.462	176 READ	CC1	E.	K.471	0.0000004	0.0000000	0.0000000	77
00000	006	176.474	175 SDX	CC5	D.	X.	0.0000003	0.0000001	0.0000000	77

00000	006	175.002	177	TSE	001	S.	E.	0.0000000	0.1000000	0.1000000	77
00000	006	177.004	177	SJX	002	J.05	X.	C.0000036	0.0000001	0.0000035	77
00000	006	177.007	177	SJX	002	J.10	X.	0.0000000	0.0000001	1.7777777	77
00000	006	177.011	174	TCJ	001	C.	J.12	0.0000002	1.6100307	1.6100307	77
00000	006	174.013	161	JUMP	307	C.	J.12	0.0000000	0.0000000	0.0000000	77
18200	006	161.323	161	SFX	000	F.4	X.	1.6050437	0.0000001	1.6050436	02
18300	006	161.324	160	SFX	006	F.5	X.	1.7400001	0.0000001	1.7400000	02
18430	006	160.326	160	JUMP	000	C.		0.0000000	0.0000000	0.0000000	02
18440	006	160.327	160	TJK	003	J.10	K.330	1.7777777	0.0000006	0.0000006	02
18500	006	160.333	175	TCF	001	C.	F.4	1.6100307	1.6050436	1.6050436	02
00000	006	175.335	174	JUMP	000	C.		0.0000000	0.0000000	0.0000000	77
00000	006	174.336	160	TBC	016	B.	C.337*	0.0000004	0.0000000	0.0000000	77
23200	006	160.355	160	TEK	002	E.	K.356	C.1000000	1.6000102	1.6000102	02
23320	006	160.360	160	TSK	001	S.	K.361	C.0000000	0.7000000	0.7000000	02
23340	006	160.362	160	TSK	001	S.	K.363	C.0000000	1.4400000	1.4400000	02
23360	006	160.364	161	JUMP	010	S.		0.0000000	0.0000000	0.0000000	02

ERR 00 00 00 02

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161.375

ERROR 00002 CARD

Contrails

C. COMPUTER RUN WITH HARDWARE PRECEDENCES AND CONNECTIONS SATISFIED

A run was made with a hardware precedence matrix and a connection matrix which were satisfied by the order of execution of automatic checkout program steps and by the requested connections. The precedence matrix and precedence link matrices were the following:

	<u>MATRIX</u>						<u>KFIRST</u>	<u>KSEC</u>
	COLUMN							
	1	2	3	4	5	6		
ROW	1	0	1	0	0	0	000001610124	000001610124
	2	0	0	1	0	0	000007550135	000007550135
	3	0	0	0	1	0	000013770131	000013770131
	4	0	0	0	0	1	000002600132	000002600132
	5	0	0	0	0	0	000000000136	000000000136
	6	0	0	0	0	0	000010000136	000010000136

The connection and connection link matrices were the following:

	<u>CONMAT</u>						<u>ACON</u>	<u>BCON</u>
	PRIME EQUIPMENT							
	1	2	3	4	5	6		
	1	0	1	0	0	0	000001610102	000001610102
	2	1	0	0	0	0	000007550103	000007550103
	3	1	0	0	0	0	000013770201	000013770201
	4	0	0	1	1	0	000002600205	000002600205
	5	0	1	0	0	0	000000000304	000000000304
	6	0	0	0	0	0	000010000404	000010000404

During the execution of the automatic checkout program, comments were written for precedences and connections satisfied, and the program terminated normally. The run is listed on the following pages.

* XEC
ENTRY POINTS TO SUBROUTINES REQUESTED FROM LIBRARY,
(FPT) EXIT (TSPM) (RTN) (STHM) (FIL) DUMP

PREPROCESSING TIME = 000.28 MIN.

EXECUTICN					
6	00000161C124	00000755C135	00001377C131	00000260C132	
	00000000C136	00010000C136			
	00000161G124	00000755C135	00001377G131	00000260C132	
	00000000C136	00010000C136			
	0 0 0 0 0 1 0 0 0 0 0 C 1 C 0 0 C C 1 C C C 0 C 1 0 0 0 0 0 1 0				
	0 1 1 0 0 0 1 0 0 0 1 0 C 0 C 1 C 0 C C 1 C C C 0 C 0 0 0 0 0 0 0				
	000000000000	000000000000	000000000000	000000000000	
	000000000000	000000000000			
	00000161C102	00000755C103	00001377G2G1	00000260C205	
	000000000304	00010000C404			

²CONSISTENT MATRIX

LABEL	REV	CHN	SEC	NC	OP	W/A	DEST	SRC	OLD DEST	SCORE	NEW DEST	TN	ERRORS
08700	001	166	111	166	BLFK	CC5	F-2	K-112	0.000000	0.000000	0.000000	02	
08700	001	166	111	166	BLFK	CC5	F-3	K-113	0.000000	0.000004	0.000004	02	
08700	001	166	111	166	BLFK	CC5	F-4	K-114	0.000000	1.670037	1.670037	02	
08700	001	166	111	166	BLFK	CC5	F-5	K-115	0.000000	0.020000	0.020000	02	
08700	001	166	111	166	BLFK	CC5	F-6	K-116	0.000000	0.000000	0.000000	02	
08706	001	166	117	166	BLJK	C10	J-CC	K-120	0.000000	0.2610477	0.2610477	02	
08706	001	166	117	166	BLJK	C10	J-C1	K-121	0.000000	0.2004500	0.2004500	02	
08706	001	166	117	166	BLJK	C10	J-C2	K-122	0.000000	0.0450103	0.0450103	02	
08706	001	166	117	166	BLJK	C10	J-C3	K-123	0.000000	0.5012330	0.5012330	02	
08706	001	166	117	166	BLJK	C10	J-C4	K-124	0.000000	0.1437714	0.1437714	02	
08706	001	166	117	166	BLJK	C10	J-C5	K-125	0.000000	0.000000	0.000000	02	
08706	001	166	117	166	BLJK	C10	J-C6	K-126	0.000000	0.000000	0.000000	02	ERR 41 CC CC CC
08715	001	166	130	160	JUMP	C72	J-C7	K-127	0.000000	0.000000	0.000000	02	ERR 41 CC CC CC
50000	001	160	222	160	TCF	C14	C-324*F-4		0.000000	1.670037	1.670037	02	
50200	001	160	240	160	TFZ	CC2	F-1	Z.	0.000000	0.000000	0.000000	02	
50300	001	160	243	160	TFK	C10	F-4	K-244	1.670037	1.670037	1.670037	02	
09800	001	160	254	160	TEK	CC1	E.	K-255	0.000000	1.600053	1.600053	02	
10000	001	160	256	C14	JUMP	141			0.000000	0.000000	0.000000	02	
51700	001	014	420	C14	JUMP	000			0.000000	0.000000	0.000000	02	
51800	001	014	421	014	TGE	CC1	C-C22*E.		0.000000	1.600053	1.600053	02	
52000	001	014	423	C14	REPT	017	C2C		0.000000	0.000000	0.000000	02	
52100	001	014	424	C14	TGJ	CC0	C-C25*J-05		0.000000	0.000000	0.000000	02	
52100	001	014	425	C14	TGJ	CC0	C-C26*J-06		0.000000	0.000000	0.000000	02	
52100	001	014	426	C14	TGJ	CC0	C-C27*J-07		0.000000	0.000000	0.000000	02	
52100	001	014	427	C14	TGJ	CC0	C-C30*J-10		0.000000	0.000000	0.000000	02	
52100	001	014	430	C14	TGJ	CC0	C-C31*J-11		0.000000	0.000000	0.000000	02	
52100	001	014	431	014	TGJ	CC0	C-C32*J-12		0.000000	0.000000	0.000000	02	
52100	001	014	432	C14	TGJ	CC0	C-C33*J-13		0.000000	0.000000	0.000000	02	
52100	001	014	433	C14	TGJ	CC0	C-C34*J-14		0.000000	0.000000	0.000000	02	
52100	001	014	434	014	TGJ	CC0	C-C35*J-15		0.000000	0.000000	0.000000	02	
52100	001	014	435	C14	TGJ	CC0	C-C36*J-16		0.000000	0.000000	0.000000	02	
52100	001	014	436	C14	TGJ	CC0	C-C37*J-17		0.000000	0.000000	0.000000	02	
52100	001	014	437	014	TGJ	CC0	C-C40*J-00		0.000000	0.2610477	0.2610477	02	
52100	001	014	440	C14	TGJ	CC0	C-C41*J-01		0.000000	0.2004500	0.2004500	02	
52100	001	014	441	014	TGJ	CC0	C-C42*J-02		0.000000	0.0450103	0.0450103	02	
52100	001	014	442	014	TGJ	CC0	C-C43*J-03		0.000000	0.5012330	0.5012330	02	
52100	001	014	443	014	TGJ	CC0	C-C44*J-04		0.000000	0.1437714	0.1437714	02	
52200	001	014	445	014	REPT	CC7	G1C		0.000000	0.000000	0.000000	02	
52300	001	014	446	014	TGF	CC0	C-C47*F-7		0.000000	0.000000	0.000000	02	
52300	001	014	447	014	TCF	CC0	C-C50*F-0		0.000000	0.000000	0.000000	02	
52300	001	014	450	C14	TCF	CC0	C-C51*F-1		0.000000	0.000000	0.000000	02	
52300	001	014	451	014	TCF	CC0	C-C52*F-2		0.000000	0.000000	0.000000	02	
52300	001	014	452	C14	TCF	CC0	C-C53*F-3		0.000000	0.000000	0.000000	02	
52300	001	014	453	014	TCF	CC0	C-C54*F-4		0.000000	1.6100456	1.6100456	02	
52300	001	014	454	C14	TCF	CC0	C-C55*F-5		0.020000	0.020000	0.020000	02	
52300	001	014	455	014	TCF	CC0	C-C56*F-6		0.000000	0.000000	0.000000	02	
52400	001	014	457	C14	REPT	CC6	CC7		0.000000	0.000000	0.000000	02	
52500	001	014	460	014	TOH	CC0	O-C61*H-01		0.000000	0.000000	0.000000	02	
52500	001	014	461	C14	TOH	CC0	O-C62*H-02		0.000000	0.000000	0.000000	02	
52500	001	014	462	C14	TOH	CC0	O-C63*H-03		0.000000	0.000000	0.000000	02	
52500	001	014	463	014	TOH	CC0	O-C64*H-04		0.000000	0.000000	0.000000	02	
52500	001	014	464	C14	TOH	CC0	O-C65*H-05		0.000000	0.000000	0.000000	02	

54300 002 014.C66 014 THX CCC H.C7 0.067* 0.000000 0.000000 0.000000 02
 54400 002 014.C67 014 JUMP CCC 0.000000 0.000000 0.000000 0.000000 02
 54500 002 014.C7C 014 THX CGO H.11 X. 0.000000 0.000000 0.000000 0.000000 02
 54600 002 014.C71 014 THX CGO H.12 X. 0.000000 0.000000 0.000000 0.000000 02
 54700 002 014.C72 014 THX CGO H.13 X. 0.000000 0.000000 0.000000 0.000000 02
 54800 002 014.C73 014 THX CGO H.14 X. 0.000000 0.000000 0.000000 0.000000 02
 54900 002 014.C74 014 THX CGO H.15 X. 0.000000 0.000000 0.000000 0.000000 02
 55000 002 014.C75 014 TBC CCC B. 3.777777 1.600053 1.600053 1.600053 02
 55100 002 014.C76 014 TDC CCC D. C. 0.000000 1.600053 1.600053 1.600053 02
 55200 002 014.C77 174 TEX CGO E. X. 1.600053 0.000000 0.000000 0.000000 02
 00000 002 174.1CC 160 JUMP 053 0.000000 0.000000 0.000000 0.000000 77
 160.154
 PRECEDENCE CK FCR START CF STEP
 CONNECTIONS CK
 160.154
 PRECEDENCE CK FCR END OF STEP
 CONNECTIONS CK

10300 002 160.154 160 TPX CG1 P.124 K.155 0.000000 0.1610124 0.1610124 0.1610124 02
 10500 002 160.156 160 REPT CG7 C1C 0.000000 0.000000 0.000000 0.000000 02
 10600 002 160.157 160 TDF CGO 0.000000 0.000000 0.000000 0.000000 02
 10600 002 160.16C 160 TCF CGC 0.260*F.0 0.000000 0.000000 0.000000 02
 10600 002 160.161 160 TDF CGC 0.261*F.1 0.000000 0.000000 0.000000 02
 10600 002 160.162 160 TCF CGC 0.262*F.2 0.000000 0.000000 0.000000 02
 10600 002 160.163 160 TCF CGC 0.263*F.3 0.000000 0.000000 0.000000 02
 10600 002 160.164 160 TCF CGC 0.264*F.4 0.000000 1.6100456 1.6100456 02
 10600 002 160.165 160 TCF CGC 0.265*F.5 0.000000 0.000000 0.000000 02
 10600 002 160.166 160 TDF CGO 0.266*F.6 0.000000 0.000000 0.000000 02
 10700 002 160.17C 160 JUMP 045 0.000000 0.000000 0.000000 0.000000 02
 10800 002 160.236 160 REPT C17 02C 0.000000 0.000000 0.000000 0.000000 02
 10900 002 160.237 160 TCJ CGO 0.340*J.00 0.000000 0.2610477 0.2610477 02
 10900 002 160.24C 160 TCJ CGO 0.341*J.01 0.000000 0.2004500 0.2004500 02
 10900 002 160.241 160 TOJ CGO 0.342*J.02 0.000000 0.0450103 0.0450103 02
 10900 002 160.242 160 TOJ CGO 0.343*J.03 0.000000 0.5012330 0.5012330 02
 10900 002 160.243 160 TOJ CGO 0.344*J.04 0.000000 0.1437714 0.1437714 02
 10900 002 160.244 160 TOJ CGO 0.345*J.05 0.000000 0.0000050 0.0000050 02
 10900 002 160.245 160 TOJ CGO 0.346*J.06 0.000000 0.0000000 0.0000000 02
 10900 002 160.246 160 TOJ CGO 0.347*J.07 0.000000 0.0000000 0.0000000 02
 10900 002 160.247 160 TOJ CGO 0.350*J.10 0.000000 0.0000000 0.0000000 02
 10900 002 160.250 160 TOJ CGO 0.351*J.11 0.000000 0.0000000 0.0000000 02
 10900 002 160.251 160 TCJ CGO 0.352*J.12 0.000000 0.0000000 0.0000000 02
 10900 002 160.252 160 TCJ CGO 0.353*J.13 0.000000 0.0000000 0.0000000 02
 10900 002 160.253 160 TCJ CGO 0.354*J.14 0.000000 0.0000000 0.0000000 02
 10900 002 160.254 160 TCJ CGO 0.355*J.15 0.000000 0.0000000 0.0000000 02
 10900 002 160.255 160 TCJ CGO 0.356*J.16 0.000000 0.0000000 0.0000000 02
 10900 002 160.256 160 TCJ CGO 0.357*J.17 0.000000 0.0000000 0.0000000 02
 11000 002 160.26C 160 JUMP 113 0.000000 0.000000 0.000000 0.000000 02
 160.374
 PRECEDENCE CK FCR START CF STEP
 CONNECTIONS CK
 160.374
 PRECEDENCE CK FCR END OF STEP
 CONNECTIONS CK

11300 002 160.374 160 TPX 001 P.135 K.375 0.000000 0.7550135 0.7550135 0.7550135 02
 160.376
 PRECEDENCE CK FCR START CF STEP
 CONNECTIONS CK
 160.377
 PRECEDENCE CK FCR START CF STEP
 CONNECTIONS CK
 160.377
 PRECEDENCE CK FCR START CF STEP
 CONNECTIONS CK
 160.377

52800	002	014.473	014	TGX	000	G.14	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	002	014.474	014	TGX	000	G.15	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	002	014.475	014	TGX	000	G.16	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	002	014.476	014	TGX	000	G.17	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.477	014	TGX	000	G.CC	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.478	014	TGX	000	G.C1	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.479	014	TGX	000	G.C2	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.480	014	TGX	000	G.C3	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.481	014	TGX	000	G.C4	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.482	014	TGX	000	G.C5	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.483	014	TGX	000	G.C6	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.484	014	TGX	000	G.C7	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.485	014	TGX	000	G.C8	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.486	014	TGX	000	G.C9	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.487	014	TGX	000	G.C10	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.488	014	TGX	000	G.C11	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.489	014	TGX	000	G.C12	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.490	014	TGX	000	G.C13	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.491	014	TGX	000	G.C14	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.492	014	TGX	000	H.16	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.493	014	TGX	000	H.17	X.	0.0000001	0.0000001	0.0000001	0.0000001	02
52800	003	014.494	014	TGX	000	C.	G.022*	1.6000000	1.6000000	1.6000000	1.6000000	02
52800	003	014.495	014	TGX	000	J.CC		0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.496	014	TGX	000	J.C5	C.025*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.497	014	TGX	000	J.C6	C.026*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.498	014	TGX	000	J.C7	C.027*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.499	014	TGX	000	J.C8	C.028*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.500	014	TGX	000	J.C9	C.029*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.501	014	TGX	000	J.C10	C.030*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.502	014	TGX	000	J.C11	C.031*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.503	014	TGX	000	J.C12	C.032*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.504	014	TGX	000	J.C13	C.033*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.505	014	TGX	000	J.C14	C.034*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.506	014	TGX	000	J.C15	C.035*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.507	014	TGX	000	J.C16	C.036*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.508	014	TGX	000	J.C17	C.037*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.509	014	TGX	000	J.CC	C.040*	0.2610477	0.2610477	0.2610477	0.2610477	02
52800	003	014.510	014	TGX	000	J.C1	C.041*	0.2004500	0.2004500	0.2004500	0.2004500	02
52800	003	014.511	014	TGX	000	J.C2	C.042*	0.0450103	0.0450103	0.0450103	0.0450103	02
52800	003	014.512	014	TGX	000	J.C3	C.043*	0.5012330	0.5012330	0.5012330	0.5012330	02
52800	003	014.513	014	TGX	000	J.C4	C.044*	0.1437714	0.1437714	0.1437714	0.1437714	02
52800	003	014.514	014	TGX	000	F.7	C.047*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.515	014	TGX	000	F.C	C.050*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.516	014	TGX	000	F.1	C.051*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.517	014	TGX	000	F.2	C.052*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.518	014	TGX	000	F.3	C.053*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.519	014	TGX	000	F.4	C.054*	1.6100456	1.6100456	1.6100456	1.6100456	02
52800	003	014.520	014	TGX	000	F.5	C.055*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.521	014	TGX	000	F.6	C.056*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.522	014	TGX	000	H.C1	0.061*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.523	014	TGX	000	H.C2	C.	1.6000000	1.6000000	1.6000000	1.6000000	02
52800	003	014.524	014	TGX	000	H.C3	0.063*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.525	014	TGX	000	H.C4	C.064*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.526	014	TGX	000	H.C5	0.065*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.527	014	TGX	000	H.C6	0.066*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.528	014	TGX	000	H.C7	0.067*	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.529	014	TGX	000	H.11	X.	0.0000000	0.0000000	0.0000000	0.0000000	02
52800	003	014.530	014	TGX	000	H.12	X.	0.0000000	0.0000000	0.0000000	0.0000000	02

19800	005	161.106	161	TGK	CCC	G.C7	K.107	0.000001	C.2000000	0.2000000	C2
19800	005	161.107	161	TGK	CCC	G.10	K.110	C.0000001	1.1400000	1.1400000	C2
19800	005	161.110	161	TGK	CCC	G.11	K.111	C.0000001	0.1000000	0.1000000	C2
19800	005	161.111	161	TGK	CCC	G.12	K.112	C.0000001	0.0400000	0.0400000	C2
19800	005	161.112	161	TGK	CCC	G.13	K.113	C.0000001	1.0000000	1.0000000	C2
19800	005	161.113	161	TGK	CCC	G.14	K.114	C.0000001	1.7562625	1.7562625	C2
19800	005	161.114	161	TGK	CCC	G.15	K.115	C.0000001	0.0000000	0.0000000	C2
19800	005	161.115	161	TGK	CCC	G.16	K.116	C.0000001	0.0000000	0.0000000	C2
19800	005	161.116	161	TGK	CCC	G.17	K.117	C.0000001	1.7642021	1.7642021	C2
19800	005	161.117	161	TGK	CCC	G.CC	K.120	C.0000001	0.0000007	0.0000007	C2
19800	005	161.120	161	TGK	000	G.C1	K.121	C.0000001	1.7670160	1.7670160	C2
19800	005	161.121	161	TGK	CCC	G.C2	K.122	C.0000001	1.7602011	1.7602011	C2
21200	005	161.123	161	REPT	C11	C12		C.0000000	0.0000000	0.0000000	C2
21300	005	161.124	161	THK	CCC	H.C5	K.125	C.0000000	0.0000000	0.0000000	C2
21300	005	161.125	161	THK	CCC	H.C6	K.126	C.0000000	0.0000000	0.0000000	C2
21300	005	161.126	161	THK	CCC	H.C7	K.127	C.0000000	1.7451161	1.7451161	C2
21300	005	161.127	161	THK	CCC	H.10	K.130	C.0000000	1.7767622	1.7767622	C2
21300	005	161.130	161	THK	CCC	H.11	K.131	C.0000001	0.0000000	0.0000000	C2
21300	005	161.131	161	THK	CCC	H.12	K.132	C.0000001	1.7451161	1.7451161	C2
21300	005	161.132	161	THK	CCC	H.13	K.133	C.0000001	1.7750020	1.7750020	C2
21300	005	161.133	161	THK	CCC	H.14	K.134	C.0000001	1.7702242	1.7702242	C2
21300	005	161.134	161	THK	CCC	H.15	K.135	C.0000001	0.0000000	0.0000000	C2
21300	005	161.135	161	THK	CCC	H.16	K.136	C.0000001	0.0000000	0.0000000	C2
22000	005	161.137	161	TDJ	002	D.	J.C0	1.6100000	1.6100000	1.6100000	C2
22100	005	161.142	161	TCF	CCC	C.	F.3	1.6100000	0.2610477	0.2610477	C2
22200	005	161.143	161	THK	CC1	H.C4	K.144	C.0000000	1.7767622	1.7767622	C2
00000	005	161.145	176	JUMP	C11	K.160	C.	C.0000000	0.0000000	0.0000000	C2
00000	005	176.161	176	ABJ	CCC	B.	J.C2	0.0000007	0.2610477	0.0000007	C2
00000	005	176.162	176	READ	C11	F.	K.164	C.0000000	0.0000002	0.0000011	C2
00000	005	176.174	175	SDX	CC5	D.	X.	C.0000000	0.0000000	0.0000000	C2
00000	005	175.176	175	TSE	CC1	D.	J.17	1.7777777	0.0000010	1.7777777	C2
00000	005	175.200	175	A EJ	001	E.	J.01	0.3400000	1.4000000	1.7400000	C2
00000	005	175.202	177	TSE	CC1	S.	E.	C.0000000	1.7400000	1.7400000	C2
00000	005	177.204	177	SJX	002	J.C5	X.	0.0000000	0.0000001	0.0000000	C2
00000	005	177.207	177	SJX	002	J.10	X.	0.0000000	0.0000001	0.0000000	C2
00000	005	177.212	177	TBC	000	B.	C.	C.0000011	0.2610477	0.2610477	C2
00000	005	177.213	177	RGHT	CC2	H.	B.	0.2610477	0.0000000	0.0000000	C2
00000	005	177.216	176	TCH	CCC	C.	B.	0.2610477	0.0000000	0.0000000	C2
00000	005	176.217	176	XTRC	CC1	K.220	C.	C.0000007	0.0000000	0.0000000	C2
00000	005	176.221	176	ABJ	CCC	B.	J.02	0.0000007	0.0000002	0.0000011	C2
00000	005	176.222	176	READ	C11	E.	K.224	0.0000011	0.0000000	0.0000000	C2
00000	005	176.234	175	SDX	CC5	D.	X.	0.0000010	0.0000000	0.0000000	C2
00000	005	175.242	177	TSE	CC1	S.	E.	C.0000000	0.0000000	0.0000000	C2
00000	005	177.244	177	SJX	CC2	J.C5	X.	0.0000001	0.0000001	0.0000000	C2
00000	005	177.247	177	SJX	002	J.10	X.	0.0000001	0.0000001	0.0000000	C2
00000	005	177.252	177	TBC	000	B.	C.	0.0000011	0.0000000	0.0000000	C2
00000	005	177.253	177	RGHT	CC2	B.	C.	0.0000000	0.0000000	0.0000000	C2
00000	005	177.256	176	TCH	CCC	C.	H.	0.0000000	0.0000000	0.0000000	C2
00000	005	176.257	176	XTRC	CC1	K.260	C.	0.0000007	0.0000000	0.0000000	C2
00000	005	176.261	176	ABJ	CCC	B.	J.02	0.0000004	0.0000002	0.0000006	C2
00000	005	176.262	176	READ	C11	E.	K.267	0.0000006	0.0000000	0.0000000	C2
00000	005	176.274	175	SDX	005	D.	X.	0.0000007	0.0000001	0.0000006	C2
00000	005	175.302	177	TSE	CC1	S.	E.	0.0000000	0.0000000	0.0000000	C2
00000	005	177.304	177	SJX	002	J.C5	X.	0.0000001	0.0000001	0.0000001	C2
00000	005	177.307	177	SJX	002	J.10	X.	0.0000001	0.0000001	0.0000001	C2
00000	005	177.312	177	TCH	CCC	B.	C.	0.0000000	0.0000000	0.0000000	C2

ERR 41 00 00 00
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00000	005	177.313	177	RGHT	002	B.	0.0022104	0.0000003	0.0002610	77
00000	005	177.216	176	TBR	000	C.	0.002610	0.0002610	0.0002610	77
00000	005	176.217	176	XTRC	001	K.320	0.0000007	0.0000000	0.0000000	77
00000	005	176.221	176	ABJ	000	B.	0.0000000	0.0000002	0.0000002	77
00000	005	176.222	176	READ	011	J.02	0.0000002	0.0000000	1.0000000	77
00000	005	176.224	175	SDX	005	K.333	0.0000006	0.0000000	0.0000000	77
00000	005	175.242	177	TSE	001	E.	0.0000000	0.0000000	0.0000000	77
00000	005	177.244	177	SJX	002	S.	0.0000000	1.0000000	1.0000000	77
00000	005	177.247	177	SJX	002	J.05 X.	0.0000001	0.0000000	0.0000000	77
00000	005	177.252	177	TBC	000	J.10 X.	0.0000003	0.0000001	0.0000002	77
00000	005	177.253	177	RGHT	002	C.	0.0000000	0.0000003	0.0002610	77
00000	005	177.256	176	TBR	000	B.	0.0002610	0.0000000	0.0002610	77
00000	005	176.257	176	XTRC	001	K.360	0.0000007	0.0000000	0.0000001	77
00000	005	176.261	176	ABJ	000	B.	0.0000001	0.0000002	0.0000000	77
00000	005	176.262	176	READ	011	J.02	0.0000003	0.0000000	0.0000000	77
00000	005	176.274	175	SDX	005	K.372	0.0000000	0.0000000	0.0000000	77
00000	005	175.402	177	TSE	001	X.	0.0000001	0.0000001	0.0000004	77
00000	005	177.404	177	SJX	002	E.	0.0000000	0.0000000	0.0000000	77
00000	005	177.407	177	SJX	002	J.05 X.	0.0000000	0.0000001	0.0000000	77
00000	005	177.412	177	TBC	000	J.10 X.	0.0000003	0.0000001	0.0000001	77
00000	005	177.412	177	RGHT	002	B.	0.0000000	0.0000000	0.0000000	77
00000	005	177.416	176	TBR	000	C.	0.0000003	0.0000000	0.0000000	77
00000	005	176.417	176	XTRC	001	K.420	0.0000000	0.0000000	0.0000000	77
00000	005	176.421	176	ABJ	000	B.	0.0000000	0.0000000	0.0000000	77
00000	005	176.422	176	READ	011	J.02	0.0000000	0.0000000	0.0000000	77
00000	005	176.434	175	SDX	005	K.425	0.0000000	0.0000000	0.0000000	77
00000	005	175.442	177	TSE	001	X.	0.0000000	0.0000001	0.0000000	77
00000	005	177.444	177	SJX	002	S.	0.0000000	0.0000000	0.0000000	77
00000	005	177.447	177	SJX	002	J.05 X.	0.0000001	0.0000000	0.0000000	77
00000	005	177.452	177	TBC	000	J.10 X.	0.0000000	0.0000000	0.0000000	77
00000	005	177.453	177	RGHT	002	B.	0.0000000	0.0000000	0.0000000	77
00000	005	177.456	176	TBR	000	C.	0.0000000	0.0000000	0.0000000	77
00000	005	176.457	176	XTRC	001	K.460	0.0000000	0.0000000	0.0000000	77
00000	005	176.461	176	ABJ	000	B.	0.0000000	0.0000000	0.0000000	77
00000	006	176.474	175	SDX	005	J.02	0.0000000	0.0000000	0.0000000	77
00000	006	175.002	177	TSE	001	K.471	0.0000000	0.0000000	0.0000000	77
00000	006	177.004	177	SJX	002	X.	0.0000000	0.0000000	0.0000000	77
00000	006	177.007	177	SJX	002	E.	0.0000000	0.0000000	0.0000000	77
00000	006	177.011	174	TCJ	001	J.05 X.	0.0000000	0.0000000	0.0000000	77
00000	006	174.012	161	JUMP	007	J.12	0.0000000	0.0000000	1.7777777	77
18200	006	161.222	161	SFX	000	F.4 X.	0.0000000	0.0000000	0.0000000	77
18300	006	161.224	160	SFX	006	F.5 X.	1.6000000	0.0000000	1.6000000	02
18430	006	160.326	160	JUMP	000	C.	0.0000000	0.0000000	0.0000000	02
18440	006	160.327	160	TJK	003	J.10	0.0000000	0.0000000	0.0000000	02
18500	006	160.332	175	TCF	001	C.	1.7400001	0.0000000	1.7400000	02
00000	006	175.235	174	JUMP	000	F.4	0.0000000	0.0000000	0.0000000	02
00000	006	174.330	160	TBC	016	B.	0.0000000	0.0000000	0.0000000	77
23200	006	160.355	160	TEK	002	E.	0.0000000	0.0000000	0.0000000	02
23320	006	160.360	160	TSK	001	S.	0.0000000	0.0000000	0.0000000	02
23340	006	160.362	160	TSK	001	S.	0.0000000	0.0000000	0.0000000	02
23360	006	160.364	161	JUMP	010	S.	0.0000000	0.0000000	0.0000000	02

00000

161.375

ERR 00 20 00 02

D. COMPUTER RUN WITH HARDWARE PRECEDENCES VIOLATED

A run was made with a hardware precedence matrix for which the order of execution of automatic checkout program steps violated the specified precedences. The precedence matrix and precedence link matrices were the following:

ROW	<u>MATRIX</u>						<u>KFIRST</u>	<u>KSEC</u>
	COLUMN							
	1	2	3	4	5	6		
	1	0	1	0	0	0	000001610124	000001610124
	2	0	0	0	1	0	000007550135	000007550135
	3	0	0	0	0	1	000013770131	000013770131
	4	0	0	1	0	0	000002600132	000002600132
	5	0	0	0	0	0	000000000136	000000000136
	6	0	0	0	0	0	000010000136	000010000136

The connection and connection link matrices were the following:

	<u>CONMAT</u>						<u>ACON</u>	<u>BCON</u>
	PRIME EQUIPMENT							
	1	2	3	4	5	6		
	1	0	1	0	0	0	000001610102	000001610102
AUTOMATIC	2	1	0	0	0	0	000007550103	000007550103
CHECKOUT	3	1	0	0	0	0	000013770201	000013770201
EQUIPMENT	4	0	0	1	1	0	000002600205	000002600205
	5	0	1	0	0	0	000000000304	000000000304
	6	0	0	0	0	0	000010000404	000010000404

The precedence constraint that step 4 must precede step 3 was violated by the attempted execution of step 3 before step 4. At that point in the execution of the program, the diagnostic, "ERROR NUMBER 4" (precedences violated), was written, and the program terminated. The run is listed on the following pages.

* XEC

ENTRY POINTS TO SUBROUTINES REQUESTED FROM LIBRARY, (FPT) EXIT (TSFM) (RTN) (STHW) (FIL) DUMP

PREPROCESSING TIME = 000.28 MIN.

EXECUTICA

```

6
00000161C124      00000755C135      00001377C131      00000260C132
00000000C136      00010000C136      00001377C131      00000260C132
00000161C124      00000755C135      00001377C131      00000260C132
00000000C136      00010000C136      00001377C131      00000260C132
0 0 0 0 1 0 0 C 0 0 C 0 C 1 0 0 C 1 C C C C C 1 0 0 C 0 0 0
0 1 1 0 0 1 0 C 0 1 0 C C 1 0 C C 1 C C C C 0 C 0 0 0 0 0
00000000C000      00000000C000      00000000C000      00000000C000
00000000C000      00000000C000      00000000C000      00000000C000
00000161C102      00000755C102      00001377C201      00000260C205
00000000C304      00010000C404

```

2 CONSISTENT MATRIX

LABEL	REV	CFA	SEC	NC	OP	K/W	DEST	SRC	CLD	DEST	SOURCE	NEW	DEST	FN	ERRORS
08700	001	166.111		166	BLFK	CC5	F.2	K.112	0.000000	0.000000	0.000000	0.000000	0.000000	02	
08700	001	166.111		166	BLFK	CC5	F.3	K.113	0.000000	0.000000	0.000000	0.000000	0.000000	02	
08700	001	166.111		166	BLFK	CC5	F.4	K.114	0.000000	0.000000	1.670000	1.670000	0.000000	02	
08700	001	166.111		166	BLFK	CC5	F.5	K.115	0.000000	0.000000	0.000000	0.000000	0.000000	02	
08700	001	166.111		166	BLFK	CC5	F.6	K.116	0.000000	0.000000	0.000000	0.000000	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.00	K.120	0.000000	0.000000	0.2610477	0.2610477	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.01	K.121	0.000000	0.000000	0.2004500	0.2004500	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.02	K.122	0.000000	0.000000	0.0450103	0.0450103	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.03	K.123	0.000000	0.000000	0.5012330	0.5012330	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.04	K.124	0.000000	0.000000	0.1437714	0.1437714	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.05	K.125	0.000000	0.000000	0.000000	0.000000	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.06	K.126	0.000000	0.000000	0.000000	0.000000	0.000000	02	
08706	001	166.117		166	BLJK	C10	J.07	K.127	0.000000	0.000000	0.000000	0.000000	0.000000	02	
08715	001	166.130		160	JUMP	C72			0.000000	0.000000	0.000000	0.000000	02		
50000	001	160.223		160	TCF	C14	G.324*F.4		0.000000	0.000000	1.6700037	1.6700037	0.000000	02	
50200	001	160.240		160	TFZ	CC2	F.1	Z.	0.000000	0.000000	0.000000	0.000000	0.000000	02	
50300	001	160.243		160	TEK	C10	F.4	K.244	1.670000	1.670000	1.6100456	1.6100456	0.000000	02	
09800	001	160.254		160	TEK	CC1	E.	K.255	0.000000	0.000000	1.6000053	1.6000053	0.000000	02	
10000	001	160.256		160	JUMP	141			0.000000	0.000000	0.000000	0.000000	0.000000	02	
51700	001	014.420		014	TCE	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
51800	001	014.421		014	TCE	CC1			0.000000	0.000000	1.6000053	1.6000053	0.000000	02	
52000	001	014.423		014	REPT	017			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.424		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.425		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.426		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.427		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.430		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.431		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.432		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.433		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.434		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.435		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.436		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.437		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.440		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.441		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.442		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.443		014	TGJ	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52100	001	014.445		014	REPT	CC7			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52200	001	014.446		014	TDF	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52300	001	014.447		014	TDF	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52300	001	014.450		014	TDF	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52300	001	014.451		014	TDF	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52300	001	014.452		014	TDF	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52300	001	014.453		014	TDF	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52300	001	014.454		014	TDF	CC0			0.000000	0.000000	1.61000456	1.61000456	0.000000	02	
52300	001	014.455		014	TDF	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52300	001	014.457		014	REPT	CC6			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52400	001	014.460		014	TGH	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52500	001	014.461		014	TGH	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52500	001	014.462		014	TGH	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52500	001	014.463		014	TGH	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	
52500	001	014.464		014	TGH	CC0			0.000000	0.000000	0.000000	0.000000	0.000000	02	

ERR 41 00 00 00
ERR 41 00 00 00

54300 002 014.C66 C14 THC CCC H.C7 C.C67* C.C000000 C.C000000 C2
 54400 002 014.C67 C14 JUMP CCC C.C000000 C.C000000 C2
 54500 002 014.C7C C14 THX CCC H.11 X. C.C000000 C.C000000 C2
 54600 002 014.C71 C14 THX CCC H.12 X. C.C000000 C.C000000 C2
 54700 002 014.C72 C14 THX CCC H.13 X. C.C000000 C.C000000 C2
 54800 002 014.C73 C14 THX CCC H.14 X. C.C000000 C.C000000 C2
 54900 002 014.C74 C14 THX CCC H.15 X. C.C000000 C.C000000 C2
 55000 002 014.C75 C14 TBC CCC B. 3.7777777 1.6000053 1.6000053 C2
 55100 002 014.C76 C14 TCC CCC D. C.C000000 C.C000000 C2
 55200 002 014.C77 174 TEX CCC E. 1.6000053 1.6000001 C2
 00000 002 174.L0C 1CC JUMP 553 C.C000000 C.C000000 C2
 160.154
 160.155
 PRECEDENCE CK FCR START CF STEP
 CONNECTICNS CK
 160.154
 PRECEDENCE CK FCR END OF STEP
 CONNECTICNS CK
 10300 002 16C.154 160 TPK C01 P.124 K.155 C.C000000 C.C000000 C2
 10500 002 16C.15C 16C REPT C07 C.C000000 C.C000000 C2
 10600 002 16C.157 160 TCF CCC C.260*F.C C.C000000 C.C000000 C2
 10660 002 16C.16C 160 TCF CCC C.261*F.1 C.C000000 C.C000000 C2
 10690 002 16C.161 160 TCF CCC C.262*F.2 C.C000000 C.C000000 C2
 10690 002 16C.162 160 TCF CCC C.263*F.3 C.C000000 C.C000000 C2
 10690 002 16C.163 160 TCF CCC C.264*F.4 C.C000000 C.C000000 C2
 10690 002 16C.164 160 TCF CCC C.265*F.5 C.C000000 C.C000000 C2
 10690 002 16C.165 160 TCF CCC C.266*F.6 C.C000000 C.C000000 C2
 10690 002 16C.166 160 TCF CCC C.267*F.7 C.C000000 C.C000000 C2
 10700 002 16C.17C 160 JUMP C45 C.C000000 C.C000000 C2
 10800 002 16C.236 16C REPT C17 C.C000000 C.C000000 C2
 10900 002 16C.237 160 TCU CCC C.240*J.00 C.C000000 C.C000000 C2
 10900 002 16C.24C 160 TCU CCC C.241*J.01 C.C000000 C.C000000 C2
 10900 002 16C.241 160 TCU CCC C.242*J.02 C.C000000 C.C000000 C2
 10900 002 16C.242 160 TCU CCC C.243*J.03 C.C000000 C.C000000 C2
 10900 002 16C.243 160 TCU CCC C.244*J.04 C.C000000 C.C000000 C2
 10900 002 16C.244 160 TCU CCC C.245*J.05 C.C000000 C.C000000 C2
 10900 002 16C.245 160 TCU CCC C.246*J.06 C.C000000 C.C000000 C2
 10900 002 16C.246 160 TCU CCC C.247*J.07 C.C000000 C.C000000 C2
 10900 002 16C.25C 160 TCU CCC C.250*J.10 C.C000000 C.C000000 C2
 10900 002 16C.251 160 TCU CCC C.251*J.11 C.C000000 C.C000000 C2
 10900 002 16C.252 160 TCU CCC C.252*J.12 C.C000000 C.C000000 C2
 10900 002 16C.253 160 TCU CCC C.253*J.13 C.C000000 C.C000000 C2
 10900 002 16C.254 160 TCU CCC C.254*J.14 C.C000000 C.C000000 C2
 10900 002 16C.255 160 TCU CCC C.255*J.15 C.C000000 C.C000000 C2
 10900 002 16C.256 160 TCU CCC C.256*J.16 C.C000000 C.C000000 C2
 11000 002 16C.26C 160 JUMP 113 C.257*J.17 C.C000000 C.C000000 C2

Contrails

E. COMPUTER RUN WITH INVALID CONNECTIONS

A run was made with a connection matrix for which the requested connections were invalid. The precedence matrix and precedence link matrices were the following:

	<u>MATRIX</u>						<u>KFIRST</u>	<u>KSEC</u>
	COLUMN							
	1	2	3	4	5	6		
ROW	1	1					000001610124	000001610124
	2		1				000007550135	000007550135
	3			1			000013770131	000013770131
	4				1		000002600132	000002600132
	5					1	000000000136	000000000136
	6						000010000136	000010000136

The connection and connection link matrices were the following:

	<u>CONMAT</u>						<u>ACON</u>	<u>BCON</u>
	PRIME EQUIPMENT							
	1	2	3	4	5	6		
AUTOMATIC	1	0	1	0	0	0	000001610102	000001610102
CHECKOUT	2	1	0	0	0	0	000007550103	000007550103
EQUIPMENT	3	1	0	0	0	0	000013770201	000013770201
	4	0	0	1	1	0	000002600205	000002600205
	5	0	1	0	0	0	000000000604	000000000604
	6	0	0	0	0	0	000010000404	000010000404

The connection 4-6, requested by the automatic checkout program, had a zero entry in the connection matrix, indicating that no connection existed. At that point in the execution of the program, the diagnostic, "ERROR NUMBER 11" (invalid connection), was written, and the program terminated. The run is listed on the following pages.

XEC

ENTRY POINTS TO SUBROUTINES REQUESTED FROM LIBRARY, (FPT) EXIT (TSPM) (RTN) (STHM) (FIL) DUMP

PREPROCESSING TIME = 000.28 MIN.

EXECUTION

```

6 00001610124 00007550135 000013770131 00000260132
00000000136 00010000136 000013770131 00000260132
00001610124 00007550135 000013770131 00000260132
00000000136 00010000136 000013770131 00000260132
00000000000 00000000000 00000000000 00000000000
00000000000 00000000000 00000000000 00000000000
00001610102 00007550132 000013770201 000002600205
00000000000 00000000000 00000000000 00000000000

```

2 CONSISTENT MATRIX

LABEL	REV	CHN	SEC	NC	OP	W/M	DEST	SRC	OLD DEST	SOURCE	NEW CLST	TN	ERRORS
08700	001	166	111	166	BLFK	CC5	F-2	K.112	C.0000000	0.0000200	0.0000000	02	
08700	001	166	111	166	BLFK	CC5	F-3	K.113	0.0000000	C.0000004	0.0000004	02	
08700	001	166	111	166	BLFK	CC5	F-4	K.114	0.0000000	1.6700037	1.6700037	02	
08700	001	166	111	166	BLFK	CC5	F-5	K.115	0.0000000	0.0200000	0.0200000	02	
08700	001	166	111	166	BLFK	CC5	F-6	K.116	0.0000000	0.0000000	0.0000000	02	
08706	001	166	117	166	BLJK	C10	J.CC	K.120	0.0000000	C.2610477	0.2610477	02	
08706	001	166	117	166	BLJK	C10	J.C1	K.121	0.0000000	0.2004500	0.2004500	02	
08706	001	166	117	166	BLJK	C10	J.C2	K.122	0.0000000	0.0450103	0.0450103	02	
08706	001	166	117	166	BLJK	C10	J.C3	K.123	0.0000000	0.5012330	0.5012330	02	
08706	001	166	117	166	BLJK	C10	J.C4	K.124	0.0000000	0.1437714	0.1437714	02	
08706	001	166	117	166	BLJK	C10	J.C5	K.125	0.0000000	0.0000000	0.0000000	02	
08706	001	166	117	166	BLJK	C10	J.C6	K.126	0.0000000	0.0000000	0.0000000	02	
08706	001	166	117	166	BLJK	C10	J.C7	K.127	0.0000000	0.0000000	0.0000000	02	
08715	001	166	130	160	JUMP	072			0.0000000	0.0000000	0.0000000	02	
50000	001	160	223	160	TGF	014	G.324*F.4		0.0000000	1.6700037	1.6700037	02	
50200	001	160	240	160	TFZ	002	F.1	Z.	0.0000000	0.0000000	0.0000000	02	
50300	001	160	243	160	TFK	010	F.4	K.244	1.6700037	1.6100456	1.6100456	02	
09800	001	160	254	160	TEK	001	E.	K.255	0.0000000	1.6000053	1.6000053	02	
10000	001	160	256	014	JUMP	141			0.0000000	0.0000000	0.0000000	02	
51700	001	014	420	014	TCE	001			0.0000000	0.0000000	0.0000000	02	
51800	001	014	421	014	TCE	001	G.022*E.		0.0000000	1.6000053	1.6000053	02	
52000	001	014	423	014	REPT	017	02C		0.0000000	0.0000000	0.0000000	02	
52100	001	014	424	014	TGJ	000	C.025*J.05		0.0000000	0.0000000	0.0000000	02	
52100	001	014	425	014	TGJ	000	C.026*J.06		0.0000000	0.0000000	0.0000000	02	
52100	001	014	426	014	TGJ	000	C.027*J.07		0.0000000	0.0000000	0.0000000	02	
52100	001	014	427	014	TGJ	000	C.030*J.10		0.0000000	0.0000000	0.0000000	02	
52100	001	014	430	014	TGJ	000	C.031*J.11		0.0000000	0.0000000	0.0000000	02	
52100	001	014	431	014	TGJ	000	C.032*J.12		0.0000000	0.0000000	0.0000000	02	
52100	001	014	432	014	TGJ	000	C.033*J.13		0.0000000	0.0000000	0.0000000	02	
52100	001	014	433	014	TGJ	000	C.034*J.14		0.0000000	0.0000000	0.0000000	02	
52100	001	014	434	014	TGJ	000	C.035*J.15		0.0000000	0.0000000	0.0000000	02	
52100	001	014	435	014	TGJ	000	C.036*J.16		0.0000000	0.0000000	0.0000000	02	
52100	001	014	436	014	TGJ	000	C.037*J.17		0.0000000	0.0000000	0.0000000	02	
52100	001	014	437	014	TGJ	000	C.040*J.00		0.0000000	0.2610477	0.2610477	02	
52100	001	014	440	014	TGJ	000	C.041*J.01		0.0000000	0.2004500	0.2004500	02	
52100	001	014	441	014	TGJ	000	C.042*J.02		0.0000000	0.0450103	0.0450103	02	
52100	001	014	442	014	TGJ	000	G.043*J.03		0.0000000	0.5012330	0.5012330	02	
52100	001	014	443	014	TGJ	000	C.044*J.04		0.0000000	0.1437714	0.1437714	02	
52200	001	014	445	014	REPT	007	01C		0.0000000	0.0000000	0.0000000	02	
52300	001	014	446	014	TGF	000	C.047*F.7		0.0000000	0.0000000	0.0000000	02	
52300	001	014	447	014	TGF	000	C.050*F.0		0.0000000	0.0000000	0.0000000	02	
52300	001	014	450	014	TGF	000	C.051*F.1		0.0000000	0.0000000	0.0000000	02	
52300	001	014	451	014	TGF	000	G.052*F.2		0.0000000	0.0000000	0.0000000	02	
52300	001	014	452	014	TGF	000	C.053*F.3		0.0000000	0.0000000	0.0000000	02	
52300	001	014	453	014	TGF	000	C.054*F.4		0.0000000	1.6100456	1.6100456	02	
52300	001	014	454	014	TGF	000	C.055*F.5		0.0000000	0.0200000	0.0200000	02	
52300	001	014	455	014	TGF	000	C.056*F.6		0.0000000	0.0000000	0.0000000	02	
52400	001	014	457	014	REPT	006	007		0.0000000	0.0000000	0.0000000	02	
52500	001	014	460	014	TCH	000	G.061*H.01		0.0000000	0.0000000	0.0000000	02	
52500	001	014	461	014	TCH	000	G.062*H.02		0.0000000	0.0000000	0.0000000	02	
52500	001	014	462	014	TCH	000	G.063*H.03		0.0000000	0.0000000	0.0000000	02	
52500	001	014	463	014	TCH	000	G.064*H.04		0.0000000	0.0000000	0.0000000	02	
52500	001	014	464	014	TCH	000	G.065*H.05		0.0000000	0.0000000	0.0000000	02	

ERR 41 00 00 00
ERR 41 00 00 00

PRECEDENCE CK FCR END OF STEP
CONNECTICNS CK
11500 002 160.376 160 TPK 0C1 P.131 K.377 C.0000000 1.3770131 1.3770131 02
11700 002 160.400 160 TEK 0C1 E. K.401 C.0000001 1.6000017 1.6000017 02
160.402
PRECEDENCE CK FCR START CF STEP
CONNECTICNS CK
160.403
160.402 160.403
PRECEDENCE CK FCR END OF STEP
CONNECTICNS CK
11900 002 160.402 160 TPK 0C4 P.132 K.403 C.0000000 0.2600132 0.2600132 02
160.407 160.410
PRECEDENCE CK FCR START CF STEP
ERRCR NUMBER 11

F. COMPUTER RUN WITH FLOW DIAGRAM PRECEDENCES SATISFIED

A run was made with a flow diagram precedence matrix which was satisfied by the order of execution of automatic checkout program steps. The precedence matrix and precedence link matrices were the following:

	<u>MATRIX</u>							<u>KFIRST</u>	<u>KSEC</u>
	COLUMN								
	1	2	3	4	5	6	7		
	1	0	1	0	0	0	0	000000166111	000000166111
	2	0	0	1	0	0	0	000000014420	000000014420
ROW	3	0	0	0	1	1	1	000000174100	000000174100
	4	0	-1	0	0	0	0	000000160154	000000160154
	5	0	-1	0	0	0	0	000000160120	000000150120
	6	0	0	0	0	0	1	000000161101	000000161101
	7	0	0	0	0	0	0	000000176157	000000176157

During execution of the automatic checkout program, comments were written for the precedences satisfied, and the program terminated normally. The run is listed on the following pages.

52800	003	014.005	014	TGX	000	G.06	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.006	014	TGX	000	G.07	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.007	014	TGX	000	G.10	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.010	014	TGX	000	G.11	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.011	014	TGX	000	G.12	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.012	014	TGX	000	G.15	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.013	014	TGX	000	G.14	X.	0.0000001	0.0000001	0.0000001	02
52900	003	014.015	014	THX	000	H.16	X.	0.0000001	0.0000001	0.0000001	02
53000	003	014.016	015	THX	000	H.17	X.	0.0000001	0.0000001	0.0000001	02
53100	003	015.021	014	TCC	001	C.	C.022*	1.6000017	1.6000017	1.6000017	02
53200	003	014.023	014	REPT	017	C2C		0.0000000	0.0000000	0.0000000	02
53300	003	014.024	014	TJC	000	J.05	0.025*	0.0000050	0.0000050	0.0000050	02
53300	003	014.025	014	TJC	000	J.06	C.026*	0.0000000	0.0000000	0.0000000	02
53300	003	014.026	014	TJC	000	J.07	0.027*	0.0000000	0.0000000	0.0000000	02
53300	003	014.027	014	TJC	000	J.10	0.030*	0.0000000	0.0000000	0.0000000	02
53300	003	014.030	014	TJC	000	J.11	C.031*	0.0000000	0.0000000	0.0000000	02
53300	003	014.031	014	TJC	000	J.12	C.032*	0.0000000	0.0000000	0.0000000	02
53300	003	014.032	014	TJC	000	J.13	0.033*	0.0000000	0.0000000	0.0000000	02
53300	003	014.033	014	TJC	000	J.14	C.034*	0.0000000	0.0000000	0.0000000	02
53300	003	014.034	014	TJC	000	J.15	0.035*	0.0000000	0.0000000	0.0000000	02
53300	003	014.035	014	TJC	000	J.16	C.036*	0.0000000	0.0000000	0.0000000	02
53300	003	014.036	014	TJC	000	J.17	C.037*	0.0000000	0.0000000	0.0000000	02
53300	003	014.037	014	TJC	000	J.00	C.040*	0.2610477	0.2610477	0.2610477	02
53300	003	014.040	014	TJO	000	J.01	C.041*	0.2004500	0.2004500	0.2004500	02
53300	003	014.041	014	TJC	000	J.02	C.042*	0.0450103	0.0450103	0.0450103	02
53300	003	014.042	014	TJC	000	J.03	C.043*	0.5012330	0.5012330	0.5012330	02
53300	003	014.043	014	TJC	000	J.04	C.044*	0.1437714	0.1437714	0.1437714	02
53400	003	014.045	014	JUMP	000			0.0000000	0.0000000	0.0000000	02
53500	003	014.046	014	BLFO	010	F.7	C.047*	0.0000000	0.0000000	0.0000000	02
53500	003	014.046	014	BLFO	010	F.0	0.050*	0.0000000	0.0000000	0.0000000	02
53500	003	014.046	014	BLFO	010	F.1	0.051*	0.0000000	0.0000000	0.0000000	02
53500	003	014.046	014	BLFO	010	F.2	C.052*	0.0000200	0.0000200	0.0000200	02
53500	003	014.046	014	BLFO	010	F.3	0.053*	0.0000004	0.0000004	0.0000004	02
53500	003	014.046	014	BLFO	010	F.4	C.054*	1.6100456	1.6100456	1.6100456	02
53500	003	014.046	014	BLFO	010	F.5	C.055*	0.0200000	0.0200000	0.0200000	02
53500	003	014.046	014	BLFO	010	F.6	0.056*	0.0000000	0.0000000	0.0000000	02
53600	003	014.057	014	JUMP	000			0.0000000	0.0000000	0.0000000	02
53700	003	014.060	014	THC	000	H.01	C.061*	0.0000000	0.0000000	0.0000000	02
53800	003	014.061	014	THC	000	H.02	C.	1.6000017	1.6000017	1.6000017	02
53900	003	014.062	014	THC	000	H.03	0.063*	0.0000000	0.0000000	0.0000000	02
54000	003	014.063	014	THC	000	H.04	C.064*	0.0000000	0.0000000	0.0000000	02
54100	003	014.064	014	THC	000	H.05	0.065*	0.0000000	0.0000000	0.0000000	02
54200	003	014.065	014	THC	000	H.06	C.066*	0.0000000	0.0000000	0.0000000	02
54300	003	014.066	014	THC	000	H.07	C.067*	0.0000000	0.0000000	0.0000000	02
54400	003	014.067	014	JUMP	000			0.0000000	0.0000000	0.0000000	02
54500	003	014.070	014	THX	000	H.11	X.	0.0000001	0.0000001	0.0000001	02
54600	003	014.071	014	THX	000	H.12	X.	0.0000001	0.0000001	0.0000001	02
54700	003	014.072	014	THX	000	H.13	X.	0.0000001	0.0000001	0.0000001	02
54800	003	014.073	014	THX	000	H.14	X.	0.0000001	0.0000001	0.0000001	02
54900	003	014.074	014	THX	000	H.15	X.	0.0000001	0.0000001	0.0000001	02
55000	003	014.075	014	TBC	000	B.	C.	3.7777777	1.6000017	1.6000017	02
55100	003	014.076	014	TDC	000	D.	C.	1.6000017	1.6000017	1.6000017	02
55200	003	014.077	014	TEX	000	E.	X.	1.6000017	1.6000017	1.6000017	02

174.100
PRECEDENCE CK FCR START CF STEP
174.100
PRECEDENCE CK FCR END OF STEP

PRECEDENCE CK FCR	PRECEDENCE CK FCR	003 174.10C	160 JUMP 017	0.0000000	0.0000000	0.0000000	0.0000000	0.0000000	77	ERR	41 00 00 00
160.120	160.10C	12500	160 XTRP 010	K.123 P.012	0.4000000	0.0000000	0.0000000	0.0000000	02		
PRECEDENCE CK FCR	START CF STEP	13100	160 TPX 001	P.136 K.137	0.0000000	1.0000000	1.0000000	1.0000000	02		
160.120	160.10C	13300	160 JUMP 434		0.0000000	0.0000000	0.0000000	0.0000000	02		
PRECEDENCE CK FCR	ENC OF STEP	13400	160 XTRP 004	K.C73 P.010	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	13800	160 TSK 003	S.	0.0000000	1.7400000	1.7400000	1.7400000	02		
160.120	160.10C	14200	160 JUMP 077		0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	14300	160 YDK 005	D.	1.6000000	1.5000000	1.5000000	1.5000000	02		
160.120	160.10C	14700	160 BLJK 017	J.10 K.210	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	14700	160 BLJK 017	J.11 K.211	0.0000000	1.5100000	1.5100000	1.5100000	02		
160.120	160.10C	14700	160 BLJK 017	J.12 K.212	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	14700	160 BLJK 017	J.13 K.213	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	14700	160 BLJK 017	J.14 K.214	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	14700	160 BLJK 017	J.15 K.215	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	14700	160 BLJK 017	J.16 K.216	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	14700	160 BLJK 017	J.17 K.217	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	14700	160 BLJK 017	J.CC K.220	0.2610477	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	14700	160 BLJK 017	J.C1 K.221	0.2004500	1.4000000	1.4000000	1.4000000	02		
160.120	160.10C	14700	160 BLJK 017	J.C2 K.222	0.0450103	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	14700	160 BLJK 017	J.C3 K.223	0.5012330	1.6030114	1.6030114	1.6030114	02		
160.120	160.10C	14700	160 BLJK 017	J.C4 K.224	0.1437714	1.6273000	1.6273000	1.6273000	02		
160.120	160.10C	14700	160 BLJK 017	J.C5 K.225	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	14700	160 BLJK 017	J.C6 K.226	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	15400	161 BLFK 010	F.C K.230	0.0000000	1.7573161	1.7573161	1.7573161	02		
160.120	160.10C	15400	161 BLFK 010	F.1 K.231	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	15400	161 BLFK 010	F.2 K.232	0.0000000	1.7727061	1.7727061	1.7727061	02		
160.120	160.10C	15400	161 BLFK 010	F.3 K.233	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	15400	161 BLFK 010	F.4 K.234	1.6100456	1.6050437	1.6050437	1.6050437	02		
160.120	160.10C	15400	161 BLFK 010	F.5 K.235	0.0000000	1.7400000	1.7400000	1.7400000	02		
160.120	160.10C	15400	161 BLFK 010	F.6 K.236	0.0000000	1.7552161	1.7552161	1.7552161	02		
160.120	160.10C	16000	160 TFD 000	F.1 D.	0.0000000	0.0000000	0.0000000	0.0000000	02	ERR	41 00 00 00
160.120	160.10C	16050	160 JUMP 020		0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	16100	160 TBC 000	B. J.263*	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	16200	160 ABX 002	B. X.	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	16300	160 READ 015	E. K.300	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	17600	160 XTRE 001	K.305 E.	1.7600777	1.6044077	1.6044077	1.6044077	02		
160.120	160.10C	17800	160 TJB 000	J.C7 B.	0.0000000	1.6000000	1.6000000	1.6000000	02		
160.120	160.10C	17900	160 SER 000	E. B.	1.6044077	1.6000000	1.6000000	1.6000000	02		
160.120	160.10C	18000	160 TSF 000	S. F.1	0.0000000	1.5000000	1.5000000	1.5000000	02		
160.120	160.10C	18030	160 TDZ 000	D. Z.	1.5000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	18070	160 TRE 000	B. E.	1.6000000	0.0044000	0.0044000	0.0044000	02		
160.120	160.10C	18100	160 RGFT 010	B. C.	0.0044000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	18400	160 TJB 006	J.C5 R.	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	18500	175 TCF 001	C. F.4	1.6000000	1.6050437	1.6050437	1.6050437	02		
160.120	160.10C	00000	174 JUMP 001		0.0000000	0.0000000	0.0000000	0.0000000	77		
160.120	160.10C	00000	160 TBC 017	B. C.34C*	0.0000000	0.2610477	0.2610477	0.2610477	77		
160.120	160.10C	19100	160 JUMP 012		0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	19200	160 TFB 000	F.3 D.	0.0000000	0.2610477	0.2610477	0.2610477	02		
160.120	160.10C	19300	161 TEK 003	E. K.374	1.6100000	1.6100000	1.6100000	1.6100000	02		
160.120	160.10C	19500	161 TJD 014	J.CC D.	0.0000000	0.0000000	0.0000000	0.0000000	02		
160.120	160.10C	19550	014 JUMP 003		0.0000000	0.0000000	0.0000000	0.0000000	02		
		14.400									

PRECEDENCE CK FCR START CF STEP
14.420

PRECEDENCE CK FCR	START CF STEP	END OF STEP	14.400	14.420
51700	004	014.420	C14 JUMP	CCC
51800	004	014.421	C14 TCE	CCI
52000	004	014.423	C14 REPT	J17
52100	004	014.424	C14 TOJ	CCC
52100	004	014.425	C14 TOJ	CCC
52100	004	014.426	C14 TOJ	CCC
52100	004	014.427	C14 TOJ	CCC
52100	004	014.430	C14 TOJ	CCC
52100	004	014.431	C14 TOJ	CCC
52100	004	014.432	C14 TOJ	CCC
52100	004	014.433	C14 TOJ	CCC
52100	004	014.434	C14 TOJ	CCC
52100	004	014.435	C14 TOJ	CCC
52100	004	014.436	C14 TOJ	CCC
52100	004	014.437	C14 TOJ	CCC
52100	004	014.440	C14 TOJ	CCC
52100	004	014.441	C14 TOJ	CCC
52100	004	014.442	C14 TOJ	CCC
52100	004	014.443	C14 TOJ	CCC
52200	004	014.445	C14 REPT	CG7
52300	004	014.446	C14 TCF	CCC
52300	004	014.447	C14 TCF	CCC
52300	004	014.450	C14 TCF	CCC
52300	004	014.451	C14 TCF	CCC
52300	004	014.452	C14 TCF	CCC
52300	004	014.453	C14 TCF	CCC
52300	004	014.454	C14 TCF	CCC
52300	004	014.455	C14 TCF	CCC
52400	004	014.457	C14 REPT	CG6
52500	004	014.461	C14 TGH	CCC
52500	004	014.462	C14 TGF	CCC
52500	004	014.463	C14 TGF	CCC
52500	004	014.464	C14 TGH	CCC
52500	004	014.465	C14 TGF	CCC
52500	004	014.466	C14 TGF	CCC
52600	004	014.470	C14 JUMP	CG1
52700	004	014.472	C14 REPT	CG2
52800	004	014.473	C14 TGH	CCC
52800	004	014.474	C14 TGH	CCC
52800	004	014.475	C14 TGH	CCC
52800	004	014.476	C14 TGH	CCC
52800	005	014.477	C14 TGH	CCC
52800	005	014.480	C14 TGH	CCC
52800	005	014.482	C14 TGH	CCC
52800	005	014.483	C14 TGH	CCC
52800	005	014.484	C14 TGH	CCC
52800	005	014.485	C14 TGH	CCC
52800	005	014.486	C14 TGH	CCC
52800	005	014.487	C14 TGH	CCC
52800	005	014.488	C14 TGH	CCC
52800	005	014.489	C14 TGH	CCC
52800	005	014.490	C14 TGH	CCC
52800	005	014.491	C14 TGH	CCC
52800	005	014.492	C14 TGH	CCC
52800	005	014.493	C14 TGH	CCC
52800	005	014.494	C14 TGH	CCC
52800	005	014.495	C14 TGH	CCC
52800	005	014.496	C14 TGH	CCC
52800	005	014.497	C14 TGH	CCC
52800	005	014.498	C14 TGH	CCC
52800	005	014.499	C14 TGH	CCC
52800	005	014.500	C14 TGH	CCC

52800	005	014.C13	C14	TX	CCC	G.14	X.	0.000000	0.000000	0.000000	02
52900	005	014.C15	C14	THX	CCC	H.16	X.	0.000000	0.000000	0.000000	02
53000	005	014.C16	C15	THX	CCC	H.17	X.	0.000000	0.000000	0.000000	02
53100	005	015.C21	C14	TCC	CCC	C.	C.022*	1.605437	1.610000	1.610000	02
53200	005	014.C23	C14	REPT	017	02C	C.	0.000000	0.000000	0.000000	02
53300	005	014.C24	C14	TJC	CCC	J.C5	C.025*	0.000000	0.000000	0.000000	02
53300	005	014.C25	C14	TJC	CCC	J.C6	C.026*	0.000000	0.000000	0.000000	02
53300	005	014.C26	C14	TJC	CCC	J.C7	C.027*	1.600077	1.600077	1.600077	02
53300	005	014.C30	C14	TJC	CCC	J.10	C.030*	0.000000	0.000000	0.000000	02
53300	005	014.C31	C14	TJC	CCC	J.11	C.031*	0.000000	0.000000	0.000000	02
53300	005	014.C32	C14	TJC	CCC	J.12	C.032*	1.6100307	1.6100307	1.6100307	02
53300	005	014.C33	C14	TJC	CCC	J.13	C.033*	0.000000	0.000000	0.000000	02
53300	005	014.C34	C14	TJC	CCC	J.14	C.034*	0.000000	0.000000	0.000000	02
53300	005	014.C35	C14	TJC	CCC	J.15	C.035*	0.000000	0.000000	0.000000	02
53300	005	014.C36	C14	TJC	CCC	J.16	C.036*	0.000000	0.000000	0.000000	02
53300	005	014.C37	C14	TJC	CCC	J.17	C.037*	0.000000	0.000000	0.000000	02
53300	005	014.C40	C14	TJC	CCC	J.CC	C.040*	0.000000	0.000000	0.000000	02
53300	005	014.C41	C14	TJC	CCC	J.C1	C.041*	1.400000	1.400000	1.400000	02
53300	005	014.C42	C14	TJC	CCC	J.C2	C.042*	0.000000	0.000000	0.000000	02
53300	005	014.C43	C14	TJC	CCC	J.C3	C.043*	1.6030114	1.6030114	1.6030114	02
53300	005	014.C44	C14	TJC	CCC	J.C4	C.044*	1.6273000	1.6273000	1.6273000	02
53400	005	014.C45	C14	JUMP	CCC			0.000000	0.000000	0.000000	02
53500	005	014.C46	C14	BLFC	010	F.7	C.047*	0.000000	0.000000	0.000000	02
53500	005	014.C46	C14	BLFC	010	F.8	C.05*	1.7573161	1.7573161	1.7573161	02
53500	005	014.C46	C14	BLFC	010	F.1	C.051*	1.5000000	1.5000000	1.5000000	02
53500	005	014.C46	C14	BLFC	010	F.2	C.052*	1.7727061	1.7727061	1.7727061	02
53500	005	014.C46	C14	BLFC	010	F.3	C.053*	0.2610477	0.2610477	0.2610477	02
53500	005	014.C46	C14	BLFC	010	F.4	C.054*	1.6050437	1.6050437	1.6050437	02
53500	005	014.C46	C14	BLFC	010	F.5	C.055*	1.7400001	1.7400001	1.7400001	02
53500	005	014.C46	C14	BLFC	010	F.6	C.056*	1.7552161	1.7552161	1.7552161	02
53600	005	014.C57	C14	JUMP	CCC			0.000000	0.000000	0.000000	02
53700	005	014.C60	C14	THC	CCC	H.C1	C.061*	0.000000	0.000000	0.000000	02
53800	005	014.C61	C14	THC	CCC	H.C2	C.	1.600017	1.610000	1.610000	02
53900	005	014.C62	C14	THC	CCC	H.C3	C.063*	0.000000	0.000000	0.000000	02
54000	005	014.C63	C14	THC	CCC	H.C4	C.064*	0.000000	0.000000	0.000000	02
54100	005	014.C64	C14	THC	CCC	H.C5	C.065*	0.000000	0.000000	0.000000	02
54200	005	014.C65	C14	THC	CCC	H.C6	C.066*	0.000000	0.000000	0.000000	02
54300	005	014.C66	C14	THC	CCC	H.C7	C.067*	0.000000	0.000000	0.000000	02
54400	005	014.C67	C14	JUMP	CCC			0.000000	0.000000	0.000000	02
54500	005	014.C70	C14	THX	CCC	H.11	X.	0.000000	0.000000	0.000000	02
54600	005	014.C71	C14	THX	CCC	H.12	X.	0.000000	0.000000	0.000000	02
54700	005	014.C71	C14	THX	CCC	H.13	X.	0.000000	0.000000	0.000000	02
54800	005	014.C73	C14	THX	CCC	H.14	X.	0.000000	0.000000	0.000000	02
54900	005	014.C74	C14	THX	CCC	H.15	X.	0.000000	0.000000	0.000000	02
55000	005	014.C75	C14	TBC	CCC	B.	C.	3.7777777	1.610000	1.610000	02
55100	005	014.C76	C14	TDC	CCC	D.	C.	0.000000	1.610000	1.610000	02
55200	005	014.C77	C14	TEX	CCC	E.	X.	1.610000	0.000000	0.000000	02
174.100		174.100									
PRECEDENCE CK FCR START CF STEP											
174.100		174.100									
PRECEDENCE CK FCR ENC OF STEP											
00000		005 174.100	161	JUMP	CCC			0.000000	0.000000	0.000000	77
161.101		161.100									
PRECEDENCE CK FCR START CF STEP											
161.101		161.100									
PRECEDENCE CK FCR ENC OF STEP											
19700		005 161.101	161	REPT	017	02C		0.000000	0.000000	0.000000	02

00000	005	176.257	176 XTRC	CC1	K.260 C.	C.000007	C.0026104	0.000004	77
00000	005	176.261	176 ABJ	CC0	B.	0.000004	0.0000002	0.000006	77
00000	005	176.262	176 READ	011	E. K.267	0.000006	0.0000005	0.2000000	77
00000	005	176.274	175 SDX	CC5	D. X.	0.000007	0.0000001	0.000006	77
00000	005	175.302	177 TSE	CC1	S. E.	0.000000	0.2000000	0.2000000	77
00000	005	177.304	177 SJX	CC2	J.05 X.	0.0000042	0.0000001	0.0000041	77
00000	005	177.307	177 SJX	CC2	J.10 X.	0.0000004	0.0000001	0.0000003	77
00000	005	177.312	177 TBC	CC0	B.	0.0000006	0.0026104	0.0000004	77
00000	005	177.313	177 RGT	CC2	B.	0.0026104	0.0000003	0.0000003	77
00000	005	177.316	176 TCB	CC0	C.	0.0026104	0.0000003	0.0000003	77
00000	005	177.317	176 XTRC	CC1	K.320 C.	0.000007	0.0000001	0.0000000	77
00000	005	176.321	176 ABJ	CC0	B.	0.0000002	0.0000002	0.0000000	77
00000	005	176.322	176 READ	011	E. J.02	0.0000002	0.0000002	0.0000000	77
00000	005	176.334	175 SDX	CC5	E. K.333	0.0000002	0.0000000	1.0000000	77
00000	005	175.342	177 TSE	CC1	D. X.	0.0000000	0.0000001	0.0000005	77
00000	005	177.344	177 SJX	CC2	S. E.	0.0000000	1.0000000	1.0000000	77
00000	005	177.347	177 SJX	CC2	J.05 X.	0.0000041	0.0000000	0.0000000	77
00000	005	177.352	177 TBC	CC0	J.10 X.	0.0000003	0.0000001	0.0000002	77
00000	005	177.353	177 RGT	CC2	B.	0.0000002	0.0000002	0.0000000	77
00000	005	177.356	176 TCB	CC0	C.	0.0000002	0.0000000	0.0000000	77
00000	005	176.357	176 XTRC	CC1	B.	0.0000000	0.0000003	0.0000000	77
00000	005	176.361	176 ABJ	CC0	K.360 C.	0.0000007	0.0000001	0.0000001	77
00000	005	176.362	176 READ	011	B.	0.0000001	0.0000002	0.0000000	77
00000	005	176.374	175 SDX	CC5	E. K.372	0.0000003	0.0000000	0.0000000	77
00000	005	175.402	177 TSE	CC1	D. X.	0.0000005	0.0000001	0.0000004	77
00000	005	177.404	177 SJX	CC2	S. E.	0.0000000	0.0000000	0.0000000	77
00000	005	177.407	177 SJX	CC2	J.05 X.	0.0000040	0.0000001	0.0000003	77
00000	005	177.412	177 TBC	CC0	J.10 X.	0.0000002	0.0000001	0.0000001	77
00000	005	177.413	177 RGT	CC2	B.	0.0000002	0.0000001	0.0000001	77
00000	005	177.416	176 TCB	CC0	C.	0.0000003	0.0000001	0.0000001	77
00000	005	176.417	176 XTRC	CC0	B.	0.0000007	0.0000002	0.0000002	77
00000	005	176.421	176 ABJ	CC0	K.420 C.	0.0000006	0.0000002	0.0000000	77
00000	005	176.422	176 READ	011	B.	0.0000010	0.0000000	0.0000000	77
00000	005	176.434	175 SDX	CC5	E. K.425	0.0000000	0.0000000	1.0000000	77
00000	005	175.442	177 TSE	CC1	D. X.	0.0000004	0.0000000	0.0000000	77
00000	005	177.444	177 SJX	CC2	S. E.	0.0000000	1.0000000	1.0000000	77
00000	005	177.447	177 SJX	CC2	J.05 X.	0.0000037	0.0000001	0.0000003	77
00000	005	177.452	177 TBC	CC0	J.10 X.	0.0000001	0.0000001	0.0000000	77
00000	005	177.453	177 RGT	CC2	B.	0.0000000	0.0000002	0.0000000	77
00000	005	177.456	176 TCB	CC0	C.	0.0000002	0.0000000	0.0000000	77
00000	005	176.457	176 XTRC	CC1	K.460 C.	0.0000002	0.0000002	0.0000002	77
00000	005	176.461	176 ABJ	CC0	B.	0.0000002	0.0000000	0.0000000	77
00000	006	176.462	176 READ	011	E. J.02	0.0000004	0.0000000	0.0000000	77
00000	006	175.002	175 SDX	CC5	D. X.	0.0000003	0.0000001	0.0000002	77
00000	006	177.004	177 SJX	CC2	S. E.	0.0000000	0.1000000	0.1000000	77
00000	006	177.007	177 SJX	CC2	J.05 X.	0.0000036	0.0000001	0.0000003	77
00000	006	177.011	174 TCB	CC0	J.10 X.	0.0000000	0.0000001	1.7777777	77
00000	006	174.012	161 JUMP	307	C. J.12	0.0000002	1.6100307	1.6100307	77
00000	006	161.323	161 SFX	CC0	F.4 X.	0.0000000	0.0000000	0.0000000	77
18200	006	161.324	160 SFX	CC6	F.5 X.	1.6050437	0.0000001	1.6050436	02
18300	006	160.326	160 JUMP	CC0	C.	0.0000000	0.0000001	1.7400000	02
18440	006	160.327	160 TJK	003	J.10 K.330	1.7777777	0.0000000	0.0000000	02
18500	006	160.332	175 TCF	CC1	C. F.4	1.6100307	1.6050436	1.6050436	02
00000	006	175.335	174 JUMP	CC0	B.	0.0000000	0.0000000	0.0000000	77
00000	006	174.236	160 TBC	016	B. K.337*	0.0000004	0.0000000	0.0000000	77
23200	006	160.355	160 TEK	002	E. K.356	0.1000000	1.6000102	1.6000102	02

Contrails

23320	006	160.360	160	TSK	CC1	S.	K.361	0.000000	0.700000	02
23340	006	160.362	160	TSK	CC1	S.	K.363	0.000000	1.440000	02
23360	006	160.364	161	JUMP	G1C			0.000000	0.000000	02
C0000		161.375								ERR 00 00 00 02

ERRCR 000002 CARD

G. COMPUTER RUN WITH FLOW DIAGRAM PRECEDENCES VIOLATED

A run was made with a flow diagram precedence matrix for which the order of execution of automatic checkout program steps violated the specified precedences. The precedence matrix and precedence link matrices were the following:

	<u>MATRIX</u>							<u>KFIRST</u>	<u>KSEC</u>
	COLUMN								
	1	2	3	4	5	6	7		
	1	0	1	0	0	0	0	000000166111	000000166111
	2	0	0	1	0	0	0	000000014420	000000014420
	3	0	0	0	1	1	1	000000174100	000000174100
ROW	4	0	-1	0	0	0	0	000000160154	000000160154
	5	0	-1	0	0	0	0	000000160120	000000160120
	6	0	0	0	0	0	0	000000161101	000000161101
	7	0	0	0	0	0	1	000000176157	000000176157

The precedence constraint that step 7 must precede step 6 was violated by the attempted execution of step 6 before step 7. At that point in the execution of the program, the diagnostic, "ERROR NUMBER 4" (precedences violated), was written, and the program was terminated. The run is listed on the following pages.

TN ERRORS

LABEL	REV	CFN	SEC	NC	OP	W/M	DEST	SRC	OLD DEST	SOURCE	NEW DEST	TN	ERRORS
166.111	0												
PRECEDENCE CK FCR	START	CF	STEP										
166.111	166.												
PRECEDENCE CK FCR	ENC	OF	STEP										
08700	001	166.111		166	BLFK	0G5	F.2	K.112	0.0000000	0.0000200	0.0000200	02	
08700	001	166.111		166	BLFK	0G5	F.3	K.113	0.0000000	0.0000004	0.0000004	02	
08700	001	166.111		166	BLFK	005	F.4	K.114	0.0000000	1.6700037	1.6700037	02	
08700	001	166.111		166	BLFK	005	F.5	K.115	0.0000000	0.0200000	0.0200000	02	
08700	001	166.111		166	BLFK	0G5	F.6	K.116	0.0000000	0.0000000	0.0000000	02	
08706	001	166.117		166	BLJK	010	J.CC	K.120	0.0000000	0.2610477	0.2610477	02	
08706	001	166.117		166	BLJK	010	J.C1	K.121	0.0000000	0.2004500	0.2004500	02	
08706	001	166.117		166	BLJK	010	J.C2	K.122	0.0000000	0.0450103	0.0450103	02	
08706	001	166.117		166	BLJK	010	J.C3	K.123	0.0000000	0.5012330	0.5012330	02	
08706	001	166.117		166	BLJK	010	J.C4	K.124	0.0000000	0.1437714	0.1437714	02	
08706	001	166.117		166	BLJK	010	J.C5	K.125	0.0000000	0.0000050	0.0000050	02	
08706	001	166.117		166	BLJK	010	J.C6	K.126	0.0000000	0.0000000	0.0000000	02	
08706	001	166.117		166	BLJK	010	J.C7	K.127	0.0000000	0.0000000	0.0000000	02	
08715	001	166.13C		160	JUMP	C72			0.0000000	0.0000000	0.0000000	02	
50000	001	16C.223		160	TOF	014	C.324*F.4		0.0000000	1.6700037	1.6700037	02	
5C200	001	16C.24C		160	TFZ	002	F.1	Z.	0.0000000	0.0000000	0.0000000	02	
5C300	001	16C.243		160	TFK	010	F.4	K.244	1.6700037	1.6100456	1.6100456	02	
09800	001	16C.254		160	TEK	001	E.	K.255	0.0000000	1.6000053	1.6000053	02	ERR
10000	001	16C.256		141	JUMP	141			0.0000000	0.0000000	0.0000000	02	ERR
14.420													41 00 00 00
PRECEDENCE CK FCR	START	CF	STEP										41 00 00 00
14.420													ERR
PRECEDENCE CK FCR	ENC	OF	STEP										
51700	001	014.42C		014	JUMP	0C0			0.0000000	0.0000000	0.0000000	02	
51800	001	014.421		014	TGE	0C1			0.0000000	1.6000053	1.6000053	02	
52000	001	014.423		014	REPT	017			0.0000000	0.0000000	0.0000000	02	
52100	001	014.424		014	TOJ	0CC			0.0000000	0.0000050	0.0000050	02	
52100	001	014.425		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.426		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.427		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.43C		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.431		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.432		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.433		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.434		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.435		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.436		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.437		014	TOJ	0CC			0.0000000	0.0000000	0.0000000	02	
52100	001	014.44C		014	TOJ	0CC			0.0000000	0.2610477	0.2610477	02	
52100	001	014.441		014	TOJ	0CC			0.0000000	0.2004500	0.2004500	02	
52100	001	014.442		014	TOJ	0CC			0.0000000	0.0450103	0.0450103	02	
52100	001	014.443		014	TOJ	0CC			0.0000000	0.5012330	0.5012330	02	
52200	001	014.445		014	REPT	0C7			0.0000000	0.1437714	0.1437714	02	
52300	001	014.446		014	TOF	000			0.0000000	0.0000000	0.0000000	02	
52300	001	014.447		014	TOF	000			0.0000000	0.0000000	0.0000000	02	
52300	001	014.45C		014	TOF	000			0.0000000	0.0000000	0.0000000	02	
52300	001	014.451		014	TOF	000			0.0000000	0.0000200	0.0000200	02	
52300	001	014.452		014	TOF	000			0.0000000	0.0000004	0.0000004	02	
52300	001	014.453		014	TOF	000			0.0000000	1.6100456	1.6100456	02	

53500	002 014.C46	C14 BLFC 010	F.6	C-.056*	0.0000000	0.0000000	0.0000000	02
53600	002 014.C57	014 JUMP 000			0.0000000	0.0000000	0.0000000	02
53700	002 014.C60	C14 THC 000	H.C1	0.061*	0.0000000	0.0000000	0.0000000	02
53800	002 014.C61	014 THC 000	H.C2	C.	0.0000000	1.6000053	0.0000000	02
53900	002 014.C62	014 THC 000	H.C3	0.063*	0.0000000	0.0000000	0.0000000	02
54000	002 014.C63	014 THC 000	H.C4	0.064*	0.0000000	0.0000000	0.0000000	02
54100	002 014.C64	014 THC 000	H.C5	C.095*	0.0000000	0.0000000	0.0000000	02
54200	002 014.C65	014 THC 000	H.C6	0.066*	0.0000000	0.0000000	0.0000000	02
54300	002 014.C66	014 THC 000	H.C7	0.067*	0.0000000	0.0000000	0.0000000	02
54400	002 014.C67	014 JUMP 000			0.0000000	0.0000000	0.0000000	02
54500	002 014.C70	014 THX 000	H.11	X.	0.0000000	0.0000001	0.0000001	02
54600	002 014.C71	014 THX 000	H.12	X.	0.0000000	0.0000001	0.0000001	02
54700	002 014.C72	014 THX 000	H.13	X.	0.0000000	0.0000001	0.0000001	02
54800	002 014.C73	014 THX 000	H.14	X.	0.0000000	0.0000001	0.0000001	02
54900	002 014.C74	014 THX 000	H.15	X.	0.0000000	0.0000001	0.0000001	02
55000	002 014.C75	014 TBC 000	B.	C.	3.7777777	1.6000053	1.6000053	02
55100	002 014.C76	014 TDC 000	D.	C.	0.0000000	1.6000053	1.6000053	02
55200	002 014.C77	174 TEX 000	E.	X.	0.0000000	0.0000001	0.0000001	02
	174.100							
	PRECEDENCE CK FCR START CF STEP							
	174.100							
	PRECEDENCE CK FCR END OF STEP							
	00000	002 174.100			0.0000000	0.0000000	0.0000000	77
	160.154							
	PRECEDENCE CK FCR START CF STEP							
	160.154							
	PRECEDENCE CK FCR END CF STEP							
10300	002 160.154	160 TPK 001	P.124	K.155	0.0000000	0.1610124	0.1610124	02
10500	002 160.156	160 REPT 007	G10		0.0000000	0.0000000	0.0000000	02
10600	002 160.157	160 TOF 000	0.260*	F.0	0.0000000	0.0000000	0.0000000	02
10600	002 160.160	160 TOF 000	0.261*	F.1	0.0000000	0.0000000	0.0000000	02
10600	002 160.161	160 TOF 000	0.262*	F.2	0.0000000	0.0000200	0.0000200	02
10600	002 160.162	160 TOF 000	0.263*	F.3	0.0000000	0.0000004	0.0000004	02
10600	002 160.163	160 TCF 000	0.264*	F.4	0.0000000	1.6100456	1.6100456	02
10600	002 160.164	160 TCF 000	0.265*	F.5	0.0000000	0.0200000	0.0200000	02
10600	002 160.165	160 TCF 000	0.266*	F.6	0.0000000	0.0000000	0.0000000	02
10600	002 160.166	160 TCF 000	0.267*	F.7	0.0000000	0.0000000	0.0000000	02
10700	002 160.170	160 JUMP 045			0.0000000	0.0000000	0.0000000	02
10800	002 160.236	160 REPT 017	C20		0.0000000	0.0000000	0.0000000	02
10900	002 160.237	160 TOJ 000	0.340*	J.00	0.0000000	0.2610477	0.2610477	02
10900	002 160.240	160 TOJ 000	0.341*	J.01	0.0000000	0.2004500	0.2004500	02
10900	002 160.241	160 TOJ 000	0.342*	J.02	0.0000000	0.0450103	0.0450103	02
10900	002 160.242	160 TOJ 000	0.343*	J.03	0.0000000	0.5012330	0.5012330	02
10900	002 160.243	160 TOJ 000	0.344*	J.04	0.0000000	0.1437714	0.1437714	02
10900	002 160.244	160 TOJ 000	0.345*	J.05	0.0000000	0.0000050	0.0000050	02
10900	002 160.245	160 TOJ 000	0.346*	J.06	0.0000000	0.0000000	0.0000000	02
10900	002 160.246	160 TOJ 000	0.347*	J.07	0.0000000	0.0000000	0.0000000	02
10900	002 160.247	160 TOJ 000	0.350*	J.10	0.0000000	0.0000000	0.0000000	02
10900	002 160.250	160 TOJ 000	0.351*	J.11	0.0000000	0.0000000	0.0000000	02
10900	002 160.251	160 TOJ 000	0.352*	J.12	0.0000000	0.0000000	0.0000000	02
10900	002 160.252	160 TOJ 000	0.353*	J.13	0.0000000	0.0000000	0.0000000	02
10900	002 160.253	160 TOJ 000	0.354*	J.14	0.0000000	0.0000000	0.0000000	02
10900	002 160.254	160 TOJ 000	0.355*	J.15	0.0000000	0.0000000	0.0000000	02
10900	002 160.255	160 TOJ 000	0.356*	J.16	0.0000000	0.0000000	0.0000000	02
10900	002 160.256	160 TOJ 000	0.357*	J.17	0.0000000	0.0000000	0.0000000	02
11000	002 160.260	160 JUMP 113			0.0000000	0.0000000	0.0000000	02
11300	002 160.374	160 TPK 001	P.135	K.375	0.0000000	0.7550135	0.7550135	02

52800	003	014.C05	G14	TGX	000	G.C6	X.	0.0000001	0.0000001	0.0000001	02
52900	003	014.C06	C14	TGX	000	G.C7	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.C07	C14	TGX	000	G.C11	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.C10	C14	TGX	000	G.11	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.C11	C14	TGX	000	G.12	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.C12	C14	TGX	000	G.13	X.	0.0000001	0.0000001	0.0000001	02
52800	003	014.C13	C14	TGX	000	G.14	X.	0.0000001	0.0000001	0.0000001	02
52900	003	014.C15	C14	THX	000	H.16	X.	0.0000001	0.0000001	0.0000001	02
53000	003	014.C16	C14	THX	000	H.17	X.	0.0000001	0.0000001	0.0000001	02
53100	003	015.C21	C14	TCC	001	C.	C.C22*	1.6000017	1.6000017	1.6000017	02
53200	003	014.C23	C14	REPT	017	C2C		0.0000000	0.0000000	0.0000000	02
53300	003	014.C24	C14	TJC	000	J.C5	0.025*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C25	C14	TJC	000	J.C6	0.026*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C26	C14	TJC	000	J.C7	0.027*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C27	C14	TJC	000	J.C10	0.030*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C30	C14	TJC	000	J.11	C.C31*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C31	C14	TJC	000	J.12	G.032*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C32	C14	TJC	000	J.13	C.C33*	G.0000000	0.0000000	0.0000000	02
53300	003	014.C33	C14	TJC	000	J.14	C.C34*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C34	C14	TJC	000	J.15	0.035*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C35	C14	TJC	000	J.16	C.036*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C36	C14	TJC	000	J.17	G.037*	0.0000000	0.0000000	0.0000000	02
53300	003	014.C37	C14	TJC	000	J.CC	0.040*	0.2610477	0.2610477	0.2610477	02
53300	003	014.C40	C14	TJC	000	J.C1	0.041*	0.2004500	0.2004500	0.2004500	02
53300	003	014.C41	C14	TJC	000	J.C2	0.042*	0.0450103	0.0450103	0.0450103	02
53300	003	014.C42	C14	TJC	000	J.C3	C.043*	0.5012330	0.5012330	0.5012330	02
53300	003	014.C43	C14	TJC	000	J.C4	G.044*	0.1437714	0.1437714	0.1437714	02
53400	003	014.C45	C14	JUMP	000			0.0000000	0.0000000	0.0000000	02
53500	003	014.C46	C14	BLFO	010	F.7	0.047*	0.0000000	0.0000000	0.0000000	02
53500	003	014.C46	C14	BLFO	010	F.C	0.050*	0.0000000	0.0000000	0.0000000	02
53500	003	014.C46	C14	BLFO	010	F.1	0.051*	0.0000000	0.0000000	0.0000000	02
53500	003	014.C46	C14	BLFO	010	F.2	0.052*	0.0000000	0.0000000	0.0000000	02
53500	003	014.C46	C14	BLFO	010	F.3	0.053*	0.0000000	0.0000000	0.0000000	02
53500	003	014.C46	C14	BLFO	010	F.4	0.054*	1.6100456	1.6100456	1.6100456	02
53500	003	014.C46	C14	BLFO	010	F.5	C.055*	0.0200000	0.0200000	0.0200000	02
53500	003	014.C46	C14	BLFO	010	F.6	C.C56*	0.0000000	0.0000000	0.0000000	02
53600	003	014.C57	C14	JUMP	000			0.0000000	0.0000000	0.0000000	02
53700	003	014.C60	C14	THC	000	H.01	C.C61*	0.0000000	0.0000000	0.0000000	02
53800	003	014.C61	C14	THC	000	H.C2	C.	1.6000053	1.6000017	1.6000017	02
53900	003	014.C62	C14	THC	000	H.03	G.063*	0.0000000	0.0000000	0.0000000	02
54000	003	014.C63	C14	THC	000	H.C4	0.064*	0.0000000	0.0000000	0.0000000	02
54100	003	014.C64	C14	THC	000	H.C5	C.065*	0.0000000	0.0000000	0.0000000	02
54200	003	014.C65	C14	THC	000	H.C6	0.066*	0.0000000	0.0000000	0.0000000	02
54300	003	014.C66	C14	THC	000	H.C7	0.067*	0.0000000	0.0000000	0.0000000	02
54400	003	014.C67	C14	JUMP	000			0.0000000	0.0000000	0.0000000	02
54500	003	014.C70	C14	THX	000	H.11	X.	G.0000001	0.0000001	0.0000001	02
54600	003	014.C71	C14	THX	000	H.12	X.	0.0000001	0.0000001	0.0000001	02
54700	003	014.C72	C14	THX	000	H.13	X.	0.0000001	0.0000001	0.0000001	02
54800	003	014.C73	C14	THX	000	H.14	X.	0.0000001	0.0000001	0.0000001	02
54900	003	014.C74	C14	THX	000	H.15	X.	0.0000001	0.0000001	0.0000001	02
55000	003	014.C75	C14	TBC	000	H.	C.	3.7777777	1.6000017	1.6000017	02
55100	003	014.C76	C14	TDC	000	D.	C.	1.6000053	1.6000017	1.6000017	02
55200	003	014.C77	174	TEX	000	E.	X.	1.6000017	0.0000001	0.0000001	02

174.100 174.100
PRECEDENCE CK FCR START CF STEP
174.100 174.100
PRECEDENCE CK FCR END OF STEP

PRECEDENCE CK FOR START CF STEP
14.420
PRECEDENCE CK FOR END OF STEP

51700	004	014.420	C14	JUMP	000	0.000000	0.000000	0.000000	0.000000	02
51800	004	014.421	C14	T0E	001	0.000000	1.6100000	1.6100000	1.6100000	02
52000	004	014.423	C14	REPT	C17	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.424	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.425	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.426	C14	T0J	000	0.000000	1.6000077	1.6000077	1.6000077	02
52100	004	014.427	C14	T0J	000	0.000000	0.0000006	0.0000006	0.0000006	02
52100	004	014.430	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.431	C14	T0J	000	0.000000	1.6100307	1.6100307	1.6100307	02
52100	004	014.432	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.433	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.434	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.435	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.436	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.437	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.440	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.441	C14	T0J	000	0.000000	1.4000000	1.4000000	1.4000000	02
52100	004	014.442	C14	T0J	000	0.000000	0.000000	0.000000	0.000000	02
52100	004	014.443	C14	T0J	000	0.000000	1.6030114	1.6030114	1.6030114	02
52200	004	014.445	C14	REPT	007	0.000000	1.6273000	1.6273000	1.6273000	02
52300	004	014.446	C14	T0F	000	0.000000	0.000000	0.000000	0.000000	02
52300	004	014.447	C14	T0F	000	0.000000	0.000000	0.000000	0.000000	02
52300	004	014.450	C14	T0F	000	0.000000	1.7573161	1.7573161	1.7573161	02
52300	004	014.451	C14	T0F	000	0.000000	1.5000000	1.5000000	1.5000000	02
52300	004	014.452	C14	T0F	000	0.000000	1.7727061	1.7727061	1.7727061	02
52300	004	014.453	C14	T0F	000	0.000000	0.2610477	0.2610477	0.2610477	02
52300	004	014.454	C14	T0F	000	0.000000	1.6050437	1.6050437	1.6050437	02
52300	004	014.455	C14	T0F	000	0.000000	1.7400001	1.7400001	1.7400001	02
52400	004	014.457	C14	REPT	006	0.000000	1.7552161	1.7552161	1.7552161	02
52500	004	014.460	C14	T0H	000	0.000000	0.000000	0.000000	0.000000	02
52500	004	014.461	C14	T0H	000	0.000000	1.6000017	1.6000017	1.6000017	02
52500	004	014.462	C14	T0H	000	0.000000	0.000000	0.000000	0.000000	02
52500	004	014.463	C14	T0H	000	0.000000	0.000000	0.000000	0.000000	02
52500	004	014.464	C14	T0H	000	0.000000	0.000000	0.000000	0.000000	02
52500	004	014.465	C14	T0H	000	0.000000	0.000000	0.000000	0.000000	02
52500	004	014.466	C14	T0H	000	0.000000	0.000000	0.000000	0.000000	02
52600	004	014.470	C14	JUMP	001	0.000000	0.000000	0.000000	0.000000	02
52700	004	014.472	C14	REPT	020	0.000000	0.000000	0.000000	0.000000	02
52800	004	014.473	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	004	014.474	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	004	014.475	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	004	014.476	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.477	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.480	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.482	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.483	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.484	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.485	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.486	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.487	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.488	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.489	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.490	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.491	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.492	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.493	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.494	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.495	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.496	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.497	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.498	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.499	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.500	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.501	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.502	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.503	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.504	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.505	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.506	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.507	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.508	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.509	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.510	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.511	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.512	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02
52800	005	014.513	C14	TGX	000	0.000000	0.000000	0.000000	0.000000	02

C.C22*E.
C2C
0.025*J.05
0.026*J.06
0.027*J.07
0.030*J.10
0.031*J.11
0.032*J.12
0.033*J.13
0.034*J.14
0.035*J.15
0.036*J.16
0.037*J.17
0.040*J.00
0.041*J.01
0.042*J.02
0.043*J.03
0.044*J.04
01C
0.047*F.7
0.050*F.0
0.051*F.1
0.052*F.2
0.053*F.3
0.054*F.4
0.055*F.5
0.056*F.6
007
0.061*H.01
0.062*H.02
0.063*H.03
0.064*H.04
0.065*H.05
0.066*H.06
0.067*H.07
021
G.14 X.
G.15 X.
G.16 X.
G.17 X.
G.00 X.
G.01 X.
G.02 X.
G.03 X.
G.04 X.
G.05 X.
G.06 X.
G.07 X.
G.10 X.
G.11 X.
G.12 X.
G.13 X.

H. COMPUTER RUN WITH INCONSISTENT PRECEDENCE MATRIX

A run was made with a flow diagram precedence matrix which contained an inconsistency. The precedence matrix was the following:

	<u>MATRIX</u>						
	COLUMN						
	1	2	3	4	5	6	7
1	0	1	0	0	0	0	0
2	0	0	1	0	0	0	0
3	0	0	0	1	1	1	0
ROW 4	0	-1	0	0	0	0	0
5	0	-1	0	0	0	0	0
6	0	0	0	0	0	0	1
7	0	0	0	0	0	1	0

The matrix specifies that step 6 must precede step 7 and that step 7 must precede step 6. This is an inconsistency or a loop. At the point in the program at which the consistency of the precedence matrix was checked, the diagnostic, "INCONSISTENT MATRIX," and the arrays, MATRIX and KWUNS, were written. The run is listed on the following page.

Contrails

UNCLASSIFIED

Security Classification

DOCUMENT CONTROL DATA - R&D		
(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)		
1. ORIGINATING ACTIVITY (Corporate author) IIT Research Institute Chicago, Illinois	2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	
	2b. GROUP N/A	
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4. DESCRIPTIVE NOTES (Type of report and inclusive dates) <p style="text-align: center;">Final report, 1 January 1963 - 14 December 1963</p>		
5. AUTHOR(S) (Last name, first name, initial) <p style="text-align: center;">Lewis, Theodore S. Huebner, Walter J.</p>		
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11. SUPPLEMENTARY NOTES Research conducted in support of Project 8119, which is directed by the Support Techniques Br, A.F. Aero Propulsion Lab.	12. SPONSORING MILITARY ACTIVITY Aerospace Medical Research Laboratories Wright-Patterson Air Force Base, Ohio	
13. ABSTRACT One of the two objectives of this project was the development of error control techniques for the man-computer interface of an automatic checkout system. To minimize human error in man-computer communication in the automatic checkout complex, precedence and connection matrix techniques for use with total and partial simulation methods were developed to detect errors in operational automatic checkout computer programs. Precedence and connection matrix techniques for use with total simulation methods were incorporated into a simulation computer program which comprised a total simulation of the computer which controls an operational automatic checkout system. The modified simulation was then used to process several computer runs of an operational automatic checkout computer program. The basic conclusions drawn from the results of the study of error control methods were that precedence and connection matrix techniques used with total and partial simulation methods can be useful in detecting errors in operational computer-controlled automatic checkout systems, and that further study and development should be made to allow incorporation of the techniques in present and future computer-controlled automatic checkout systems with minimum modification.		

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14.	KEY WORDS	LINK A		LINK B		LINK C	
		ROLE	WT	ROLE	WT	ROLE	WT
	Equipment, Simulation Automatic Check-Out Computer Program, Error Detection Human Engineering Simulation, Automatic Check-Out Equipment						

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